12V Wireless Power Transmitter IC for TX-A6

Product Datasheet

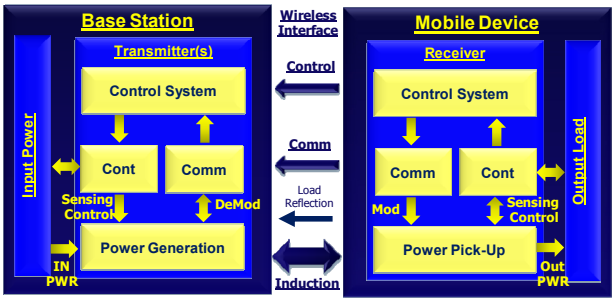
IDTP9036B

Features

- 5W Solution for Wireless Power Consortium (WPC)-Compliant Power Transmitter Design TX-A6
- Conforms to WPC Specification Version 1.1 Specifications
- Reduced EMI To Meet Requirements of WPC 1.1 Certification
- 12V Operating Input Voltage
- Closed-Loop Power Transfer Control Between Base Station and Mobile Device
- Demodulates and Decodes WPC-Compliant Message Packets
- 5V Regulated DC/DC Converter
- Integrated RESET Function
- Proprietary Back-Channel Communication
- I²C Interface
- Push-Pull or Open-Drain LED Indicator Outputs
- Over-Temperature Protection
- Security and Encryption up to 64 bits
- Foreign Object Detection (FOD)

Applications

- WPC-Compliant Wireless Charging Base Stations



Description

The IDTP9036B is a highly-integrated WPC-compliant wireless power transmitter IC for power transmitter WPC design TX-A6. This device operates with a 12Vdc adaptor, and can drive an external load directly or via an external half-bridge inverter enabling this single part to serve in either type of application. It controls the transferred power by changing the switching frequency of the half-bridge inverter from 115kHz to 205kHz as specified by the WPC specification for an "A6" transmitter. It contains logic circuits required to demodulate and decode WPC-compliant message packets sent by the mobile device to adjust the transferred power.

The IDTP9036B is an intelligent device which manages mobile device detection, and then the selection of one section of the triple A6 coil without user supervision. The A6 configuration allows free mobile device positioning over a wider area than configurations that use a single coil, detecting a mobile device for charging while minimizing idle power. Once the mobile device is detected and authenticated, the IDTP9036B continuously monitors all communications from the mobile device, and adjusts the transmitted power accordingly by varying the switching frequency of the half-bridge inverter.

The IDTP9036B features a proprietary back-channel communication mode which enables the device to communicate with IDT's wireless power receiver solutions (e.g. IDTP902X). This feature enables additional layers of capabilities beyond the standard WPC requirements.

This device also features optional security and encryptions to securely authenticate the receiver before transferring power. This feature is available when an IDTP902X is used for the receiver.

The IDTP9036B includes over-temperature/current protection and a Foreign Object Detection (FOD) method to protect the base station and mobile device from overloading in the presence of a metallic foreign object. It manages fault conditions associated with power transfer and controls status LEDs to indicate operating modes.

Typical Application Circuit

(See page 2)

Package: 6x6-48 TQFN (See page 26)
Ordering Information (See page 27)

SIMPLIFIED APPLICATION DIAGRAM

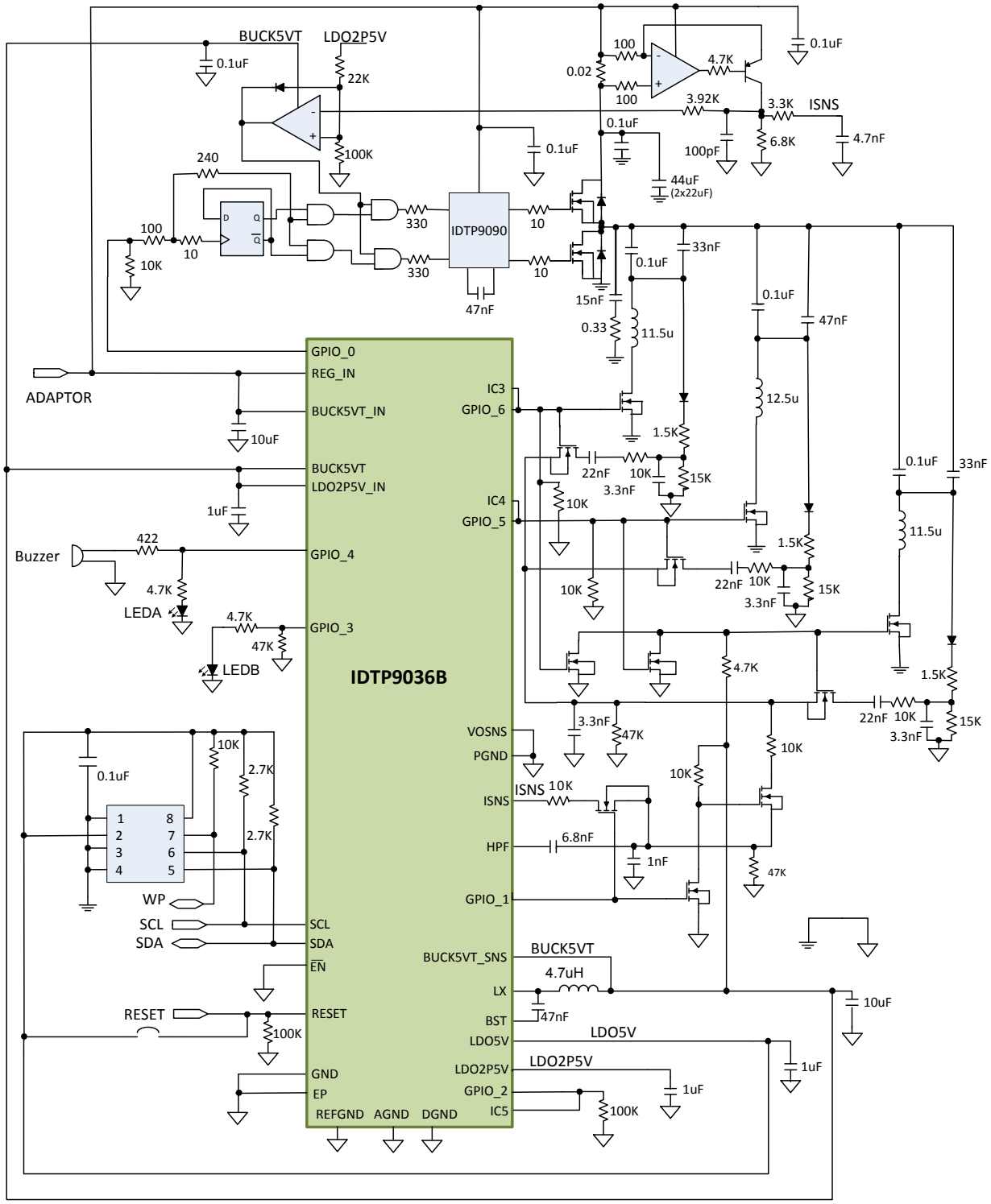


Figure 1. IDTP9036B Simplified Application Schematic

ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9036B at absolute maximum ratings is not implied. Application of the absolute maximum rating conditions affects device reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	RATING	UNITS
BUCK5VT_IN, REG_IN **(THESE PINS MUST BE CONNECTED TO GETHER AT ALL TIMES.)**	-0.3 to 24	V
IN, SW **(THESE PINS MUST BE LEFT UNCONNECTED (OPEN) AT ALL TIMES.)**	0	V
$\overline{EN}$, LX	-0.3 to VIN+0.3	V
BST	-0.3 to VIN+5	V
LDO2P5V	-0.3 to 2.75	V
AGND, DGND, PGND, REFGND	-0.3 to +0.3	V
BUCK5VT_SNS, BUCK5VT, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, HPF, ISNS, LDO2P5V_IN, LDO5V, RESET, SCL, SDA, VOSNS	-0.3 to +6.0	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient (NTG48 - TQFN)	30.8	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NTG48 - TQFN)	14.6	°C/W
θ_{JB}[2]	Thermal Resistance Junction to Board (NTG48 - TQFN)	0.75	°C/W
T_J	Junction Operating Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C, the maximum junction operating temperature. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Note 4: For the NTG48 package, connecting the 4.1 mm X 4.1 mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All	±2000	V
CDM	All	±500	V

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, REG_IN = BUCK5VT_IN = 12V. IN = SW = Open. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
External Half-Bridge Inverter						
V_{IN}	Input Supply Operating Voltage Range[1]		11.4	12	12.6	V
I_{IN}[2] I_{IN_A}	Standby Input Current			24		mA
I_{IN}[2] I_{IN_S}	Sleep Mode Input Current	$\overline{EN}$ = 5V to V_{IN}		460	600	µA
F_{SW_LOW}	Switching Frequency at SW	WPC-compliant Operating Range	115			kHz
F_{SW_HIGH}					205	kHz
UVLO						
V_{IN_UVLO}	Under-Voltage Protection Trip Point	V_{IN} rising			10.3	V
		V_{IN} falling	9.0			
		Hysteresis		625		mV
I_{IN_OCP}	Over-Current Protection Trip Point	V_{IN} = 12.6V, cycle-by-cycle protection.	5.2		6.5	A
DC-DC Converter (For Biasing Internal Circuitry Only)[3]						
$V_{BUCK5VT\_IN}$	Input Voltage Range[1]		11.4		12.6	V
$V_{BUCK5VT}$	Output Voltage	External I_{Load} = 8mA	4.5	5	5.5	V
I_{OUT}[5]	External Load				8	mA
F_{SW}	Switching Frequency at LX			3		MHz
Low Drop Out Regulators (For Biasing Internal Circuitry Only)[3]						
LDO2P5V[3]						
$V_{LDO2P5V\_IN}$	Input Voltage Range	Supplied from BUCK5VT		5		V
$V_{LDO2P5V}$	Output Voltage	I_{Load} = 2mA		2.5		V
I_{OUT}	External Load				8	mA
LDO5V[3]						
V_{REG_IN}	Input Voltage Range	See Note 1.	11.4		12.6	V
V_{LDO5V}	Output Voltage	I_{Load} = 2mA		5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Temperature Rising Threshold		140		°C
		Temperature Falling Threshold		110		

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, REG_IN = BUCK5VT_IN = 12V. IN = SW = Open. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{EN}$						
V_{IH}				900		mV
V_{IL}				550		mV
$I_{\overline{EN}}$	$\overline{EN}$ input current	$V_{\overline{EN}}$ = 5V		7.5		µA
		$V_{\overline{EN}}$ = V_{IN} = 12.6V		35		µA
General Purpose Inputs / Outputs (GPIO)						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH}=-8mA	4			V
V_{OL}	Output Logic Low	I_{OL}=8mA			0.5	V
I_{OH}	Output Current High		-8			mA
I_{OL}	Output Current Low				8	mA
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
SCL, SDA (I²C Interface)						
f_{SCL}	Clock Frequency	EEPROM loading, Step 1, IDTP9036B as Master		100		kHz
f_{SCL}	Clock Frequency	EEPROM loading, Step 2, IDTP9036B as Master		300		kHz
f_{SCL}	Clock Frequency	IDTP9036B as Slave	0		400	kHz
$t_{HD;STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD;DAT}$	Data Hold Time	I²C-bus devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition		100			ns

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, REG_IN = BUCK5VT_IN = 12V. IN = SW = Open. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance[5]			5		pF
V_{IL}	Input Threshold Low	When powered by device 5V			1.5	V
V_{IH}	Input Threshold High		3.5			V
I_{LKG}	Leakage Current		-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I_{PD}= 2mA			0.5	V
I_{OH}	Output Current High		-2			mA
I_{OL}	Output Current Low				2	mA
Analog-to-Digital Converter						
N	ADC Conversion Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		kSPS
Channel	Number of Channels at ADC MUX input			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
V_{IN_FS}	Full-Scale Input Voltage			2.39		V
Microcontroller						
F_{CLOCK}	Clock Frequency			40		MHz
V_{MCU}	MCU Supply Voltage from internal 2.5V LDO			2.5		V

Note 1: BUCK5VT_IN, REG_IN. These pins must be connected together at all times.

Note 2: This current is the sum of the input currents for REG_IN and BUCK5VT_IN.

Note 3: DC-DC BUCK5VT, LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull-up resistor loads (up to an absolute maximum of 8mA), as recommended in Figure 8 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials. If any of these outputs is used to power external loads, the performance of the IDTP9036B is not guaranteed.

Note 4: Any of the GPIO pins is capable of sourcing 8mA, but if more than one is sourcing current, the total current must not exceed 8mA.

Note 5: The 2.5V LDO is powered by the 5V DC/DC converter, so the LDO's output current must be counted in the output current budget of the DC/DC converter.

PIN CONFIGURATION

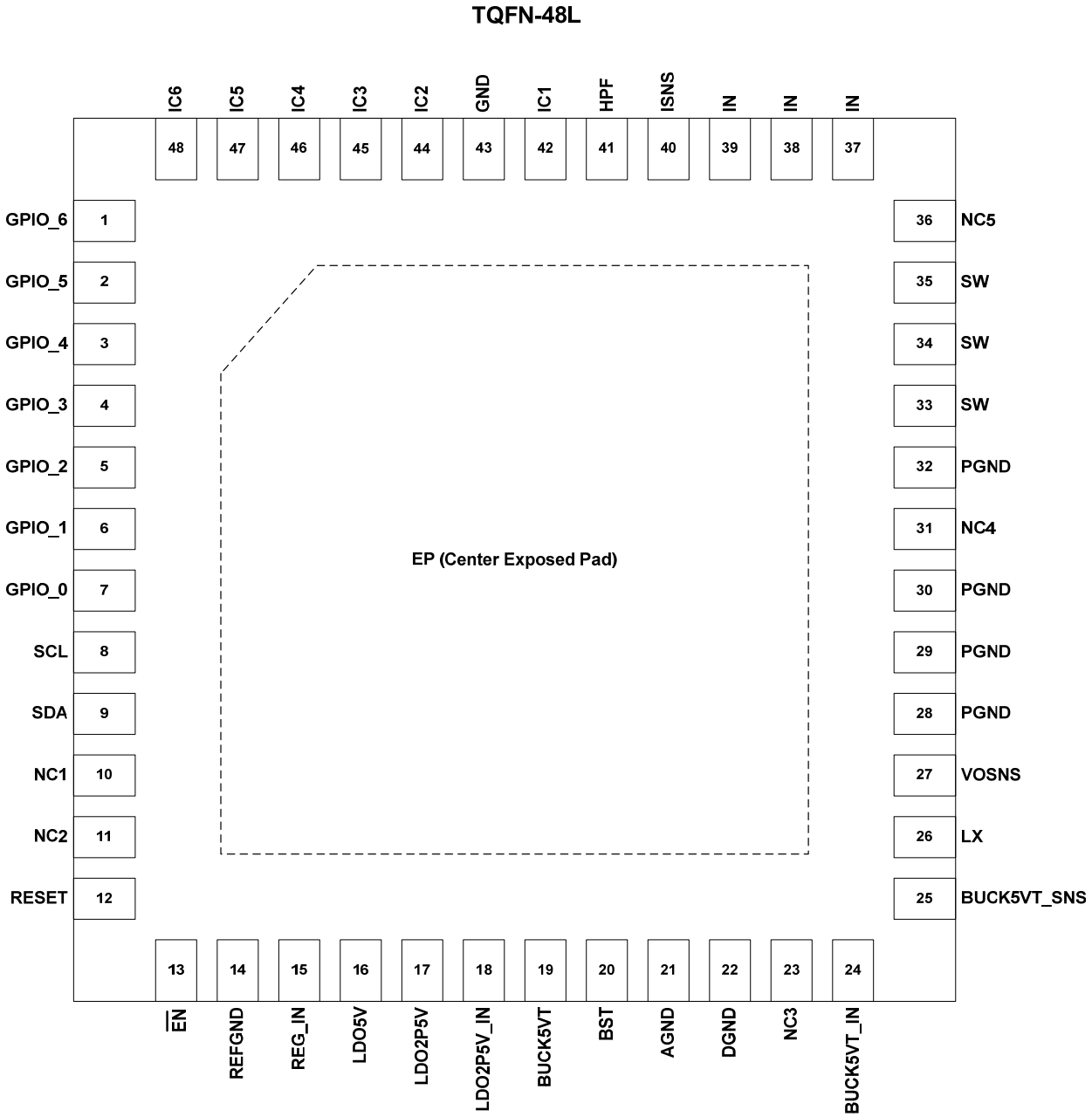


Figure 2. IDTP9036B Pin Configuration (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm, 0.4mm pitch)

PIN DESCRIPTION

Table 5. IDTP9036B NTG48 Package Pin Functions by Pin Number

1	GPIO_6	I/O	General purpose input/output 6. Must be connected to pin 45.
2	GPIO_5	I/O	General purpose input/output 5. Must be connected to pin 46.
3	GPIO_4	I/O	General purpose input/output 4.
4	GPIO_3	I/O	General purpose input/output 3.
5	GPIO_2	I/O	General purpose input/output 2. Must be connected to pin 47.
6	GPIO_1	I/O	General purpose input/output 1.
7	GPIO_0	I/O	General purpose input/output 0.
8	SCL	I/O	I^2C clock.
9	SDA	I/O	I^2C data.
10	NC1	-	Internally connected. Must be connected to GND.
11	NC2	-	Internally connected. Must be left unconnected.
12	RESET	I	Active-high chip reset pin. A 1µF ceramic capacitor must be connected between this pin and LDO5V, and a 100kΩ resistor to GND.
13	$\overline{EN}$	I	Active-low enable pin. Device is suspended and placed in low current (sleep) mode when pulled high. Tie to GND for stand-alone operation.
14	REFGND	-	Signal ground connection. Must be connected to AGND.
15	REG_IN[1]	I	LDO5V power supply input. A 1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pin 24.
16	LDO5V[2]	O	5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
17	LDO2P5V[2]	O	2.5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
18	LDO2P5V_IN	I	2.5V LDO input. The LDO2P5V_IN input must be connected to BUCK5VT. A 1µF ceramic capacitor must be connected between this pin and GND.
19	BUCK5VT[2]	I	Power and digital supply input to internal circuitry.

Table 5. IDTP9036B NTG48 Package Pin Functions by Pin Number

PIN	NAME	TYPE	DESCRIPTION
20	BST	I	Bootstrap pin for BUCK converter top switch gate drive supply.
21	AGND	-	Analog ground connection. Connect to signal ground. Must be connected to REFGND.
22	DGND	-	Digital ground connection. Must be connected to GND.
23	NC3	-	Internally connected. Must be left unconnected.
24	BUCK5VT_IN[1]	I	Buck converter power supply input. Connect 0.1µF and 1µF ceramic capacitors between this pin and PGND. This pin must be connected to pin 15.
25	BUCK5VT_SNS	I	Buck regulator feedback. Connect to the high side of the buck converter output capacitor.
26	LX	O	Switch Node of BUCK converter. Connects to one of the inductor's terminals.
27	VOSNS	I	Coil voltage sense input. Not used. Connect to ground.
28	PGND	-	Power ground.
29	PGND	-	Power ground.
30	PGND	-	Power ground.
31	NC4	-	Internally connected. Must be left unconnected.
32	PGND	-	Power ground.
33	SW	-	Internally connected. These pins must be left unconnected (open) at all times.
34	SW	-	
35	SW	-	
36	NC5	-	Internally connected. Must be left unconnected.
37	IN[1]	-	Internally connected. These pins must be left unconnected (open) at all times.
38	IN[1]	-	
39	IN[1]	-	
40	ISNS	O	ISNS output signal.

Table 5. IDTP9036B NTG48 Package Pin Functions by Pin Number

PIN	NAME	TYPE	DESCRIPTION
41	HPF	I	High pass filter input.
42	IC1		Reserved for special designs. Must be connected to GND.
43	GND	-	Ground.
44	IC2		Reserved for special designs. Must be connected to GND.
45	IC3		Reserved for special designs. Must be connected to GPIO6.
46	IC4		Reserved for special designs. Must be connected to GPIO5.
47	IC5		Reserved for special designs. Must be connected to GPIO2.
48	IC6		Reserved for special designs. Must be left unconnected.
49	Center Exposed Pad	Thermal	EP, Center Exposed Pad, is on the bottom of the package and must be electrically tied to GND. For good thermal performance, solder to a large copper pad embedded with a pattern of plated through-hole vias. The die is not electrically bonded to the EP, and the EP must not be used as a current-carrying electrical connection.

Note 1: REG_IN, BUCK5VT_IN. These pins must be connected together at all times.

Note 2: DC-DC BUCK5VT, LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull-up resistor loads (up to an absolute maximum of 8mA), as recommended in Figure 8 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials.

TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, REG_IN = BUCK5VT_IN = 12V. IN = SW = Open. TA = 25°C, unless otherwise noted.

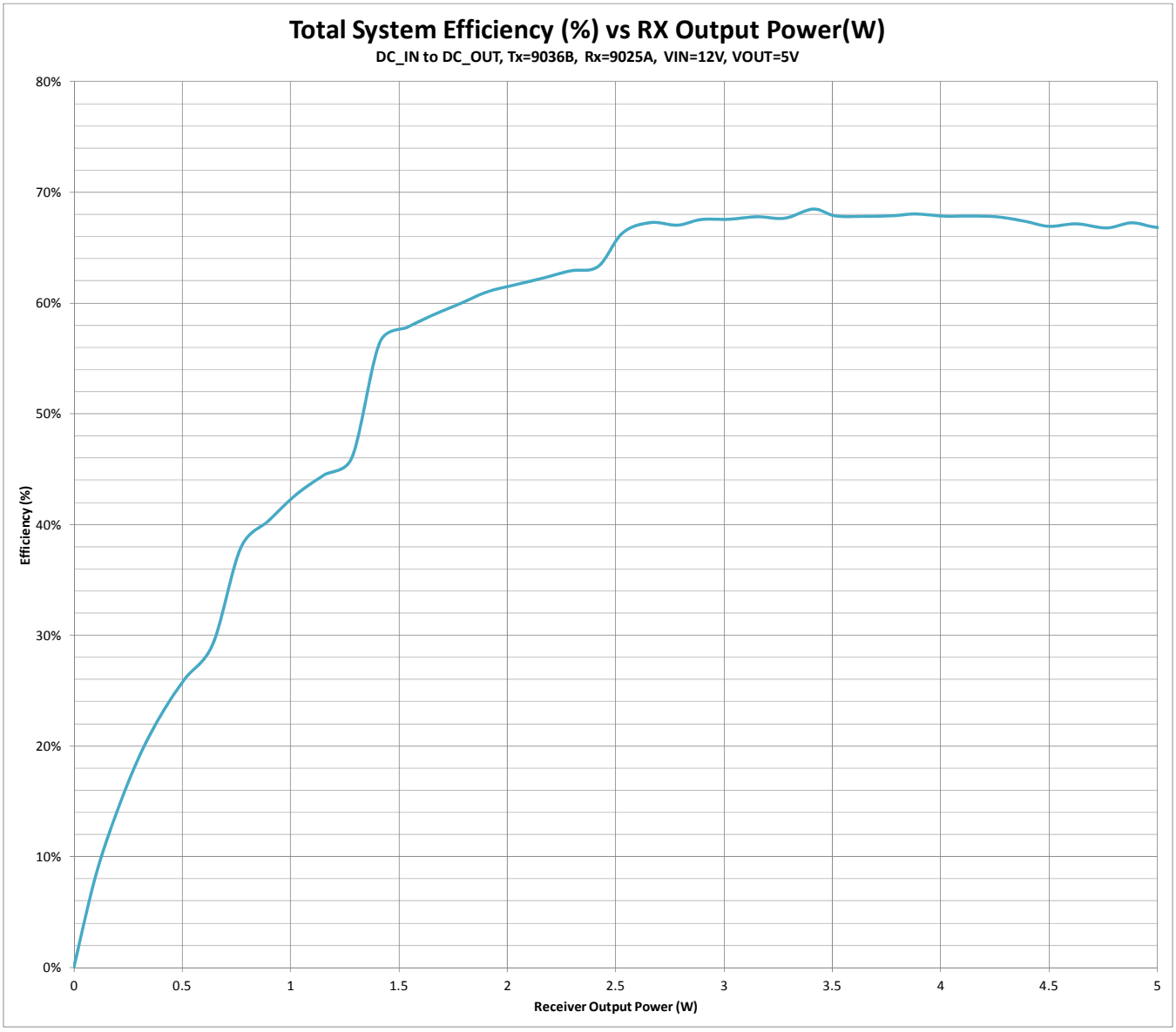


Figure 3. Efficiency vs. RX Output Power

BLOCK DIAGRAM

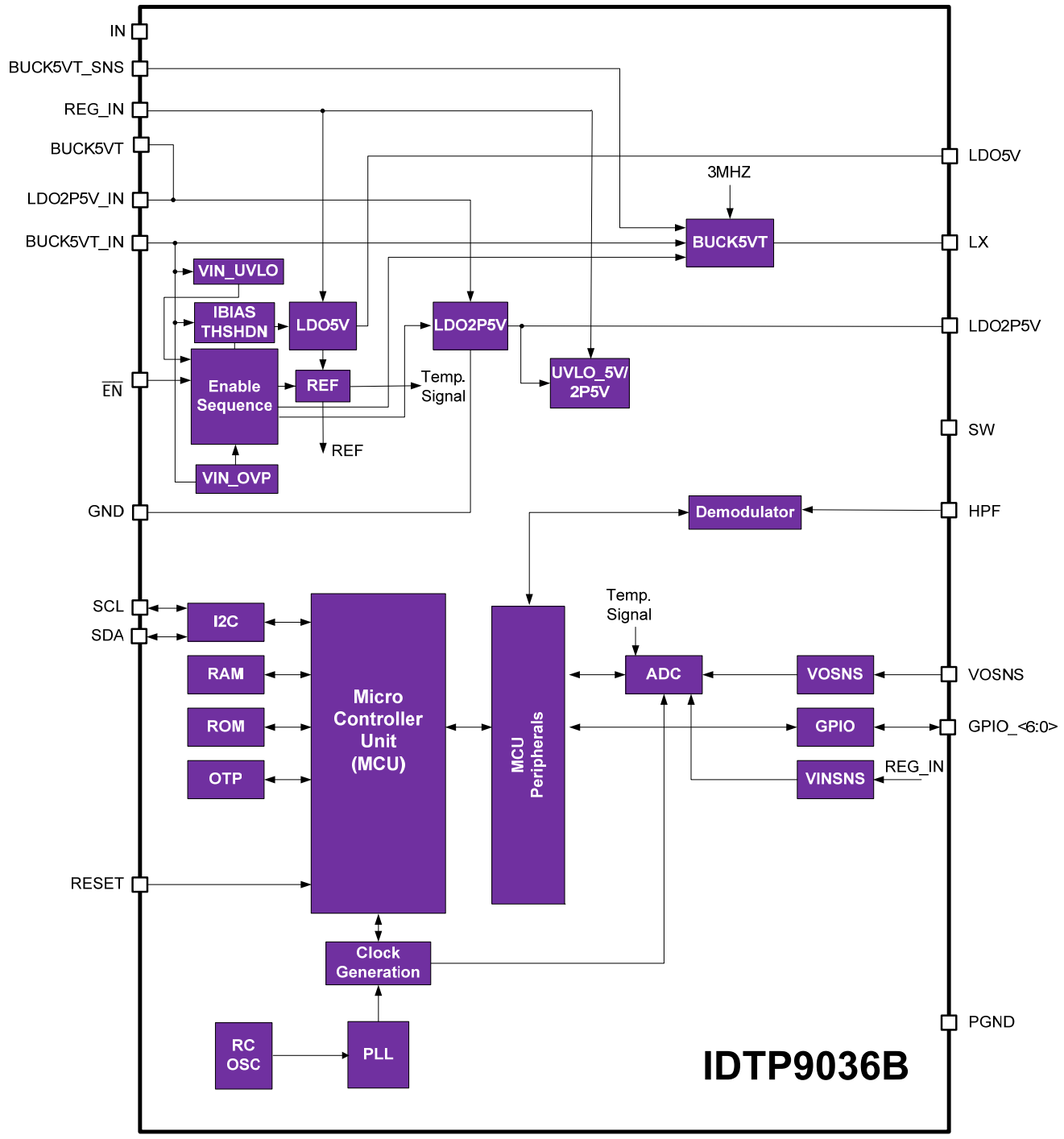


Figure 4. IDTP9036B Internal Functional Block Diagram

THEORY OF OPERATION

The IDTP9036B is a highly-integrated WPC[1] (Wireless Power Consortium)-compliant wireless power charging IC solution for the transmitter base station. It can deliver more than 5W of power to the receiver when used with the IDTP9020 or 5W in WPC "Qi" mode using near-field magnetic induction as a means to transfer energy

OVERVIEW

Figure 4 shows the block diagram of the IDTP9036B. When the VIN_UVLO block detects that the voltage at REG_IN and BUCK5VT_IN (connected together externally) is above the Vin_rising UVLO threshold and $\overline{EN}$ is at a logic LOW, the Enable Sequence circuitry activates the voltage reference, the 5V and 2.5V LDOs, and the 5V buck switching regulator.

The voltages at the outputs of the LDOs and the buck regulator are monitored to ensure that they remain in regulation, and the adaptor voltage, coil current, and internal temperature are monitored.

The digital block and the MCU output a PWM signal via GPIO0 to the external output inverter powering the selected external field-generating coil.

Communication packets from the receiver in the mobile device are detected and filtered by an external operational amplifier and passive filter, then provided to the ISNS pin to be further processed by the Demodulator and converted to digital signals that can be read by the MCU.

Several internal voltages are digitized by the ADC and supplied to the MCU for system control and algorithm – related purposes. Two GPIO ports are available to the system designer for driving LEDs and a buzzer. The clock for the MCU and other circuitry is generated by an internal RC oscillator. I^2C SDA and SCL pins permit communication with an external device or host.

UNDER VOLTAGE LOCKOUT (UVLO)

The IDTP9036B has a built-in UVLO circuit that monitors the input voltage and enables normal operation, as shown in Figure 5.

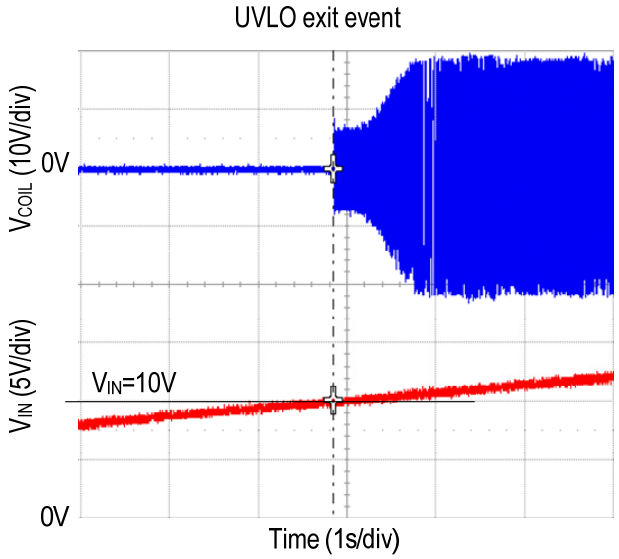


Figure 5. V_{IN} versus UVLO threshold with /EN low.

OVER-TEMPERATURE PROTECTION

The internal temperature of the IDTP9036B is monitored, and the part shuts down if the temperature exceeds 140°C and reactivates when the temperature falls below 110°C.

EXTERNAL DRIVERS and INVERTER

The external gate driver circuitry drives the off-chip power FETs. The FETs are configured as a power inverter that switches the top sides of the resonant circuits between the VIN supply voltage and ground at a rate set by the MCU control algorithm.

Note 1 - Refer to the WPC specification at http://www.wirelesspowerconsortium.com/ for the most current information

DEMODULATOR

Power is transferred from the transmitter to the receiver through the coupling of their respective coils: a loosely-coupled transformer. The amount of power transferred is determined by the transmitter's switching frequency (115kHz-205kHz, by WPC[1]), and is controlled by the receiver through instructions the receiver sends back through the same coils to the transmitter to increase or decrease power, end power transfer, or another WPC command. The instructions take the form of data packets which the receiver modulates on the carrier. The modulation is detected and then coupled through a series of filters connected to the IDTP9036B's Demodulator and then fed to the HPF pin. Recovering the data packets is the function of the Demodulator. Decoding and executing the packets is one of the functions of the MCU.

MICROCONTROLLER UNIT (MCU)

The IDTP9036B's MCU processes the algorithm, commands, and data that control the power transferred to the receiver. The MCU is provided with RAM and ROM, and parametric trim and operational modes are set at the factory through the One-Time Programming (OTP) block, read by the MCU at power-up. Communication with external memory is performed through I^2C via the SCL and SDA pins.

APPLICATIONS INFORMATION

The recommended applications schematic diagram is shown in Figure 8. The IDTP9036B operates from a $12V_{DC}$ (±5%) input. The switching frequency varies from 115kHz to 205kHz. The power transfer is controlled via changes in switching frequency. The base or TX-side has three series-resonance circuits made of a WPC Type-A6 triple coil and three capacitors. Two of the coils are 11.5µH each, and the other one is 12.5µH, each with a series resonant capacitor (~133nF or 147nF). The resonant circuits are driven by an external half-bridge inverter, as shown in Figure 6. Only the resonant circuit that is aligned with a receiver coil gets a complete path from the inverter output to power ground. The selection is made by voltage levels from GPIO5 and GPIO6, each of which drives a selection FET directly and drives an input of a wired-NAND circuit that activates or de-activates the third resonant circuit.

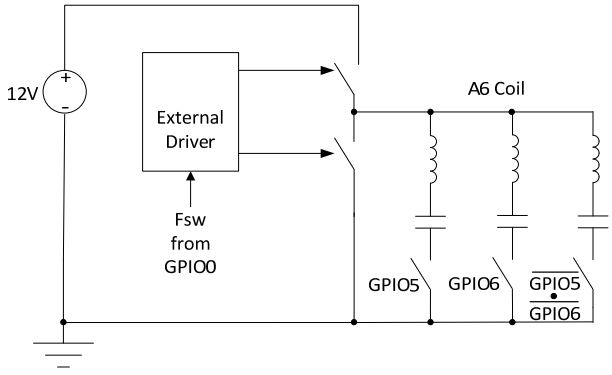


Figure 6. Half Bridge inverter TX Coil Driver.

EXTERNAL CHIP RESET and $\overline{EN}$

The IDTP9036B can be externally reset by pulling the RESET pin to a logic high above the V_{IH} level.

The RESET pin is a dedicated high-impedance active-high digital input, and its effect is similar to the power-up reset function. Because of the internal low-voltage monitoring scheme, the use of the external RESET pin is not mandatory. A manual external reset scheme can be added by connecting 5V to the RESET pin through a simple switch. When RESET is HIGH, the microcontroller's registers are set to the default configuration. When the RESET pin is released to a LOW, the microcontroller starts executing the code from the EEPROM.

If the particular application requires the IDTP9036B to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active.

The current into $\overline{EN}$ is approximately

$$I_{\overline{EN}} = \frac{V_{\overline{EN}} - 2V}{300k\Omega}$$

for input voltages between V_{IN} and +2V, and close to zero if V($\overline{EN}$) is less than 2V.

SYSTEM FEEDBACK CONTROL (WPC)

The IDTP9036B contains logic to demodulate and decode error packets sent by the mobile device (Rx-side), and adjusts power transfer accordingly. The IDTP9036B varies the switching frequency of the external half bridge inverter between 115kHz to 205 kHz to adjust power transfer. The mobile device controls the amount of power transferred via a communication link that exists from the mobile

device to the base station. The mobile device (IDTP9020 or another WPC-compliant receiver) communicates with the IDTP9036B via Communication Packets. Each packet has the following format:

Table 6 – Data Packet Format.

Preamble	Header	Message	Checksum

The overall system behavior between the transmitter and receiver follows the state machine diagram below:

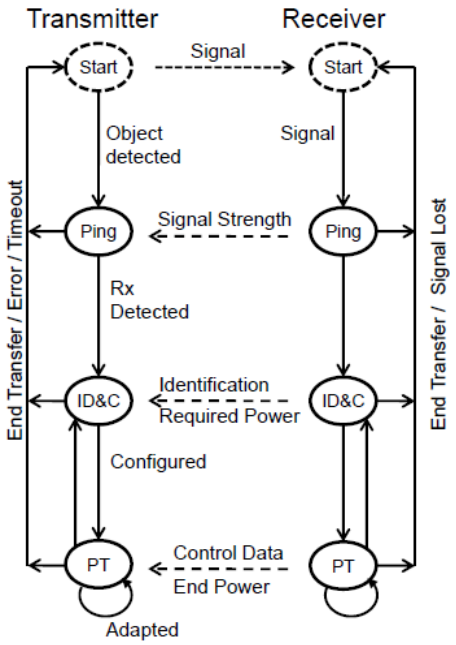


Figure 7. System state machine diagram

The IDTP9036B performs four phases: Selection, Ping, Identification & Configuration, and Power Transfer.

START (SELECTION) PHASE

In this phase, the IDTP9036B operates in a low power mode to determine if a potential receiver has been placed on the coil surface prior to the PING state. Twice a second, the IDTP9036B applies a brief AC signal sequentially to each one of the coils of the triple A6 coil and listens for a response. When a response is found, it locks its output and communication sense line to that coil.

PING PHASE

In this phase, the IDTP9036B applies a power signal at 175 kHz with a fixed 50% duty cycle and attempts to establish a communication link with a mobile device.

Required packet(s) in PING:

1. Signal Strength Packet (0x01)

The mobile device must send a Signal Strength Packet within a time period specified by the WPC, otherwise the power signal is terminated and the process repeats.

The mobile device calculates the Signal Strength Packet value, which is an unsigned integer value between 0-255, based on this formula:

$$Signal\ Strength\ Value = \left(\frac{U}{U_{max}}\right).256$$

where U is a monitored variable (i.e. rectified voltage/current/power) and U_{max} is a maximum value of that monitored variable expected during the digital ping phase at 175 kHz.

If the IDTP9036B does not detect the start bit of the header byte of the Signal Strength Packet during the Ping Phase, it removes the Power Signal after a delay. If a Signal Strength Packet is received, the IDTP9036B goes to the Identification and Configuration Phase. If the IDTP9036B does not move to the Identification and Configuration Phase after receiving the Signal Strength Packet, or if a packet other than a Signal Strength Packet is received, then power is terminated and eventually a new selection phase will begin.

IDENTIFICATION AND CONFIGURATION (ID & Config)

In this phase, the IDTP9036B tries to identify the mobile device and collects configuration information.

Required packet(s) in ID & Config:

1. Identification Packet (0x71)
2. Extended Identification Packet (0x81)*
3. Configuration Packet (0x51)

* *If Ext bit of 0x71 packet is set to 1.*

Also, the IDTP9036B must correctly receive the following sequence of packets without changing the operating point (175 kHz @ 50% duty cycle):

1. Identification Packet (0x71)
2. Extented Identification (0x81)
3. Up to 7 optional configuration packets from the following set:

a. Power Control Hold-Off Packet (0x06)
b. Proprietary Packet (0x18 – 0xF2)
c. Reserved Packet

4. Configuration Packet (0x51)

If the IDTP9036B does not detect the start bit of the header byte of the next packet in the sequence within a WPC-specified time after receiving the stop bit of the checksum byte of the preceding Signal Strength Packet, then the Power Signal is removed within after a delay. If a correct Control Packet in the above sequence is received late, or if Control Packets that are not in the sequence are received, the IDTP9036B removes the Power Signal after a delay.

POWER TRANSFER PHASE

In this phase, the IDTP9036B adapts the power transfer to the receiver based on control data it receives in Control Error Packets.

Required packet(s) in Power Transfer:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)

For this purpose, the IDTP9036B may receive zero or more of the following packets:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)
3. Charge Status Packet (0x05)
4. End Power Transfer Packet (0x02)
5. Any Proprietary Packet
6. Any reserved Packets

If the IDTP9036B does not correctly receive the first Control Error Packet in time, it removes the Power Signal after a delay. Because Control Error Packets come at a regular interval, the IDTP9036B expects a new Control Error Packet after receiving the stop bit of the checksum byte of the preceding Control Error Packet. If that does not happen, then the IDTP9036B removes the Power Signal. Similary, the IDTP9036B must receive a Rectified Power Packet within a WPC-specified time after receiving the stop bit of the checksum byte of the Configuration Packet (which was received earlier in the *identification and configuration* phase). Otherwise, it removes the Power Signal.

Upon receiving a Control Error value, the IDTP9036B makes adjustments to its operating point after a delay to enable the Primary Coil current to stabilize again after communication.

If the IDTP9036B correctly receives a packet that does not comply with the sequence, then it removes the Power Signal.

FOREIGN OBJECT DETECTION (FOD)

In addition to over-temperature protection, the IDTP9036B employs a proprietary FOD technique which detects foreign objects placed on the base station. The FOD algorithm is multi-layered and may issue warnings and/or change device operation depending on the severity of the warning.

FOD is an optional feature that is not included in the standard firmware. Please contact IDT to incorporate this feature into a specific product, indicating volume and business case.

APPLICATIONS INFORMATION

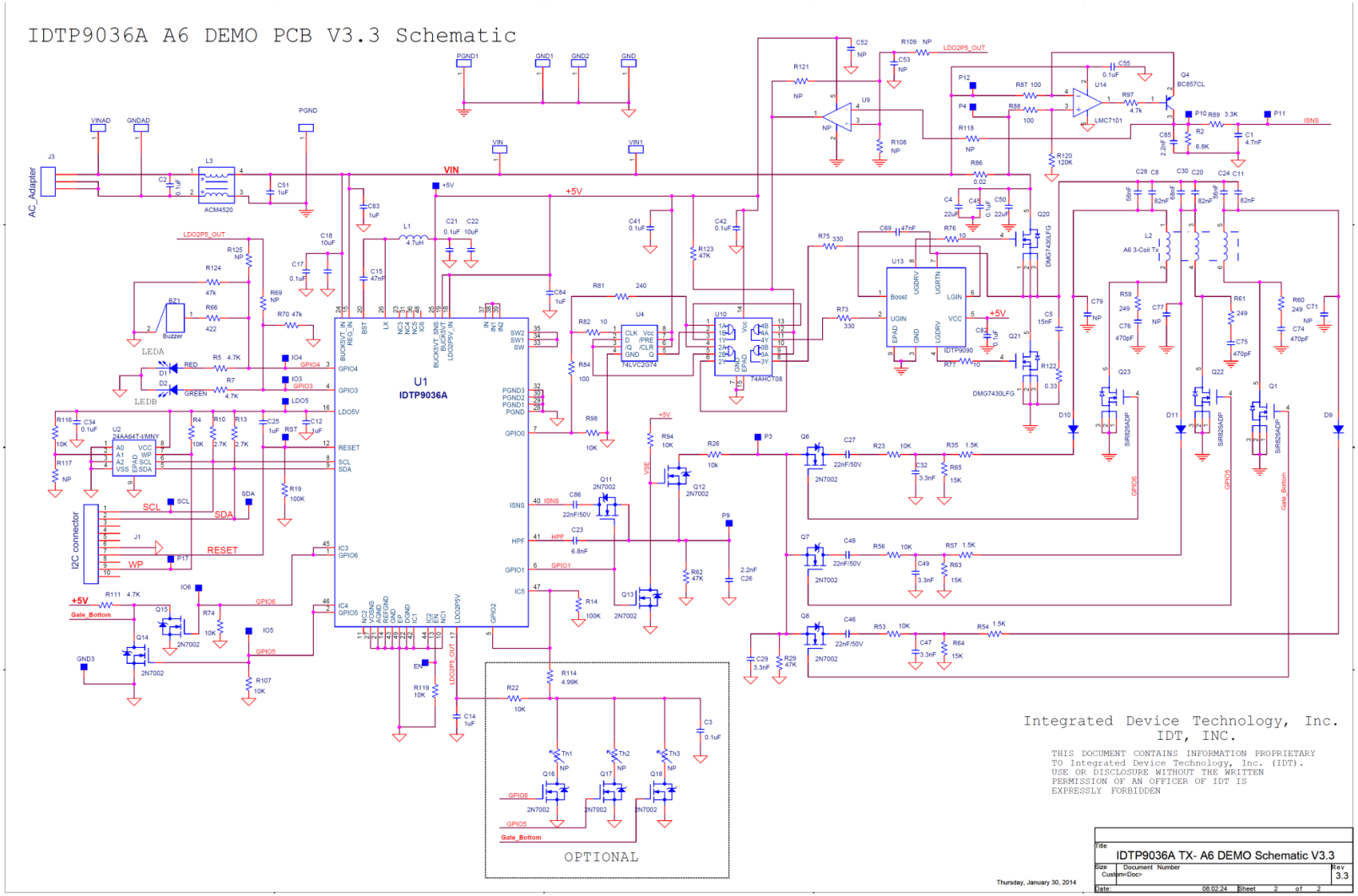


Figure 8. P9036B update to IDTP9036A WPC1.1 "Qi" Compliance Low-cost Schematic (See IDTP9036A Evaluation Kit User Manual for complete details and optional components.)

Table 7. IDTP9036A WPC "Qi" Compliance Bill of Materials

Item	Quantity	Reference	Manufacturer	Value	Part Number	PCB Footprint
1	9	VIN1,PGND1,GND1,GND2, VINAD,VIN,PGND,GNDAD, AGND		TEST POINT	5015	TEST_PT_SM_135X70
2	1	BZ1	TDK	Buzzer	PS1240P02CT3	buzz_ps1240
3	1	C1	TDK	4.7nF	C1005X7R1H472K050BA	402
4	6	C2,C41,C42,C45,C55,C82	TDK	0.1uF	C1005X7R1H104K	402
5	4	C3,C17,C21,C34	Murata	0.1uF	GRM188R71H104KA93D	603
6	2	C4,C50	Murata	22uF	GRM31CR61E226KE15L	1206
7	1	C5	Murata	15nF	GRM155R71H153KA12D	402
8	3	C8,C11,C20	Kemet	82nF	C1812C823J1GACTU	1812
9	6	C12,C14,C25,C51,C83,C84	TDK	1uF	C1608X7R1E105K	603
10	2	C15,C69	Murata	47nF	GRM188R71C473KA01D	603
11	2	C18,C22	TDK	10uF	C2012X5R1E106M	805
12	1	C23	TDK	6.8nF	C1005X7R1H682K	402
13	2	C24,C28	Kemet	56nF	C1812C563J1GACTU	1812
14	2	C26,C85	TDK	2.2nF	C1005X7R1E222K	402
15	4	C27,C46,C48,C86	TDK	22nF/50V	C1608X7R1H223K	603
16	1	C29	TDK	3.3nF	C1005X7R1H332K	402
17	1	C30	Kemet	68nF	C1812C683J1GACTU	1812
18	3	C32,C47,C49	TDK	3.3nF	C1608X7R2A332K	603
19	5	C52,R108,R109,R118,R121		NP	TBD	402
20	4	C53,R69,R117,R125		NP	NP	402
21	3	C71,C77,C79	Kemet	NP	C0805X101J2GACTU	805
22	3	C74,C75,C76	TDK	470pF	C1608X7R1H471K	603
23	1	D1	OSRAM	RED	L29K-G1J2-1-0-2-R18-Z	0603_DIODE
24	1	D2	OSRAM	GREEN	LG L29K-G2J1-24-Z	0603_DIODE
25	3	D9,D10,D11	Diodes Inc.	Diode	BAV21W-7-F	SOD123
26	18	P1,P2,P3,GND3,P4,P5,IO5, P6,IO6,P7,P8,P9,P10,P11, P12,P13,P17,EN		VC6		TEST_PT30DPAD
27	1	J1	TE Connectivity	I2C connector	5103308-1	LOPRO8PIN01INREVB
28	1	J3	CUI Inc.	AC_Adapter	PJ-002AH	CONN_POWER_JACK5_5MM
29	1	L1	CoilCraft	4.7uH	XPL2010-472MLB	805
30	1	L2	TDK MingStar Sumida Sunlord E&E	A6 3-Coil Tx	Y31-60050F	3coil_a6_standard
31	1	L3	TDK	ACM4520	ACM4520-901-2P-T-000	emi_tdk_acm4520
32	3	Q1,Q22,Q23	Vishay	SiR826ADP	SiR826ADP	SOIC8LD_PWRPAK_FET
33	1	Q4	On Semi	BC857CL	BC857CLT1G	SOT23_3
34	8	Q6,Q7,Q8,Q11,Q12,Q13,Q14, Q15	NXP	2N7002	2N7002	SOT23_3
35	3	Q16,Q17,Q18	On Semi	2N7002	2N7002WT1G	SOT23_3
36	2	Q20,Q21	Diodes Inc.	DMG7430LFG	DMG7430LFG	powerdi3333_8ld_fet
37	1	R2	Yageo	6.8K	RC0402FR-076K8L	402
38	8	R4,R26,R74,R94,R98,R107, R116,R119	Panasonic	10K	ERJ-3GEYJ103V	402
39	4	R5,R7,R97,R111	Panasonic	4.7K	ERJ-2GEJ472X	402
40	2	R10,R13	Panasonic	2.7K	ERJ-2GEJ272X	402
41	2	R14,R19	Panasonic	100K	ERJ-2GEJ104X	402
42	1	R22	Panasonic	10K	ERJ-2RKF1002X	402
43	3	R23,R53,R56	Panasonic	10K	ERJ-3EKF1002V	603
44	5	R29,R62,R70,R123,R124	Panasonic	47k	ERJ-2GEJ473X	402
45	3	R35,R54,R57	Panasonic	1.5K	ERJ-3GEYJ152V	603
46	3	R59,R60,R61	Panasonic	249	ERJ-3EKF2490V	603
47	3	R63,R64,R65	Panasonic	15K	ERJ-3GEYJ153V	603
48	1	R66	Panasonic	422	ERJ-2RKF4220X	402
49	2	R73,R75	Panasonic	330	ERJ-1GEJ331C	201
50	3	R76,R77,R82	Panasonic	10	ERJ-1GEJ100C	201
51	1	R81	Panasonic	240	ERJ-2GEJ241X	402
52	1	R84	Panasonic	100	ERJ-3GEYJ101V	603
53	1	R86	Panasonic	0.02	PF1206FRF070R02L	1206
54	1	R87	Panasonic	100	ERJ-2GEJ101X	402
55	1	R88	Panasonic	100	ERJ-2GEJ101X	402
56	1	R89	Panasonic	3.3K	ERJ-2GEJ332X	402
57	1	R114	Panasonic	4.99K	ERJ-2RKF4991X	402
58	1	R120	Yageo	120K	RC0402JR-07120KL	402
59	1	R122	Panasonic	0.33	ERJ-3RQJR33V	603
60	3	Th1,Th2,Th3	Vishay/Dale	NP	NTCLE203E3103JB0	NTC1
61	1	U1	IDT Inc.	IDTP9036B	P9036B	NTG_48LD_6X6MM_0P4PITCH
62	1	U2	Vishay/Dale	24AA64T-I/MNY	24AA64T-I/MNY	DFN8
63	1	U4	TI	74LVC2G74	SN74LVC2G74	LSSOP_8LD
64	1	U9		NP	TBD	SOT_23_5
65	1	U10	TI	74AHCT08	74AHCT08BQ,115	DHVQFN_14LD_2p5x3mm
66	1	U13	IDT Inc.	IDTP9090	IDTP9090	nlg8LD_3x3_0p65mm
67	1	U14	TI	LMC7101	LMC7101BIM5/NOPB	SOT_23_5

Note 1: Recommended capacitor temperature/dielectric and voltage ratings: 100V capacitors are recommended because 100Vp-p voltage transients may appear on the resonance capacitors as stated in the WPC specification. C0G/NPO-type capacitor values stay relatively constant with voltage while X7R and X5R ceramic capacitor values de-rate from 40% to over 80%. The decision to use lower voltage 50V C0G/NPO capacitors is left to the end user.

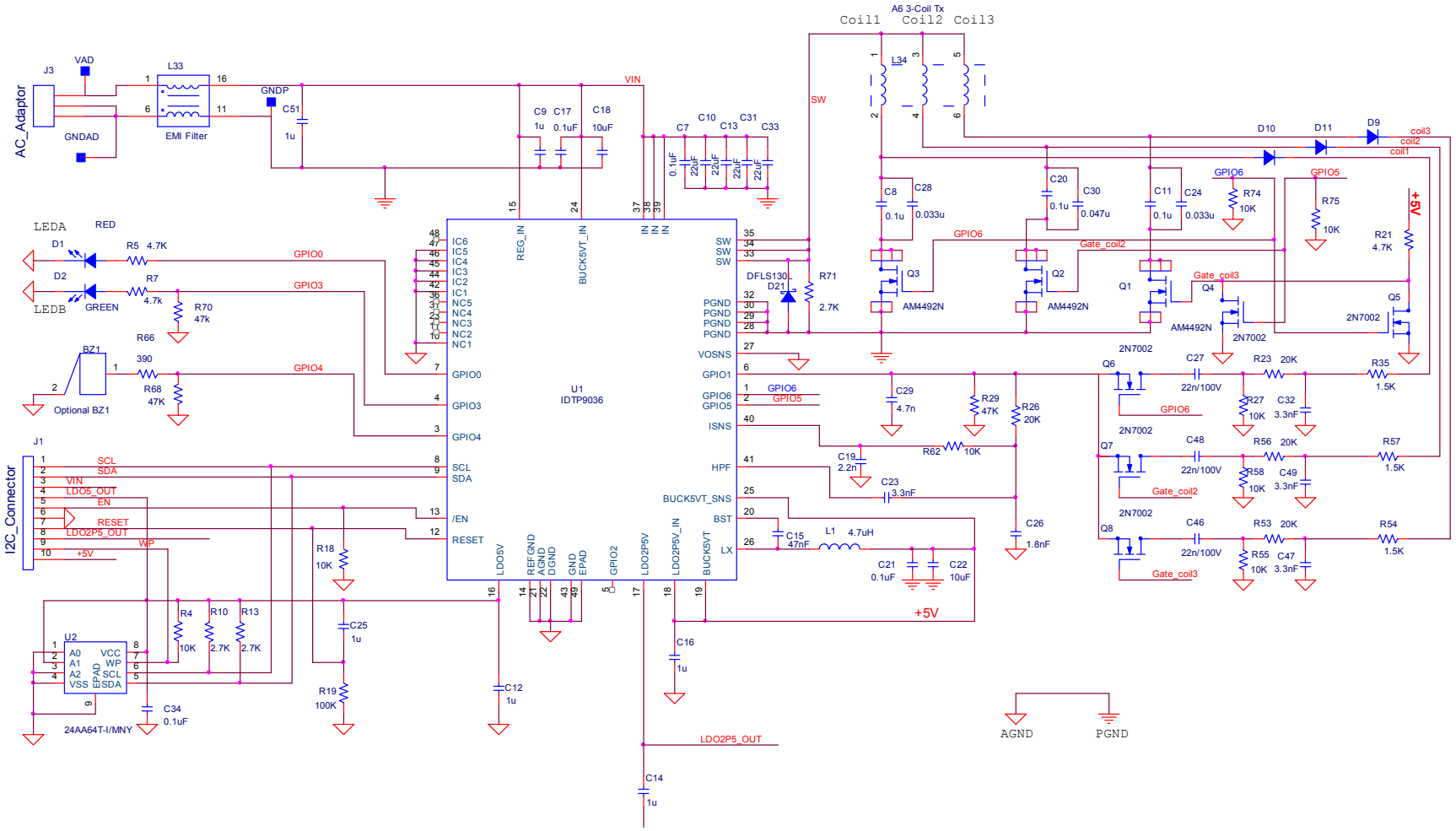


Figure 9. P9036B update to IDTP9036 WPC1.0 “Qi” Compliance Low-Cost Schematic (See IDTP9036 Evaluation Kit User Manual for complete details and optional components.)

Table 8. IDTP9036 WPC1.0 "Qi" Compliance Low-Cost Bill of Materials

Item	Quantity	Reference	Part	Manufacturer	Part_Number	PCB Footprint
1	1	BZ1	BUZZER PIEZO 4KHZ	TDK	PS1240P02CT3	12.2MM PC MNT
2	1	C6	POSCON 100uF 16V 5%	Panasonic/Sanyo	16TQC100MYF	POSCON_D3
3	4	C7,C17,C21,C34	CAP CER 0.1UF 50V 10% X7R	Murata	GRM188R71H104KA93D	603
4	3	C8,C11,C20	CAP CER 0.1UF 100V 5% NP0	TDK	C4532C0G2A104J	1812
5	6	C9,C12,C14,C16,C25,C51	CAP CER 1UF 35V 10% X5R	Taiyo Yuden	GMK107BJ105KA-T	603
6	4	C10,C13,C31,C33	CAP CER 22UF 25V 10% X7R	Murata	GRM32ER71E226KE15L	1210
7	1	C15	CAP CER 0.047UF 16V 10% X7R	Murata	GRM188R71C473KA01D	603
8	1	C18	CAP CER 10UF 25V 20% X5R	TDK	C2012X5R1E106M	805
9	1	C19	CAP CER 2200PF 50V 10% X7R	Taiyo Yuden	UMK105B7222KV-F	402
10	1	C22	CAP CER 10UF 10V 10% X7R	Murata	GRM21BR71A106KE51L	805
11	1	C23	CAP CER 3300PF 50V 10% X7R	Murata	GRM155R71H332KA01D	402
12	1	C24	CAP CER 0.047UF 100V 5% NP0	TDK	C3225C0G2A473J	1210
13	1	C26	CAP CER 1800PF 50V 10% X7R	Murata	GRM155R71H182KA01D	402
14	3	C27,C46,C48	CAP CER 0.022UF 100V X7R	TDK	C1608X7R2A223K	603
15	2	C28,C30	CAP CER 0.033UF 100V 5% NP0	TDK	C3225C0G2A333J	1210
16	1	C29	CAP CER 4700PF 100V 10% X7S	TDK	C1005X7S2A472K	402
17	3	C32,C47,C49	CAP CER 1200PF 100V 5% NP0	TDK	C1608C0G2A122J	603
18	1	D1	LED SMARTLED 630NM RED	Osram	L29K-G1J2-1-0-2-R18-Z	0603_DIODE
19	1	D2	LED SMARTLED GREEN 570NM	Osram	LG L29K-G2J1-24-Z	0603_DIODE
20	1	D21	1.0A SCHOTTKY BARRIER RECTIFIER	Diodes Inc.	DFLS130L	PowerDI123
21	3	D9,D10,D11	DIODE SWITCH 200V 250MW	Diodes Inc.	BAV21W-7-F	SOD123
22	7	GND1,VIN,VAD,PGND,GNDP, GNDAD,GND	VC6	Keystone	5015	TEST_PT_SM_135X70
23	1	J1	CONN HEADER LOPRO STR 10POS GOLD	TE Connectivity	5103308-1	CON10
24	1	J3	CONN POWER JACK 2.1X5.5MM HI CUR	CUI Inc.	PJ-002AH	JACK_5MM
25	1	L1	4.7uH 10% 580mA	Coilcraft	XPL2010-472ME_	IND_2SQ_TO_3P3REC
26	1	L33	EMI Filter	Coilcraft	NA6054-CE	clcft_na6054
27	1	L34	WPC A6 3-Coil Tx	TDK	WT-1005660-12K2-A6-G	3coil_A6_WPC standard
				E&E	Y31-60054F	
28	3	Q1,Q2,Q3	N-Channel 100-V (D-S) MOSFET	Analog Power	AM4492N	SOIC8
29	5	Q4,Q5,Q6,Q7,Q8	MOSFET N-CHAN DUAL 60V SOT363	Fairchild	2N7002	SOT363
30	5	R4,R18,R62,R74,R75	RES 10.0K OHM 1/16W 1%	Yageo	RC0402FR-0710KL	402
31	3	R5,R7,R21	RES 4.99K OHM 1/10W 1%	Panasonic	ERJ-2RKF4991X	402
32	2	R10,R13	RES 2.7K OHM 1/10W 5%	Panasonic	ERJ-2GEJ272X	402
33	1	R19	RES 100K OHM 1/16W 1%	Yageo	RC0402FR-07100KL	402
34	1	R20	RES 100 OHM 1/16W 1%	Yageo	RC0402FR-07100RL	402
35	3	R23,R53,R56	RES 20.0K OHM 1/10W 1%	Panasonic	ERJ-3EKF2002V	603
36	1	R26	RES 20.0K OHM 1/10W 1%	Panasonic	ERJ-2RKF2002X	402
37	3	R27,R55,R58	RES 10.0K OHM 1/10W 1%	Panasonic	ERJ-3EKF1002V	603
38	3	R29,R68,R70	RES 47K OHM 1/10W 5%	Panasonic	ERJ-2GEJ473X	402
39	3	R35,R54,R57	RES 1.00K OHM 1/10W 1%	Panasonic	ERJ-3EKF1001V	603
40	1	R66	RES 390 OHM 1/10W 5%	Panasonic	ERJ-3GEYJ391V	603
41	1	R71	RES 2.7K OHM 1/10W 5%	Panasonic	ERJ-3GEYJ272V	603
42	2	R72,R73	RES 0.0 OHM 1/8W	Panasonic	ERJ-6GEY0R00V	805
43	1	S1	MOM SPST	Wurth	434 121 043 816	we_mom_spst_4341
44	1	U2	IC EEPROM 64KBIT 400KHZ	Microchip	24AA64T-I/MNY	TDFN8
45	1	U1	12V Wireless Transmitter IC for TX-A6	IDT	IDTP9036B	48LD_6X6MM_0P4

Note 1: Recommended capacitor temperature/dielectric and voltage ratings: 100V capacitors are recommended because 100Vp-p voltage transients may appear on the resonance capacitors as stated in the WPC specification. C0G/NPO-type capacitor values stay relatively constant with voltage while X7R and X5R ceramic capacitor values de-rate from 40% to over 80%. The decision to use lower voltage 50V capacitors or other type temperature/dielectric capacitors is left to the end user.

External Components

The IDTP9036B requires a minimum number of external components for proper operation (see the BOM in Table 7). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 8. It includes WPC "Qi" LED signaling, buzzer, and an EEPROM for loading IDTP9036B firmware.

I²C Communication

The IDTP9036B includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9036B will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the IDTP9036B does not support multi-master mode, and it is important for system designers to

avoid any bus master conflict until the IDTP9036B has finished any firmware uploading and has released control of the bus as I²C Master. After any firmware uploading from external memory is complete, and when the IDTP9036B begins normal operation, the IDTP9036B is normally configured by the firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the IDTP9036B tries to communicate with the first address on the EEPROM at 100kHz. If no ACK is received, communication is attempted at the other addresses at 300kHz.

EEPROM

The IDTP9036B requires an external EEPROM which contains either standard or custom TX firmware. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when 12V power is applied. The IDTP9036B uses I²C slave address 0x52 to access the EEPROM. The IDTP9036B slave address is 0x39. The EEPROM can be reprogrammed to update the start-up program using the IDT Windows GUI (see the IDTP9036B-Qi Demo Board User Manual for complete details). A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard default firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

Overview of Standard GPIO Usage

There are 7 GPIO's on the IDTP9036B transmitter IC, of which two are available for use as follows:

- GPIO3: Green LED_B to indicate standby, power transfer, and power complete. Table 8 lists how the red and green LEDs can be used to display information about the IDTP9036B's operating modes. The table also includes information about external resistors or internal pull up/down options to select LED modes. Eight of the ten LED modes (those associated with advanced charging modes) are currently designated as "Future" modes.
- GPIO4: Red LED and AC or DC buzzer (optional) with resistor options for different buzzer.

LED FUNCTIONS

Two GPIOs are used to drive LEDs which indicate, through various on/off and illumination options, the state of charging and some possible fault conditions.

A red LED indicates various Fault and FOD ("Foreign Object Detection") states. The green LED indicates Power Transfer and Charge Complete state information. Upon power up, the two LEDs together may optionally indicate the Standby State and remain in this state until another of the defined Operational States occurs

As shown in Figure 10, one or two resistors configure the defined LED option combinations. The DC voltage set in this way is read one time during power-on to determine the LED configuration. To avoid interfering with the LED operation, the useful DC voltage range must be limited to not greater than 1Vdc.

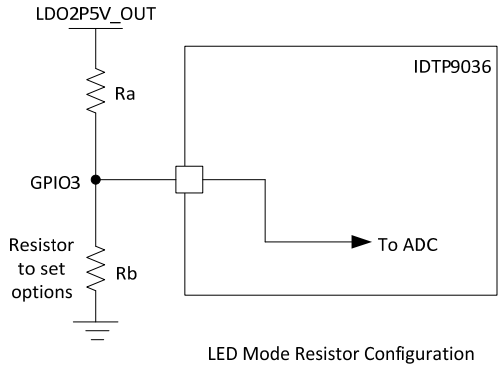


Figure 10. IDTP9036B LED Resistor Options.

LED Pattern Operational Status Definitions:

Blink Slow, Fast, repeat.

Table 9 – IDTP9036B LED Resistor Optioning (Ra or Rb=47KΩ).

LED Control Option	LED Select Resistor Value	Description	LED #/ Color	Operational Status				FOD Warning
				Standby	Transfer	Complete	Condition	
1	Pull Down	Standby LEDs ON	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
2	Pull Up	Standby LEDs OFF	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST

Buzzer Function

An optional buzzer feature is supported on GPIO4. The default configuration is an "AC" buzzer. The signal is created by toggling GPIO4 active-high/active-low at a 2kHz frequency.

Buzzer Action: Power Transfer Indication

The IDTP9036B supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the power transfer indication sound is 400ms.

The latency between reaching the Power Transfer state and sounding the buzzer does not exceed 500ms. Additionally, the buzzer sound is concurrent within ±250ms of any change to the LED configuration indicating the start of power transfer.

Buzzer Action: No Power Transfer due to Foreign Object Detected (FOD)

When a major FOD situation is detected such that, for safety reasons, power transfer is not initiated, or that power transfer is terminated, the buzzer is sounded in a repeating sequence:

For 30 seconds: 400ms ON, 800ms OFF, repeat
Next 30 seconds: Off/silence (but no change to LED on/off patterns)
The pattern is repeated while the error condition exists

The buzzer is synchronized with the FOD LED such that the 400ms on tone corresponds with the red LED illumination and 800ms off (no sound) corresponds with the red LED being off.

Decoupling/Bulk Capacitors

As with any high-performance mixed-signal IC, the IDTP9036B must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of 0.1µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor must be mounted on the component side of the PCB. Additionally, medium value capacitors in the 22µF range must be used at the VIN input to minimize ripple current and voltage droop due to the large current requirements of the resonant half Half-Bridge driver. At least four 22µF capacitors must be used close to the drain of the top MOSFET of the external half-bridge. The value of the capacitors will decrease as the voltage applied approaches the nominal voltage, due to the ceramic dielectric characteristics. For example, a 22µF X7R 25V capacitor's value could be as low as 6µF when operating at 13V, depending on the manufacturer.

Adding an 82µF to 100µF bulk capacitor connected at the point where the input voltage to the board is applied will reduce supply ripple. A 100µF 16V POSCON can be connected between the input supply and ground. POSCON capacitors have much lower ESR than aluminum electrolytic capacitors and will reduce voltage ripple.

ADC Considerations

The GPIO pins can be configured to connect internally to the successive approximation ADC through the ADC's input multiplexer. The ADC has a limited input range, so attention must be paid to the maximum VIN (2.4V). 0.01µF decoupling capacitors can be added to the GPIO inputs to minimize noise.

WPC TX-A6 Coil

The external half-bridge output connects to three series-resonance circuits made by a WPC triple Type-A6 coil (two 11.5µH side coils and one 12.5µH center coil) and series resonant capacitors (total value 133nF for the two side coils and total value 147nF for the center coil). The selected inductor serves as the primary coil of a loosely-coupled transformer, the secondary of which is the inductor connected to the power receiver (IDTP9020 or another).

The TX-A6 power transmitter coils are mounted on a ferrite base acting as a shield to concentrate the field on

the top side of the coil and to reduce EMI. The coil assembly can be mounted next to the IDTP9036B. Either ground plane or grounded metal shielding (preferably copper) can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the IDTP9036B ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating to 100V. Use one 33nF and one 100nF capacitor for each side coil, and one 47nF and one 100nF capacitor for the center coil. The part numbers are shown in Table 7.

Buck Converter

The input capacitors (C_{IN}) must be connected directly between the power pins (REG_IN and BUCK5VT_IN) and power PGND pins as near as possible to the IC pins. The output capacitor (C_{OUT}) must be placed as close to the device and power ground pins (PGND) as possible.

Connect a 47nF bootstrap capacitor rated above 25V between the BST pin and the LX pin.

The output-sense connection to the feedback pin, BUCK5VT_SNS, must be separated from any power trace. Connect the output-sense trace as close as possible to the load point to avoid additional load regulation errors. The buck will regulate the voltage at the point on the output the sense line is connected to.

The power traces, including PGND traces, the LX or 5V output traces, and the VIN trace must be kept short, direct and wide to allow large current flow. Use several via pads when routing power lines between layers.

LDOs

Input Capacitor

The input capacitors must be located as physically close as possible to the power pin (LDO2P5V_IN) and power ground (GND). Ceramic capacitors are recommended for their low ESR and small profile. Also, ceramic capacitors are inherently more capable than tantalum capacitors to withstand input current surges from low impedance sources such as batteries used in portable devices. Typically, 10V- or 16V-rated capacitors are required. The recommended external components are shown in Table 7.

Output Capacitor

For proper voltage regulation and stability, a capacitor is required on the output of each LDO (LDO2P5V and LDO5V). The output capacitor must be placed as close to the device and power (PGND) pins as possible. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.
- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.
- The 0.1µF decoupling capacitors must be mounted on the component side of the board as close as possible to the pins intended to be decoupled. Keep PCB traces to each power pin and to ground vias as short as possible.
- To optimize board layout, place all components on the same side of the board. Route signal traces away from the IDTP9036B.
- The NQG48 6.0mm x 6.0mm x 0.75mm 48L package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.
- The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad for the NTG48. The PTH vias perform as

thermal conduits to the ground plane (thermally, a heat spreader) from the solder side of the board.

- On the solder side of the board, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
    4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).

Power Dissipation/Thermal Requirements

The IDTP9036B is offered in a TQFN-48L package. The maximum power dissipation capability is 1.3W, limited by the die's specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 31°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout. Care should be exercised to avoid the placement of the IDTP9036B IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB itself upon which the TQFN is mounted. Changing the design or configuration of the PCB impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

Thermal Overload Protection

The IDTP9036B integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C.

Special Notes

NQG TQFN-48 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

PACKAGE OUTLINE DRAWING

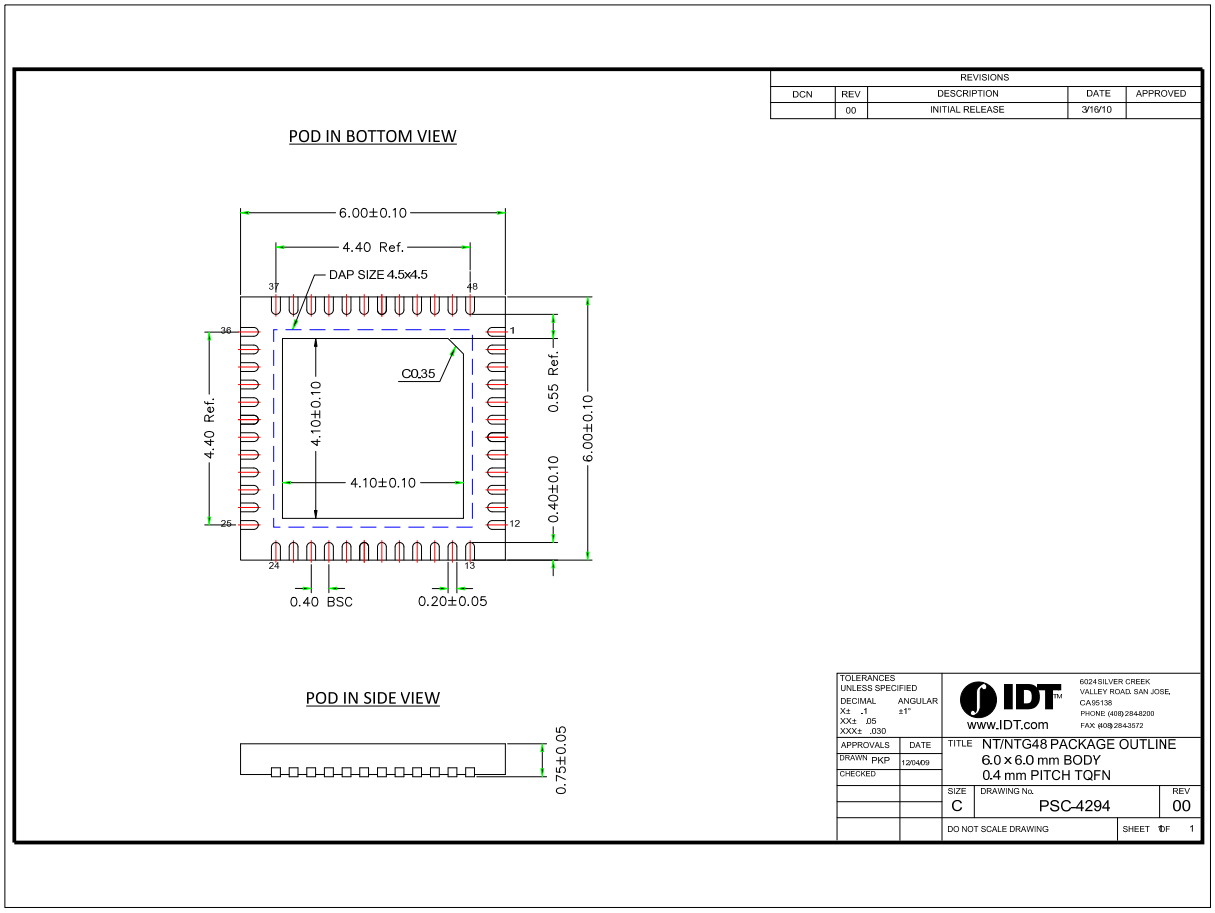


Figure 11. IDTP9036B Package Outline Drawing (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm48L, 0.4mm pitch)

ORDERING GUIDE

Table 9. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9036B-0NTGI	P9036BNTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tray	25
P9036B-0NTGI8	P9036BNTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tape and Reel	2,500

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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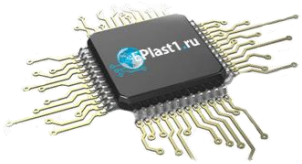
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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