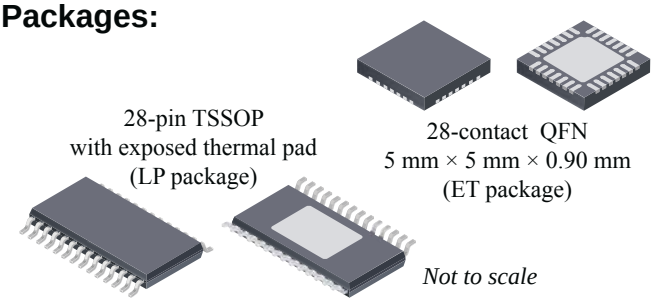
3-Phase MOSFET Driver

Features and Benefits

- 5 to 50 V supply voltage
- Latched TSD with fault output
- Drives six N-channel high current MOSFETs
- Internally controlled synchronous rectification
- Speed voltage input enables internal PWM duty cycle control of full bridge
- Center aligned PWM
- Internal UVLO and crossover current protection
- Hall switch inputs
- Adjustable dead time protection
- Low power sleep mode for battery-powered applications

Packages:



28-pin TSSOP
with exposed thermal pad
(LP package)

28-contact QFN
5 mm × 5 mm × 0.90 mm
(ET package)

Not to scale

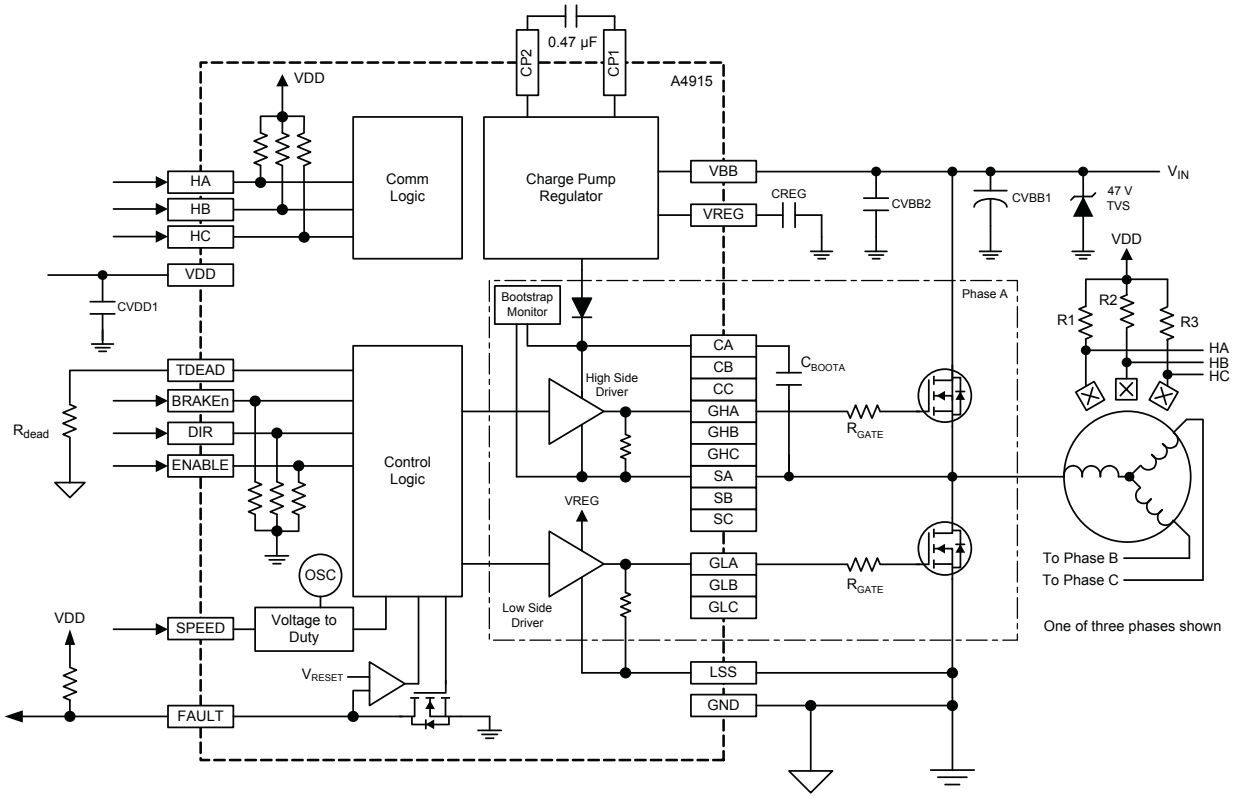
Description

The A4915 is designed for pulse width modulated (PWM) current control of 3-phase brushless DC motors. The A4915 is capable of high current gate drive for 6 all N-channel power MOSFETs. An internal charge pump ensures gate drive down to 7 V supply and provides limited gate drive down to 5 V. A bootstrap capacitor is used to generate a supply voltage greater than the source voltage of the high side MOSFET, required for N-channel MOSFETs.

Internal synchronous rectification control circuitry is provided to improve power dissipation in the external MOSFETs during PWM operation. Internal circuit protection includes latched thermal shutdown, dead time protection, and undervoltage lockout. Special power up sequencing is not required.

The A4915 is supplied in a 28-pin TSSOP with an exposed thermal pad (suffix LP) and a 28-contact 5 × 5 mm QFN with an exposed thermal pad (suffix ET). These packages are lead (Pd) free, with 100% matte-tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Package	Packing*
A4915METTR-T	28-contact QFN with exposed thermal pad	1500 pieces per 7-in. reel
A4915MLPTR-T	28-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel

Absolute Maximum Ratings

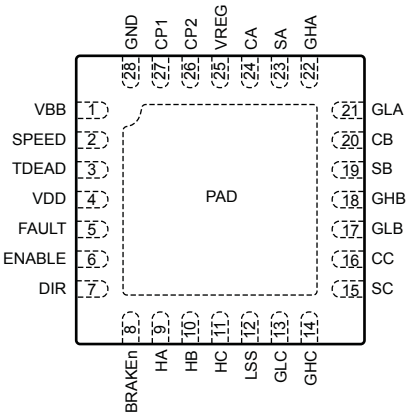
Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 6	V
VREG Pin	V_{REG}		–0.3 to 16	V
CP1 Pin	V_{CP1}		–0.3 to 16	V
CP2 Pin	V_{CP2}		V_{CP1} – 0.3 to V_{REG} + 0.3	V
Logic Inputs	V_I		–0.3 to 6	V
Hall Inputs	V_{Hx}		–0.3 to 6	V
Logic Outputs	V_O		–0.3 to 6	V
SPEED Input	V_{SPEED}		–0.3 to 6	V
CA, CB, and CC Pins	V_{Cx}		–0.3 to V_{REG} + 50	V
GHA, GHB, and GHC Pins	V_{GHx}		V_{Cx} – 16 to V_{CX} + 0.3	V
SA, SB, and SC Pins	V_{Sx}		V_{Cx} – 16 to V_{Cx} + 0.3	V
GLA, GLB, GLC Pins	V_{GLx}		V_{REG} – 16 to 18	V
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Ambient Temperature Range	T_A		–20 to 105	°C

Thermal Characteristics may require derating at maximum conditions, see application information

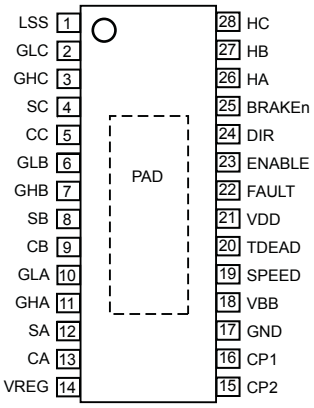
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package ET, on 4-layer PCB based on JEDEC standard	32	ºC/W
		Package LP, on 4-layer PCB based on JEDEC standard	28	ºC/W

*Additional thermal information available on the Allegro website.

Pin-out Diagrams



ET Package



LP Package

Terminal List Table

Name	Function	Number		Name	Function	Number	
		ET	LP			ET	LP
VBB	Supply voltage	1	18	SC	High-side source connection	15	4
SPEED	Reference voltage input	2	19	CC	Bootstrap output phase C	16	5
TDEAD	Terminal for dead time setting	3	20	GLB	Low-side gate drive	17	6
VDD	Logic supply input	4	21	GHB	High-side gate drive	18	7
FAULT	Fault output	5	22	SB	High-side source connection	19	8
ENABLE	Logic input, PWM control	6	23	CB	Bootstrap output phase B	20	9
DIR	Logic input, motor direction	7	24	GLA	Low-side gate drive	21	10
BRAKEn	Logic input, motor brake (active low)	8	25	GHA	High-side gate drive	22	11
HA	Hall input phase A	9	26	SA	High-side source connection	23	12
HB	Hall input phase B	10	27	CA	Bootstrap output phase a	24	13
HC	Hall input phase C	11	28	VREG	Gate drive supply output	25	14
LSS	Sense input	12	1	CP2	Charge pump capacitor terminal	26	15
GLC	Low-side gate drive	13	2	CP1	Charge pump capacitor terminal	27	16
GHC	High-side gate drive	14	3	GND	Ground	28	17
				PAD	Exposed pad for enhanced thermal dissipation	–	–

ELECTRICAL CHARACTERISTICS Valid at T_A = 25°C, V_{BB} = 24 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply and Reference						
Operating Voltage Range	V_{BB}	Operating, outputs active	5.0	–	50	V
Motor Supply Current	I_{BB}	f_{ENB} = 30 kHz, C_{LOAD} = 10 nF	–	10	20	mA
		$f_{PWM} \approx$ 20 kHz, C_{LOAD} = 10 nF	–	12	24	mA
		V_{REG} = 13 V, outputs disabled	–	3	3.5	mA
		Sleep mode	–	–	1	µA
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Current Limit	V_{DBOOT}		250	500	750	mA
VDD Input Voltage	V_{DD}		3	–	5.5	V
VDD Input Current	I_{DDQ}	ENABLE = high, outputs disabled	–	6	10	mA
	I_{DDS}	Sleep mode	–	–	10	µA
ENABLE Input Current Sleep Mode	$I_{ENB(SLP)}$	ENABLE = low for longer than t_{SLEEP}, SPEED = high	–	–	1	µA
SPEED Input Current Sleep Mode	$I_{SPEED(SLP)}$	ENABLE = high, SPEED = low for longer than t_{SLEEP}	–	–	1	µA
BRAKEn Input Current Sleep Mode	$I_{BRAKE(SLP)}$	ENABLE = low for longer than t_{SLEEP}	–	–	1	µA
DIR Input Current Sleep Mode	$I_{DIR(SLP)}$	ENABLE = low for longer than t_{SLEEP}	–	–	1	µA
ENABLE Input Frequency Range	f_{ENB}	$V_{SPEED} = V_{DD}$	1	–	100	kHz
Internal PWM Frequency	f_{PWM}	$V_{ENABLE} = V_{DD}$	14	20	26	kHz
SPEED Input Voltage Range	V_{SPEED}		0	–	V_{DD}	V
SPEED Disable Voltage	$V_{SPEED(D)}$	Measured as V_{SPEED} / V_{DD}, duty cycle = 0%	10	15	20	%
SPEED Enable Voltage*	$V_{SPEED(E)}$	Measured as V_{SPEED} / V_{DD}, duty cycle = 100%	79	82	86	%
SPEED Bias Current	$I_{SPEED(bias)}$	$V_{SPEED} = V_{DD}$= 5 V	–25	0	25	µA
VREG Output Voltage	V_{REG}	V_{BB} = 9 V	11.8	13	13.75	V
		V_{BB} = 7.5 V	11.5	13	13.75	V
		V_{BB} = 6 V	2 × V_{BB} – 3.5 V	–	–	V
		V_{BB} = 5.5 V	8.0	9.5	–	V
Protection						
Thermal Shutdown Temperature	T_{TSD}	FAULT rising	155	170	185	°C
VREG Undervoltage	V_{REGON}	V_{REG} rising	7.0	7.8	8.6	V
	V_{REGOFF}	V_{REG} falling	6.39	7.1	7.81	V
VREG Undervoltage Hysteresis	V_{REGhys}		–	700	–	mV

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ELECTRICAL CHARACTERISTICS (continued) Valid at T_A = 25°C, V_{BB} = 24 V; unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Protection (continued)							
Bootstrap Undervoltage	V_{BOOTUV}	Measured as a percentage of V_{REG}		55	–	65	%
Bootstrap Undervoltage Hysteresis	$V_{BOOTUVhys}$	Measured as a percentage of V_{REG}		–	20	–	%
VDD Undervoltage	V_{DDUV}	V_{DD} rising		–	2.75	2.95	V
		V_{DD} falling		2.45	2.6	–	V
VDD Undervoltage Hysteresis	$V_{DDUVhys}$			50	100	150	mV
Sleep Wake-up Delay	t_{WAKE}			–	–	3	ms
Gate Drive							
High-Side Gate Drive Output	V_{GHx}	C_{BOOTx} fully charged, C_{LOAD} = 10 nF		V_{Cx} – 0.2	–	–	V
		I_{GHx} < 10 µA		–	–	V_{Sx} + 0.3	V
Low-Side Gate Drive Output	V_{GLx}	V_{REG} = 13 V, C_{LOAD} = 10 nF		V_{REG} – 0.2	–	–	V
		I_{GLx} < 10 µA		–	–	0.3	V
Gate Drive Pull-Up Resistance	$R_{GHx(ON)UP}$	T_J = 25°C, I_{GHx} = –150 mA		6	9	12	Ω
		T_J = 125°C, I_{GHx} = –150 mA		–	17	–	Ω
Gate Drive Pull-Down Resistance	$R_{GLx(ON)DN}$	T_J = 25°C, I_{GLx} = –150 mA		2.4	3.5	4.6	Ω
		T_J = 125°C, I_{GLx} = –150 mA		–	5	–	Ω
GHx Passive Pull-Down	$R_{GHx(PPD)}$	V_{GHx} – V_{Sx} < 0.3 V		–	5000	–	Ω
GLx Passive Pull-Down	$R_{GLx(PPD)}$	V_{GLx} – V_{LSS} < 0.3 V		–	5000	–	Ω
Output Switching Time	t_{rGx}	20% to 80%, C_{LOAD} = 10 nF		–	200	–	ns
	t_{fGx}	80% to 20%, C_{LOAD} = 10 nF		–	150	–	ns
Dead Time	t_{DEAD}	Time delay measured from turn-off to turn-on	TDEAD tied to GND	10	–	–	ns
			R_{TDEAD} = 12 kΩ	–	150	–	ns
			R_{TDEAD} = 64 kΩ	800	925	1050	ns
			R_{TDEAD} = 220 kΩ	–	2.9	–	µs
Logic I/O							
Logic Input Voltage	$V_{IN(H)}$	BRAKEn, DIR, ENABLE, HA, HB, and HC pins		0.7 × V_{DD}	–	–	V
	$V_{IN(L)}$			–	–	0.3 × V_{DD}	V
Logic Input Current	$I_{IN(H)}$	V_{IN} = high		–	10	–	µA
	$I_{IN(L)}$	V_{IN} = low, ENABLE = low		–1	0	1	µA
FAULT Output Voltage	V_{FAUlT}	No fault present, I_{SINK} = 1mA		–	–	0.2	V
ENABLE and SPEED Sleep Timer	t_{SLEEP}	ENABLE = low, SPEED = high		1	2	3	ms
		ENABLE = high, SPEED = low		1	2	3	ms

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) Valid at T_A = 25°C, V_{BB} = 24 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic I/O (continued)						
SPEED Sleep Threshold	$V_{SPEEDSLPth}$	SPEED = low for longer than t_{SLEEP}	–	–	295	mV
Fault Latch Reset Voltage	V_{RESET}	Fault is present, outputs latched	–	–	0.8	V
Fault Latch Reset Pulse Time	t_{FAULT}	Fault is present, outputs latched	12	–	–	µs
Hall Input Pull-Up Resistor	$R_{Hx(PU)}$	Hx pins, V_{IN} = 0 V	–	100	–	kΩ
Hall Input Current	I_{HALL}	Hx pins, V_{IN} = 5 V	–	0	1	µA
Logic Input Pull-Down Resistor	$R_{IN(PD)}$	ENABLE, DIR, BRAKEn, V_{IN} = 5 V	–	50	–	kΩ
Login Input Current Sleep Mode	$I_{IN(SLP)}$	ENABLE, DIR, BRAKEn	–	–	1	µA
Propagation Delay	$t_{pd(on)}$	DIR or BRAKEn input to output change, C_{LOAD} = 0 nF	–	–	1200	ns
		ENABLE input to output change, C_{LOAD} = 0 nF	–	–	900	ns
	$t_{pd(off)}$	DIR or BRAKEn input to output change, C_{LOAD} = 0 nF	–	–	1200	ns
		ENABLE input to output change, C_{LOAD} = 0 nF	–	–	900	ns
Input Pin Glitch Reject	t_{glitch}	ENABLE	–	–	900	ns
		DIR, BRAKEn	–	–	1000	ns

*Output duty cycle limited by t_{DEAD}.

Functional Description

Basic Operation

The A4915 is a 3-phase MOSFET driver intended to drive high current MOSFETs. It is designed for use in battery operated equipment where low-voltage operation is critical. The A4915 also features a low current sleep mode which disables the device and draws minimum supply current. The A4915 is capable of driving 6 N-channel MOSFETs. Commutation logic includes Enable, Direction, and Brake modes for external PWM control.

A Speed input is provided which allows an external source to PWM the bridge at 30 kHz typical. The PWM duty cycle is controlled by applying an analog voltage to the SPEED pin from 0 V to V_{DD}.

Pin Descriptions

DIR The Direction pin is used to change the commutation direction of the 3 bridges. Refer to table 1 for phase commutation information.

ENABLE The ENABLE input terminal allows external PWM control. Setting ENABLE high turns on the selected sink-source pair, and setting it low switches off the appropriate drivers and the load current decays. If external PWM is used, the SPEED pin must be tied to VDD.

When the ENABLE input is held low for longer than t_{SLEEP} the A4915 turns off all internal circuitry and draws minimum current from the supply. When coming out of sleep allow 3 ms for the charge pump regulator to stabilize.

SPEED The duty cycle of the internally generated carrier frequency is controlled by applying a DC voltage on the SPEED input. A plot showing the relationship of Speed to duty cycle is shown in figure 1. When SPEED is pulled directly to VDD the internal carrier is disabled and the Enable input can be used to PWM the bridge. When $V_{SPEED} < V_{SPEED(D)}$ the output is guaranteed to be 0%. When $V_{SPEED} > V_{SPEED(E)}$ the output is guaranteed to be 100%.

BRAKEn Brake mode turns all three sink drivers on and effectively shorts out the motor generated BEMF. The BRAKEn input overrides the ENABLE and SPEED inputs except when in Sleep mode. Refer to table 2 for the logic truth table. In order to comply with Failure Mode Effects and Analysis (FMEA), the brake function is normally active (logic low). If the BRAKEn pin on the device is open due to some failure of solder joint or microprocessor failure, the device will automatically implement Brake mode, preventing the motor from turning or pumping up the supply. Applying logic high to the BRAKEn terminal deactivates Brake mode and allows normal operation.

Care must be taken when applying the Brake command because large currents can be generated. The user must ensure that the maximum ratings of the MOSFETs are not exceeded under worst

Table 1. Commutation Table

	HA	HB	HC	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	1	0	1	1	0	0	1	1	0	0	High	–	Low
2	1	0	0	1	0	0	1	0	1	0	–	High	Low
3	1	1	0	1	1	0	0	0	1	0	Low	High	–
4	0	1	0	1	1	0	0	0	0	1	Low	–	High
5	0	1	1	1	0	1	0	0	0	1	–	Low	High
6	0	0	1	1	0	1	0	1	0	0	High	Low	–
1	1	0	1	0	1	0	0	0	0	1	Low	–	High
2	1	0	0	0	0	1	0	0	0	1	–	Low	High
3	1	1	0	0	0	1	0	1	0	0	High	Low	–
4	0	1	0	0	0	0	1	1	0	0	High	–	Low
5	0	1	1	0	0	0	1	0	1	0	–	High	Low
6	0	0	1	0	1	0	0	0	1	0	Low	High	–
Hall Fault	1	1	1	X	0	0	0	0	0	0	–	–	–
Hall Fault	0	0	0	X	0	0	0	0	0	0	–	–	–

case braking conditions. Maximum motor current during Brake mode can be approximated by:

$$I_{BRAKEn} = V_{BEMF} / R_L$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding.

VREG A regulated voltage output that is used to supply the low-side gate drivers and to charge the bootstrap capacitors.

FAULT The Fault output is active high. Under normal operation the open drain output pulls the Fault output to ground. When a fault occurs the open drain output is released, and the Fault output is then pulled to a logic high through a connected external passive pullup resistor. Fault conditions are shown in table 3.

The presence of an invalid Hall combination is referred to as a *Hall Fault*. Invalid Hall combinations are documented in table 1. When a Hall Fault is present, the outputs are disabled. Invalid Hall Faults are not latched, and do not affect the state of the FAULT pin. Latched faults that result in disabled outputs can be reset in a number of ways:

- A UVLO on VDD will serve as a reset
- If the device is put into sleep mode the latch is reset
- A microprocessor can create a reset on the FAULT pin directly by forcing V_{RESET} on the FAULT pin when a fault is active for longer than t_{FAULT} (that is, when the outputs are latched)

LSS The LSS terminal is the low-side drain connection for the MOSFET. If an external PWM current control loop is used, a low

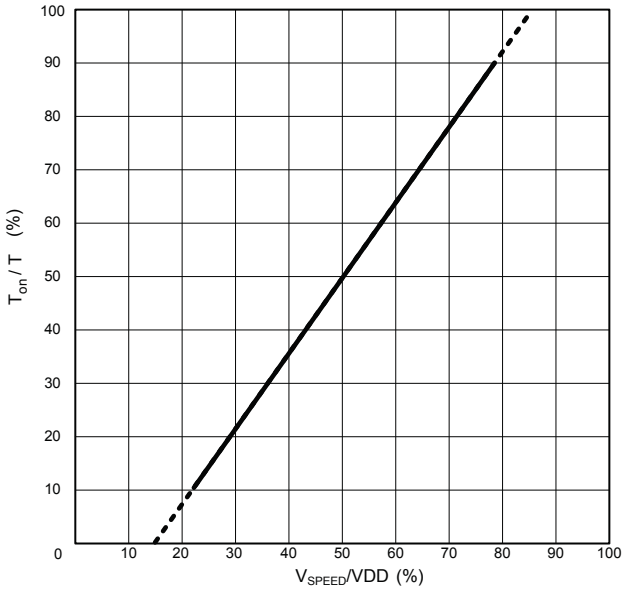


Figure 1. Speed in relation to duty cycle

Table 3. Fault Conditions

Event	Fault Pin	Outputs	Latched
TSD	High	Disabled	Yes
SLEEP	High	Disabled	No
UVLO VREG/VDD	High	Disabled	No
Invalid Hall	Low	Disabled	No

Table 2. Input Logic Truth Table

Inputs			Mode of Operation
ENABLE	SPEED	BRAKEn	
Low	High	High	PWM chop slow decay synchronous rectification (center aligned)
Low	High	Low	Brake mode – All low-side gates on
High	High	High	Selected drivers on[b]
High	High	Low	Brake mode – All low-side gates on
High	$V_{DD} \times V_{SPEED(E)}$ to $V_{DD} \times V_{SPEED(D)}$	High	PWM chop slow decay synchronous rectification (center aligned)[c]
High	$> V_{DD} \times V_{SPEED(E)}$	High	Selected drivers on[b]
High	$< V_{DD} \times V_{SPEED(D)}$	High	PWM chop slow decay synchronous rectification (center aligned)
Low longer than t_{SLEEP}	High	X[a]	Sleep mode – coast
High	Low longer than t_{SLEEP}	X[a]	Sleep mode – coast

[a]X = don't care.
[b]Maximum and minium duty cycle limited by boot capacitor charge management.
[c]Internal PWM active.

value sense resistor can be placed from LSS to ground for current sensing purposes, otherwise LSS should be connected directly to power ground.

CA, CB, CC High-side connections for the bootstrap capacitors (CBOOTx) and positive supply for high-side gate drive.

GHA, GHB, GHC High-side gate drive outputs for N-channel MOSFETs.

SA, SB, SC Motor phase connections, serve as the negative supplies for the high-side gate drive.

GLA, GLB, GLC Low-side gate drive outputs for N-channel MOSFETs.

CP1, CP2 Connections for the charge pump switching capacitor. Typical capacitance should be 0.47 µF.

HA, HB, HC Hall input connections from Hall switches at the motor.

Thermal Shutdown

If the die temperature exceeds T_{TSD}, the FAULT output is turned off and the outputs are disabled. Thermal shutdown is a latched fault.

Dead Time

To prevent cross-conduction (shoot through) in any phase of the bridge, it is necessary to have a dead time, t_{DEAD}, between a high- or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead time resistor (R_{DEAD}) between the TDEAD pin and ground.

For R_{DEAD} values between 12 and 220 kΩ, at 25°C the nominal value of t_{DEAD} in ns can be approximated by:

$$t_{DEAD} = 40 + (1.28^{-2} \times R_{DEAD})$$

Current, I_{DEAD}, can be calculated by:

$$I_{DEAD} = 1.2 / R_{DEAD}$$

As values for R increase, current offsets and resistor mismatch cause the error terms to increase. Figure 2 shows the typical expected error for a given R_{DEAD} value.

Sleep Mode

The A4915 has a low-current Sleep mode to limit current draw on the battery. When in low-current Sleep mode (when ENABLE = low for longer than t_{SLEEP} and SPEED = high), current into VBB and VDD is less than 1 µA.

When ENABLE is held low for longer than t_{SLEEP} and the SPEED input is held high, the pull-up resistors on the Hall inputs and the pull-down resistor on the BRAKEn pin are open-circuited to minimize current draw into logic input terminals. Only the condition where SPEED = high and ENABLE = low for longer than t_{SLEEP} results in low current on logic input terminals.

Center Aligned PWM

The A4915 features center aligned PWM, which improves power dissipation and helps reduce EMI. During an off-time triggered by either an internal PWM or by an external Enable chop command, current recirculation will be in either the high-side FETs or the low-side FETs, depending on the state of an internal latch. On each bridge Enable command, the latch is reset and the current recirculation shifts from high-side recirculation to low-side recirculation.

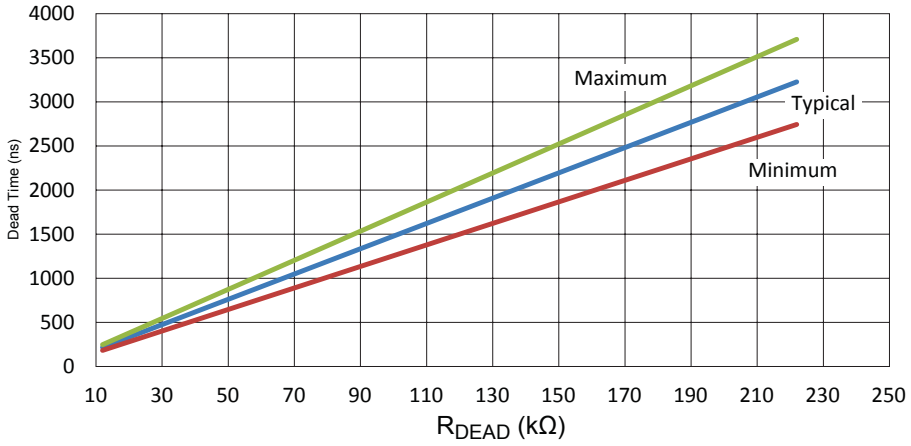


Figure 2. R_{DEAD} versus Dead Time Error

This method of recirculation shifts 50% of the power to the high-side drivers during the off-time, reducing the power dissipation in the sink drivers. Reducing the overall temperature of the output drivers by sharing power between the 6 FETs improves system efficiency and battery life.

Internal/External PWM

The A4915 can be pulse width modulated (PWM) to control current. There are two methods by which PWM can be applied to the device.

- External PWM. This method requires a PWM signal be applied to the ENABLE pin. When the SPEED pin is tied directly to VDD, the ENABLE pin can be chopped from 0 to 100%. If the ENABLE input is held low for more than sleep timer, t_{SLEEP}, the device enters low current sleep mode.
- Internal PWM. This method uses the internally generated PWM, which is controlled by applying a DC voltage to the SPEED pin. When the ENABLE pin is tied directly to VDD, the speed can be controlled from 0 to 100%. See the SPEED pin description for further information.

For complete description of all operating conditions, see table 2.

Synchronous Rectification

When a PWM off-time cycle is triggered by an ENABLE chop command or by an internal PWM off-time, load current recirculates. The A4915 synchronous rectification feature will turn on the appropriate MOSFETs during the off-time and effectively short out the body diodes with the low $R_{SD(on)}$ driver. This will lower power dissipation significantly and eliminates the need for external Schottky diodes.

Charge Pump Regulator

The gate drives for the low-side MOSFETs and the bootstrap charge for the high-side drivers is accomplished by the charge pump regulator. For V_{BB} above 16 V, the regulator acts as a linear regulator. Below 16 V, the regulated supply is maintained by a charge pump boost converter that requires a pump capacitor between CP1 and CP2.

The regulated voltage VREG is decoupled on the VREG terminal. The decoupling capacitance is based on the bootstrap capacitor which is dependent on the MOSFET selection. Refer to the Application Information section for details on correct sizing of VREG and bootstrap capacitors.

Gate Drive and RGATE

The gate drive for the external MOSFETs is capable of providing the large current transients needed to quickly charge and discharge the gate capacitance to maintain fast switching speeds and minimal power dissipation. The low-side driver current is sourced by the capacitor on the VREG terminal. The high-side gate drive current is supplied by the respective bootstrap capacitance connected between the Cx and Sx terminals. The charge and discharge of the gate can be controlled by using an external resistor (R_{GATE}) in series with the gate.

Bootstrap Charge Management

In order to protect the external MOSFETs from insufficient gate drive, it is important that the bootstrap capacitor voltage be monitored. Before a high-side switch is allowed to turn on, it must have sufficient charge on the bootstrap capacitor. If the voltage on the bootstrap capacitor is below the turn-on voltage limit, the A4915 will attempt to charge the bootstrap capacitor by turning on the associated low-side driver. The bootstrap monitor stays active during the duration of the switch on-time. If the voltage falls out of compliance at any time when the high-side driver is enabled, the driver is disabled and the low-side switch is activated to charge the bootstrap capacitor.

During normal operation and in conditions where the PWM duty cycle creates short off-times, the low-side switch may be activated more often to keep sufficient charge on the bootstrap capacitor. Proper sizing of the bootstrap and VREG capacitors is critical to being able to maintain effective gate drive. Refer to the Application Information section for details on correct sizing of VREG and bootstrap capacitors.

Application Information

Bootstrap Capacitor Selection

In order to properly size the capacitor CBOOT, the total gate charge must be known. Too large a bootstrap capacitor and the charge time will be long, resulting in maximum duty cycle limitation. Too small a capacitor and the voltage ripple will be large when charging the gate.

Size the CBOOT capacitor such that the charge, Q_{BOOT}, is 20 times larger than the required charge for the gate of the MOSFET, Q_{GATE}:

$$C_{BOOT} = (Q_{GATE} \times 20) / V_{BOOT}$$

where V_{BOOT} is the voltage across the bootstrap capacitor. The voltage drop across the bootstrap capacitor as the MOSFET gate is being charged, ΔV, can be approximated by:

$$\Delta V = Q_{GATE} / C_{BOOT}$$

For the bootstrap capacitor, a ceramic type rated at 16 V or larger should be used.

VREG Capacitor Selection

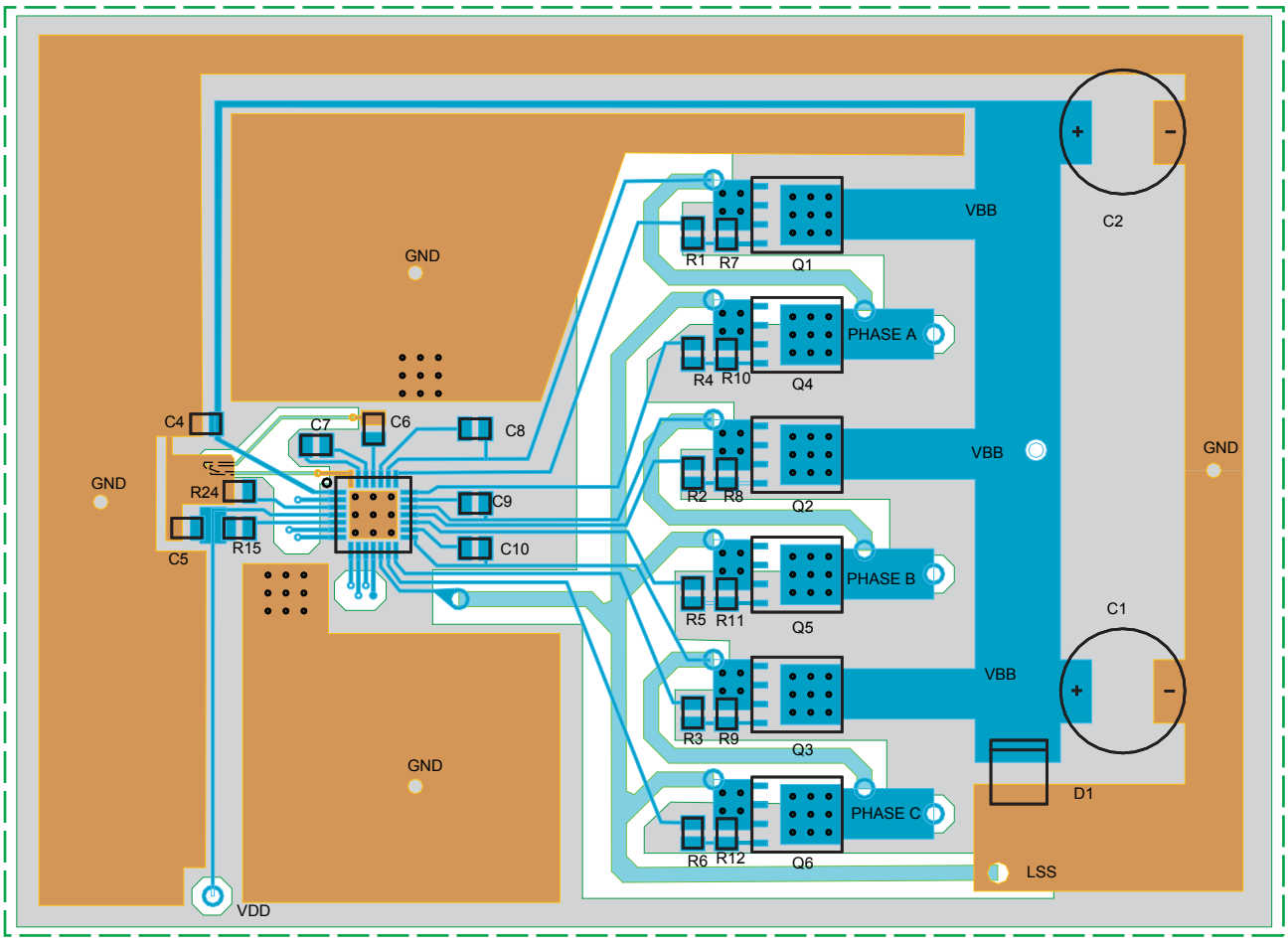
VREG is responsible for providing all the gate charge for the low side MOSFETs and for providing all the charge current for the three bootstrap capacitors. For these purposes, the VREG capacitor, C_{REG}, should be 20 times the value of C_{BOOT}:

$$C_{REG} = 20 \times C_{BOOT}$$

Layout Recommendations

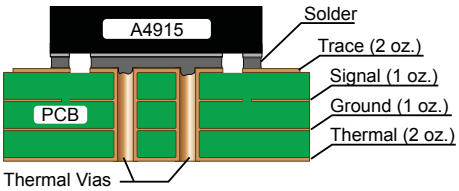
Careful consideration must be given to PCB layout when designing high frequency, fast-switching, high-current circuits (refer to figures 3 and 4):

- The A4915 ground, GND, and the high-current return of the external MOSFETs should return separately to the negative side of the motor supply filtering capacitor. This minimizes the effect of switching noise on the A4915.
- The exposed thermal pad should be connected to GND.
- Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This minimizes voltages induced by fast switching of large load currents.
- Consider the use of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs, to limit fast transient voltage spikes caused by inductance in the traces.
- Keep the gate discharge return connections Sx and LSS as short as possible. Any inductance on these traces causes negative transitions on the corresponding A4915 terminals, which may exceed the Absolute Maximum Ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to GND.
- Supply decoupling for VBB, VREG, and VDD should be connected independently, close to the GND terminal. The decoupling capacitors should also be connected as close as possible to the relevant supply terminal.
- Gate charge drive paths and gate discharge return paths may carry large transient current pulses. Therefore the traces from GHx, GLx, Sx (x = A, B, or C) and LSS should be as short as possible to reduce the inductance of the trace.
- Provide an independent connection from LSS to the common point of the power bridge. This can be the negative side of the motor supply filtering capacitor or one end of a sense resistor. It is not recommended to connect LSS directly to the GND terminal, as this may increase the noise at the digital inputs.



ET Package Typical PCB Layout

ET Package Schematic Corresponding to Typical PCB Layout



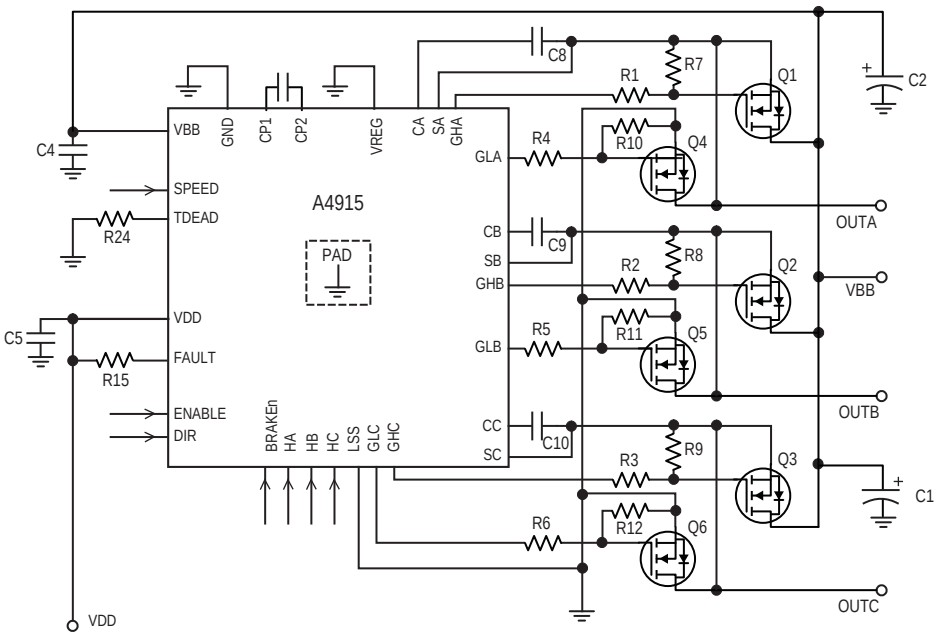
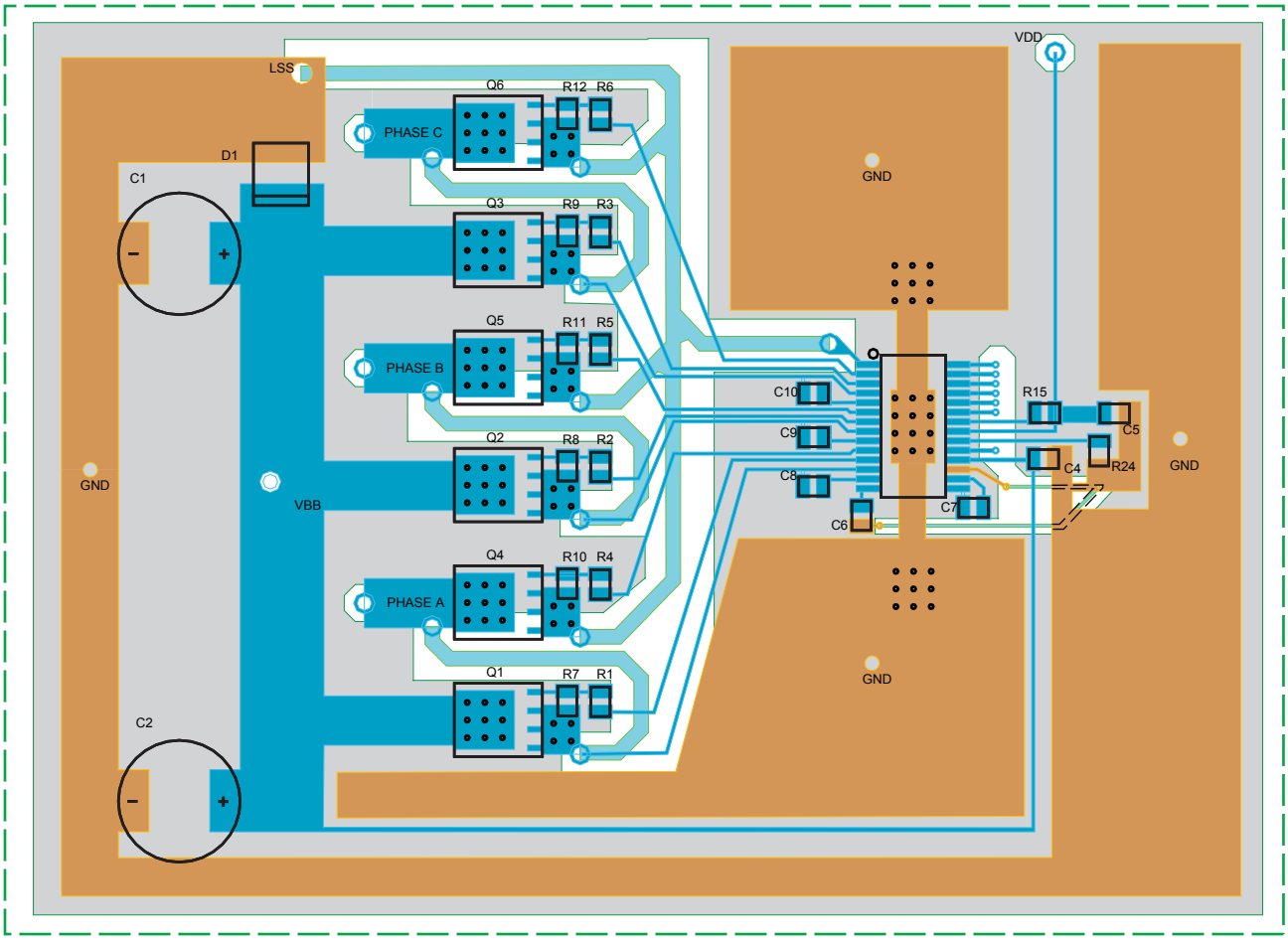
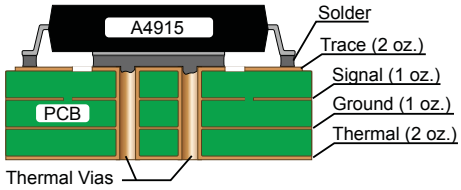


Figure 3. Typical application information for ET package



LP Package Typical PCB Layout

LP Package Schematic Corresponding to Typical PCB Layout



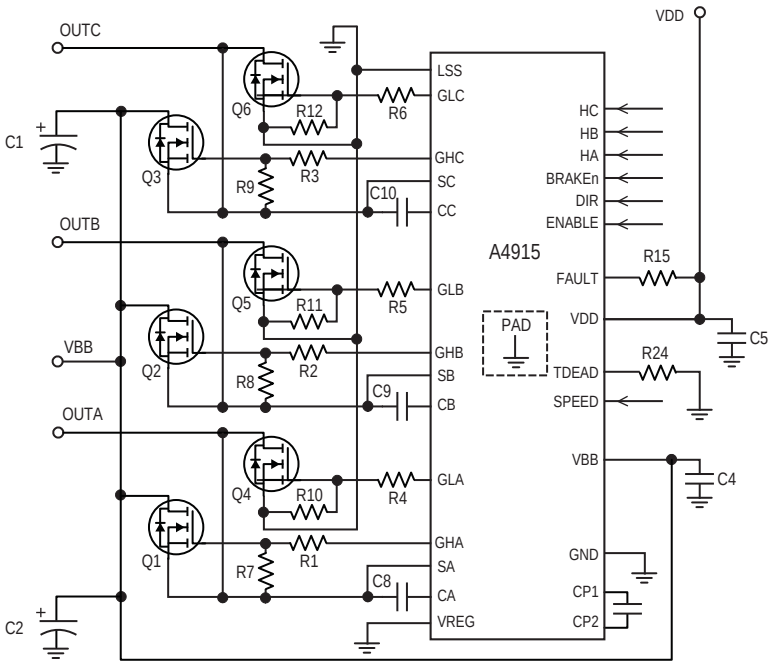


Figure 4. Typical application information for LP package

Input / Output Structures

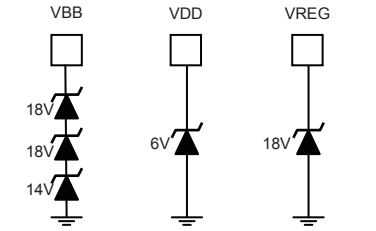


Figure 5. Supplies

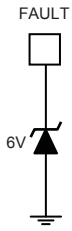


Figure 6. Fault output

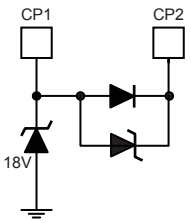


Figure 7. Charge pump

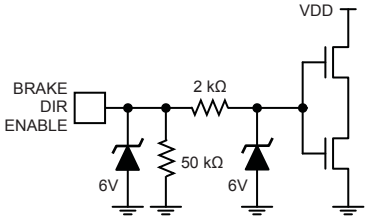


Figure 8. Logic inputs with pull-down: BRAKEn, DIR, ENABLE

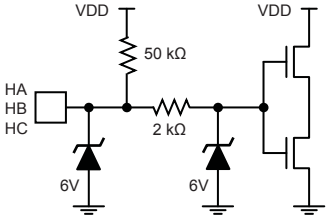


Figure 9. Hall inputs with pull-up: HA, HB, HC

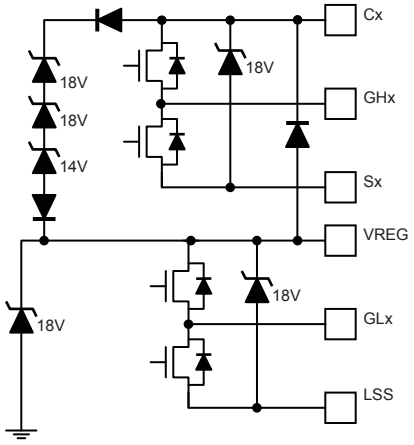


Figure 10. Gate drive outputs

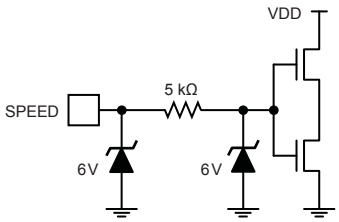
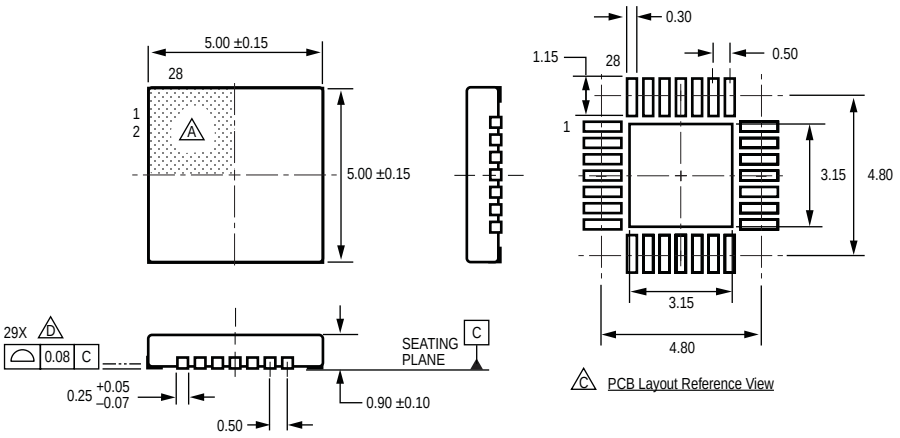
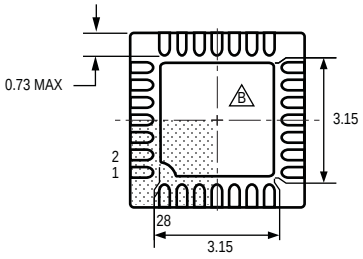


Figure 11. Speed input

Package ET, 28-Pin QFN with Exposed Thermal Pad





For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

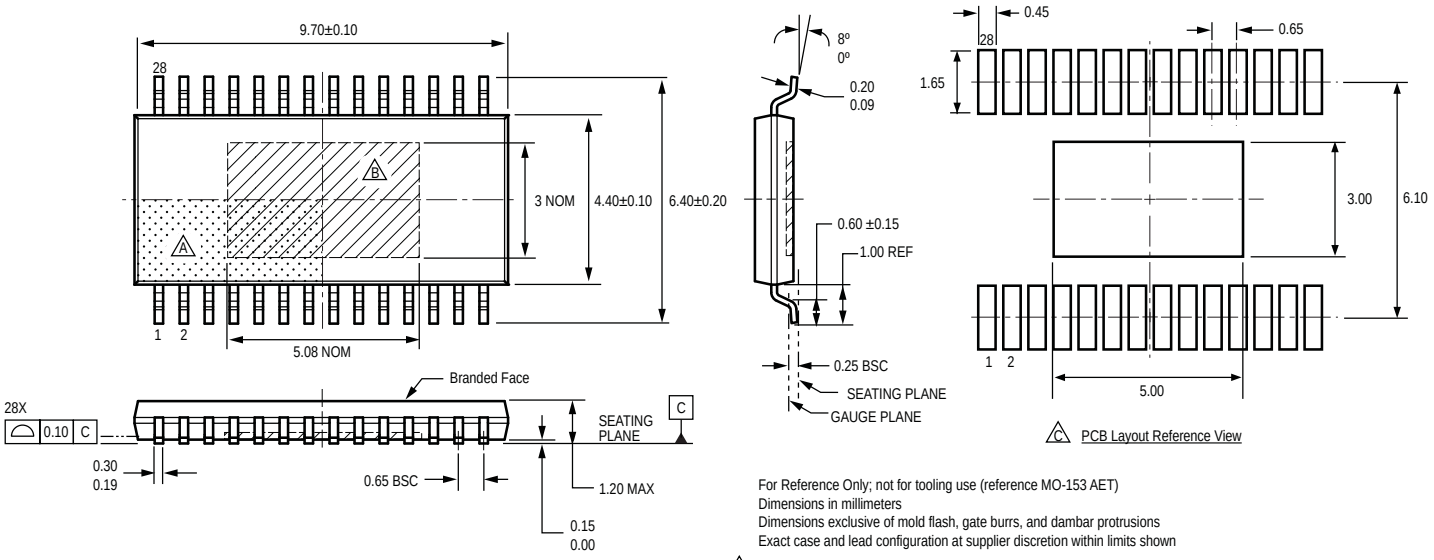
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package LP, 28-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Current Revision Date	Description of Revision
Rev. 1	April 1, 2013	Update EC table parameters

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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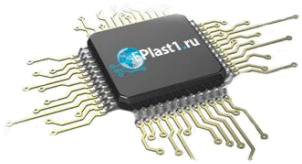
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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