GPS RADIONOVA® RF Antenna Module

Part No. M10382

Product Specification

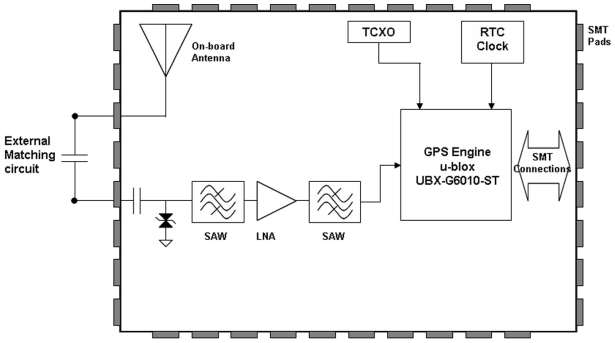
Applications

- **Personal Navigation Devices (PNDs)**
- **Portable Media Players (PMPs)**
- **Personal Digital Assistants (PDAs)**
- **Feature phones / Smart phones**
- **Tablet PCs / eReaders**
- **Asset Tracking / Personal Safety**

Features

- Low cost single package GPS RF antenna module
- u-blox 6 GPS Position Engine
- Low 3.9mm height for thin devices
- Low current consumption
- Easy to use 'drop-in solution'
- Novel external matching ensure easy tuning for each platform
- Anti-jamming technology

Functional Block Diagram



Product Description

Antenova M2M's GPS RADIONOVA® M10382 is a single package solution that combines a full GPS engine and antenna on a small SMD module. The M10382 is a highly integrated GPS RF Antenna Module suitable for L1-band GPS and A-GPS systems. The device combines the high performance u-blox 6 GPS position engine with Antenova's high efficiency antenna technology in a small SMD module. M10382 also benefits from novel external matching that ensures easy tuning for each platform.

All front-end and receiver components are contained in a single package laminate base module, providing a complete GPS receiver for optimum performance. The M10382 operates on 1.8V or 3.3V positive supply with low power consumption and several low power modes for further power savings. An accurate 0.5ppm TCXO and very low noise LNA ensures high sensitivity and short TTFF. The M10382 is supported by u-blox stand alone software and is compatible with UART, SPI, DDC, I²C and USB host processor interfaces.

Package Style

24.2 x 9.9mm RF Antenna Module

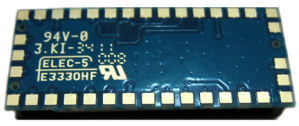
Top View



Component side view (w/o shielding can)



Bottom View



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Main Supply Voltage	-0.5	3.6	V
V_BCKP	Battery backup voltage	-0.5	3.6	V
VIO	Supply voltage I/O ring	-0.5	3.6	V
VDD_USB	Supply voltage USB	-0.5	3.6	V
V_TH	Input Voltage Reset Threshold level	-0.5	3.6	V
VI_{DIG}	Input Voltage on any digital I/O pin with respect to ground	-0.5	3.6	V
LNA_IN	RF Input Power at ANT_IN		-25	dBm
T_{STG}	Storage Temperature	-40	+125	°C
I_{PIN}	DC Current through any digital I/O pin (except supplies)		10	mA
P_{TOT}	Total Power Dissipation		500	mW
ESD	Electrostatic Discharge Immunity (HBM)	-2.0	+2.0	kV

* Exposure to absolute ratings may adversely affect reliability and may cause permanent damage.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Temperature	-40	+25	+85	°C
VCC (1V8)	1V8 Supply Voltage Mode	1.75	1.8	1.89	V
VCC (3V3)	3V3 Supply Voltage Mode	2.5	3.3	3.6	V
VCC (USB)	USB Supply Voltage Mode	2.5	3.3	3.6	V
V-BCKP	Battery backup voltage	1.4		3.6	V
VIO	Supply voltage I/O ring	1.65	3.3	3.6	V
VDD_USB	Supply voltage USB	3.0	3.3	3.6	V

DC Electrical Characteristics

Conditions: Ta = 25 °C

Symbol	Parameter	Min	Typ	Max	Unit
ICC_{ACQ}	Total Supply Current - Acquisition Mode		52 †		mA
ICC_{TRK}	Tracking - Max Performance Mode		45 †		mA
	Tracking - Eco Mode		42 †		mA
	Tracking - Power Save Mode		22 ††		mA
I_{BCKP}	Battery backup current		25		µA

† Current consumption is very dynamic and can peak at 100mA. The value given is the average over 1 minute.

†† At 1fix/s

RF Specifications

Conditions: VCC = 1.8V, T_A = 25 °C

Symbol	Parameter	Typ	Unit
G_{LNA}	LNA Gain	20	dB
NF_{LNA}	LNA Noise Figure	0.7	dB
P_{1dB}	In band 1dB Compression Point	-15.5	dBm
ANT_{RL}	Antenna Return Loss	>10	dB
ANT_{BW}	Antenna Bandwidth at 10dB return loss	20	MHz
ANT_{EFF}	Antenna Total Efficiency	>40%	%
ANT_{EFF_RHCP}	Antenna RHCP Efficiency	>30%	%

Band Rejection*

Frequency	Standard	Typ*	Unit
698-798	LTE700	50	dB
824-849	Cellular CDMA	55	dB
869-894	GSM850	55	dB
880-915	GSM900	60	dB
1710-1785	GSM1800/DCS	33	dB
1850-1910	GSM1900/PCS	30	dB
1920-1980	WCDMA	30	dB
2400-2492	WLAN, BT and WiMAX	30	dB
2500-2690	LTE2600	30	dB

*Rejection before LNA. Does not include antenna rejection.

Digital I/O

Symbol	Paramater	Condition	Min	Typ	Max	Unit
I_{leak}	Leakage current input pins			<1		nA
V_{IL}	Low Level Input Voltage		0		0.2*VIO	V
V_{IH}	High Level Input Voltage		0.7*VIO		VIO	V
V_{OL}	Low Level Output Voltage	I_{OL}=4mA			0.4	V
V_{OH}	High Level Output Voltage	I_{OH}=4mA	VIO - 0.4V		-	V
R_{PU_IIC}	Pull-up resistor for PIO0...3			13		kΩ
R_{PU}	Pull-up resistor			115		kΩ
R_{PD}	Pull-down resistor			87		kΩ

Symbol	Paramater	Condition	Min	Typ	Max	Unit
I_{leak}	Leakage current input pins			<1		nA
V_{IL}	Low Level Input Voltage	VDD_USB >= 3.0V	0		0.8	V
V_{IH}	High Level Input Voltage	VDD_USB >= 3.0V	2.0		VDD_USB	V
V_{OL}	Low Level Output Voltage	RL = 14.25 kΩ to VDD_USB, VDD_ USB > = 3.0V, 22 Ω external series resister			0.3	V
V_{OH}	High Level Output Voltage	RL = 14.25 kΩ to VDD_USB, VDD_ USB > = 3.0V, 22 Ω external series resister	2.8			V
R_{PUI}	Pull-up resistor, Idle State		900	1200	1575	Ω
R_{PUO}	Pull-up resistor, Operational State		1425	1925	3090	Ω

Mechanical Specifications

Parameter	Typ	Unit
Module exterior dimensions (L x W x H)	24.2 (+/-0.1) x 9.9 (+0.3 / -0.0) x 3.8 (+0.2 / - 0.0)	mm
Module support and connection	Suface mounted, 36 pin	-
Module mass	1.1	g

System Specifications

Communication	Specification
Data Output Protocol	NMEA 0183 (2.3, compatible to 3.0) and/or UBX (u-blox Binary)
Host Interfaces	UART (4.8 kb/s to 115 kb/s)
	USB 2.0 FS (12Mb/s)
	SPI (slave)
	DDC (I2C compatible)
Default data rate on UART	9.6kb/s
Serial port settings	8 Data bits, No Parity, 1 Stop bit

Accuracy of Time Pulse signal	
RMS	30 ns
99%	<60 ns
Time Pulse	Configurable f = 0.25 Hz ... 1 kHz (TP = 1/f = 4 s ... 1ms)
GPS Engine	
Chip	u-blox 6 UBX-G6010-ST
Firmware Version	FW v7.03 or higher
TCXO	26MHz, 0.5ppm
Channels	Up to 50 Channels
Accuracy	
Horizontal Position Accuracy[1]	2.5m CEP
Maximum Position Update Rate	5 Hz
Velocity Accuracy[2]	0.1m/s
Heading Accuracy[2]	0.5°
Sensitivity	
Autonomous Acquisition	-148dBm
Tracking	-162Bm
TTFF	
Hot Start	1s
Warm Start	6s (typical)
Cold Start[3]	32s at 50% probability
	37s at 90% probability
General	
Maximum Altitude[4]	50000m
Maximum Speed	514 m/s
Active Jammer Remover	Removes in-band jammers up to 80 dB-Hz Tracks up to 8 CW jammers
A-GPS Support	AssistNOW Online AssistNOW Offline AssistNOW Autonomous OMA and SUPL Compliant
Additional Features	SBAS, WAAS, EGNOS, MSAS, GAGAN Support

[1] 50% CEP, Open-Sky, 24hr Static, good view of the sky

[2] 50% at 30m/s

[3] With good view of the sky

[4] Assuming airborne <4g platform

Quality and Environmental Specifications

Test	Standard	Parameters
PCB Inspection	IPC-6012B, Class 2. Qualification and Performance Specification for Rigid Printed Boards - Jan 2007	
Assembly Inspection	IPC-A-610-D, Class 2 “Acceptability of electronic assemblies”	
Temperature Range	ETSI EN 300 019-2-7 specification T 7.3	-30 °C, +25 °C, +85 °C, operating
Damp Heat	ETSI EN 300 019-2-7 specification T 7.3	+70 °C, 80% RH, 96 hrs, non-operating
Thermal Shock	ETSI EN 300 019-2-7 specification T 7.3 E	-40 °C ... +85 °C, 200 cycles
Vibration	ISO16750-3	Random vibration, 10~1000Hz, 27.8m/s², 8hrs/axis, X, Y, Z 8hrs for each 3 axis non-operating
Shock	ISO16750-3	Half-sinusoidal 50g, 6ms, 10time/face, ±X, ±Y and ±Z non-operating
Free Fall	ISO16750-3	1m height, 2 drops on opposite side
ESD Sensitivity	JEDEC, JESD22-A114 ESD Sensitivity Testing Human Body Model (HBM). Class 2 JEDEC, JESD22-A115 ESD Sensitivity Testing Machine Model (MM), Class B	+2000V - Human hand assembly +200V - Machine automatic final assembly
Shear	IEC 60068-2-21, Test Ue3: Shear	Force of 5N applied to the side of the PCB
Moisture/Reflow Sensitivity[1]	IPC/JEDEC J-STD-020D.1	MSL3
Storage (Dry Pack)[1]	IPC/JEDEC J-STD-033C	MSL3
Solderability	EN/IEC 60068-2-58 Test Td	More than 90% of the electrode should be covered by solder. Solder temperature 245 °C ± 5 °C

[1] Moisture Sensitivity

Antenova ships all devices dry packed in trays with desiccant and moisture level indicator sealed in an air tight package.

If on receiving the goods the moisture indicator is pink in color or a puncture of the air tight seal packaging is observed, then follow J-STD-033 “Handling and Use of Moisture/Reflow Sensitive Surface Mount Devices”.

Please note it is a required process for the modules to be pre-baked before reflow for 3 hours at 125ºC. This is due to the integrated antenna. The module can be baked in trays that they come packaged in. When baking, stack no more than 3 trays high to ensure even temperature distribution.

Storage (Dry Packed)

The M10382 modules can be stored for up to 12 months from the date shown on the bag seal when stored in a non-condensing atmospheric environment of <40°C/90% RH.

Storage (Out of Bag)

The M10382 modules meet MSL Level 3 of the JEDEC specification J-STD-020D - 168 hours Floor Life (out of bag) ≤30 °C/60% RH. After opening, all modules must complete the pre-bake process and all solder reflow processing prior to expiry of the stated floor life. If the stated floor life expires prior to reflow process then follow J-STD-033 “Handling and Use of Moisture/Reflow Sensitive Surface Mount Devices”.

Pin out Description

Table 1 shows the designation and function of each pin on the M10382 module. Please note that several pins have multiple functions.

Pin	Designator	Corresponding u-blox full name and description	Power Domain	I/O Reset	I/O Power Off
1	ANT_IN	RF from external matching circuit back into module		Input	Input
2	GND				
3	ANT_OUT	RF from on-board antenna to external matching		Output	Output
4	GND				
5	VIO	DC supply to digital I/O. Sets the voltage used by the I/O. VIO must be supplied in order for the system to boot.	VIO	Input	Input
6	USB_DP	I/O Differential USB D+	VDD_USB		
7	USB_DM	I/O Differential USB D-	VDD_USB		
8	SO	MISO/PIO20/CFG_COM1: • I/O SPI MISO • CFG_COM1 (see Table 4) • PIO20	VIO	Input Pull-up	Input Pull-up
9	CFG_GPS0/ SCK	SPI Clock signal • I/O SPI Clock • CFG_GPS0 to toggle Max performance/ECO mode (see Table 3) • PIO21	VIO	Input Pull-up	Input Pull-up
10	SPI SELECT	PIO6/SS_N/SCSO_N • I/O SPI Chip/Slave Select • PIO6	VIO	Input Pull-up	Input Pull-up
11	TX	PIO5/TXD1 • Output UART1 TxD • PIO6	VIO	Input Pull-up	Input Pull-up
12	V_TH	Reset Threshold Analog	VDD_B		
13	RX	PIO4/RXD1 • Input UART 1 RxD • PIO4 • Wake-up	VIO	Input Pull-up	Input Pull-up
14	GND				
15	V_BCKP	Supplies RTC and back-up RAM	VDD_B		
16	SI	MOSI/PIO19/CFG_COM0: • I/O SPI MOSI • CFG_COM0 (see Table 4) • PIO119	VIO	Input Pull-up	Input Pull-up

17	GND				
18	SDA	PIO2/SDA2 • I/O DDC for perifpherals Serial Data • PIO2	VIO	Input Pull-up	Input Pull-up
19	SCL	PIO3/SCL2 • I/O DDC for peripherals Serial Clock • PIO3	VIO	Input Pull-up	Input Pull-up
20	SAFEBOOT_ N/TDI	• Input JTAG Test • Data In Safe Boot Mode (see Table 1)	VIO	Input Pull-up	Input Pull-up
21	GND				
22	TCK	Input JTAG Test Clock	VIO	Input Pull-up	Input Pull-up
23	TIMEPULSE/ TDO	• Input JTAG Test Data Out • Time Pulse	VIO	Output low	Input Pull-up
24	GND				
25	VDD_RF	Voltage supply to RF unit			
26	GND				
27	VCC	Main DC supply			
28	GND				
29	EXT_ INTERRUPT	PIO7/EXTINTO • Input External Interrupt • Time Mark 0 • PIO7	VIO	Input Pull-up	Input Pull-up
30	V_EN	DCDC_EN • Enables external DC-DC converter	VIO	Output Pull-up	Input Pull-down
31	CFG	CFG_PIN/TMS • CFG_PIN (see Table 2) • JTAG Test mode select	VIO	Input Pull-up	Input Pull-up
32	VDD_USB	USB I/O interface power supply. Connect to ground if USB is not used.	VDD_USB		
33	GND				
34	GND				
35	GND				
36	GND				

Configuration Pins

Some PIO pins are read at system start and can be used to submit some start-up configuration into the boot process. In the following tables, all default settings (pin left open) are **bolded**.

SAFEBOOT Configuration

If it is pulled to low level, the system will start up in safe mode using as few configuration settings as possible and establishing only the minimum functionality reuqired for establishing communication with the host. No GPS operation is started. This mode is primarily used for production testing.

The state of SAFEBOOT_N at system start is preserved in bit BOOTMODE0 of the special function register (SF).

Pin	Designator	Value	GPS Mode
20	SAFEBOOT_N	**1**	Normal boot
		0	Safe Mode, minimal ROM boot, Ignore Backup RAM & FLASH

Table 1: SAFEBOOT_N options

CFG_PIN

The CFG_PIN decides whether external parallel FLASH memory is accessed at all. If the CFG_PIN is left open (i.e. = 1) at power up the receiver reads the configuration from the configuration pins.

The detection of serial FLASH and SPI and serial EEPROM on DDC interfaces is not affected by CFG_PIN. In default, only pin configurations will be read.

The state of CFG_PIN at system start is preserved in bit BOOTMODE1 of the special function register (SF).

Pin	Designator	Value	GPS Mode
31	CFG_PIN	**1**	Use CFG pins
		0	Ignore CFG pins, required setting for parallel FLASH

Table 2: CFG_PIN options

GPS Operation Configuration

Pin	Designator	Value	GPS Mode
9	CFG_GPS0	**1**	Maximum Performance
		0	Eco Mode

Table 3: CFG_GPS0 options

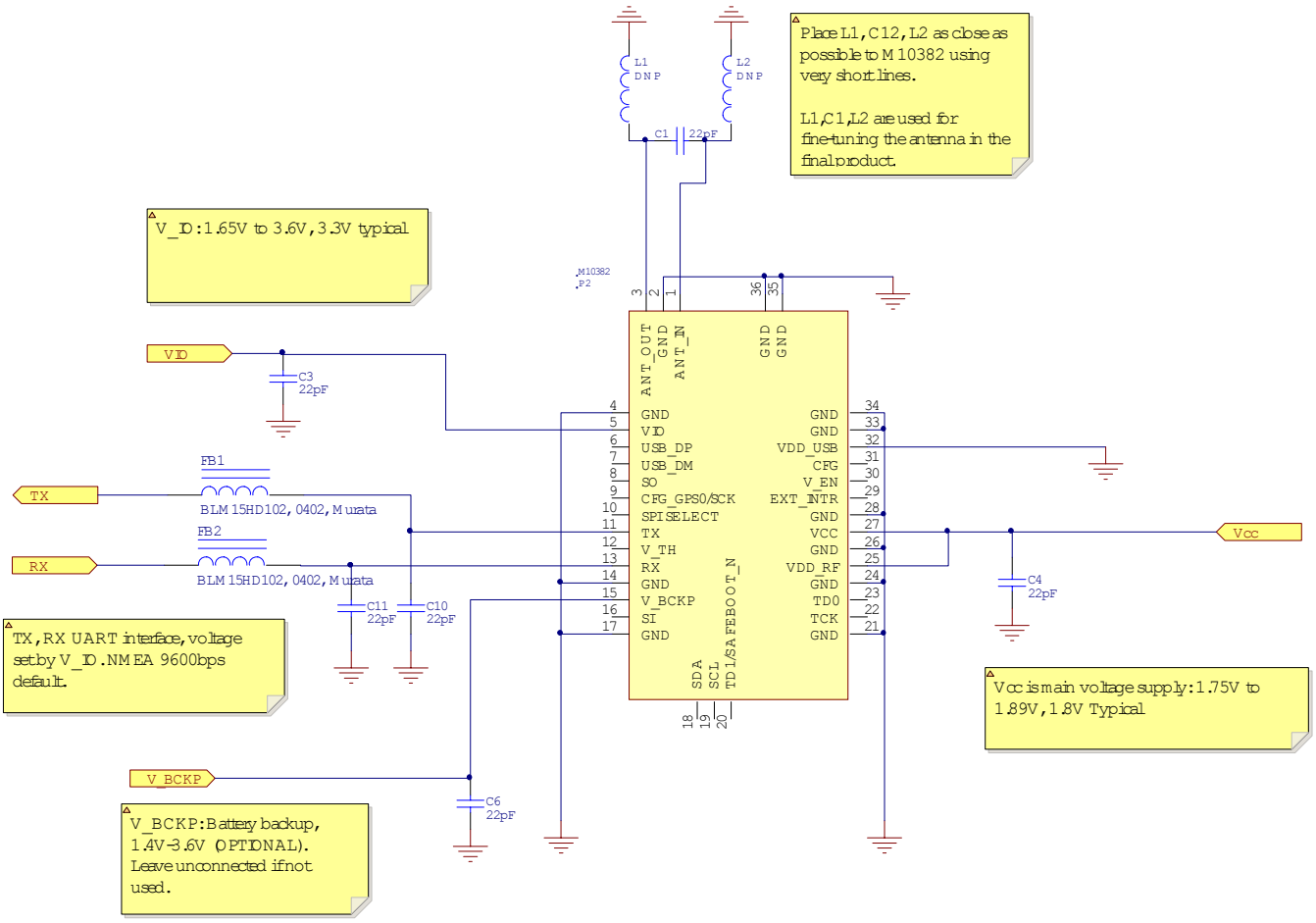
Designator	Designator	Protocol	Messages	UART Baud Rate	USB Power
CFG_COM1 (PIN8)	CFG_COM0 (PIN 16)				
1	**1**	NMEA	GSV, RMC, GSA, GGA, GLL, VTG, TXT	9600	BUS Powered
1	0	NMEA	GSV, RMC, GSA, GGA, GLL, VTG, TXT	38400	Self Powered
0	1	NMEA	GSV†, RMC, GSA, GGA, VTG, TXT	4800	BUS Powered
0	0	UBX	NAV-SOL, NAV-STATUS, NAV-SVINFO, NAV-CLOCK, INF, MON-EXCEPT, AID-ALPSERV	57600	BUS Powered
† Every 5th fix					

Table 4: Communication interfaces start-up settings

Recommended Application Schematic for M10382-A1; 1.8V Power Supply, UART

Paramater	Condition
Voltage Supply	1.75V - 1.89V, 1.8V typical
Power Mode	Maximum performance†
Interface	UART, NMEA, 9600bps†

†At system boot. Can be changed using software commands.



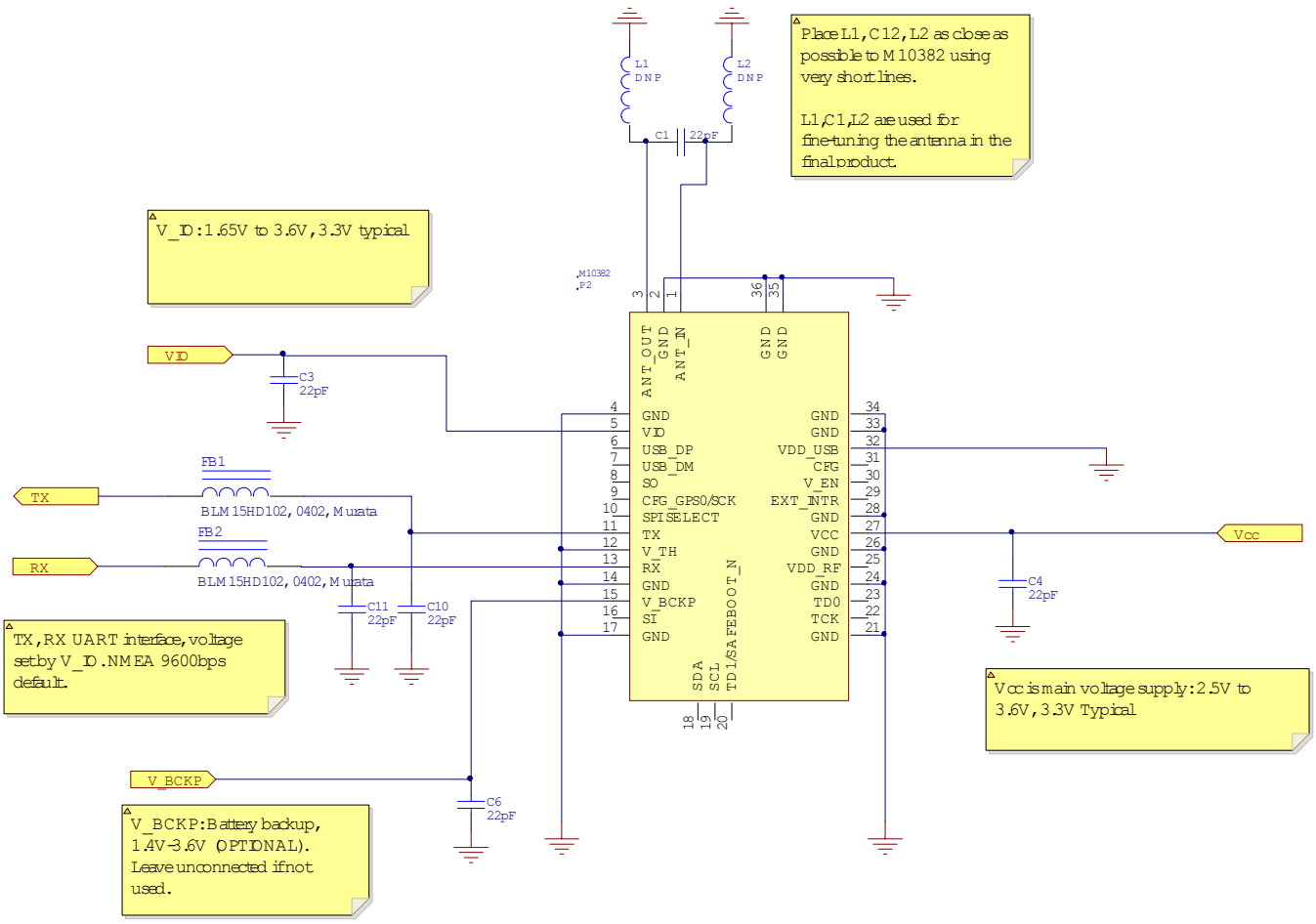
Bill of Material

Ref. Designator	Type	QTY.	Description/Comments
FB1, FB2	Ferrite	2	Murata BLM15HD102, 0402
C3, C4, C6, C10, C11	Capacitor	5	22pF, COG, 0402
C1, L1, L2	TBD	3	Value and type depend on antenna matching (see External Matching)

Recommended Application Schematic for M10382-A1; 3.3V Power Supply, UART

Paramater	Condition
Voltage Supply	2.5V - 3.6V, 3.3V typical
Power Mode	Maximum performance†
Interface	UART, NMEA, 9600bps†

† At system boot. Can be changed using software commands.



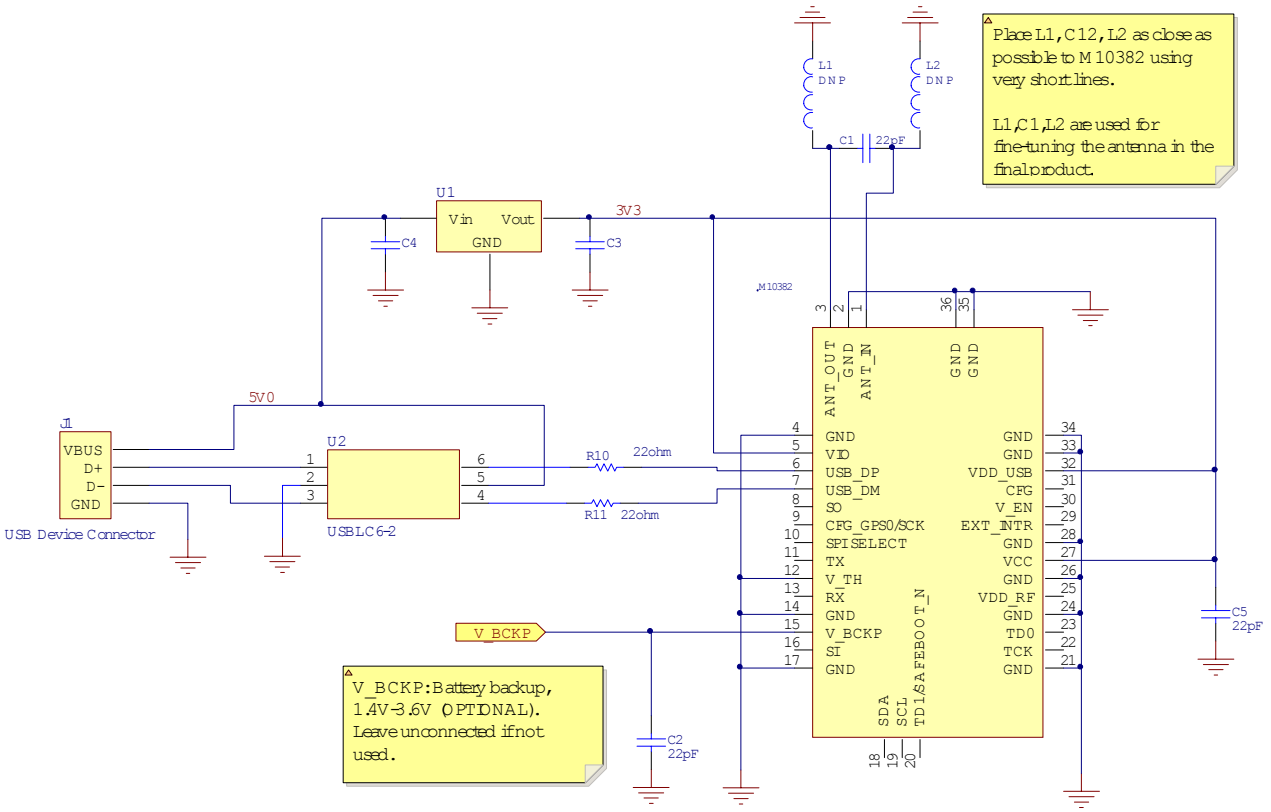
Bill of Material

Ref. Designator	Type	QTY.	Description/Comments
FB1, FB2	Ferrite	2	Murata BLM15HD102, 0402
C3, C4, C6, C10, C11	Capacitor	5	22pF, COG, 0402
C1, L1, L2	TBD	3	Value and type depend on antenna matching (see External Matching)

Recommended Application Schematic for M10382-A1; USB Bus Powered

Paramater	Condition
Voltage Supply	5.0V from USB Bus
Power Mode	Maximum performance†
Interface	USB, NMEA, 9600bps†

† At system boot. Can be changed using software commands.



Bill of Material

Ref. Designator	Type	QTY.	Description/Comments
U1	LDO, Regulates VBUS (4.4 ... 5.25V) down to 3.3V	1	Must be able to deliver the maximum current of about 100 mA. A DC/DC converter may be used as an alternative
U2	ESD Protection Diode	1	Use low capacitance ESD protection such as STMictroelectronics USBLC6-2
C1, C2	Capacitor	2	22pF, COG, 0402
C3, C4	Capacitor	2	Value depends on U1 specification
R10, R11	Resistor	2	22 Ω
J1	Connector		USB connector
C1, L1, L2	TBD	3	Value and type depends on antenna matching (see External Matching)

External Matching

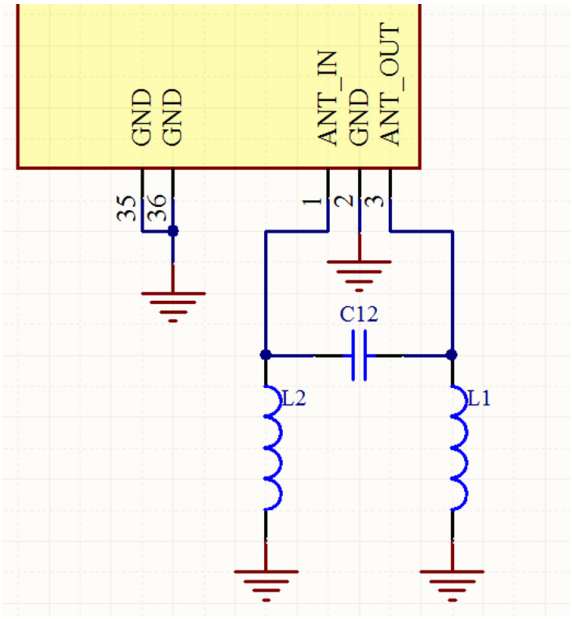
The M10382 module uses a matching circuit on the host PCB in order to fine-tune the on-board antenna to each specific application. This “external matching” allows compensating for the detuning of the antenna caused by various different components that can be close to the M10382 module in the actual application (plastic case, battery, speakers etc).

The external matching must be placed on the host PCB between ANT_OUT (PIN3) and ANT_IN (PIN1). Although 2 components are typically more than enough to match the antenna to the 50Ω impedance required, a Π-network topology with 3 components is recommended for safe proving.

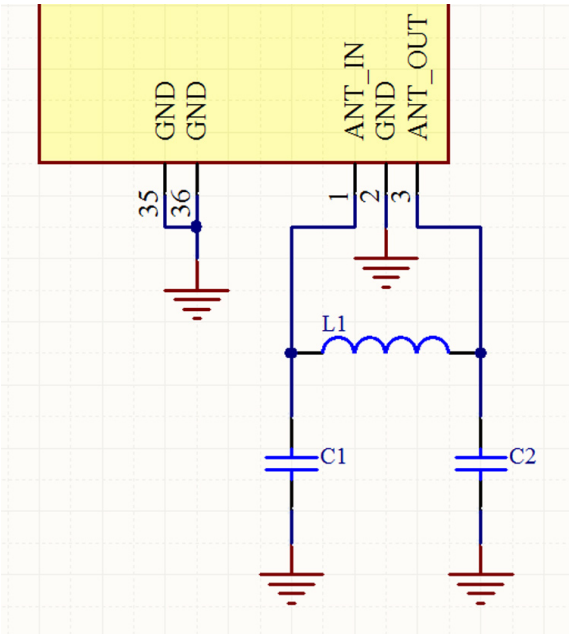
Schematic

Both low-pass and hi-pass topologies for the matching network can be used with similar results. As the same footprint can be used for both topologies, the exact type and value of the components used can be determined during the optimization phase.

- The initial values can be simply chosen as the null-circuit (no impedance matching):
  - Hi-pass:
    - C12 = 18pF
    - L1, L2 = Not Fitted
  - Low-pass:
    - L1 = Jumper (0Ω resistor)
    - C1, C2 = Not fitted



External matching circuit schematic
Hi-pass configuration



External matching circuit schematic
Low-pass configuration

Type of Matching Components

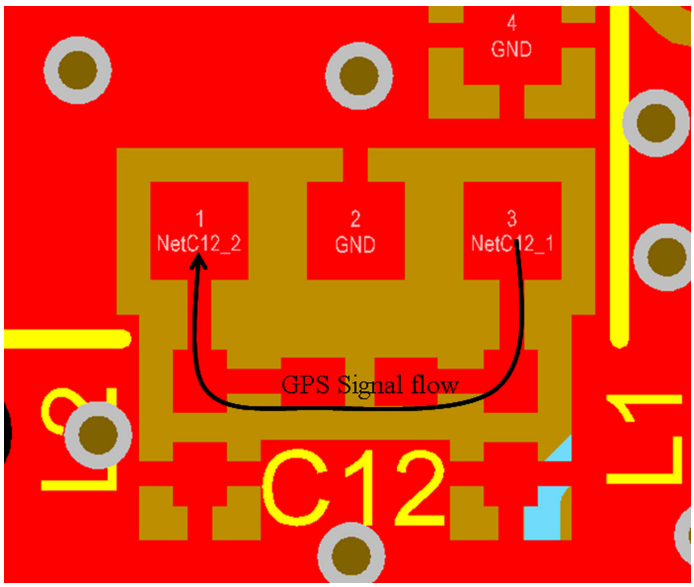
- Capacitors:
  - Use 0402, COG components
- Inductors:
  - High-Q, wire wound inductors in 0402 size are recommended for maximum performance, e.g. Murata LQW15 series
  - Good quality multi-layer type inductors (e.g. Murata LQG15 series) can also be used as a lower cost alternative

Layout

The layout of the external matching circuit should be done using the following guidlines:

- Minimize the length of the tracks connecting the ANT_OUT and ANT_IN pads to the matching
- Minimize the length of the tracks between the components
- Use a solid groundplane under the matching circuit area
- Absolutely avoid routing any track under the matching circuit area
- Connect the top ground layer with the ground layer underneath using several vias

Layout drawings (Gerber or other format) are available from Antenova. Please contact your local FAE.



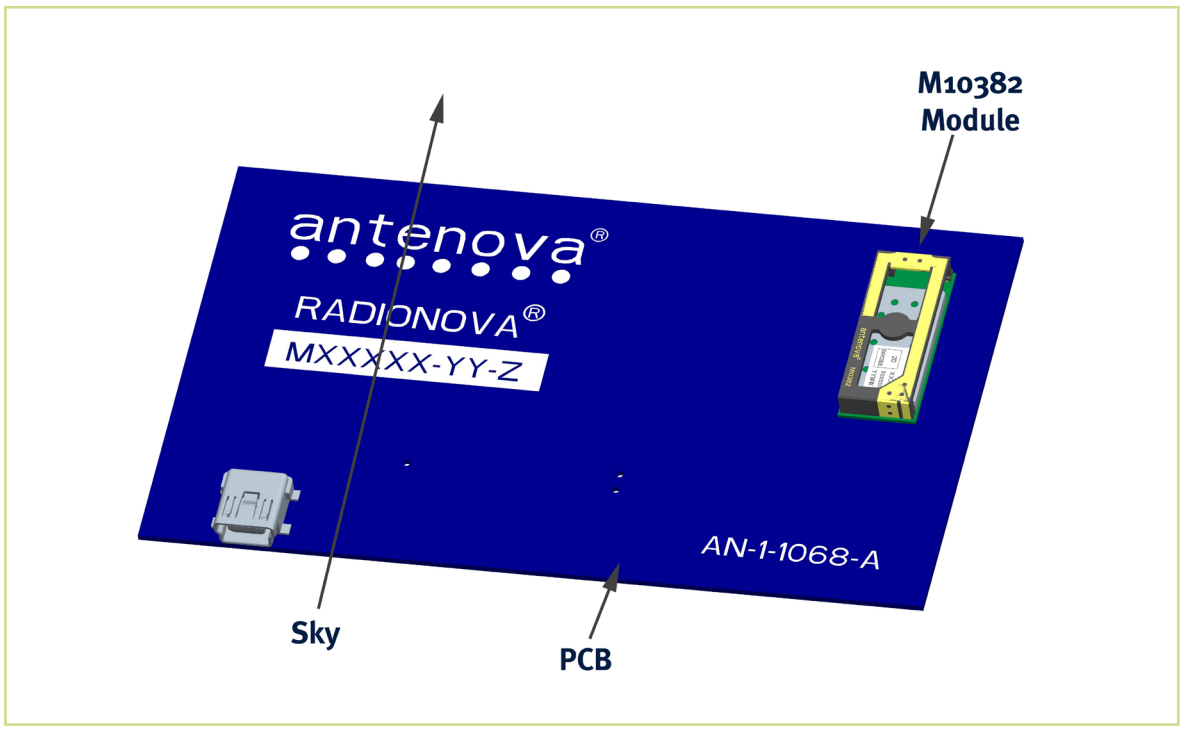
Example of external matching circuit layout

Matching Procedure

The types and values of the matching components must be chosen so that the impedance seen by port ANT_IN (PIN1) is as close as possible as 50Ω. Althought it is a relatively simple operation, it requires some RF skills and a VNA (Vector Network Analyzer). **Please contact an Antenova M2M FAE to get support on defining the optimal matching for your specific device.**

Typical RF Antenna Module Placement

Note: Module placement locations and orientations are critical for achieving optimal system performance. It is strongly recommended to contact Antenova M2M for design recommendations.



Front View



Back View



Side View



Optimal Placement

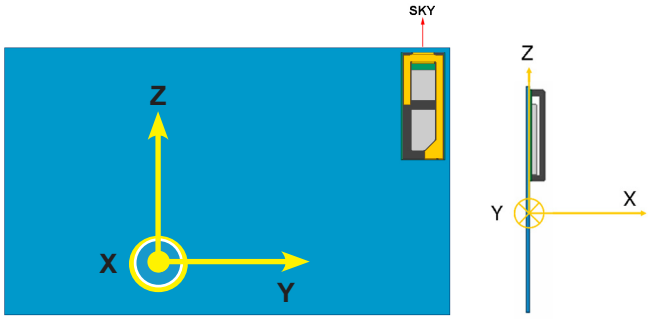
This section provides information about the efficiency and gain patterns of the antenna on the M10382 GPS module in optimal positions on four typical user device size PCBs;

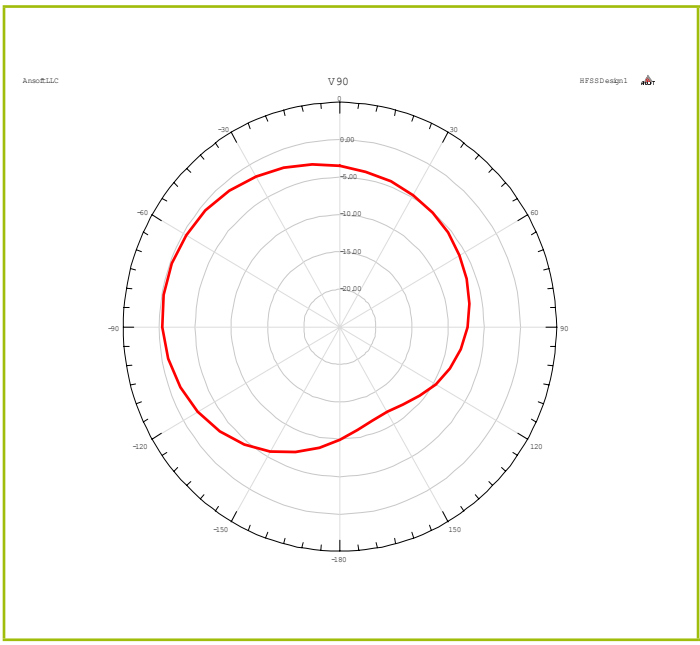
- PND/PMP device PCB - 100 x 60mm
- Small device (e.g. tracker) PCB - 30 x 40mm
- Handset size device PCB - 40 x100mm
- 10” Tablet size PCB - 250 x180mm

Please note that in all positions the sky is up as indicated on the PCB images. The information is provided to help customers position the module in the optimal location for GPS applications. Efficiency and gain patterns for other positions on the PCBs are available from Antenova M2M. Please email sales@antenova-m2m.com for a full set of these results.

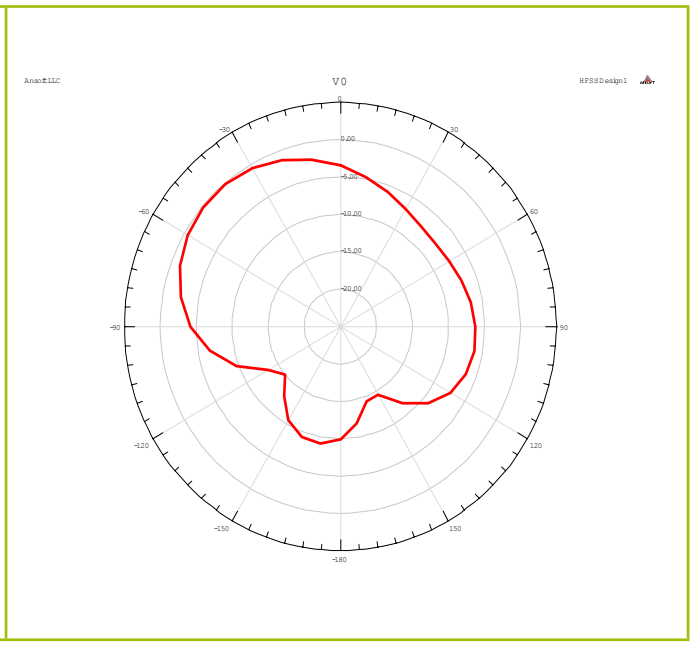
PND/PMP device PCB - 100 x 60mm

100mm x 60mm Top Right (up)	
Peak Efficiency [%]	72
Average RHCP Gain [dB]	-4.3
Average LHCP Gain [dB]	-4.8
RHCP/LHCP	+0.5





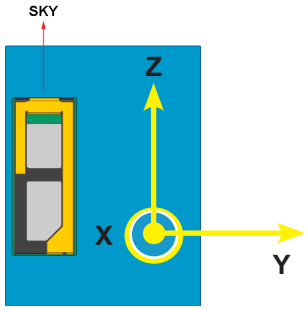
ZX

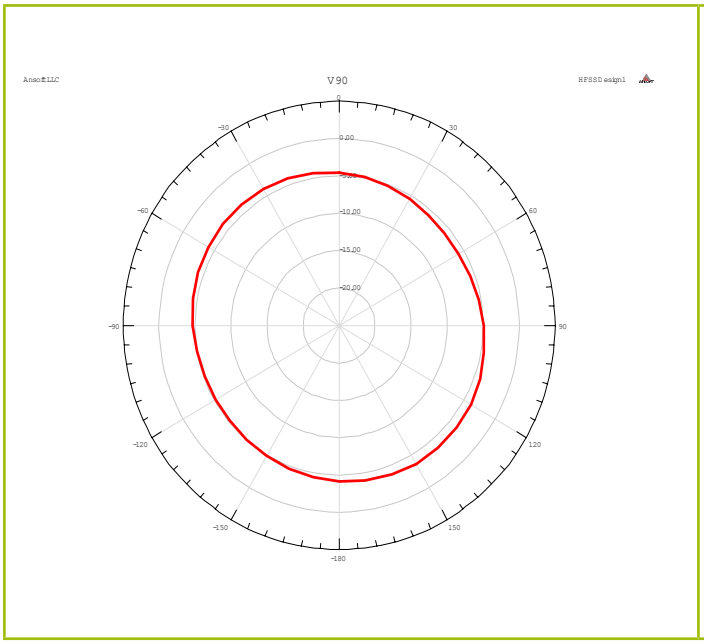


ZY

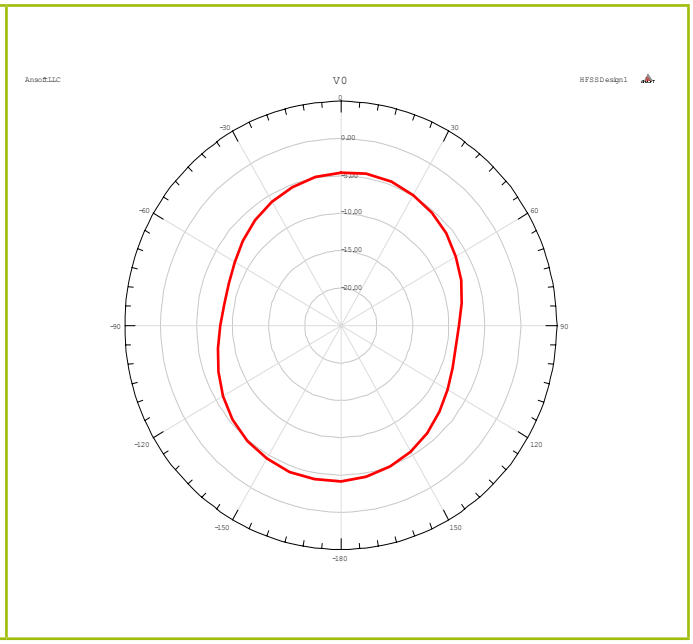
Small device (e.g. tracker) PCB - 30 x 40mm

30mm x 40mm Left (up)	
Peak Efficiency [%]	39
Average RHCP Gain [dB]	-5.5
Average LHCP Gain [dB]	-10.2
RHCP/LHCP	+4.7





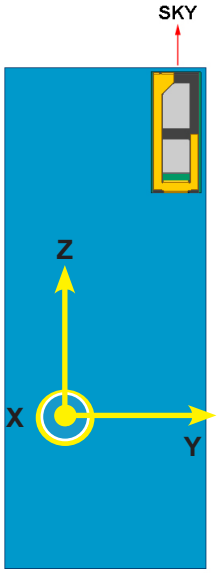
ZX

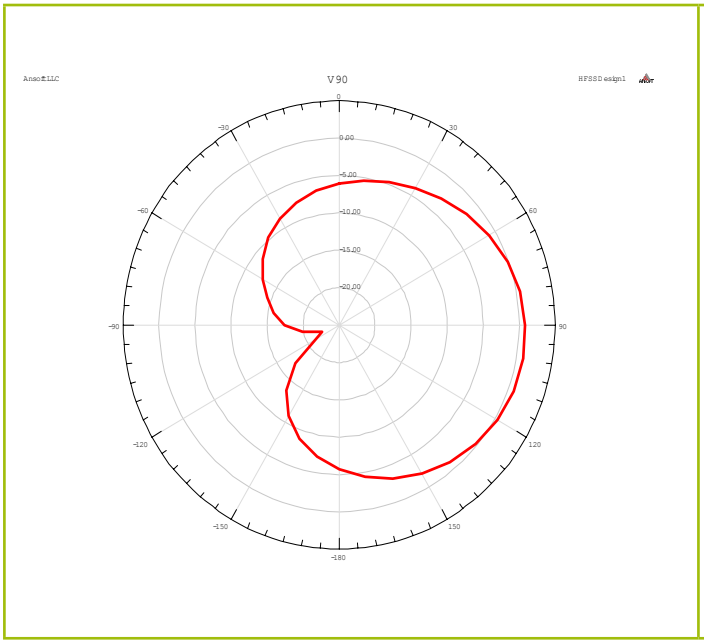


ZY

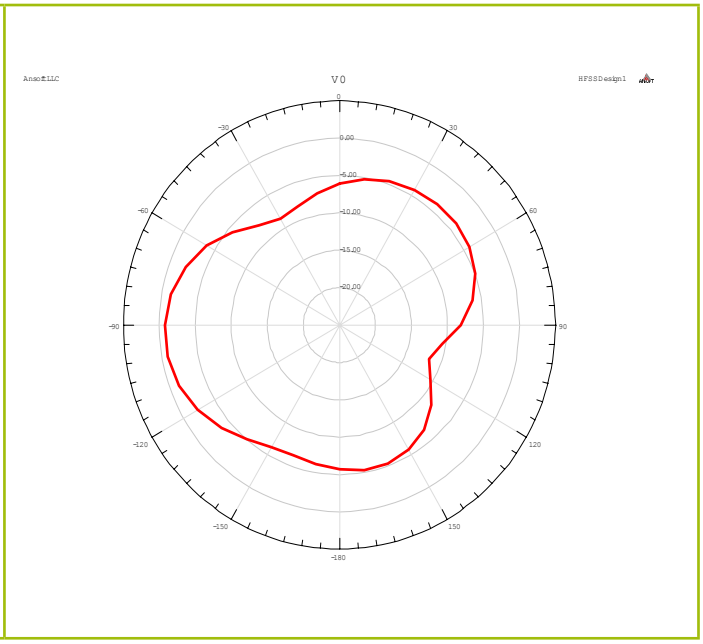
Handset size device PCB - 40 x100 mm

40mm x 100mm Top Right (down)	
Peak Efficiency [%]	69
Average RHCP Gain [dB]	-3.7
Average LHCP Gain [dB]	-5.9
RHCP/LHCP	+2.2





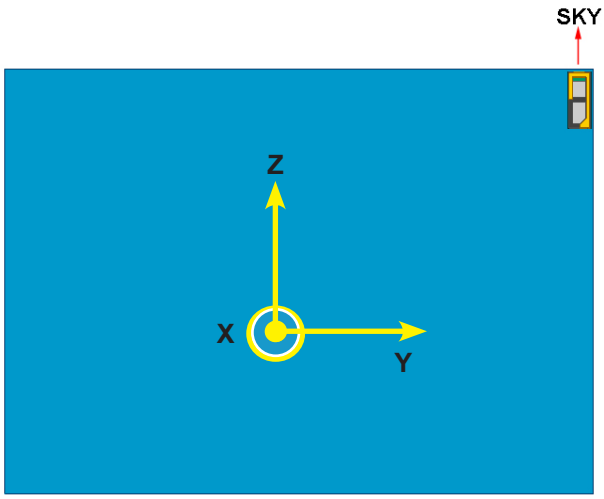
ZX

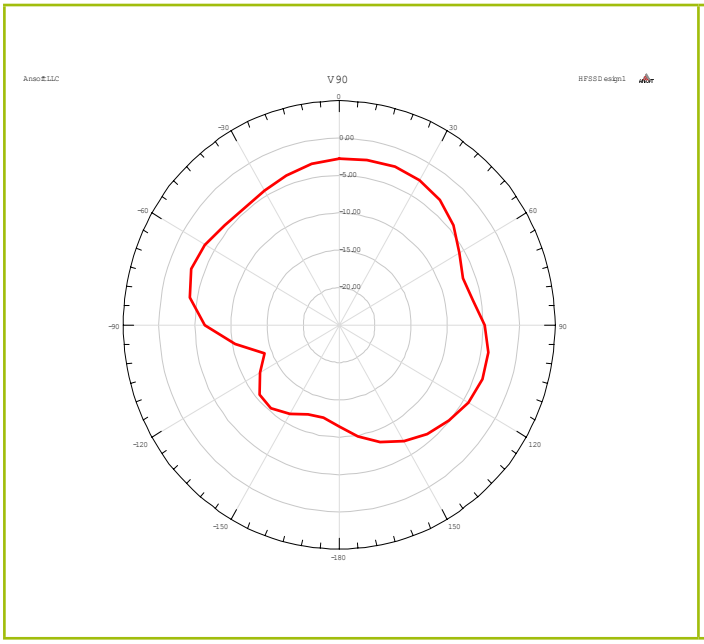


ZY

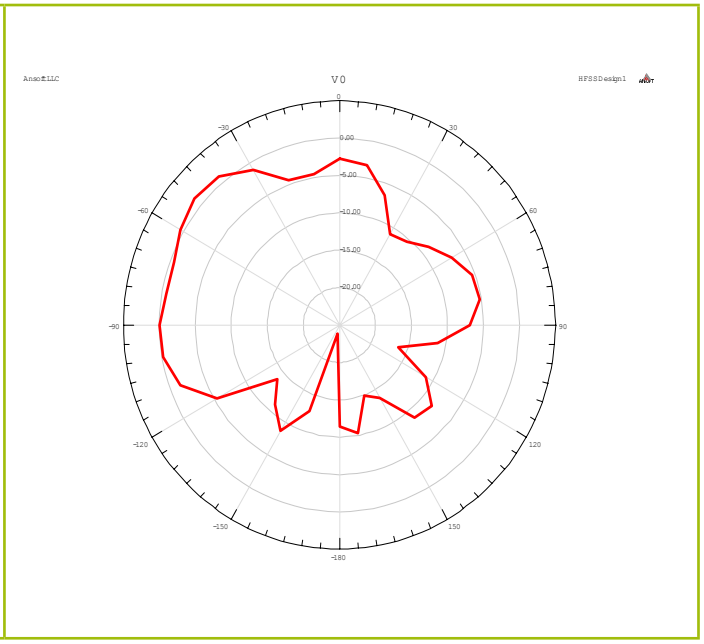
10” Tablet size PCB - 250 x 180mm

250mm x 180mm Top Right (up)	
Peak Efficiency [%]	81
Average RHCP Gain [dB]	-3.9
Average LHCP Gain [dB]	-4.3
RHCP/LHCP	+0.3





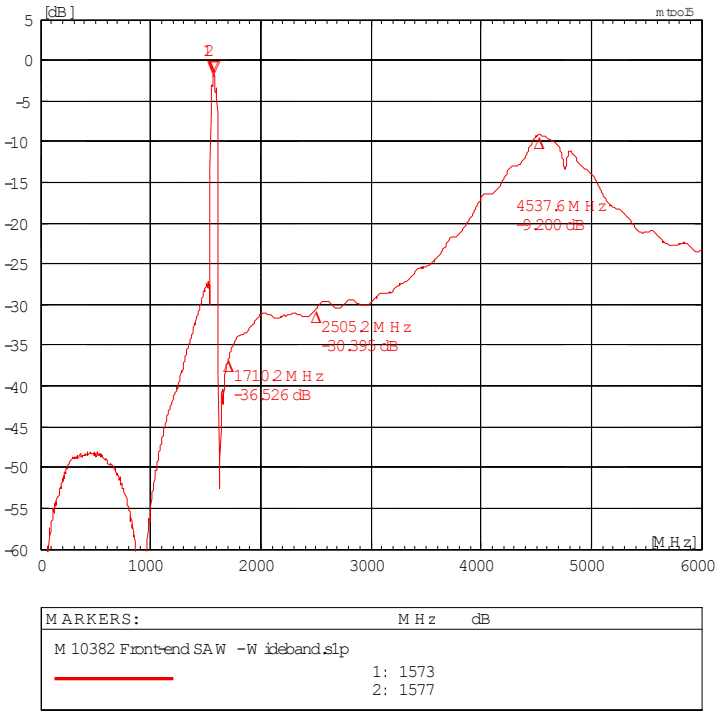
ZX



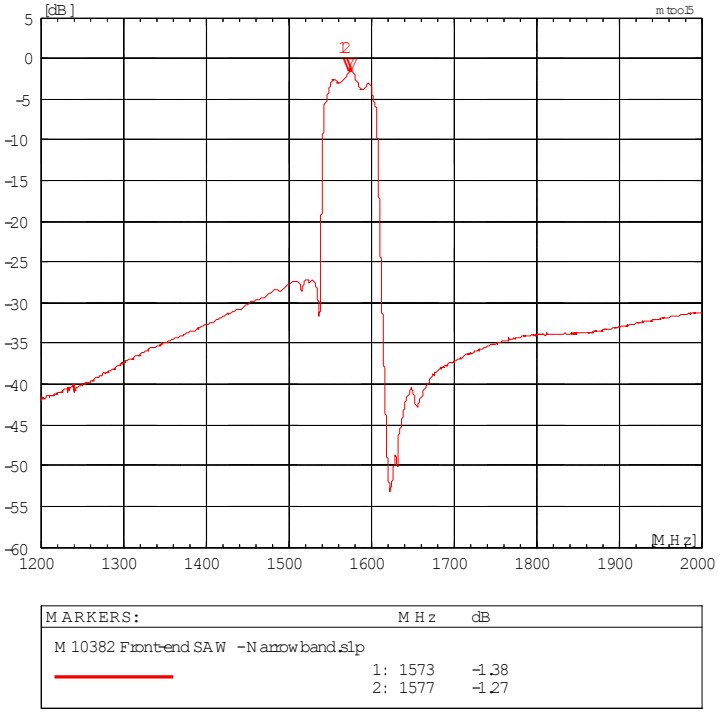
ZY

Front-end Rejection

The figure below shows the rejection for the input SAW filter before the LNA, including the effect of pads, tracks, ESD protection and decoupling. The plot can be useful to calculate the isolation required from adjacent transmitters in order to avoid the saturation of the LNA.



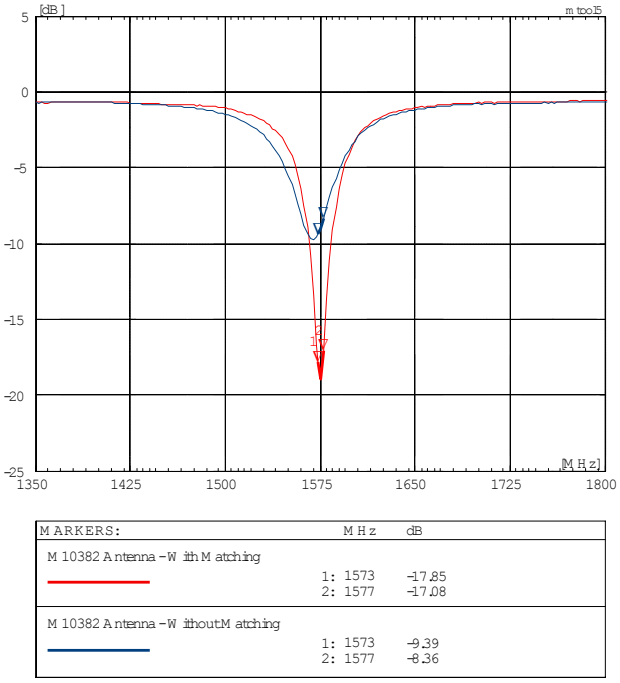
Input SAW Rejection - Wideband



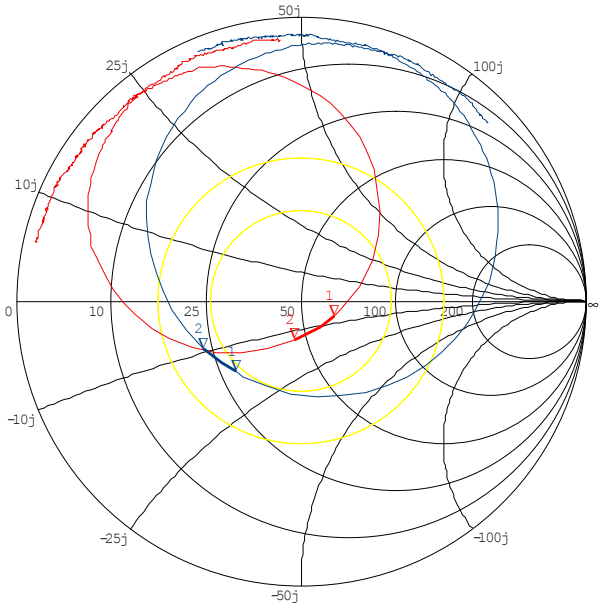
Input SAW Rejection - Narrowband

Antenna Matching

Typical antenna matching as seen by ANT_IN Port is shown in the following plot. The matching bandwidth at -10dB is typically 20MHz. Measured on M10382-U1 test board.



Typical antenna return loss before and after matching



Typical antenna impedance before and after matching

Reflow Soldering

Placement

Typical placement systems used for any BGA/LGA package are acceptable. Recommended nozzle diameter for placement: 5mm

Moisture Preconditioning

Before submitting the M10382 module to the reflow soldering process, it is mandatory to bake the module at 125 ºC for 3 hours. If the module is not baked, it could develop defects during the reflow soldering process; in particular, bubbles or other defects could appear on the metallised pattern of the antenna.

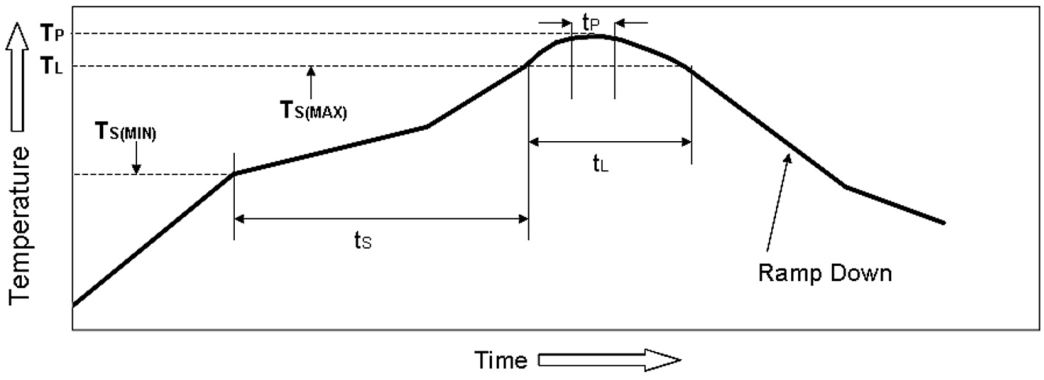
Soldering Paste

Use of “No Clean” soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. An example of suitable soldering paste is Alpha OM350.

Soldering

The recommended soldering profile for M10382 is show below. However, it is the responsibility of the Contract manufacturer to determine the exact reflow profile used, taking into consideration the parameters of the host PCB, solder paste used, etc.

Profile Feature		Pb-Free Solder
Pre-Heat	Temperature (T_S) Min	130°C
	Temperature (T_S) Max	220°C
	Time (t_S)	<150s
Reflow	Liquidus Temperature - (T_L)	220°C
	Time (t_L)	45-90s
Peak Package Body Temperature (T_P)		245°C
Time within 5°C of peak temp (t_P)		30s
Average Ramp up rate - T_S(max) to (T_P)		3°C/s
Ramp Down Rate		6°C/s max



Example Reflow profile

The Pb Free Process-Package Peak Reflow Temperature is 260ºC.

Exceeding the maximum soldering temperature could permanently damage the module.

Multiple Soldering

The M10382 module can be submitted up to 3 reflow soldering processes.

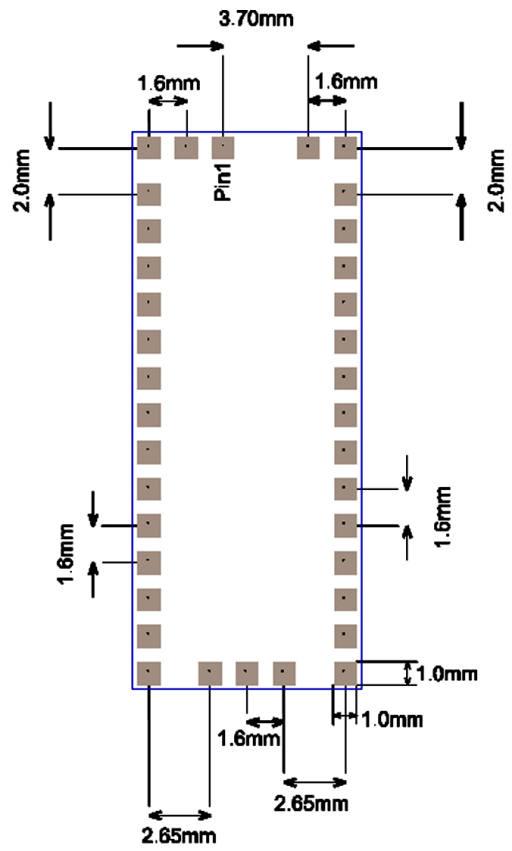
Upside-down soldering is acceptable but it is recommended that the Contract Manufacturer qualify the process before mass production. The second reflow must take place within the recommended floor life limit (MSL3). Please contact Antenova for further information.

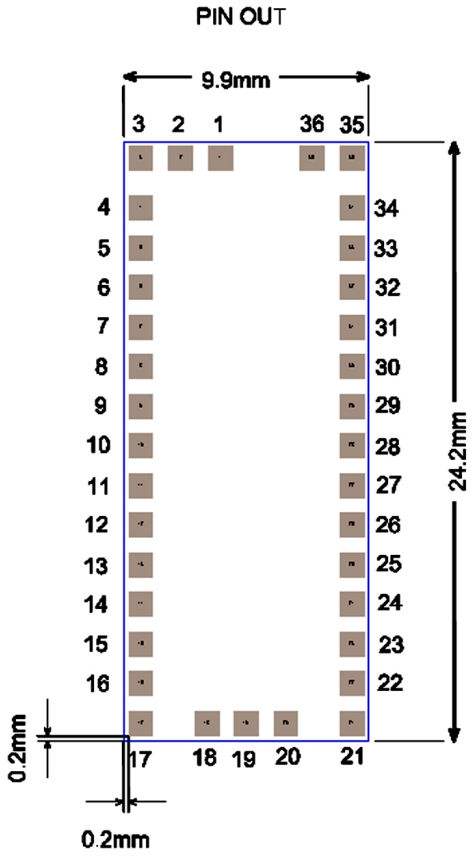
Hand Soldering

Hand-soldering and rework of the M10382 module are not recommended.

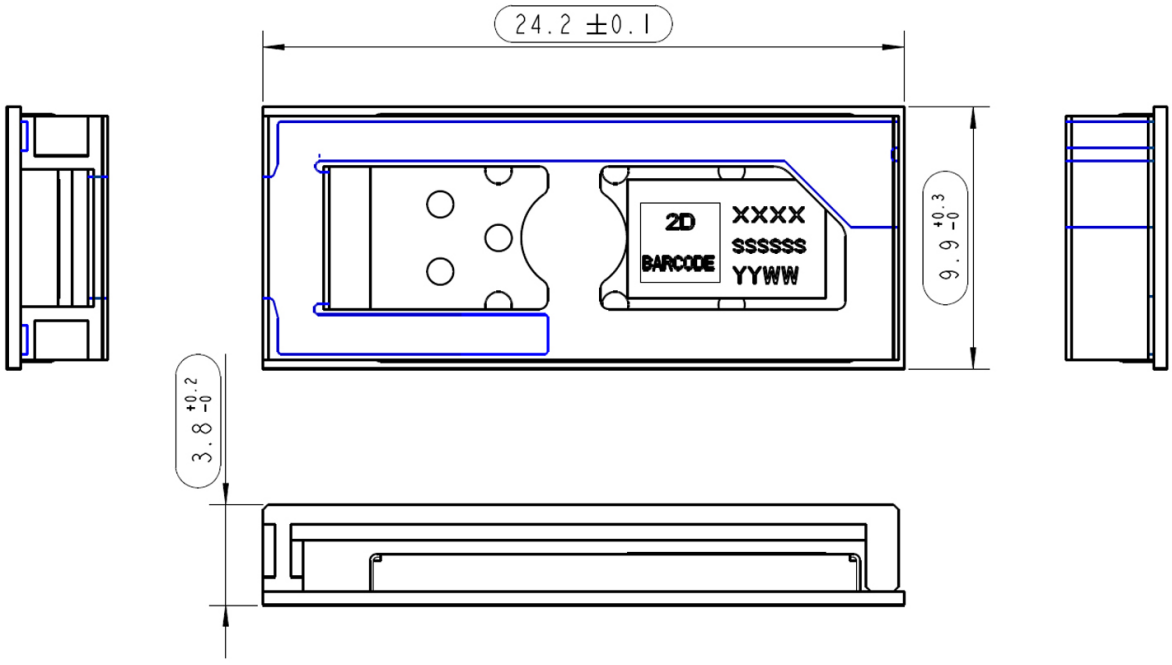
Module Footprint

Note: All module pads are 1mm x 1mm. Pitch is 1.6mm unless otherwise stated. Overall module footprint size is 24.2mm x 9.9mm.





Mechanical Drawing



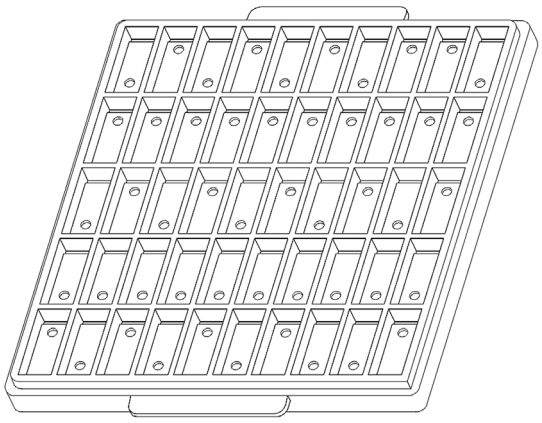
Hazardous material regulation conformance

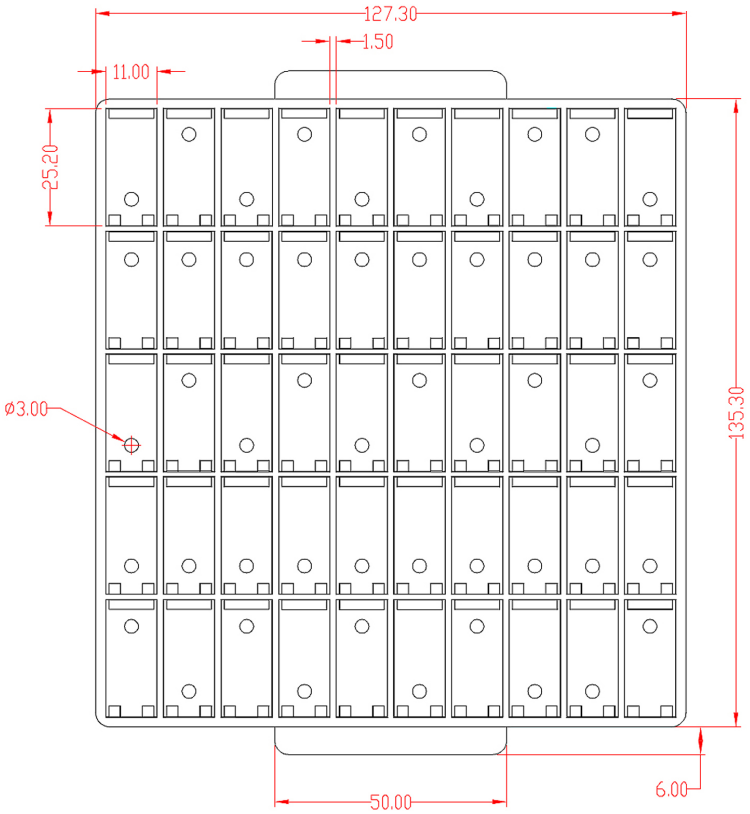
The RF antenna module has been tested to confirm to RoHS requirements. A certificate of comformance is available from Antenova's website.

Packaging

M10382 are delivered in trays of 50 pieces packaged in boxes of 1000 pieces.

Quantity	No. of Trays	Trays
1000 pcs/box	20 per box	50 pcs





Dimensions in mm

www.antenova-m2m.com

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Certificate No: 4598

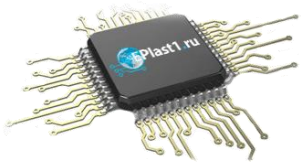
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- Защита от снятия компонента с производства.



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