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# New 8FX 8-bit Microcontrollers

The MB95560H/570H/580H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

#### **Features**

- F2MC-8FX CPU core
  - □ Instruction set optimized for controllers
    - · Multiplication and division instructions
    - · 16-bit arithmetic operations
    - · Bit test branch instructions
    - · Bit manipulation instructions, etc.
- Clock (The main oscillation clock and the suboscillation clock are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)
  - □ Selectable main clock source
    - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    - Main CR clock (4 MHz ± 2%)
      - The main CR clock frequency becomes 8 MHz when the PLL multiplication rate is 2.
      - The main CR clock frequency becomes 10 MHz when the PLL multiplication rate is 2.5.
      - The main CR clock frequency becomes 12 MHz when the PLL multiplication rate is 3.
      - The main CR clock frequency becomes 16 MHz when the PLL multiplication rate is 4.

□Selectable subclock source

- Suboscillation clock (32.768 kHz)
- External clock (32.768 kHz)
- Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

#### ■ Timer

- 8/16-bit composite timer × 2 channels (only one channel on MB95F572H/F572K/F573H/F573K/F574H/F574K/F582H/ F582K/F583H/F583K/F584H/F584K)
- □ Time-base timer × 1 channel
- □ Watch prescaler × 1 channel
- LIN-UART (only available on MB95F562H/F562K/F563H/ F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/ F584K)
  - □ Full duplex double buffer
  - □ Capable of clock synchronous serial data transfer and clock asynchronous serial data transfer
- External interrupt
  - □ Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes

- ☐ There are four standby modes as follows:
  - Stop mode
  - · Sleep mode
  - · Watch mode
  - · Time-base timer mode
- ☐ In standby mode, the device can be made to enter either normal standby mode or deep standby mode.
- I/O port
  - □ MB95F562H/F563H/F564H (maximum no. of I/O ports: 16)
    - General-purpose I/O ports (CMOS I/O): 15
    - General-purpose I/O ports (N-ch open drain): 1
  - □ MB95F562K/F563K/F564K (maximum no. of I/O ports: 17)
    - General-purpose I/O ports (CMOS I/O): 15
    - General-purpose I/O ports (N-ch open drain): 2
  - □ MB95F572H/F573H/F574H (maximum no. of I/O ports: 4)
    - General-purpose I/O ports (CMOS I/O): 3
    - General-purpose I/O ports (N-ch open drain): 1
  - □ MB95F572K/F573K/F574K (maximum no. of I/O ports: 5)
    - General-purpose I/O ports (CMOS I/O): 3
    - General-purpose I/O ports (N-ch open drain): 2
  - □ MB95F582H/F583H/F584H (maximum no. of I/O ports: 12)
    - General-purpose I/O ports (CMOS I/O): 11
    - General-purpose I/O ports (N-ch open drain): 1
  - □ MB95F582K/F583K/F584K (maximum no. of I/O ports: 13)
    - General-purpose I/O ports (CMOS I/O): 11
    - General-purpose I/O ports (N-ch open drain): 2
- On-chip debug
  - □ 1-wire serial control
  - □ Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
- ☐ Built-in hardware watchdog timer
- □ Built-in software watchdog timer
- Power-on reset
  - □ A power-on reset is generated when the power is switched on.
- Low-voltage detection reset circuit (only available on MB95F562K/F563K/F564K/F572K/F573K/F574K/F582K/F583K/F584K)
  - □ Built-in low-voltage detector
- Clock supervisor counter
  - Built-in clock supervisor counter function
- Dual operation Flash memory
  - ☐ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - □ Protects the content of the Flash memory.



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## 1. Product Line-up

## • MB95560H Series

Part number	Series									
, are manipor	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K				
Parameter	1112001 00211	IIIBooi oooii	1112001 00411	IIIBOOI GOZIK	IIIBoor coort	MB001 004IX				
Туре		Flash memory product								
Clock		Tidon momory product								
	lt cunanicae th	supervises the main clock oscillation.								
counter	it supervises tri	e main clock os	omation.							
Flash memory			1	1						
capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte				
RAM capacity	240 bytes	240 bytes								
Power-on reset	240 Dytes	430 Dytes		es	430 Dytes	496 bytes				
Low-voltage										
detection reset		No			Yes					
Reset input		Dedicated		Color	stad through act	thuoro				
Reset input	. Number of be		. 126	Selec	ted through sof	tware				
		asic instructions								
	Instruction bit		: 8 bits	L. 4						
COLLITINATIONS	Instruction leads	•	: 1 to 3							
	Data bit lengt			nd 16 bits		40 OF MILE)				
	<ul> <li>Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)</li> <li>Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz)</li> </ul>									
			: 0.6 µs			5.25 MHZ)				
	I/O ports (Ma	•		I/O ports (Ma						
nurnaca I/( )	CMOS I/O	: 15		• CMOS I/O	: 15					
•	N-ch open dr	ain: 1		N-ch open dr						
Time-base timer			s (external clock	trequency = 4	MHz)					
	<ul> <li>Reset general</li> </ul>									
software			MHz: 105 ms (I							
watchdog timer				e clock of the h	ardware watcho	log timer.				
		to replace 3 byt								
				oe selected by a	dedicated reloa	ad timer.				
		uplex double bu								
LIN-UART	<ul> <li>Both clock synchronous serial data transfer and clock asynchronous serial data transfer are</li> </ul>									
	enabled.									
		tion can be use	d as a LIN mast	ter or a LIN slav	e.					
	6 channels									
		esolution can be	e selected.							
	2 channels									
				er × 2 channels"						
8/16-bit	<ul> <li>It has the following</li> </ul>	owing functions:	interval timer fu	ınction, PWC fu	nction, PWM fui	nction and input				
composite timer	capture funct	ion.								
	Count clock: it can be selected from internal clocks (7 types) and external clocks.									
	<ul> <li>It can output</li> </ul>	square wave.								
External	6 channels									
	<ul> <li>Interrupt by e</li> </ul>	dge detection (	The rising edge	, falling edge, o	r both edges ca	n be selected.)				
interrupt	<ul> <li>It can be use</li> </ul>	d to wake up th	e device from th	ne standby mod	e.	Ĺ				
On chin dahua	<ul> <li>1-wire serial</li> </ul>	control		-						
On-chip debug	<ul> <li>It supports se</li> </ul>	erial writing (asy	nchronous mod	de).						



Part number Parameter	MB95F562H	MB95F563H	MB95F564H	MB95	5F562K	MB95F563K	MB95F564K
Watch prescaler	Eight different t	ime intervals ca	an be selected.				
Flash memory	<ul> <li>It supports automatic programming (Embedded Algorithm), and program/erase/eras suspend/erase-resume commands.</li> <li>It has a flag indicating the completion of the operation of Embedded Algorithm.</li> <li>Flash security feature for protecting the content of the Flash memory</li> <li>Number of program/erase cycles</li> <li>1000</li> <li>10000</li> <li>100000</li> <li>Data retention time</li> <li>20 years</li> <li>10 years</li> <li>5 years</li> </ul>					hm.	
Standby mode	Sleep mode, st	Sleep mode, stop mode, watch mode, time-base timer mode					
Package			SO	P032 J020 G020			

### • MB95570H Series

• MB95570H	Part number									
rait ilullibei	MB95F572H	MB95F573H	MB95F572K	MB95F573K	MB95F574K					
Parameter	MB301 07211	1112301 07011	MB95F574H	WIBSSI STER	MB301 070K	MB301 07 410				
Туре		Flash memory product								
Clock										
supervisor	It supervises th	e main clock os	scillation.							
counter										
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte				
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes				
Power-on reset			Y	es						
Low-voltage		No			Yes					
detection reset		NO			165					
Reset input		Dedicated		Selec	cted through sof	tware				
•	Number of basic instructions : 136									
	Instruction bit length : 8 bits									
CPU functions	<ul> <li>Instruction lei</li> </ul>	ngth	: 1 to 3	•						
CF O IUIICIIOIIS	• Data bit length : 1, 8 and 16 bits									
	<ul> <li>Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)</li> </ul>									
	<ul> <li>Interrupt prod</li> </ul>	essing time	: 0.6 µs		k frequency = 16	6.25 MHz)				
General-	<ul> <li>I/O ports (Ma</li> </ul>	x):4		<ul> <li>I/O ports (Ma</li> </ul>	x):5					
purpose I/O	<ul> <li>CMOS I/O</li> </ul>	: 3		<ul> <li>CMOS I/O</li> </ul>	: 3					
purpose i/O	<ul> <li>N-ch open dr</li> </ul>	ain: 1		<ul> <li>N-ch open dr</li> </ul>	ain: 2					
Time-base timer	Interval time: 0	.256 ms to 8.3 s	s (external clock	frequency = 4	MHz)					
Hardware/	<ul> <li>Reset genera</li> </ul>	,								
software	Main oscilla	tion clock at 10	MHz: 105 ms (I	Min)						
	<ul> <li>The sub-CR of</li> </ul>			e clock of the h	ardware watcho	log timer.				
Wild register	It can be used	to replace 3 byt	es of data.							
LIN-UART	No LIN-UART									
8/10-bit A/D	2 channels									
converter	8-bit or 10-bit re	esolution can be	-bit or 10-bit resolution can be selected.							



Part number Parameter	MB95F572H	MB95F573H	MB95F574H	MB95I	F572K	MB95F573K	MB95F574K			
Parameter	1 shannal	hannal								
	<ul><li>It has the follocapture funct</li><li>Count clock:</li></ul>	The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". It has the following functions: interval timer function, PWC function, PWM function and input capture function.  Count clock: it can be selected from internal clocks (7 types) and external clocks. It can output square wave.								
External interrupt	, ,	•	The rising edge e device from the		-	•	n be selected.)			
On-chin dehua	<ul><li>1-wire serial of the s</li></ul>		nchronous mod	le).	-					
Watch prescaler	Eight different t	ime intervals ca	an be selected.							
		e-resume comindicating the co	mands. mpletion of the	operatio	on of Em	bedded Algorit	m/erase/erase- hm.			
	Number of	program/erase	cycles 1	000	10000	100000				
	Data retention time 20 years 10 years 5 years									
Standby mode	Sleep mode, st	op mode, watch	n mode, time-ba	se timei	r mode					
Package				8008 8000						

### • MB95580H Series

Part number						
Tart Humber	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Parameter	WID951 30211	WID951 50511	WID951 30411	WID951 302K	WID95I 505K	WID951 504K
Туре			Flash mem	ory product		
Clock						
supervisor	It supervises th	e main clock os	scillation.			
counter						
Flash memory	0 Khyta	10 Khyta	20 Khyta	0 Khyta	10 Khyta	20 Khyta
capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset			Y	es		
Low-voltage		No			Yes	
detection reset		NO			res	
Reset input		Dedicated		Selec	ted through sof	tware
	<ul> <li>Number of base</li> </ul>	asic instructions	: 136			
	<ul> <li>Instruction bit</li> </ul>	t length	: 8 bits			
CDI I franctions	<ul> <li>Instruction lei</li> </ul>	ngth	: 1 to 3	bytes		
CPU functions	<ul> <li>Data bit lengt</li> </ul>	:h	: 1, 8 aı	nd 16 bits		
			on time : 61.5 n		ck frequency = 1	16.25 MHz)
	<ul> <li>Interrupt prod</li> </ul>				r frequency = 16	
0	• I/O ports (Ma	x) : 12		• I/O ports (Ma	x) : 13	·
General-	• CMOS I/Ò			• CMOS I/O : 11		
nurnose I/( )	N-ch open dr			N-ch open dr	ain: 2	



Part number	MB95F582H	MB95F583H	MB95F584I	MPO	5F582K	MB95F583K	MB95F584K			
Parameter	WD35F302F	MD301 30211   MD301 30411   MD301 30217   MD301 30317   MD301 30417								
Time-base timer	ne-base timer Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)									
Hardware/ software watchdog timer		tion clock at 10		` '	of the h	ardware watcho	dog timer.			
Wild register	It can be used t	to replace 3 byt	es of data.							
LIN-UART	<ul> <li>A wide range</li> <li>It has a full do</li> <li>Both clock sy enabled.</li> <li>The LIN functions</li> </ul>	uplex double bu nchronous seria	iffer. al data transfe	r and clo	ck async	hronous serial o	ad timer. Jata transfer are			
8/10-bit A/D	5 channels									
converter	8-bit or 10-bit re	esolution can be	e selected.							
	1 channel									
	<ul> <li>The timer car</li> <li>It has the follocapture funct</li> <li>Count clock:</li> <li>It can output:</li> </ul>	owing functions: ion. it can be selecte	interval time	function	, PWC fu	nction, PWM fu	nction and input			
External	6 channels									
interrupt	<ul><li>Interrupt by e</li><li>It can be used</li></ul>						n be selected.)			
I In chin deniid	<ul><li>1-wire serial of the supports serial of the support series serial of the support series ser</li></ul>		nchronous m	ode).						
Watch prescaler	Eight different t	ime intervals ca	n be selecte	d.						
Flash memory	<ul> <li>It supports automatic programming (Embedded Algorithm), and program/erase/erase suspend/erase-resume commands.</li> <li>It has a flag indicating the completion of the operation of Embedded Algorithm.</li> <li>Flash security feature for protecting the content of the Flash memory</li> </ul>									
	Number of	program/erase	cycles	1000	1000	0 100000				
	Data retention time 20 years 10 years 5 years									
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode									
Package			S	NP032 TB016 O016						



## 2. Packages And Corresponding Products

## • MB95560H Series

Part number Package	MB95F562H	MB95F562K	MB95F563H	MB95F563K	MB95F564H	MB95F564K
WNP032	О	О	О	О	О	О
SOJ020	О	О	О	О	О	0
STG020	О	О	О	О	О	О
STB016	Х	X	Х	Х	Х	X
SO016	Х	Х	Х	Х	Х	Х
PDA008	Х	Х	Х	Х	Х	Х
SOD008	Х	Х	Х	Х	Х	Х

#### • MB95570H Series

Part number						
	MB95F572H	MB95F572K	MB95F573H	MB95F573K	MB95F574H	MB95F574K
Package						
WNP032	Χ	X	X	X	X	X
SOJ020	Х	X	Х	Х	Х	Х
STG020	Х	X	Х	Х	Х	Х
STB016	Х	X	Х	Х	Х	Х
SO016	Х	X	Х	Х	Х	Х
PDA008	О	О	О	О	О	О
SOD008	0	0	О	О	0	0

### • MB95580H Series

Part number Package	MB95F582H	MB95F582K	MB95F583H	MB95F583K	MB95F584H	MB95F584K
WNP032	O	О	О	O	O	О
SOJ020	Х	Х	Х	Х	Х	Х
STG020	Х	Х	Х	Х	Х	Х
STB016	О	О	О	O	O	О
SO016	О	О	О	O	O	О
PDA008	Х	Х	Х	Х	Х	Х
SOD008	Х	Х	Х	Х	Х	Х

O: Available X: Unavailable



## 3. Differences Among Products And Notes On Product Selection

#### · Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase. For details of current consumption, see "Electrical Characteristics".

#### Package

For details of information on each package, see "Packages And Corresponding Products" and "Package Dimension".

### · Operating voltage

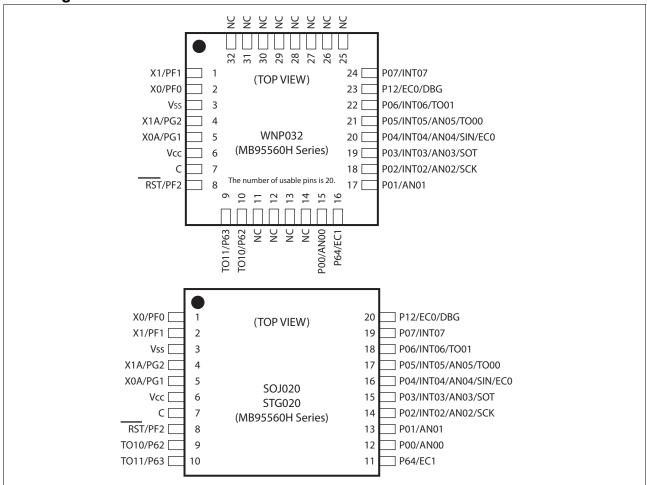
The operating voltage varies, depending on whether the on-chip debug function is used or not. For details of the operating voltage, see "Electrical Characteristics".

#### · On-chip debug function

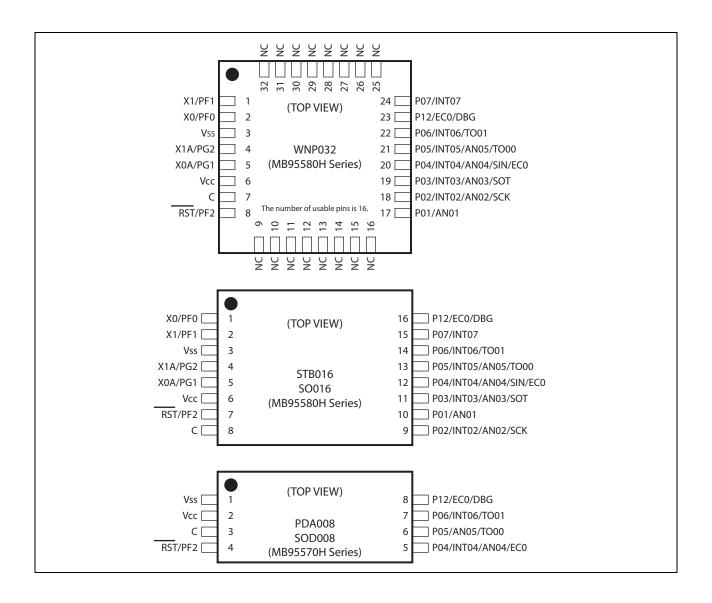
The on-chip debug function requires that V<sub>CC</sub>, V<sub>SS</sub> and one serial wire be connected to an evaluation tool. For details of the connection method, refer to "CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION" in "New 8FX MB95560H/570H/580H Hardware Manual".



## 4. Pin Assignment









# 5. Pin Functions (MB95560H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	В	General-purpose I/O port
!	X1	B	Main clock I/O oscillation pin
2	PF0	В	General-purpose I/O port
2	X0	7 P	Main clock input oscillation pin
3	Vss	_	Power supply pin (GND)
4	PG2	С	General-purpose I/O port
4	X1A		Subclock I/O oscillation pin
5	PG1	С	General-purpose I/O port
	X0A	7	Subclock input oscillation pin
6	Vcc	_	Power supply pin
7	С	_	Decoupling capacitor connection pin
	PF2		General-purpose I/O port
8	RST	Α	Reset pin
	NOT		Dedicated reset pin on MB95F562H/F563H/F564H
	P63		General-purpose I/O port
9		E	High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
	P62		General-purpose I/O port
10	_	E	High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11			
12	NC		It is an internally connected pin. Always leave it unconnected.
13	140		The is an internally conflected pin. Always leave it unconflected.
14			
	P00		General-purpose I/O port
15		D	High-current pin
	AN00		A/D converter analog input pin
	P64		General-purpose I/O port
16	-	E	High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
	P01		General-purpose I/O port
17		D	High-current pin
	AN01		A/D converter analog input pin
	P02		General-purpose I/O port
		<b>↓</b>	High-current pin
18	INT02	D	External interrupt input pin
	AN02	_	A/D converter analog input pin
	SCK		LIN-UART clock I/O pin



Pin no.	Pin name	I/O circuit type*	Function
	P03		General-purpose I/O port
	P03		High-current pin
19	INT03	D	External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
	P04		General-purpose I/O port
_	INT04		External interrupt input pin
20	AN04	D	A/D converter analog input pin
_	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
	Doc		General-purpose I/O port
	P05		High-current pin
21	INT05	D	External interrupt input pin
-	AN05		A/D converter analog input pin
-	TO00		8/16-bit composite timer ch. 0 output pin
	P06		General-purpose I/O port
00		E	High-current pin
22	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
	P12		General-purpose I/O port
23	EC0	F	8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
	D07		General-purpose I/O port
24	P07	E	High-current pin
	INT07		External interrupt input pin
25			· · ·
26			
27			
28	NO		It is an internally compacted him. Always Is and it was a set of
29	NC	_	It is an internally connected pin. Always leave it unconnected.
30			
31			
32			

<sup>\*:</sup> For the I/O circuit types, see "I/O Circuit Type".



# 6. Pin Functions (MB95560H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function		
1	PF0	В	General-purpose I/O port		
'	X0		Main clock input oscillation pin		
2	PF1	В	General-purpose I/O port		
	X1	7 6	Main clock I/O oscillation pin		
3	Vss	_	Power supply pin (GND)		
4	PG2	С	General-purpose I/O port		
7	X1A		Subclock I/O oscillation pin		
5	PG1	С	General-purpose I/O port		
	X0A		Subclock input oscillation pin		
6	Vcc	_	Power supply pin		
7	С	_	Decoupling capacitor connection pin		
	PF2		General-purpose I/O port		
8	RST	Α	Reset pin		
	NOT		Dedicated reset pin on MB95F562H/F563H/F564H		
	P62		General-purpose I/O port		
9		E	High-current pin		
	TO10		8/16-bit composite timer ch. 1 output pin		
	P63		General-purpose I/O port		
10		E	High-current pin		
	TO11		8/16-bit composite timer ch. 1 output pin		
	P64		General-purpose I/O port		
11	-	E	High-current pin		
	EC1		8/16-bit composite timer ch. 1 clock input pin		
	P00		General-purpose I/O port		
12		D	High-current pin		
	AN00		A/D converter analog input pin		
	P01	_	General-purpose I/O port		
13		D	High-current pin		
	AN01		A/D converter analog input pin		
	P02		General-purpose I/O port		
		_	High-current pin		
14	INT02	D	External interrupt input pin		
	AN02		A/D converter analog input pin		
	SCK		LIN-UART clock I/O pin		
	P03		General-purpose I/O port		
_		<b>↓</b> _	High-current pin		
15	INT03	D	External interrupt input pin		
	AN03	_	A/D converter analog input pin		
	SOT		LIN-UART data output pin		



Pin no.	Pin name	I/O circuit type*	Function		
	P04		General-purpose I/O port		
	INT04	Ī	External interrupt input pin		
16	AN04	D	A/D converter analog input pin		
	SIN	Ī	LIN-UART data input pin		
	EC0	1	8/16-bit composite timer ch. 0 clock input pin		
	DOE		General-purpose I/O port		
	P05		High-current pin		
17	INT05	D	External interrupt input pin		
	AN05	1	A/D converter analog input pin		
	TO00	1	8/16-bit composite timer ch. 0 output pin		
	P06	E	General-purpose I/O port		
18			High-current pin		
10	INT06	<b>†</b>	External interrupt input pin		
	TO01	1	8/16-bit composite timer ch. 0 output pin		
	P07		General-purpose I/O port		
19	P01	Е	High-current pin		
	INT07	1	External interrupt input pin		
	P12		General-purpose I/O port		
20	EC0	F	8/16-bit composite timer ch. 0 clock input pin		
	DBG		DBG input pin		

<sup>\*:</sup> For the I/O circuit types, see "I/O Circuit Type".



# 7. Pin Functions (MB95570H Series, 8 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	Vss	_	Power supply pin (GND)
2	Vcc	_	Power supply pin
3	С	_	Decoupling capacitor connection pin
	PF2		General-purpose I/O port
4	RST	А	Reset pin Dedicated reset pin on MB95F572H/F573H/F574H
	P04		General-purpose I/O port
5	INT04	D	External interrupt input pin
5	AN04	U	A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
	P05		General-purpose I/O port High-current pin
6	AN05	D	A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
-	P06	_	General-purpose I/O port High-current pin
7	INT06	Е	External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
	P12		General-purpose I/O port
8	EC0	F	8/16-bit composite timer ch. 0 clock input pin
	DBG	•	DBG input pin

<sup>\*:</sup> For the I/O circuit types, see "I/O Circuit Type".



# 8. Pin Functions (MB95580H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function			
	PF1	В	General-purpose I/O port			
1	1 X1		Main clock I/O oscillation pin			
	PF0	_	General-purpose I/O port			
2	X0	В	Main clock input oscillation pin			
3	Vss	<u> </u>	Power supply pin (GND)			
4	PG2	С	General-purpose I/O port			
4	X1A		Subclock I/O oscillation pin			
5	PG1	С	General-purpose I/O port			
5	X0A		Subclock input oscillation pin			
6	Vcc	_	Power supply pin			
7	С	_	Decoupling capacitor connection pin			
	PF2		General-purpose I/O port			
8	RST	A	Reset pin Dedicated reset pin on MB95F582H/F583H/F584H			
9 10 11						
12 13	NC	_	It is an internally connected pin. Always leave it unconnected.			
14						
15						
16						
17	P01	D	General-purpose I/O port High-current pin			
	AN01	]	A/D converter analog input pin			
	P02		General-purpose I/O port High-current pin			
18	INT02	D	External interrupt input pin			
	AN02	1	A/D converter analog input pin			
	SCK	1	LIN-UART clock I/O pin			
	P03		General-purpose I/O port High-current pin			
19	INT03	D	External interrupt input pin			
	AN03	1	A/D converter analog input pin			
	SOT	]	LIN-UART data output pin			



Pin no.	Pin name	I/O circuit type*	Function			
	P04		General-purpose I/O port			
	INT04	7	External interrupt input pin			
20	AN04	D	A/D converter analog input pin			
	SIN	7	LIN-UART data input pin			
	EC0		8/16-bit composite timer ch. 0 clock input pin			
	P05		General-purpose I/O port High-current pin			
21	INT05	D	External interrupt input pin			
	AN05		A/D converter analog input pin			
	TO00	7	8/16-bit composite timer ch. 0 output pin			
	P06	_	General-purpose I/O port High-current pin			
22	INT06	E	External interrupt input pin			
	TO01	7	8/16-bit composite timer ch. 0 output pin			
	P12		General-purpose I/O port			
23	EC0	F	8/16-bit composite timer ch. 0 clock input pin			
	DBG	1	DBG input pin			
24	P07	E	General-purpose I/O port High-current pin			
	INT07		External interrupt input pin			
25						
26						
27						
28	NC		It is an internally connected pin. Always leave it unconnected.			
29	INC	_	it is an internally conflected pin. Always leave it unconflected.			
30						
31						
32						

<sup>\*:</sup> For the I/O circuit types, see "I/O Circuit Type".



# 9. Pin Functions (MB95580H Series, 16 pins)

Pin no.	Pin name	I/O circuit type*	Function
4	PF0		General-purpose I/O port
1	X0	В	Main clock input oscillation pin
2	2 PF1 X1		General-purpose I/O port
			Main clock I/O oscillation pin
3	Vss	_	Power supply pin (GND)
4	PG2	С	General-purpose I/O port
4	X1A		Subclock I/O oscillation pin
5	PG1	С	General-purpose I/O port
5	X0A		Subclock input oscillation pin
6	Vcc	_	Power supply pin
	PF2		General-purpose I/O port
7	7 RST		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
8	С	_	Decoupling capacitor connection pin
	P02		General-purpose I/O port High-current pin
9	INT02	D	External interrupt input pin
	AN02	7	A/D converter analog input pin
	SCK	7	LIN-UART clock I/O pin
10	P01	D	General-purpose I/O port High-current pin
	AN01	1	A/D converter analog input pin
	P03		General-purpose I/O port High-current pin
11	INT03	D	External interrupt input pin
	AN03	1	A/D converter analog input pin
	SOT	7	LIN-UART data output pin
	P04		General-purpose I/O port
	INT04		External interrupt input pin
12	AN04	D	A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

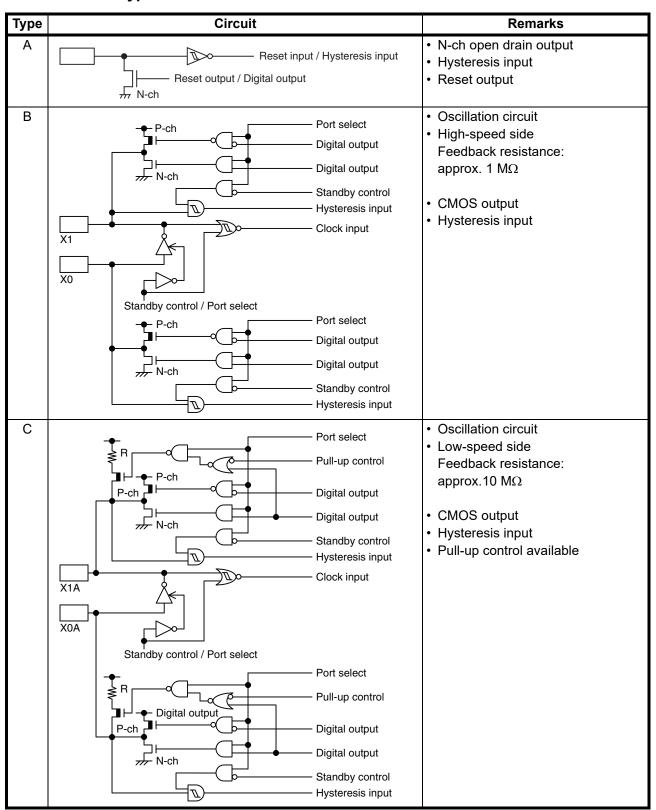


Pin no.	Pin name	I/O circuit type*	Function
	P05		General-purpose I/O port High-current pin
13	INT05	D	External interrupt input pin
	AN05	Ī	A/D converter analog input pin
	TO00	Ī	8/16-bit composite timer ch. 0 output pin
4.4	P06	_	General-purpose I/O port High-current pin
14	INT06	E	External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
15	P07	E	General-purpose I/O port High-current pin
	INT07	Ī	External interrupt input pin
	P12		General-purpose I/O port
16	EC0	F	8/16-bit composite timer ch. 0 clock input pin
-	DBG		DBG input pin

<sup>\*:</sup> For the I/O circuit types, see "I/O Circuit Type".



## 10. I/O Circuit Type





Type	Circuit	Remarks
D	Pull-up control  P-ch  Digital output  N-ch	<ul><li>CMOS output</li><li>Hysteresis input</li><li>Pull-up control available</li><li>Analog input</li></ul>
	Analog input  A/D control Standby control Hysteresis input	
Е	Pull-up control  P-ch  Digital output  Digital output  Standby control  Hysteresis input	CMOS output     Hysteresis input     Pull-up control available
F	Standby control  Hysteresis input  N-ch	N-ch open drain output     Hysteresis input

## 11. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

## 11.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

## Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.



### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### • Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

#### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

#### • Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.



### 11.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

## • Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

#### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  - When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

## Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

#### Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:



- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 M $\Omega$ ).
  - Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

#### 11.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 12. Notes On Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V<sub>CC</sub> or a voltage lower than V<sub>SS</sub> is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "24.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the V<sub>CC</sub> pin or the V<sub>SS</sub> pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage



Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V<sub>CC</sub> power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in  $V_{CC}$  ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard  $V_{CC}$  value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

#### Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

#### 13. Pin Connection

### · Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latchups. Always pull up or pull down an unused input pin through a resistor of at least 2 k $\Omega$ . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

#### · Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the Vcc pin and the Vss pin to the power supply and ground outside the device. In addition, connect the current supply source to the Vcc pin and the Vss pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a decoupling capacitor between the Vcc pin and the Vss pin at a location close to this device.

#### DBG pin

Connect the DBG pin to an external pull-up resistor of 2 k $\Omega$  or above.

After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

### • RST pin

Connect the  $\overline{\mathsf{RST}}$  pin to an external pull-up resistor of 2 k $\Omega$  or above.

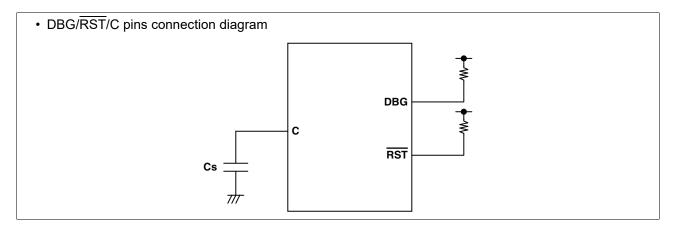
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the RST pin and that between a pull-up resistor and the Vcc pin when designing the layout of the printed circuit board.

The PF2/RST pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/RST pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

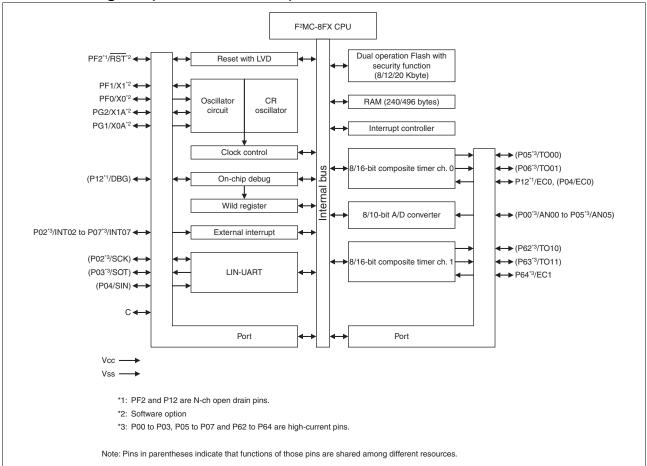
#### C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V<sub>CC</sub> pin must have a capacitance equal to or larger than the capacitance of C<sub>S</sub>. For the connection to a decoupling capacitor C<sub>S</sub>, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C<sub>S</sub> and the distance between C<sub>S</sub> and the V<sub>SS</sub> pin when designing the layout of a printed circuit board.



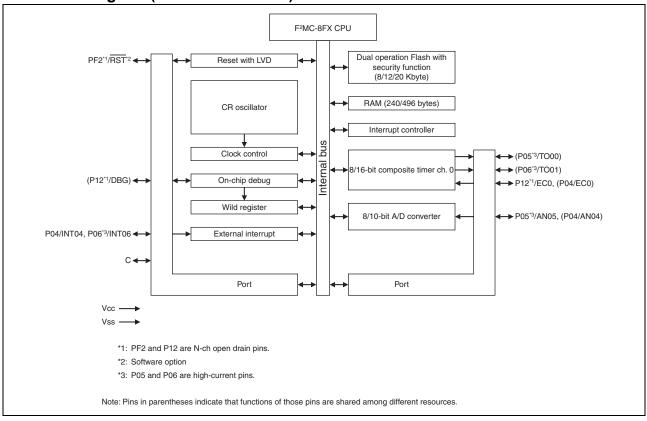


## 14. Block Diagram (MB95560H Series)



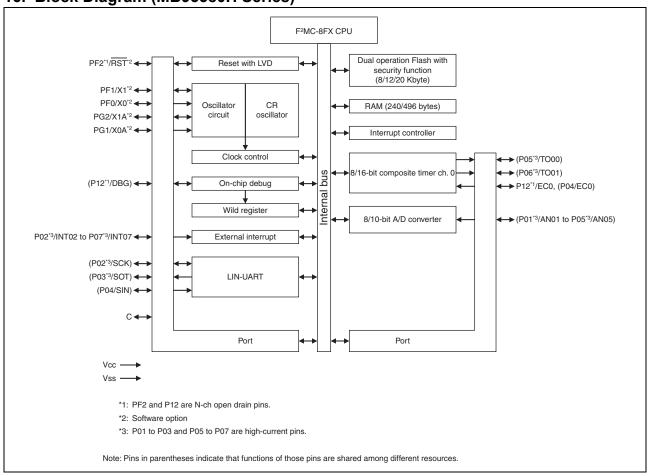


## 15. Block Diagram (MB95570H Series)





## 16. Block Diagram (MB95580H Series)





## 17. CPU Core

Memory space

The memory space of the MB95560H/570H/580H is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95560H/570H/580H are shown below.8

Memory maps

MB95F562H/F562K/F572H/ F572K/F582H/F582K		MB95F563H/F563K/F573H/ F573K/F583H/F583K		MB95F564H/F564K/F574H/ F574K/F584H/F584K	
Г	-3/2N/F302H/F302N		F3/3N/F303H/F303N		F3/4K/F304H/F304K
0000н	I/O area	0000н	I/O area	0000н	I/O area
0080н	Access prohibited	0080н	Access prohibited	0080н	Access prohibited
0090н	RAM 240 bytes	0090н	RAM 496 bytes	0090н	RAM 496 bytes
0100н 0180н	Register	0100н	Register	0100н	Register
0180H		0200н		0200н	3
0500	Access prohibited	0280 <sub>H</sub>	Access prohibited	0280н -	Access prohibited
0F80н —	Extension I/O area	0F80 <sub>H</sub> -	Extension I/O area	0F80 <sub>H</sub> -	Extension I/O area
1000н —		1000н		1000⊦	
	Access prohibited		Access prohibited		Access prohibited
В000н —		В000н		В000н	
С000н	Flash 4 Kbyte	С000н	Flash 4 Kbyte		
	Access prohibited		Access prohibited		Flash 20 Kbyte
		Е000н -			
F000 <sub>H</sub>	Flash 4 Kbyte		Flash 8 Kbyte		
FFFF <sub>H</sub> L	1 Idolf 4 Royto	FFFF <sub>H</sub> <sup>[</sup>		FFFF <sub>H</sub> <sup>↓</sup>	



# 18. I/O Map (MB95560H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000н	PDR0	Port 0 data register	R/W	0000000В
0001н	DDR0	Port 0 direction register	R/W R/W	0000000В
0002н	PDR1	Port 1 data register		0000000в
0003н	DDR1	Port 1 direction register	R/W	0000000в
0004н	_	(Disabled)		—
0005н	WATR	Oscillation stabilization wait time setting register	R/W	11111111В
0006н	PLLC	PLL control register	R/W	000Х0000в
0007н	SYCC	System clock control register	R/W	ХХХ11011в
н8000	STBC	Standby control register	R/W	0000000в
0009н	RSRR	Reset source register	R/W	000XXXXXB
000Ан	TBTC	Time-base timer control register	R/W	0000000в
000Вн	WPCR	Watch prescaler control register	R/W	0000000в
000Сн	WDTC	Watchdog timer control register	R/W	00XX0000 <sub>B</sub>
000Дн	SYCC2	System clock control register 2	R/W	XXXX0011 <sub>B</sub>
000Ен	STBC2	Standby control register 2	R/W	0000000в
000Fн		·		
to		(Disabled)	'	_
0015н		,		
0016н	PDR6	Port 6 data register	R/W	0000000в
0017н	DDR6	Port 6 direction register		0000000в
0018н			<u> </u>	
to		(Disabled)		_
0027н		,		
0028н	PDRF	Port F data register	R/W	0000000в
0029н	DDRF	Port F direction register	R/W	0000000В
002Ан	PDRG	Port G data register	R/W	0000000
002Вн	DDRG	Port G direction register	R/W	0000000в
002Сн	PUL0	Port 0 pull-up register	R/W	0000000в
002Dн		1 1 5		
to		(Disabled)		_
0032н				
0033н	PUL6	Port 6 pull-up register	R/W	0000000в
0034н	_	(Disabled)		_
0035н	PULG	Port G pull-up register	R/W	0000000в
0036н	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000в
0037н	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0000000В
0038н	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0000000В
0039н	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000В
003Ан			† · · · · ·	,
to	_	(Disabled)		_
0048н		(5.532.53)		



Address	Register abbreviation	Register name	R/W	Initial value
0049н	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0000000В
004Ан	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0000000В
004Вн	EIC30	External interrupt circuit control register ch. 6/ch. 7		0000000В
004Сн,	_	(Disabled)		_
004Dн	LVDD	IVDD manak walka manaka sala shi ma ID manisha m	DAA	0000000
004EH	LVDR	LVDR reset voltage selection ID register	R/W	0000000В
004Fн	SCR	(Disabled)		
0050н		LIN-UART serial control register	R/W	0000000в 0000000в
0051н	SMR	LIN-UART serial mode register	R/W	
0052н	SSR	LIN-UART serial status register	-	00001000в
0053н	RDR	LIN-UART receive data register	R/W	0000000в
0054	TDR	LIN-UART transmit data register	R/W	00000000в
0054н	ESCR	LIN-UART extended status control register	R/W	00000100в
0055н	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056н to		(Disabled)	_	_
006Вн		(Bloabloa)		
006Сн	ADC1	8/10-bit A/D converter control register 1	R/W	00000000в
006Dн	ADC2	8/10-bit A/D converter control register 2	R/W	0000000В
006Ен	ADDH	8/10-bit A/D converter data register (upper)	R/W	0000000В
006Fн	ADDL	8/10-bit A/D converter data register (lower)	R/W	0000000В
0070н	_	(Disabled)	T	_
0071н	FSR2	Flash memory status register 2	R/W	0000000В
0072н	FSR	Flash memory status register	R/W	000Х0000в
0073н	SWRE0	Flash memory sector write control register 0	R/W	0000000В
0074н	FSR3	Flash memory status register 3	R	000XXXXXB
0075н	FSR4	Flash memory status register 4	R/W	0000000В
0076н	WREN	Wild register address compare enable register	R/W	0000000В
0077н	WROR	Wild register data test setting register	R/W	0000000В
0078н	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0079н	ILR0	Interrupt level setting register 0	R/W	111111111
007Ан	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007Вн	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007Сн	ILR3	Interrupt level setting register 3	R/W	11111111В
007Dн	ILR4	Interrupt level setting register 4	R/W	11111111в
007Ен	ILR5	Interrupt level setting register 5	R/W	11111111В
007Fн	_	(Disabled)	_	
0F80н	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0000000В
0F81н	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0000000В
0F82н	WRDR0	Wild register data setting register ch. 0	R/W	0000000В



Address	Register abbreviation	Register name	R/W	Initial value
0F83н	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0000000В
0F84н	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0000000в
0F85н	WRDR1	Wild register data setting register ch. 1	R/W	0000000В
0F86н	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0000000в
0F87н	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0000000В
0F88н	WRDR2	Wild register data setting register ch. 2	R/W	0000000В
0F89н				
to 0F91н	_	(Disabled)	_	_
0F92н	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000в
0F93н	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0000000в
0F94н	T01DR	8/16-bit composite timer 01 data register	R/W	0000000в
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register	R/W	0000000В
0F96н	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0000000в
0F97н	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0000000в
0F98н	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000в
0F99н	T11DR	8/16-bit composite timer 11 data register	R/W	0000000в
0F9Ан	T10DR	8/16-bit composite timer 10 data register	R/W	0000000в
0F9Вн	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0000000в
0F9Сн to 0FBВн	_	(Disabled)	_	_
0FBCн	BGR1	LIN-UART baud rate generator register 1	R/W	00000000в
0FBDн	BGR0	LIN-UART baud rate generator register 0	R/W	00000000в
0FBEн to 0FC2н	_	(Disabled)	_	_
0FС3н	AIDRL	A/D input disable register (lower)	R/W	0000000в
0FC4н to 0FE3н	_	(Disabled)	_	_
0FE4н	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXXB
0FE5н	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXXB
0FE6н	_	(Disabled)	_	_
0FE7н	CRTDA	Main CR clock temperature dependent adjustment register	R/W	000XXXXXB
0FE8н	SYSC	System configuration register	R/W	11000011в
0FE9н	CMCR	Clock monitoring control register	R/W	0000000
0FEAн	CMDR	Clock monitoring data register	R	00000000в



Address	Register abbreviation	Register name	R/W	Initial value
0FEBн	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXXB
0FEC <sub>H</sub>	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXX
0FEDн to 0FFFн	_	(Disabled)		_

• R/W access symbols

R/W : Readable / Writable

R : Read only

· Initial value symbols

The initial value of this bit is "0".The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.



# 19. I/O Map (MB95570H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000н	PDR0	Port 0 data register	R/W	0000000В
0001н	DDR0	Port 0 direction register	R/W	0000000В
0002н	PDR1	Port 1 data register	R/W	0000000В
0003н	DDR1	Port 1 direction register	R/W	0000000В
0004н		(Disabled)	_	
0005н	WATR	Oscillation stabilization wait time setting register	R/W	111111111
0006н	PLLC	PLL control register	R/W	000Х0000в
0007н	SYCC	System clock control register	R/W	XXX11011 <sub>B</sub>
0008н	STBC	Standby control register	R/W	0000000В
0009н	RSRR	Reset source register	R/W	000XXXXXB
000Ан	TBTC	Time-base timer control register	R/W	0000000в
000Вн	WPCR	Watch prescaler control register	R/W	0000000В
000Сн	WDTC	Watchdog timer control register	R/W	00XX0000 <sub>B</sub>
000Дн	SYCC2	System clock control register 2	R/W	XXXX0011 <sub>B</sub>
000Ен	STBC2	Standby control register 2	R/W	0000000в
000Fн		-		
to	_	(Disabled)	_	_
0027н				
0028н	PDRF	Port F data register	R/W	0000000в
0029н	DDRF	Port F direction register	R/W	00000000в
002Ан,		(Disabled)		
002Вн	_	(Disabled)	_	
002Сн	PUL0	Port 0 pull-up register	R/W	00000000в
002Dн				
to	_	(Disabled)	_	_
0035н		, , ,		
0036н	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000в
0037н	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000в
0038н				
to	_	(Disabled)	_	
0049н		, , ,		
004Ан	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000в
004Вн	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0000000в
004Сн,				
004Dн	_	(Disabled)		_
004Ен	LVDR	LVDR reset voltage selection ID register	R/W	0000000В
004Fн				
to	<del></del>	(Disabled)	_	
006Вн		, ,		



Address	Register abbreviation	Register name	R/W	Initial value
006Сн	ADC1	8/10-bit A/D converter control register 1	R/W	0000000в
006Dн	ADC2	8/10-bit A/D converter control register 2	R/W	0000000в
006Ен	ADDH	8/10-bit A/D converter data register (upper)	R/W	0000000в
006Fн	ADDL	8/10-bit A/D converter data register (lower)	R/W	0000000в
0070н	_	(Disabled)	<u> </u>	_
0071н	FSR2	Flash memory status register 2	R/W	0000000в
0072н	FSR	Flash memory status register	R/W	000Х0000в
0073н	SWRE0	Flash memory sector write control register 0	R/W	0000000в
0074н	FSR3	Flash memory status register 3	R	000XXXXXB
0075н	FSR4	Flash memory status register 4	R/W	0000000в
0076н	WREN	Wild register address compare enable register	R/W	0000000в
0077н	WROR	Wild register data test setting register	R/W	0000000в
0078н	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0079н	ILR0	Interrupt level setting register 0	R/W	111111111
007Ан	ILR1	Interrupt level setting register 1	R/W	111111111
007Вн,		(Dischlad)		
007Сн	_	(Disabled)	_	_
007Dн	ILR4	Interrupt level setting register 4	R/W	111111111
007Ен	ILR5	Interrupt level setting register 5	R/W	111111111
007Fн	_	(Disabled)	_	_
0F80н	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0000000в
0F81н	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0000000в
0F82н	WRDR0	Wild register data setting register ch. 0	R/W	00000000в
0F83н	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000в
0F84н	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000в
0F85н	WRDR1	Wild register data setting register ch. 1	R/W	00000000в
0F86н	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000в
0F87н	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0000000в
0F88н	WRDR2	Wild register data setting register ch. 2	R/W	0000000В
0F89н				
to	_	(Disabled)	_	
0F91н		, , ,		
0F92н	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0000000
0F93н	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0000000В
0F94н	T01DR	8/16-bit composite timer 01 data register	R/W	0000000в
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register	R/W	0000000в
0F96н	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0000000в
0F97н				
to	_	(Disabled)	_	_
0FC2н		, ,		



Address	Register abbreviation	Register name	R/W	Initial value
0FС3н	AIDRL	A/D input disable register (lower)	R/W	0000000в
0FC4н to 0FE3н	1	(Disabled)		_
0FE4н	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXXB
0FE5н	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXXB
0FE6н	_	(Disabled)	_	_
0FE7н	CRTDA	Main CR clock temperature dependent adjustment register	R/W	000XXXXXB
0FE8н	SYSC	System configuration register	R/W	11000011в
0FE9н	CMCR	Clock monitoring control register	R/W	0000000в
0FEAн	CMDR	Clock monitoring data register	R	0000000в
0FEBн	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXXB
0FECн	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXX
0FEDн to 0FFFн	_	(Disabled)	_	_

• R/W access symbols

R/W : Readable / Writable

R : Read only

• Initial value symbols

The initial value of this bit is "0".The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.



# 20. I/O Map (MB95580H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000н	PDR0	Port 0 data register	R/W	0000000В
0001н	DDR0	Port 0 direction register	R/W	0000000В
0002н	PDR1	Port 1 data register	R/W	0000000В
0003н	DDR1	Port 1 direction register	R/W	0000000В
0004н	_	(Disabled)	_	
0005н	WATR	Oscillation stabilization wait time setting register	R/W	111111111
0006н	PLLC	PLL control register	R/W	000Х0000в
0007н	SYCC	System clock control register	R/W	XXX11011 <sub>B</sub>
0008н	STBC	Standby control register	R/W	0000000В
0009н	RSRR	Reset source register	R/W	000XXXXXB
000Ан	TBTC	Time-base timer control register	R/W	0000000в
000Вн	WPCR	Watch prescaler control register	R/W	0000000В
000Сн	WDTC	Watchdog timer control register	R/W	00XX0000 <sub>B</sub>
000Дн	SYCC2	System clock control register 2	R/W	XXXX0011 <sub>B</sub>
000Ен	STBC2	Standby control register 2	R/W	0000000в
000Fн				
to	_	(Disabled)		
0027н		,		
0028н	PDRF	Port F data register	R/W	0000000в
0029н	DDRF	Port F direction register	R/W	0000000в
002Ан	PDRG	Port G data register	R/W	0000000в
002Вн	DDRG	Port G direction register	R/W	0000000в
002Сн	PUL0	Port 0 pull-up register	R/W	0000000в
002Dн				
to	_	(Disabled)	_	
0034н		,		
0035н	PULG	Port G pull-up register	R/W	0000000В
0036н	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0000000в
0037н	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0000000в
0038н		·		
to	_	(Disabled)	_	
0048н				
0049н	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0000000В
004Ан	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0000000В
004Вн	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0000000В
004Сн,		,		
004Dн	<del>-</del>	(Disabled)	-	
004Ен	LVDR	LVDR reset voltage selection ID register	R/W	0000000В
004Fн	_	(Disabled)	<u> </u>	_



Address	Register abbreviation	Register name	R/W	Initial value
0050н	SCR	LIN-UART serial control register	R/W	0000000в
0051н	SMR	LIN-UART serial mode register	R/W	0000000в
0052н	SSR	LIN-UART serial status register	R/W	00001000в
0053н	RDR	LIN-UART receive data register	R/W	0000000в
0055н	TDR	LIN-UART transmit data register	R/W	0000000в
0054н	ESCR	LIN-UART extended status control register	R/W	00000100в
0055н	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056н		-		
to	_	(Disabled)	<b> </b> —	_
006Вн		, , ,		
006Сн	ADC1	8/10-bit A/D converter control register 1	R/W	0000000
006Dн	ADC2	8/10-bit A/D converter control register 2	R/W	0000000
006Ен	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000в
006Fн	ADDL	8/10-bit A/D converter data register (lower)	R/W	0000000В
0070н	_	(Disabled)	_	_
0071н	FSR2	Flash memory status register 2	R/W	0000000В
0072н	FSR	Flash memory status register	R/W	000Х0000в
0073н	SWRE0	Flash memory sector write control register 0	R/W	0000000В
0074н	FSR3	Flash memory status register 3	R	000XXXXXB
0075н	FSR4	Flash memory status register 4	R/W	0000000В
0076н	WREN	Wild register address compare enable register	R/W	0000000В
0077н	WROR	Wild register data test setting register	R/W	0000000В
0078н	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	-	_
0079н	ILR0	Interrupt level setting register 0	R/W	11111111В
007Ан	ILR1	Interrupt level setting register 1	R/W	111111111
007Вн	ILR2	Interrupt level setting register 2	R/W	11111111В
007Сн	_	(Disabled)	<u> </u>	_
007Dн	ILR4	Interrupt level setting register 4	R/W	111111111
007Ен	ILR5	Interrupt level setting register 5	R/W	111111111
007Fн	_	(Disabled)	<u> </u>	_
0F80н	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0000000в
0F81н	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0000000в
0F82н	WRDR0	Wild register data setting register ch. 0	R/W	0000000в
0F83н	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0000000в
0F84н	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0000000в
0F85⊦	WRDR1	Wild register data setting register ch. 1	R/W	0000000в
0F86н	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0000000в
0F87н	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0000000в
0F88н	WRDR2	Wild register data setting register ch. 2	R/W	0000000В



Address	Register abbreviation	Register name	R/W	Initial value
0F89н				
to	_	(Disabled)	_	_
0F91н				
0F92н	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0000000В
0F93н	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0000000В
0F94н	T01DR	8/16-bit composite timer 01 data register	R/W	0000000В
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register	R/W	0000000В
0F96н	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0000000В
0F97 <sub>H</sub>				
to	_	(Disabled)	_	
0FBBн				
0FBCн	BGR1	LIN-UART baud rate generator register 1	R/W	0000000В
0FBDн	BGR0	LIN-UART baud rate generator register 0	R/W	0000000В
0FBЕн				
to	_	(Disabled)	_	
0FC2н				
0FС3н	AIDRL	A/D input disable register (lower)	R/W	0000000в
0FC4н				
to	_	(Disabled)	_	
0FЕ3н				
0FE4н	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXXB
0FE5н	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXXB
0FE6н	_	(Disabled)	_	<del></del>
0FE7н	CRTDA	Main CR clock temperature dependent adjustment register	R/W	000XXXXXB
0FE8н	SYSC	System configuration register	R/W	11000011в
0FE9н	CMCR	Clock monitoring control register	R/W	0000000В
0FEAн	CMDR	Clock monitoring data register	R	0000000в
0FEBн	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX
0FEC <sub>H</sub>	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXXB
0FEDн		,		
to	_	(Disabled)	—	
0FFFн				

# • R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is "0".1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.



# 21. Interrupt Source Table (MB95560H Series)

		Vector tab	le address		Priority order of
Interrupt source	Interrupt request number	Upper	Lower	Bit name of interrupt level setting register	interruptsources of the same level (occurring simultaneously)
External interrupt ch. 4	IRQ00	FFFA⊦	FFFB⊦	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	<b>A</b>
External interrupt ch. 2	IRQ02	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	1.02 [1:0]	
External interrupt ch. 6	IRQUZ	ГГГОН		L02 [1:0]	
External interrupt ch. 3	IRQ03	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	1.02 [4:0]	
External interrupt ch. 7	IRQUS		ГГГЭН	L03 [1:0]	
_	IRQ04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEEH	FFEFH	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC⊦	FFEDH	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA⊦	FFEB⊦	L08 [1:0]	
<del>-</del>	IRQ09	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]	
_	IRQ10	FFE6⊦	FFE7 <sub>H</sub>	L10 [1:0]	
	IRQ11	FFE4 <sub>H</sub>	FFE5⊦	L11 [1:0]	
_	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
_	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE <sub>H</sub>	FFDFн	L14 [1:0]	
	IRQ15	FFDC⊦	FFDD⊦	L15 [1:0]	
_	IRQ16	FFDA⊦	FFDB⊦	L16 [1:0]	
-	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6⊦	FFD7 <sub>H</sub>	L18 [1:0]	
Time-base timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2⊦	FFD3 <sub>H</sub>	L20 [1:0]	
_	IRQ21	FFD0⊦	FFD1 <sub>H</sub>	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCEH	FFCF <sub>H</sub>	L22 [1:0]	
Flash memory	IRQ23	FFCCH	FFCDH	L23 [1:0]	Low



# 22. Interrupt Source Table (MB95570H Series)

		Vector tab	le address		Priority order of
Interrupt source	Interrupt request number	Upper	Lower	Bit name of interrupt level setting register	interruptsources of the same level (occurring simultaneously)
External interrupt ch. 4	IRQ00	FFFA⊦	FFFB⊦	L00 [1:0]	High
_	IRQ01	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	<b>A</b>
External interrupt ch. 6	IRQ02	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1:0]	
_ _	IRQ03	FFF4 <sub>H</sub>	FFF5⊦	L03 [1:0]	
	IRQ04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 <sub>H</sub>	FFF1н	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEEH	FFEFH	L06 [1:0]	
<del></del>	IRQ07	FFECH	FFEDH	L07 [1:0]	
<del></del>	IRQ08	FFEAH	FFEBH	L08 [1:0]	
_	IRQ09	FFE8 <sub>H</sub>	FFE9н	L09 [1:0]	
_	IRQ10	FFE6⊦	FFE7 <sub>H</sub>	L10 [1:0]	
_	IRQ11	FFE4 <sub>H</sub>	FFE5⊦	L11 [1:0]	
_	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
_	IRQ13	FFE0⊦	FFE1 <sub>H</sub>	L13 [1:0]	
_	IRQ14	FFDE⊦⊦	FFDF⊨	L14 [1:0]	
_	IRQ15	FFDC⊦	FFDD⊦	L15 [1:0]	
_	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]	
_	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6⊦	FFD7 <sub>H</sub>	L18 [1:0]	
Time-base timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	
<del></del>	IRQ21	FFD0н	FFD1 <sub>H</sub>	L21 [1:0]	
_	IRQ22	FFCEH	FFCF <sub>H</sub>	L22 [1:0]	▼
Flash memory	IRQ23	FFCCH	FFCDн	L23 [1:0]	Low



# 23. Interrupt Source Table (MB95580H Series)

		Vector tab	le address		Priority order of
Interrupt source	Interrupt request number	Upper	Lower	Bit name of interrupt level setting register	interruptsources of the same level (occurring simultaneously)
External interrupt ch. 4	IRQ00	FFFA⊦	FFFB⊦	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	<b>A</b>
External interrupt ch. 2	IRQ02	FFF6⊦	FFF7 <sub>H</sub>	L02 [1:0]	
External interrupt ch. 6	II\QUZ	TTTOH	1117H	LUZ [1.0]	
External interrupt ch. 3	IRQ03	FFF4 <sub>H</sub>	FFF5⊧	L03 [1:0]	
External interrupt ch. 7	IIIQUS	1114	I I I JH	L03 [1.0]	
_	IRQ04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEEH	FFEFH	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFECH	FFEDH	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEAH	FFEBH	L08 [1:0]	
_	IRQ09	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]	
_	IRQ10	FFE6⊦	FFE7 <sub>H</sub>	L10 [1:0]	
_	IRQ11	FFE4 <sub>H</sub>	FFE5⊧	L11 [1:0]	
_	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
_	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	
_	IRQ14	FFDE⊦	FFDFн	L14 [1:0]	
_	IRQ15	FFDCH	FFDDн	L15 [1:0]	
_	IRQ16	FFDA⊦	FFDB⊦	L16 [1:0]	
_	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6⊧	FFD7 <sub>H</sub>	L18 [1:0]	
Time-base timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	
_	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]	
	IRQ22	FFCEH	FFCF <sub>H</sub>	L22 [1:0]	▼
Flash memory	IRQ23	FFCCH	FFCDH	L23 [1:0]	Low



# 24. Electrical Characteristics

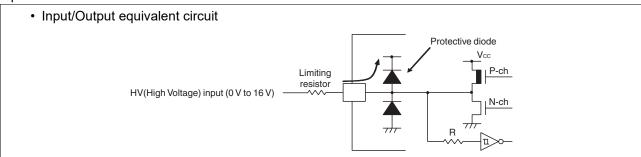
# 24.1 Absolute Maximum Ratings

Davamatav	Cumahad	Rating		l lm!4	Pamarka		
Parameter	Symbol	Min	Max	Unit	Remarks		
Power supply voltage*1	Vcc	Vss - 0.3	Vss + 6	V			
Input voltage*1	Vı	Vss - 0.3	Vss + 6	V	*2		
Output voltage*1	Vo	Vss - 0.3	Vss + 6	V	*2		
Maximum clamp current	<b>I</b> CLAMP	-2	+2	mA	Applicable to specific pins*3		
Total maximum clamp current	$\Sigma$   CLAMP	_	20	mA	Applicable to specific pins*3		
"L" level maximum output current	lol	_	15	mA			
"L" level average current	lolav1	_	4	mA	Other than P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin)		
	lolav2		12		P00 to P03, P05 to P07, P62 to P64*4  Average output current= operating current × operating ratio (1 pin)		
"L" level total maximum output current	ΣΙοι	_	100	mA			
"L" level total average output current	$\Sigma$ lolav		50	mA	Total average output current= operating current × operating ratio (Total number of pins)		
"H" level maximum output current	Іон	_	-15	mA			
"H" level average	Iонаv1	_	-4	mA	Other than P00 to P03, P05 to P07, P62 to P64 <sup>*4</sup> Average output current= operating current × operating ratio (1 pin)		
current	lohav2		-8		P00 to P03, P05 to P07, P62 to P64 <sup>*4</sup> Average output current= operating current × operating ratio (1 pin)		
"H" level total maximum output current	$\Sigma$ Іон	_	-100	mA			
"H" level total average output current	ΣΙοнаν	_	<b>–50</b>	mA	Total average output current= operating current × operating ratio (Total number of pins)		
Power consumption	Pd	_	320	mW			
Operating temperature	TA	-40	+85	°C			
Storage temperature	T <sub>stg</sub>	-55	+150	°C			

<sup>\*1:</sup> These parameters are based on the condition that Vss is 0.0 V.



- \*2: V<sub>I</sub> and V<sub>O</sub> must not exceed V<sub>CC</sub> + 0.3 V. V<sub>I</sub> must not exceed the rated voltage. However, if the maximum current to/ from an input is limited by means of an external component, the I<sub>CLAMP</sub> rating is used instead of the V<sub>I</sub> rating.
- \*3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0. PF1, PG1, and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)
  - · Use under recommended operating conditions.
  - · Use with DC voltage (current).
  - The HV (High Voltage) signal is an input signal exceeding the Vcc voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
  - The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
  - When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the Vcc pin, affecting other devices.
  - If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
  - If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
  - · Do not leave the HV (High Voltage) input pin unconnected.
  - · Example of a recommended circuit:



\*4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.

Do not exceed any of these ratings.

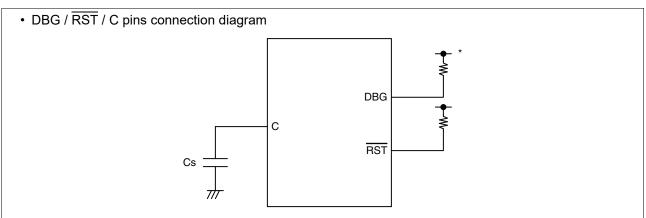


### 24.2 Recommended Operating Conditions

(Vss = 0.0 V)

Parameter	Symbol	Val	lue	Unit	Pom	arks
Faranietei	Symbol	Min	Max	Oiiit	Ken	idi KS
	2.4*1, *2 5.5*1 In normal operation		Other than on-chip debug			
Power supply	Vcc	2.3	5.5	V	Hold condition in stop mode	mode
voltage		2.9	5.5	]	In normal operation	On-chip debug mode
	,	2.3	5.5		Hold condition in stop mode	On-only debug mode
Decoupling capacitor	Cs	0.022	1	μF	*3	
Operating	TA	-40	+85	°C Other than on-chip debug mode		ode
temperature +5 +35		On-chip debug mode				

- \*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.
- \*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.
- \*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the Vcc pin must have a capacitance equal to or larger than the capacitance of Cs. For the connection to a decoupling capacitor Cs, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and Cs and the distance between Cs and the Vss pin when designing the layout of a printed circuit board.



\*: Connect the DBG pin to an external pull-up resistor of 2 k $\Omega$  or above. After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.



### 24.3 DC Characteristics

(Vcc = 5.0 V  $\pm$  10%, Vss = 0.0 V, Ta = -40 °C to +85 °C)

				(1111	Value	•		/, TA = -40 C to +60
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Unit	Remarks
	ViH	P04	_	0.7 Vcc	_	Vcc + 0.3	V	Hysteresis input
"H" level input voltage	V <sub>IHS</sub>	P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4	_	0.8 Vcc		Vcc + 0.3	V	Hysteresis input
	Vінм	PF2	_	0.8 Vcc		Vcc + 0.3	V	Hysteresis input
	VIL	P04	_	Vss - 0.3	_	0.3 Vcc	V	Hysteresis input
"L" level input voltage	VILS	P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4	_	Vss - 0.3		0.2 Vcc	V	Hysteresis input
	VILM	PF2	_	Vss - 0.3	_	0.2 Vcc	V	Hysteresis input
Open-drain output application voltage	VD	P12, PF2	_	Vss - 0.3	_	Vss + 5.5	V	
"H" level	Vон1	P04, PF0*4, PF1*4, PG1*4, PG2	Iон = -4 mA	Vcc - 0.5	_	_	V	
output voltage	V <sub>OH2</sub>	P00*3 to P03*4, P05 to P07*4, P62 to P64*3	Iон = −8 mA	Vcc - 0.5	_	_	V	
"L" level	V <sub>OL1</sub>	P04, P12, PF0 to PF2*4, PG1*4, PG2*4	IoL = 4 mA	_		0.4	V	
voltage	V <sub>OL2</sub>	P00*3 to P03*4, P05 to P07*4, P62 to P64*3	IoL = 12 mA	_		0.4	V	
Input leak current (Hi-Z output leak current)	lu	All input pins	0.0 V < V <sub>I</sub> < V <sub>CC</sub>	-5	—	+5	μΑ	When the internal pull-up resistor is disabled
Internal pull-up resistor	Rpull	P00*3 to P07*4, P62 to P64*3, PG1*4, PG2*4	V <sub>I</sub> = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	Cin	Other than Vcc and Vss	f = 1 MHz	_	5	15	pF	



(Vcc = 5.0 V  $\pm$  10%, Vss = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Danamatan	Ola a l	Din nome	O a maliki a m		Value		11	Demonto
Parameter	Symbol	Pin name	Condition	Min	Typ*1	Max*2	Unit	Remarks
			FcH = 32 MHz	_	3.5	4.4	mA	Except during Flash memory programming and erasing
	Icc		F <sub>MP</sub> = 16 MHz Main clock mode (divided by 2)	_	7.4	9.8	mA	During Flash memory programming and erasing
				_	5.1	6.4	mΑ	At A/D conversion
	Iccs	Vcc (External clock operation)	F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main sleep mode (divided by 2)	_	1.2	1.5	mA	
	IccL		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subclock mode (divided by 2) T <sub>A</sub> = +25 °C	_	65	71	μΑ	
Power supply current*5	Iccls*6		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subsleep mode (divided by 2) T <sub>A</sub> = +25 °C		5.4	7	μΑ	In deep standby mode
	Ісст <sup>*6</sup>		F <sub>CL</sub> = 32 kHz Watch mode T <sub>A</sub> = +25 °C	_	4.8	6.9	μΑ	In deep standby mode
	Іссмск	Vcc	F <sub>CRH</sub> = 4 MHz F <sub>MP</sub> = 4 MHz Main CR clock mode	_	1.1	1.4	mA	
	Iccscr	<b>V</b> CC	Sub-CR clock mode (divided by 2) T <sub>A</sub> = +25 °C	_	58	64	μΑ	
	Ісстѕ	Vсс (External clock operation)	F <sub>CH</sub> = 32 MHz Time-base timer mode T <sub>A</sub> = +25 °C	_	290	340	μΑ	In deep standby mode
	Іссн		Main stop mode (single external clock product)/ Substop mode (dual external clock product) TA = +25 °C	_	4.1	6.5	μΑ	In deep standby mode



 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ Vss} = 0.0 \text{ V}, \text{ T}_{A} = -40 \text{ °C to } +85 \text{ °C})$ 

Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks
i arameter	Syllibol	i iii iiaiiie	Condition	Min	Typ*1	Max*2	Oill	Remarks
Power supply current* <sup>5</sup>	ILVD		Current consumption for the low-voltage detection circuit	_	3.6	6.6	μА	
	Іскн		Current consumption for the main CR oscillator	_	220	280	μΑ	
	Icrl	<b>V</b> cc	Current consumption for the sub-CR oscillator oscillating at 100 kHz	_	5.1	9.3	μΑ	
	І́мѕтву		Current consumption difference between normal standby mode and deep standby mode T <sub>A</sub> = +25 °C		20	30	μΑ	

<sup>\*1:</sup> Vcc = 5.0 V. T<sub>A</sub> = + 25 °C

- \*5: The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (ILVD) to one of the value from Icc to Icch. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (ICRH, ICRL) and a specified value. In on-chip debug mode, the CR oscillator (ICRH) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
  - See "24.4 AC Characteristics: Clock Timing" for Fch and Fcl.
  - See "24.4 AC Characteristics: Source Clock / Machine Clock" for FMP and FMPL.

<sup>\*2:</sup> Vcc = 5.5 V, T<sub>A</sub> = +85 °C (unless otherwise specified)

<sup>\*3:</sup> P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

<sup>\*4:</sup> P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

<sup>\*6:</sup> In sub-CR clock mode, the power supply current value is the sum of adding Icrl to Iccls or Iccl. In addition, when the sub-CR clock mode is selected with FMPL being 50 kHz, the current consumption increases accordingly.



## 24.4 AC Characteristics

24.4.1 Clock Timing

 $(V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}, \text{Vss} = 0.0 \text{ V}, \text{T}_{A} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$ 

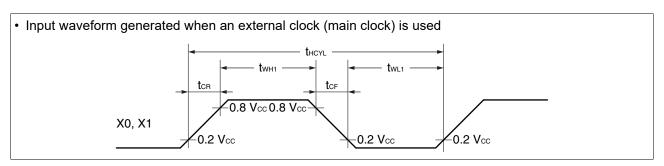
Danassatas	0	Dia	0           -		Value		1122	Dame - star
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Unit	Remarks
	Fсн	X0, X1	_	1	_	16.25	MHz	When the main oscillation circuit is used
	FCH	X0	X1: open	1		12		When the main external clock
		X0, X1	*	1	_	32.5	MHz	is used
				3.92	4	4.08	MHz	Operating conditions  • The main CR clock is used.  • 0 °C ≤ T <sub>A</sub> ≤ +70 °C
	Fcrh	_	_	3.8	4	4.2	MHz	Operating conditions  • The main CR clock is used.  • -40 °C ≤ T <sub>A</sub> < 0 °C,  +70 °C < T <sub>A</sub> ≤ +85 °C
				7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T <sub>A</sub> ≤ +70 °C
		_		7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • -40 °C ≤ T <sub>A</sub> < 0 °C, +70 °C < T <sub>A</sub> ≤ +85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • $0 \text{ °C} \le T_A \le +70 \text{ °C}$
Clock frequency				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • -40 °C ≤ T <sub>A</sub> < 0 °C, +70 °C < T <sub>A</sub> ≤ +85 °C
	FMCRPLL			11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T <sub>A</sub> ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • −40 °C ≤ T <sub>A</sub> < 0 °C, +70 °C < T <sub>A</sub> ≤ +85 °C
				15.68	16	16.32	MHz	Operating conditions  • PLL multiplication rate: 4  • 0 °C ≤ T <sub>A</sub> ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • −40 °C ≤ T <sub>A</sub> < 0 °C, +70 °C < T <sub>A</sub> ≤ +85 °C
	_			_	32.768	_	kHz	When the suboscillation circuit is used
	FcL	X0A, X1A	_	<u> </u>	32.768	_	kHz	When the sub-external clock is used
	FCRL	_	_	50	100	150	kHz	When the sub-CR clock is used

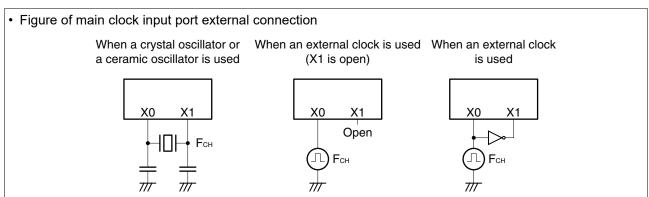


 $(V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}, \text{ Vss} = 0.0 \text{ V}, \text{ TA} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$ 

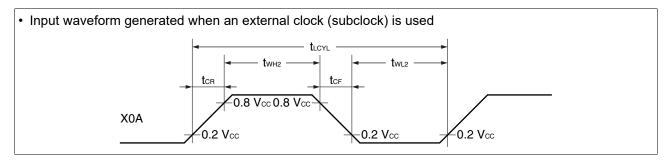
Parameter	Symbol	Din namo	Condition		Value		Unit	Remarks
Faranietei	Syllibol	Fill Haille	Condition	Min	Тур	Max	Oilit	Remarks
		X0, X1	_	61.5	_	1000	ns	When the main oscillation circuit is used
Clock cycle time	<b>t</b> HCYL	X0	X1: open	83.4	_	1000	ns	When an external clock is
ume		X0, X1	*	30.8	_	1000	ns	used
	<b>t</b> LCYL	X0A, X1A	_	_	30.5	_	μs	When the subclock is used
	tw <sub>H1</sub> ,	X0	X1: open	33.4			ns	NA/hara ara arata wa ali alia alicia
Input clock	twL1	X0, X1	*	12.4	_	_	ns	When an external clock is used, the duty ratio should
pulse width	tw <sub>H2</sub> ,	X0A	_	_	15.2	_	μs	range between 40% and 60%.
Input clock	ton	X0, X0A	X1: open	_	_	5	ns	When an external clock is
rising time and falling time	tcr, tcf	X0, X1, X0A, X1A	*	_	_	5	ns	used
CR oscillation	<b>t</b> crhwk	_	_	_	_	50	μs	When the main CR clock is used
start time	tcrlwk	_	_	_		30	μs	When the sub-CR clock is used

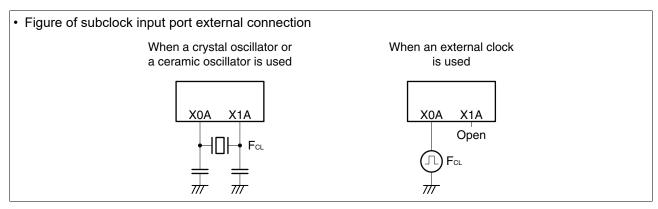
\*: The external clock signal is input to X0 and the inverted external clock signal to X1.













#### 24.4.2 Source Clock / Machine Clock

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ Vss} = 0.0 \text{ V}, \text{ T}_{A} = -40 \text{ °C to } +85 \text{ °C})$ 

Downwater	Cumbal	Pin		Value		Unit	Domonico
Parameter	Symbol	name	Min	Тур	Max	Unit	Remarks
							When the main external clock is used
			61.5	_	2000	ns	Min: Fcн = 32.5 MHz, divided by 2
							Max: Fcн = 1 MHz, divided by 2
							When the main CR clock is used
Source clock	<b>t</b> sclk		62.5	_	1000	ns	Min: Fcrh = 4 MHz, multiplied by 4
cycle time*1	LOCER						Max: Fcrh = 4 MHz, divided by 4
				61		μs	When the suboscillation clock is used
				01		μδ	Fcl = 32.768 kHz, divided by 2
			_	20		μs	When the sub-CR clock is used
				20			F <sub>CRL</sub> = 100 kHz, divided by 2
	Fsp		0.5	_	16.25	MHz	When the main oscillation clock is used
Source clock	1 01			4	_	MHz	
frequency				16.384	_	kHz	When the suboscillation clock is used
n oquonoy	FSPL			50	_	kHz	When the sub-CR clock is used
							FCRL = 100 kHz, divided by 2
							When the main oscillation clock is used
			61.5	_	32000	ns	Min: $F_{SP}$ = 16.25 MHz, no division
							Max: F <sub>SP</sub> = 0.5 MHz, divided by 16
Machine clock							When the main CR clock is used
cycle time*2			250	_	1000	ns	Min: F <sub>SP</sub> = 4 MHz, no division
(minimum	<b>t</b> MCLK						Max: F <sub>SP</sub> = 4 MHz, divided by 4
instruction	LIVIOLIX						When the suboscillation clock is used
execution			61	_	976.5	μs	Min: F <sub>SPL</sub> = 16.384 kHz, no division
time)							Max: F <sub>SPL</sub> = 16.384 kHz, divided by 16
							When the sub-CR clock is used
			20	_	320	μs	Min: F <sub>SPL</sub> = 50 kHz, no division
							Max: F <sub>SPL</sub> = 50 kHz, divided by 16
	FMP		0.031	_	16.25	MHz	
Machine clock	1 IVIF		0.25	_	16	MHz	
frequency		] —	1.024	_	16.384	kHz	When the suboscillation clock is used
nequency	FMPL		3.125		50	kHz	When the sub-CR clock is used
			0.120		- 50	10112	Fcrl = 100 kHz

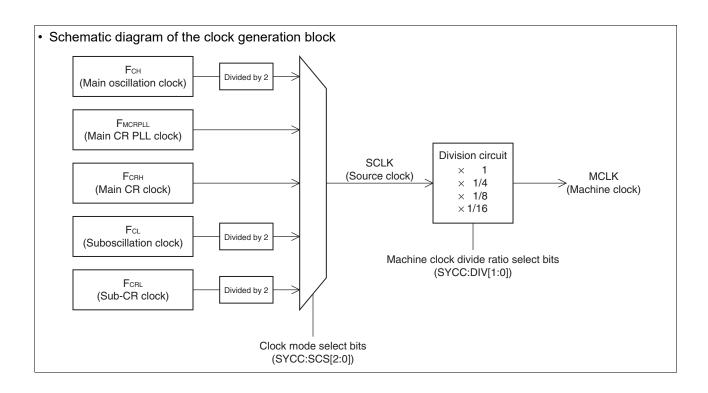
<sup>\*1:</sup> This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- · Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

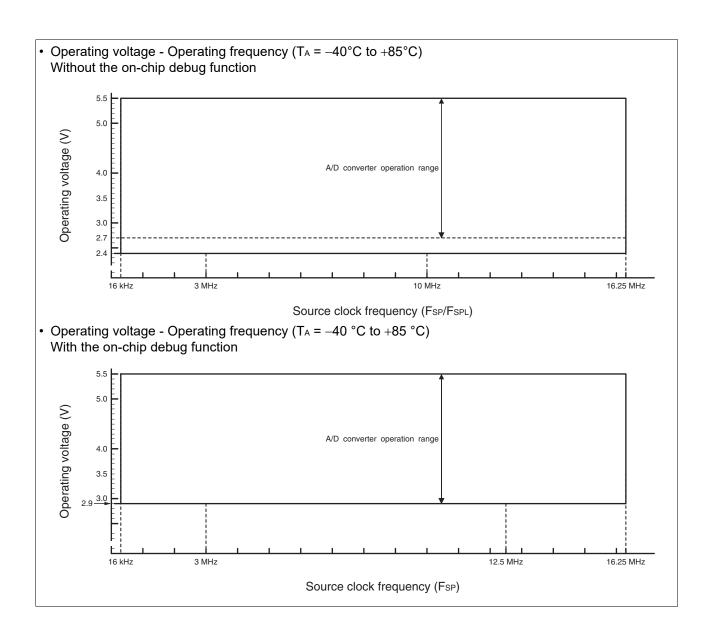
- · Source clock (no division)
- · Source clock divided by 4
- · Source clock divided by 8
- · Source clock divided by 16

<sup>\*2:</sup> This is the operating clock of the microcontroller. A machine clock can be selected from the following.









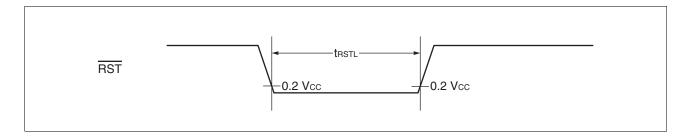


### 24.4.3 External Reset

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ Vss} = 0.0 \text{ V}, \text{ T}_{A} = -40 \text{ °C to } +85 \text{ °C})$ 

Parameter	Svmbol	Value		Unit	Remarks	
rarameter	Syllibol	Min	Max		Kemarks	
RST "L" level pulse width	<b>t</b> RSTL	2 tmcLK*1	1	ns	In normal operation	

<sup>\*1:</sup> See "Source Clock / Machine Clock" for tmclk.

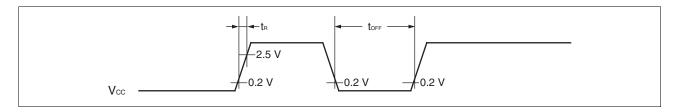




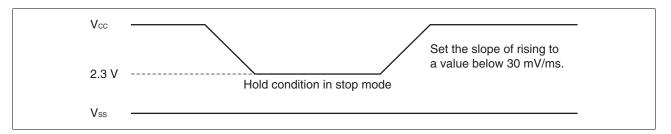
#### 24.4.4 Power-on Reset

 $(V_{SS} = 0.0 \text{ V}, T_A = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$ 

Parameter	Parameter Symbol Condition		Val	lue	Unit	Remarks	
Faranietei			Min	Max	Ullit		
Power supply rising time	<b>t</b> R	_	_	50	ms		
Power supply cutoff time	<b>t</b> off		1		ms	Wait time until power-on	



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

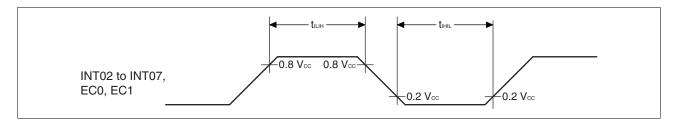


#### 24.4.5 Peripheral Input Timing

 $(Vcc = 5.0 V \pm 10\%, Vss = 0.0 V, T_A = -40 °C to +85 °C)$ 

Parameter	Symbol	Pin name	Va	Unit	
r ai ailletei	Syllibol	r III IIaille	Min	Max	Ollit
Peripheral input "H" pulse width	tılıн	INT02 to INT07*1,*2, EC0*1, EC1*3	2 tmclk*4	_	ns
Peripheral input "L" pulse width	tıHIL	11N 102 to 11N 107 % -, ECO -, ECT -	2 tmclk*4	_	ns

- \*1: INT04, INT06 and EC0 are available on all products.
- \*2: INT02, INT03, INT05 and INT07 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.
- \*3: EC1 is only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.
- \*4: See "Source Clock / Machine Clock" for tmclk.





24.4.6 LIN-UART Timing (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)

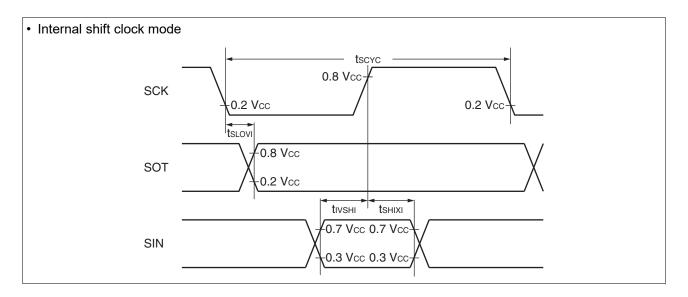
Sampling is executed at the rising edge of the sampling  $clock^{*1}$ , and serial clock delay is disabled  $clock^{*2}$ . (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{AV}_{SS} = \text{V}_{SS} = 0.0 \text{ V}, \text{T}_{A} = -40 \text{ °C to } +85 \text{ °C})$ 

Parameter	Symbol	Pin name	Condition	Va	Unit	
i arameter	Symbol	i ili ilalile	Condition	Min	Max	Oill
Serial clock cycle time	<b>t</b> scyc	SCK		<b>5 t</b> мськ* <sup>3</sup>	_	ns
SCK ↓→ SOT delay time	<b>t</b> sLOVI	SCK, SOT	Internal clock operation output pin:	-50	+50	ns
Valid SIN $\rightarrow$ SCK $↑$	<b>t</b> ıvshı	SCK, SIN	C <sub>L</sub> = 80 pF + 1 TTL	tmcLK*3 + 80	_	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	<b>t</b> shixi	SCK, SIN	•	0	_	ns
Serial clock "L" pulse width	<b>t</b> slsh	SCK		3 tмськ*3 — tR	_	ns
Serial clock "H" pulse width	<b>t</b> shsl	SCK		tмськ*3 + 10	_	ns
SCK ↓→ SOT delay time	<b>t</b> slove	SCK, SOT	External clock	_	2 tmcLK*3 + 60	ns
Valid SIN → SCK ↑	tivshe	SCK, SIN	operation output pin:	30	_	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	<b>t</b> shixe	SCK, SIN	C∟ = 80 pF + 1 TTL	tмськ*3 + 30	_	ns
SCK fall time	t⊧	SCK		_	10	ns
SCK rise time	<b>t</b> R	SCK		_	10	ns

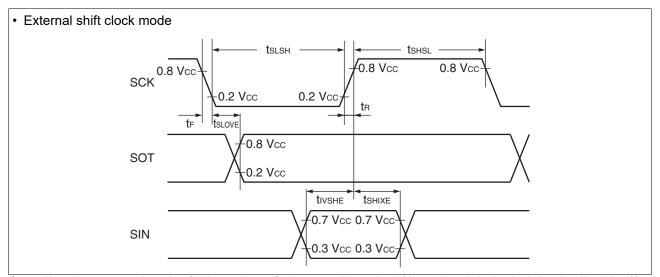
<sup>\*1:</sup> There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*3: See "Source Clock / Machine Clock" for tmclk.



<sup>\*2:</sup> The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.





Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is disabled\*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ Vss} = 0.0 \text{ V}, \text{ T}_{A} = -40 \text{ °C to } +85 \text{ °C})$ 

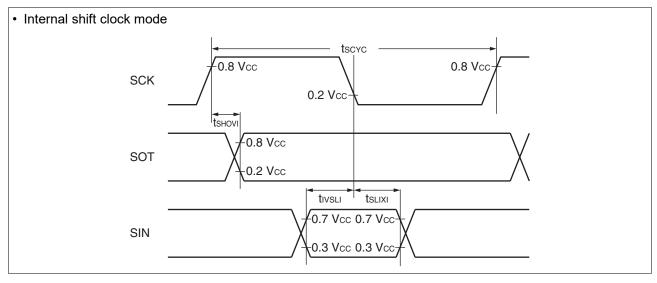
Doromotor	Symbol	Din nama	Condition	Va	Unit		
Parameter	Symbol Pin name		Condition	Min	Max	Oilit	
Serial clock cycle time	<b>t</b> scyc	SCK		5 tmclk*3	_	ns	
SCK ↑→ SOT delay time	<b>t</b> shovi	SCK, SOT	Internal clock operation output pin:	-50	+50	ns	
Valid SIN → SCK $\downarrow$	tıvslı	SCK, SIN	C <sub>L</sub> = 80 pF + 1 TTL	tмськ*3 + 80	_	ns	
SCK $\downarrow \rightarrow$ valid SIN hold time	<b>t</b> slixi	SCK, SIN	'	0	_	ns	
Serial clock "H" pulse width	<b>t</b> shsl	SCK		3 tмськ*3 — tR	_	ns	
Serial clock "L" pulse width	<b>t</b> slsh	SCK		tмськ*3 + 10	_	ns	
SCK ↑→ SOT delay time	<b>t</b> shove	SCK, SOT	External clock	_	2 tмськ*3 + 60	ns	
Valid SIN → SCK $\downarrow$	tivsle	SCK, SIN	operation output pin:	30	_	ns	
SCK $\downarrow \rightarrow$ valid SIN hold time	<b>t</b> slixe	SCK, SIN	C <sub>L</sub> = 80 pF + 1 TTL	tмськ*3 + 30	_	ns	
SCK fall time	t⊧	SCK		_	10	ns	
SCK rise time	<b>t</b> R	SCK		_	10	ns	

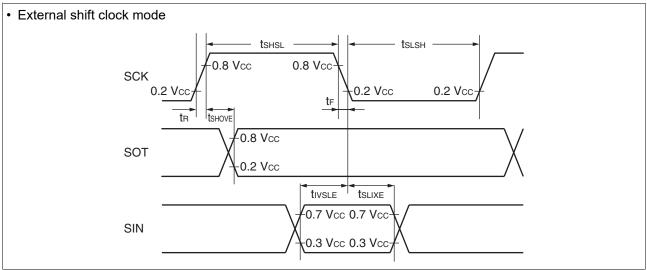
<sup>\*1:</sup> There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

<sup>\*2:</sup> The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

<sup>\*3:</sup> See "Source Clock / Machine Clock" for tmclk.





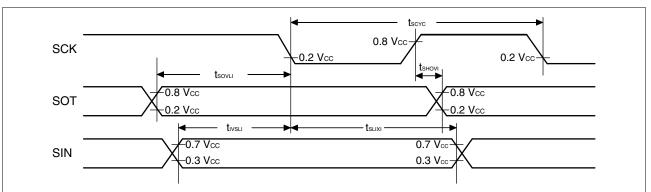




Sampling is executed at the rising edge of the sampling clock\*1, and serial clock delay is enabled\*2. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

Parameter	Symbol Pin name		Condition	Va	Unit		
Faranietei	Syllibol	Fill Hallie	Condition	Min	Max	Oilit	
Serial clock cycle time	<b>t</b> scyc	SCK		5 tmclk*3	_	ns	
SCK ↑→ SOT delay time	<b>t</b> shovi	SCK, SOT	Internal clock	-50	+50	ns	
Valid SIN → SCK $\downarrow$	tıvslı	SCK, SIN	operation output pin:	tмськ*3 + 80	_	ns	
$SCK \downarrow \rightarrow valid SIN hold time$	<b>t</b> slixi	SCK, SIN	C∟ = 80 pF + 1 TTL	0	_	ns	
$SOT  o SCK \downarrow delay time$	tsovli	SCK, SOT		3 tмськ*3 – 70	_	ns	

- \*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.
- \*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.
- \*3: See "Source Clock / Machine Clock" for tmclk.



Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is enabled\*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

$$(V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ Vss} = 0.0 \text{ V}, \text{ T}_{A} = -40 \text{ °C to } +85 \text{ °C})$$

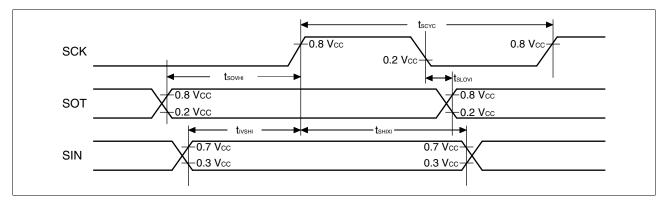
						_	
Parameter	Symbol	Pin name	Condition	Val	Unit		
raiametei	Symbol	Fili lialile	Condition	Min	Max	Oilit	
Serial clock cycle time	<b>t</b> scyc	SCK		<b>5 t</b> мськ*³	_	ns	
SCK ↓→ SOT delay time	<b>t</b> slovi	SCK, SOT	Internal clock	-50	+50	ns	
Valid SIN $\rightarrow$ SCK $↑$	<b>t</b> ıvshı	SCK, SIN	operating output pin:	tмськ*3 + 80	_	ns	
SCK ↑→ valid SIN hold time	<b>t</b> shixi	SCK, SIN	C∟ = 80 pF + 1 TTL	0	_	ns	
SOT → SCK ↑ delay time	tsovні	SCK, SOT		3 tmclk*3 - 70	_	ns	

<sup>\*1:</sup> There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

<sup>\*2:</sup> The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

<sup>\*3:</sup> See "Source Clock / Machine Clock" for tmclk.





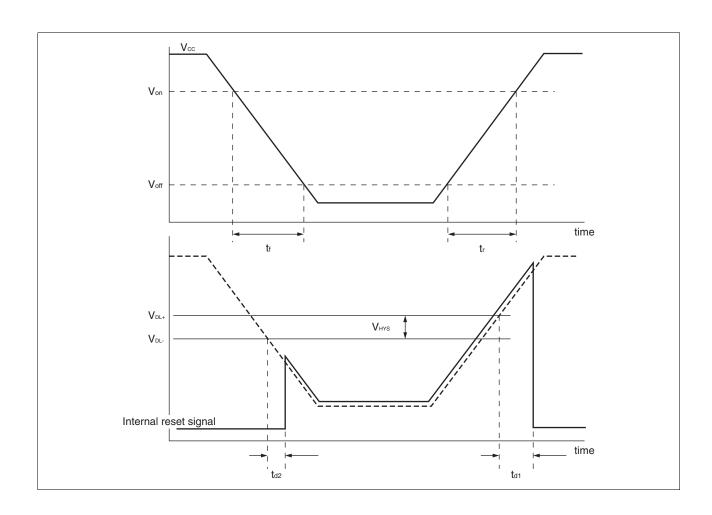
24.4.7 Low-voltage Detection

 $(V_{SS} = 0.0 \text{ V}, T_A = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$ 

_ ,			Value			
Parameter	Symbol	Min	Тур	Max	Unit	Remarks
		2.52	2.7	2.88		
Pologgo voltago*	$V_{DL+}$	2.61	2.8	2.99	V	At newer cumply rice
Release voltage*	V DL+	2.89	3.1	3.31	] V	At power supply rise
		3.08	3.3	3.52		
		2.43	2.6	2.77		
Detection voltage*	.,	2.52	2.7	2.88	V	At nower cumply fall
Detection voltage	$V_{DL-}$	2.80	3	3.20	]	At power supply fall
		2.99	3.2	3.41		
Hysteresis width	V <sub>HYS</sub>	_	100		mV	
Power supply start voltage	Voff	_	_	2.3	V	
Power supply end voltage	Von	4.9	_		V	
Power supply voltage change time (at power supply rise)	<b>t</b> r	650		_	μs	Slope of power supply that the reset release signal generates within the rating (VDL+)
Power supply voltage change time (at power supply fall)	tr	650	_	_	μs	Slope of power supply that the reset detection signal generates within the rating (V <sub>DL</sub> -)
Reset release delay time	<b>t</b> d1	_	_	30	μs	
Reset detection delay time	<b>t</b> d2	_	_	30	μs	
LVD threshold voltage transition stabilization time	<b>t</b> stb	10		_	μs	

<sup>\*:</sup> The release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDR register, refer to "CHAPTER 18 LOW-VOLTAGE DETECTION RESET CIRCUIT" in "New 8FX MB95560H/570H/580H Hardware Manual".







### 24.5 A/D Converter

### 24.5.1 A/D Converter Electrical Characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0.0 V,  $T_A = -40 \, ^{\circ}\text{C}$  to +85  $^{\circ}\text{C}$ )

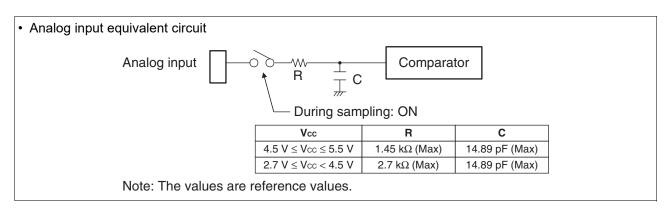
Parameter	Symbol	Value				Remarks	
Parameter	Symbol	Min Typ		Max	Unit	Remarks	
Resolution		_	_	10	bit		
Total error		-3	—	+3	LSB		
Linearity error	—	-2.5	_	+2.5	LSB		
Differential linearity error		-1.9	_	+1.9	LSB		
Zero transition voltage	Vот	Vss – 1.5 LSB	Vss + 0.5 LSB	Vss + 2.5 LSB	٧		
Full-scale transition voltage	V <sub>FST</sub>	Vcc – 4.5 LSB	Vcc – 2 LSB	Vcc + 0.5 LSB	٧		
Compare time	_	1	_	10	μs	4.5 V ≤ Vcc ≤ 5.5 V	
		3	_	10	μs	2.7 V ≤ Vcc < 4.5 V	
Sampling time	_	0.6	_	∞	μs	$2.7~V \le V_{CC} \le 5.5~V,$ with external impedance < $3.3~k\Omega$	
Analog input current	Iain	-0.3	_	+0.3	μΑ		
Analog input voltage	Vain	Vss	—	Vcc	V		

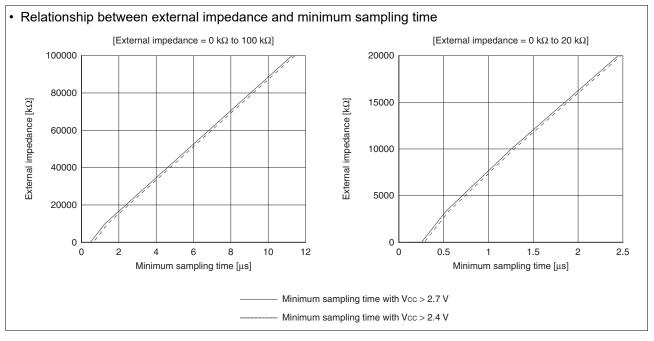


#### 24.5.2 Notes on Using A/D Converter

· External impedance of analog input and its sampling time

The A/D converter of the MB95560H/570H/580H has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1  $\mu$ F to the analog input pin.





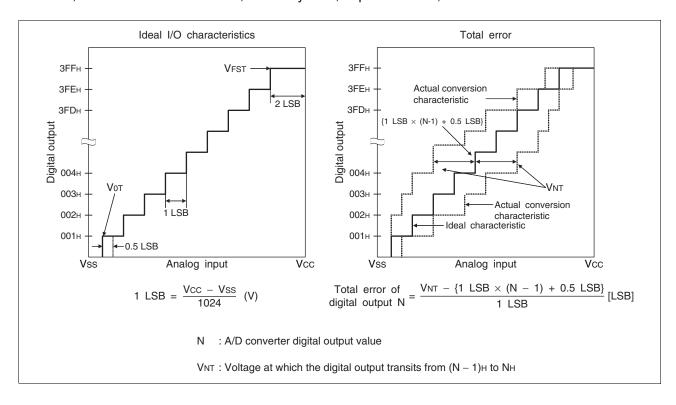
#### • A/D conversion error

As |Vcc - Vss| decreases, the A/D conversion error increases proportionately.

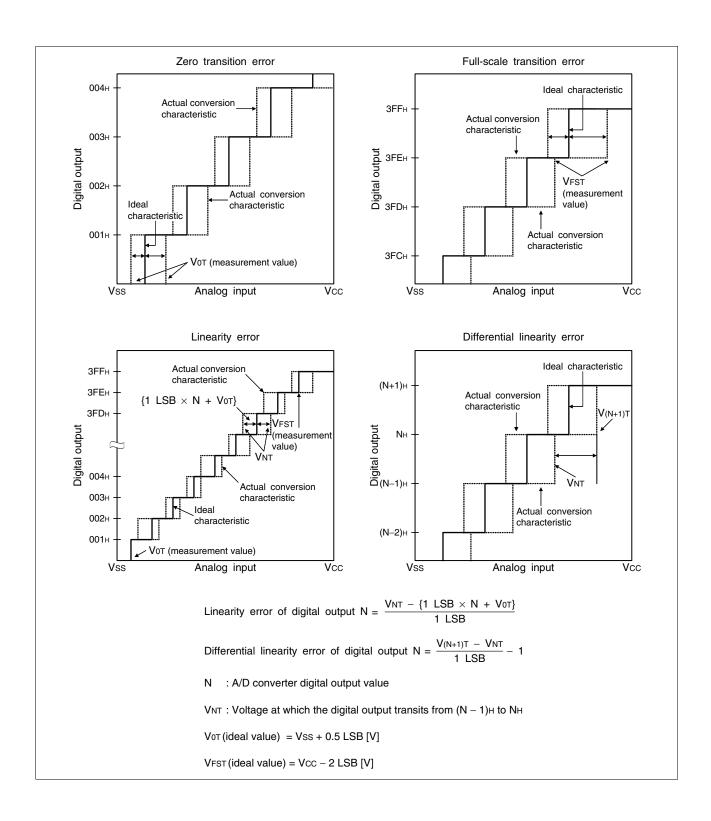


#### 24.5.3 Definitions of A/D Converter Terms

- Resolution
  - It indicates the level of analog variation that can be distinguished by the A/D converter. When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .
- · Linearity error (unit: LSB)
  - It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("000000000"  $\leftarrow \rightarrow$  "0000000001") of a device to the full-scale transition point ("1111111111") of the same device.
- Differential linear error (unit: LSB)
  - It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  - It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.









24.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks	
Parameter	Min	Тур	Max	Unit	Remarks	
Sector erase time (2 Kbyte sector)	_	0.3*1	1.6*2	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.	
Sector erase time (16 Kbyte sector)	_	0.6*1	3.1*2	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.	
Byte writing time	_	17	272	μs	System-level overhead is excluded.	
Program/erase cycle	100000	_	_	cycle		
Power supply voltage at program/erase	2.4	_	5.5	V		
Flash memory data retention time	5*³	_		year	Average T <sub>A</sub> = +85 °C	

<sup>\*1:</sup>  $V_{CC} = 5.5 \text{ V}$ ,  $T_A = +25 \text{ °C}$ , 0 cycle

<sup>\*2:</sup> Vcc = 2.4 V,  $T_A = +85 ^{\circ}\text{C}$ , 100000 cycles

<sup>\*3:</sup> This value was converted from the result of a technology reliability assessment. (The value was converted from the result of a high temperature accelerated test using the Arrhenius equation with an average temperature of +85 °C).

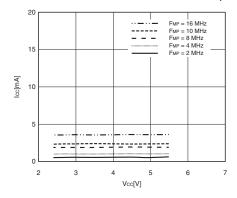


## 25. Sample Characteristics

· Power supply current temperature characteristics

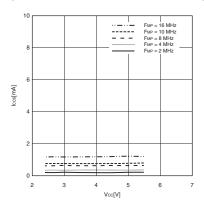
Icc - Vcc

 $T_A = +25$  °C,  $F_{MP} = 2, 4, 8, 10, 16$  MHz (divided by 2) Main clock mode with the external clock operating



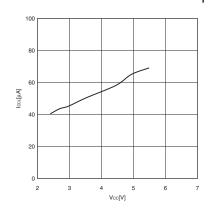
 $\mathsf{Iccs} - \mathsf{Vcc}$ 

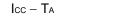
 $T_A = +25$  °C,  $F_{MP} = 2, 4, 8, 10, 16$  MHz (divided by 2) Main sleep mode with the external clock operating



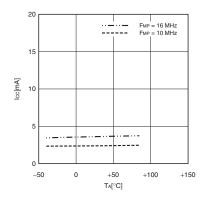
 $\mathsf{I}_\mathsf{CCL} - V_\mathsf{CC}$ 

 $T_A = +25$  °C,  $F_{MPL} = 16$  kHz (divided by 2) Subclock mode with the external clock operating



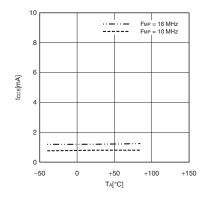


 $Vcc = 5.5 \text{ V}, F_{MP} = 10, 16 \text{ MHz}$  (divided by 2) Main clock mode with the external clock operating



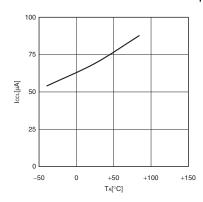
Iccs - Ta

 $V_{CC} = 5.5 \text{ V}, F_{MP} = 10, 16 \text{ MHz}$  (divided by 2) Main sleep mode with the external clock operating



Iccl - Ta

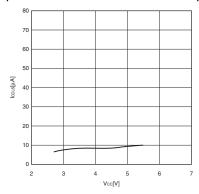
 $V_{CC} = 5.5 \text{ V}$ ,  $F_{MPL} = 16 \text{ kHz}$  (divided by 2) Subclock mode with the external clock operating





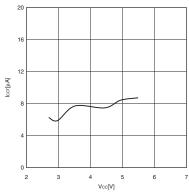


 $T_A = +25$  °C,  $F_{MPL} = 16$  kHz (divided by 2) Subsleep mode with the external clock operating



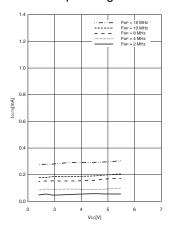
 $I_{\text{CCT}} - V_{\text{CC}}$ 

 $T_A = +25$  °C,  $F_{MPL} = 16$  kHz (divided by 2) Watch mode with the external clock operating



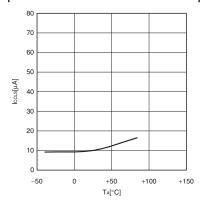
Iccтs – Vcc

 $T_A = +25$  °C,  $F_{MP} = 2, 4, 8, 10, 16$  MHz (divided by 2) Time-base timer mode with the external clock operating



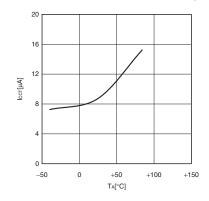
#### Iccls - Ta

 $V_{CC} = 5.5 \text{ V}, F_{MPL} = 16 \text{ kHz}$  (divided by 2) Subsleep mode with the external clock operating



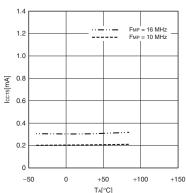
ICCT - TA

 $V_{CC} = 5.5 \text{ V}, F_{MPL} = 16 \text{ kHz (divided by 2)}$  Watch mode with the external clock operating

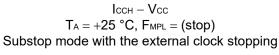


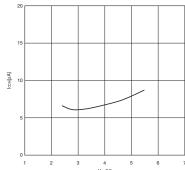
 $I_{\text{CCTS}} - T_{\text{A}}$ 

 $V_{\text{CC}} = 5.5 \text{ V}, \, F_{\text{MP}} = 10, \, 16 \, \text{MHz} \, (\text{divided by 2})$  Time-base timer mode with the external clock operating

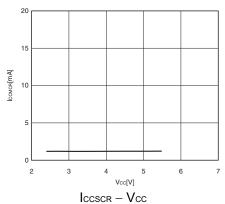




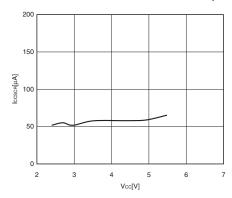


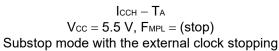


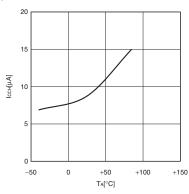
 $I_{\text{CCMCR}} - V_{\text{CC}}$   $T_{\text{A}} = +25~^{\circ}\text{C}, \; F_{\text{MP}} = 4~\text{MHz (no division)}$  Main clock mode with the main CR clock operating



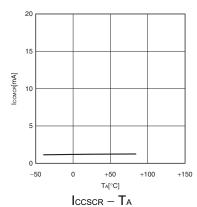
 $T_A = +25$  °C,  $F_{MPL} = 50$  kHz (divided by 2) Subclock mode with the sub-CR clock operating



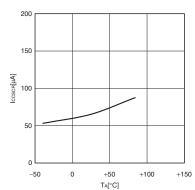




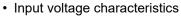
 $\label{eq:CC} I_{\text{CCMCR}} - T_{\text{A}}$   $V_{\text{CC}} = 5.5 \text{ V}, \text{ F}_{\text{MP}} = 4 \text{ MHz (no division)}$  Main clock mode with the main CR clock operating

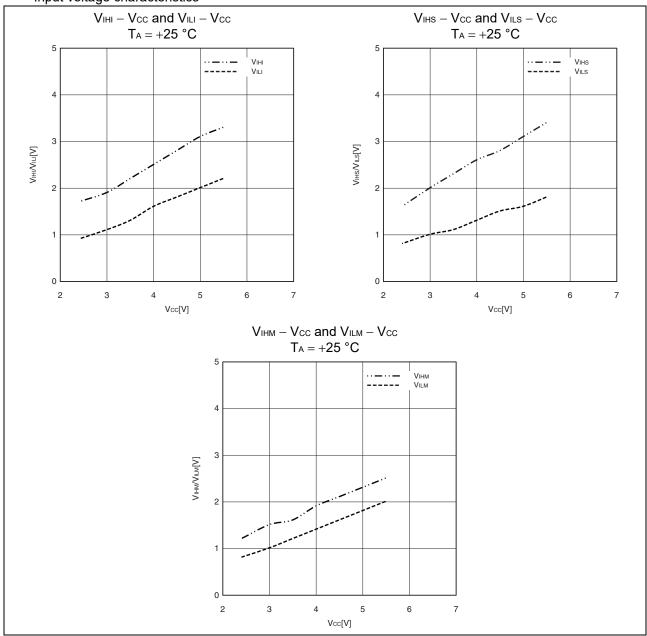


 $V_{\text{CC}} = 5.5 \text{ V}, \; F_{\text{MPL}} = 50 \text{ kHz} \; (\text{divided by 2})$  Subclock mode with the sub-CR clock operating

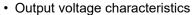


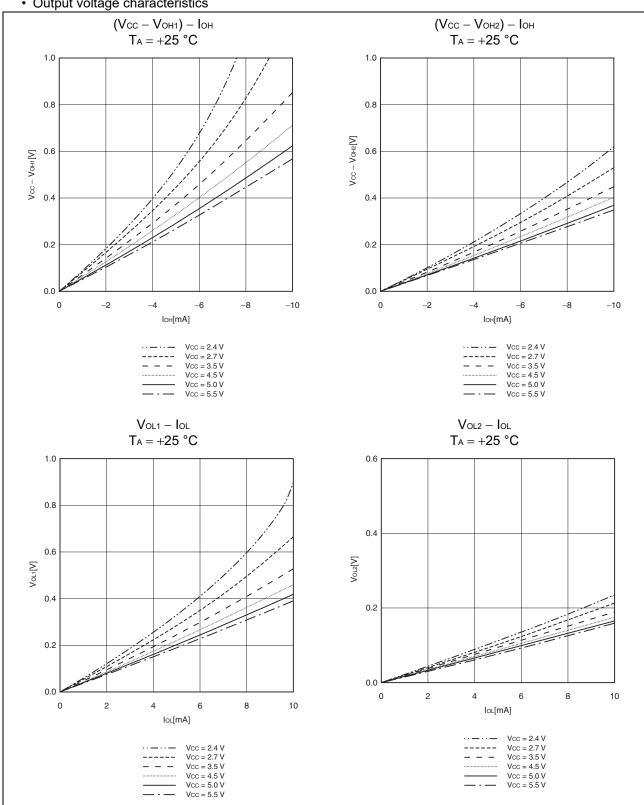




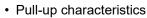


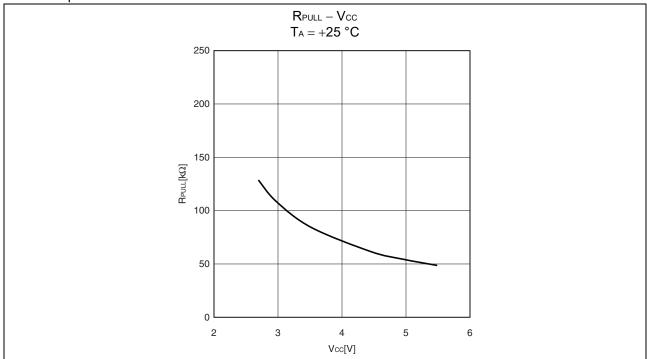














# 26. Mask Options

		MB95F562H	MB95F562K
	Part Number		
		MB95F563H	MB95F563K
		MB95F564H	MB95F564K
		MB95F572H	MB95F572K
l		MB95F573H	MB95F573K
No.		MB95F574H	MB95F574K
		MB95F582H	MB95F582K
		MB95F583H	MB95F583K
		MB95F584H	MB95F584K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input



# 27. Ordering Information

Part number	Package	Packing
MB95F562HWQN-G-SNE1 MB95F562KWQN-G-SNE1 MB95F563HWQN-G-SNE1 MB95F563KWQN-G-SNE1 MB95F564HWQN-G-SNE1 MB95F564KWQN-G-SNE1	32-pin plastic QFN	Tray
MB95F562HWQN-G-SNERE1 MB95F562KWQN-G-SNERE1 MB95F563HWQN-G-SNERE1 MB95F563KWQN-G-SNERE1 MB95F564HWQN-G-SNERE1 MB95F564KWQN-G-SNERE1	(WNP032)	Reel
MB95F562HPF-G-SNE2 MB95F562KPF-G-SNE2 MB95F563HPF-G-SNE2 MB95F563KPF-G-SNE2 MB95F564HPF-G-SNE2 MB95F564KPF-G-UNE2	20-pin plastic SOP (SOJ020)	Tube
MB95F562HPFT-G-SNE2 MB95F562KPFT-G-SNE2 MB95F563HPFT-G-SNE2 MB95F563KPFT-G-SNE2 MB95F564HPFT-G-SNE2 MB95F564KPFT-G-UNE2	20-pin plastic TSSOP (STG020)	Tube
MB95F562KPFT-G-UNERE2 MB95F563HPFT-G-UNERE2 MB95F563KPFT-G-UNERE2 MB95F564KPFT-G-UNERE2		Reel
MB95F582HWQN-G-SNE1 MB95F582KWQN-G-SNE1 MB95F583HWQN-G-SNE1 MB95F583KWQN-G-SNE1 MB95F584HWQN-G-SNE1 MB95F584KWQN-G-SNE1	32-pin plastic QFN	Tray
MB95F582HWQN-G-SNERE1 MB95F582KWQN-G-SNERE1 MB95F583HWQN-G-SNERE1 MB95F583KWQN-G-SNERE1 MB95F584HWQN-G-SNERE1 MB95F584KWQN-G-SNERE1	(WNP032)	Reel
MB95F582HPFT-G-SNE2 MB95F582KPFT-G-SNE2 MB95F583HPFT-G-SNE2 MB95F583KPFT-G-SNE2 MB95F584HPFT-G-SNE2 MB95F584KPFT-G-SNE2	16-pin plastic TSSOP (STB016)	Tube

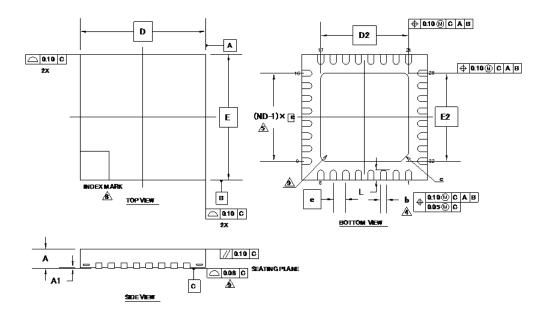


Part number	Package	Packing
MB95F582HPF-G-SNE2 MB95F582KPF-G-SNE2 MB95F583HPF-G-SNE2 MB95F583KPF-G-SNE2 MB95F584HPF-G-SNE2 MB95F584KPF-G-SNE2	16-pin plastic SOP (SO016)	Tube
MB95F572HPH-G-SNE2 MB95F572KPH-G-SNE2 MB95F573HPH-G-SNE2 MB95F573KPH-G-SNE2 MB95F574HPH-G-SNE2 MB95F574KPH-G-SNE2	8-pin plastic DIP (PDA008)	Tube
MB95F572HPF-G-SNE2 MB95F572KPF-G-SNE2 MB95F573HPF-G-SNE2 MB95F573KPF-G-SNE2 MB95F574HPF-G-SNE2 MB95F574KPF-G-SNE2	8-pin plastic SOP (SOD008)	Tube



## 28. Package Dimension

Package Type	Package Code	
QFN 32	WNP032	



SYMBOL	DIMENSIONS		
SIMDUL	MIN.	NOM.	MAX
А			0.80
A <sub>1</sub>	0.00		0.05
D	5.00 BSC		
E	5.00 BSC		
ь	0.18 0.25 0.30		
D2	3.50 BSC		
E2	3.50 BSC		
e	0.50 BSC		
C	0.30 REF		
L	0.35	0.40	0.45

#### NOTE

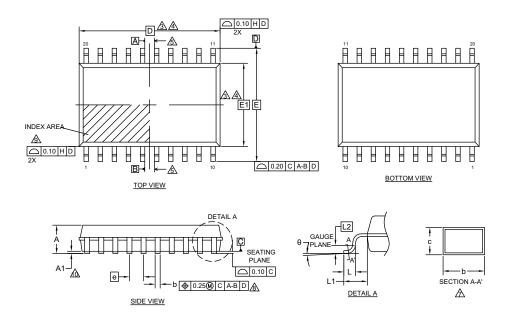
- ${\bf 1.\,ALL\,DIMENSIONS\,ARE\,IN\,\,MILLIMETERS}$
- 2. DIMENSIONING AND TOLERANGING CONFORMS TO ASMEY14.5-1994.
- 3. N IS THE TOTAL NUMBER OF TERM INALS.
- ADIMENSION "S" APPLIES TO METALLIZED TERMINAL AND IS MEASURED
  BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIPLIF THE TERMINAL HAS
  THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL THE
  DIMENSION "S" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- <u></u> **∆**ND REFER TO THE NUMBER OF TERMINALS ON DORESIDE.
- 6. MAX. PACKAGEWARPAGEIS 0.05mm.
- 7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
- **A**PIN #1 ID ON TOPWILL BE LOCATED WITHIN INDICATED ZONE.
- ⚠ BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG ASWELL AS THE TERMINALS.
- 10. JEDEC SPECIFICATION NO. REF: N/A

PÁCKÁSE ÓUTUNE, 32 LEÁD GEN SÚDSJÚDÍJSKI MIWNEÚZ 3,553,5M MIEPÁD(SÁMNÍ) FIEVSK

002-15160 \*\*



Package Type	Package Code	
SOP 20	SOJ020	



SYMBOL	DIMENSIONS		
STWBOL	MIN.	NOM.	MAX.
Α	_	_	2.65
A1	0.05	_	0.20
D	12.70 BSC		
Е	10.20 BSC		
E1	7.50 BSC		
θ	0°		8°
С	0.22	_	0.32
b	0.35	0.40	0.49
L	0.50	0.80	1.27
L <sub>1</sub>	1.35 REF		
L 2	0.25 BSC		
е	1.27 BSC		

### NOTES

- 1. ALL DIMENSIONS ARE IN MILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ⚠ DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- ⚠THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

  DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST

  EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

  THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

  ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUMS A & B TO BE DETERMINED AT DATUM H.
- 6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- ★ THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

  \*\*THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

  \*\*THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

  \*\*THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

  \*\*THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

  \*\*THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm
  TO 0.25mm FROM THE LEAD TIP.

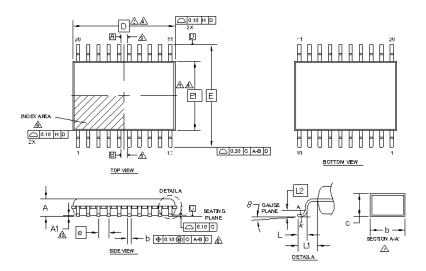
  \*\*THE DIMENSION APPLY TO THE LEAD TIP.

  \*
- ⚠ DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
- THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. JEDEC SPECIFICATION NO. REF: N/A

002-16348 \*\*



Package Type	Package Code	
TSSOP 20	STG020	



SYMBOL	DIMENSONS		
STWIEDL	MIN.	NOM.	MAX.
A	_		1.20
A1	0.05	_	0.15
D	6	5.50B9C	
E	6.40B90		
E 1	٠	4.40BSC	
6	0°	_	8*
c	0.10		0.19
ь	0.20	0.24	0.28
L	0.45	0.60	0.75
L 1		.00REF	
L 2	0.25 BSC		
e	0.65 BSC		

NOT	E8

- 1. ALL DIMENSIONS ARE IN MILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER, ASVE Y14.5M 1994.
- A DIMENSIONING DINCLUDE MOLD FLASH, DIMENSIONING B1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION, INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED ⊎.025 Intil PER SIDE, D and E1 DIVENSION ARE DETERMINED A1 DATUM IT.
- ⚠ THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

  DIMENSIONING DIANGET ARE DETERMINED AT THE OUTERMOST.

  EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

  THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

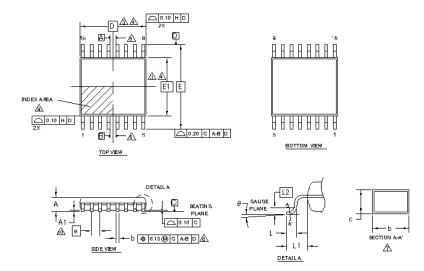
  ANY MISNATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- $\triangle$  DATUMS A \$ B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- $\triangle$  THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 min TO 0.25mm FROM THE LEAD TIP.
- À DIMENSION "IS DOES NOT INCLUDE THE DAMBAR PROTRUSION, ALLOW/BLE DAVBAR PROTRUSION STIALL BE 0.10mm FOTAL IN EXCESS OF THE "S" DIMENSION AT MAXIMAL MATERIAL CONDITION, THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF "HE FOOT.
- ATHIS CHAMFER FEATURE IS OPTIONAL, LETITIS NOT PRESENT, THEN A PIN 1 IDENTIFIER MILIST BE LOCATED WITHIN THE INDEX AREA INDICATED
- A 1'A' IS DEFINED AS INTO VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. EDEOSPECIFICATON NO. REF: N/A

PÁCKÁGE OUTLINE, 20 LEÁD TSSOP 8.50x8.40x1.20 mm STG020 FEV®

002-15916 \*\*



Package Type	Package Code
TSSOP 16	STB016



SYMBOL	DIMENSONS		
3 IM LEDE	MIN.	NOM.	MAX.
A	_	_	120
A1	0.05	_	0.15
D	4	4.96 BSC	
E	6.40B9C		
E 1	4.40B9C		
6	0°	_	8°
c	0.10	_	0.19
ь	0.16 0.24 0.32		0.32
L	0.45 0.60 0.75		0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

1. ALL DIMENSIONS ARE INMILLIMETER.

- 2. DIMENSIONING AND TOLERANCING PER, ASVE Y14.5M 1994.
- ⚠ DIMENSIONING DINCLUDE MOLD FLASH, DIMENSIONING BIDGES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION, INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 Imm PER SIDE, D and E1 DIVENSION ARE DETERMINED AT DATUM IT.
- A THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

  DIMENSIONING DIAGRET ARE DEFERMINED AT THE OUTERMOST
  EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,
  THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING
  ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ADATUMS A & B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- $\triangle$  THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN  $0.49~\mathrm{min}$  TO 0.25mm FROM THE LEAD TIP.
- TO 0.25mm FROM THE LEAD TIP.

  ADMENSION "5" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOW/ISLE DAVBAR PROTRUSION SITALL BE 0.15mm TOTAL IN EXCESS OF THE "5" DIMENSION AT MAXIMUM MATERIAL CONDITION.

  THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ⚠ THIS CHAMFER FEATURE IS OPTIONAL, LE IT IS NOT PRESENT. THEN A PIN 1 A IDENTIFIER MILET BE LOCATED WITH NITHE INDEX AREA INDICATED
- AL 18 DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.

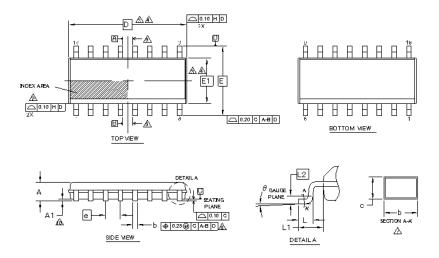
11. JEDEOSPECIFICATION NO. REF: N/A

PÁCKÁGE OUTLINE, 16 LEÁD TSSÓP 4.96X8.40X1.20 MM STEO16 FEV®

002-15914 \*\*



Package Type	Package Code	
SOP 16	SO016	



SYMBOL	DIMENSONS		
STWIEDE	MIN.	NOM.	MAX.
A	_	_	175
A1	0.10 —		025
D	,	9.96 BSC	
E	6.00BSC		
E 1	3.90B9C		
8	0°	_	8°
С	0.13	_	0.20
ь	0.36	0.40	0.51
L	0.45	0.60	0.80
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 B9C		

#### NOTES

- 1. ALL DIMENSIONS ARE NIMILLIMETER.
- 2. DIMENSIONING AND TOLERANCING PER, ASVE Y14.5M 1994.
- Å DIMENSIONING DI INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION, INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE, D and E1 DIVENSION ARE DETERMINED A1 DATUM II.
- ⚠ THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

  DIMENSIONING ID and ET ARE DETERMINED AT THE OUTERMOST

  EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH,

  THE BAR BURRS, GATTE BURRS AND INTERLEAD FLASH, BUT INCLUDING

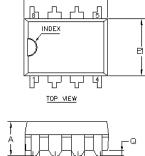
  ANY MISNATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ΔDATUMS A & B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- $\bigwedge$  THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10  $\min$  TO 0.25mm FROM THE LEAD TIP.
- ⚠ DIMENSION "5" DOES NOT INCLUDE THE DAMBAR PROTRUSION, ALLOWABLE UA YBAR PRO IRUSION SIIALL BE 0.10mm I DI IAL IN EXCESS OF ITTE "5" DIMENSION AT MAXIMALM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF "HE FOOT,
- ⚠THIS CHAVIFER FEATURE IS OPTIONAL. LETT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MIIST BE LOCATED WITHIN THE INDEX AREA INDICATED
- ALL 1S DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- 11. JEDEOSPECIFICATON NO. REF: N/A

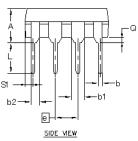
PACKAGE OUTLINE, 18 LEAD SOP 9.98X8.00X1.75 MM SO018 REVISE

002-15861 \*\*



Package Type	Package Code	
DIP 8	PDA008	







SYMBOL	DIMENSIONS		
SIMBOL	MIN.	MIN. NOM.	
A	_	_	4.36
L	3.00	_	_
D	9.10	9.40	9.80
E		7.62 TYP	
E1	6.10	6.35	6.60
6	_	_	15°
С	0.20	0.25	0.30
ь	0.38	0.46	0.54
b1	_	1.52	1.82
b2	_	0.99	1.29
e	2.54 TYP		
S1	0.59	0.89	1.24
Q	050	_	_

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.

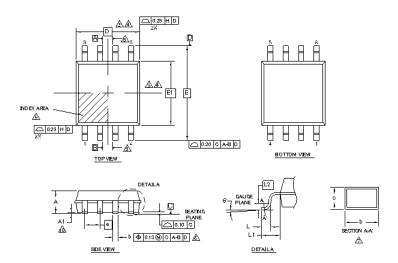
2. JED EC SPECIFICATION NO . REF : N/A

PACKAGE OUTLINE, 8 LEAD POIP 9.40X8.35X3.88 MM PDA008 REV®

002-16909 \*\*



Package Type	Package Code
SOP 8	SOD008



SYMBOL	DIMENSION		
3 IMEDE	MIN.	NOM.	MAX.
Α	_	_	2.10
A1	0.05	_	0.25
D		.24B90	
E	7.80BSC		
E1	5.30BSC		
6	0°	_	8°
С	0.15	_	0.25
ь	0.38	0.43	0.48
L	0.55	0.75	0.85
L 1	1.25 REF		
L 2	0.25 BSC		
e	1.27 BSC		

NK.	)T	Ξ	ŝ

- 1. ALL DIMENSIONS ARE IN MILLIMETER
- 2. DIMENSIONING AND TOLERANCING PER, ASME Y14.5M 1994.
- Å DIMENSIONING DINCLUDE VOLD FLASH, DIMENSIONING ET DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCECT 9.025 Incl PER SIDE. Dand ET DIMENSION ARE DETERMINED AT DIALUM II.
- ⚠ THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM.

  DIVENSIONING ID and ET ARE DETERMINED AT THE OUTERMOST

  EXTREMES OF THE FLASTIC BODY FXCLUSIVE OF MOLLOT ASH,

  THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING

  ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUVS A & B TO BE DETERMINED AT DATUM H. "N" 3 THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- $\triangle$  THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10  $_{\rm MIR}$  TO 0.25mm FROM THE LEAD TIP.
- À DIMENSION "b" DOES NOT INCLUDE THE DAVBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION STALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.

  THE DAMBAR MAY NOT BE LOCA"ED ON THE LOWER RADIUS OF THE FOOT.
- ÀTH 3 CHANFER FEATURE IS OPTIONAL. LE IT IS NOT PRESENT. THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- A: "AI" IS DEFINED AS THE VENTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE JID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS. 11.JEDEOSPECIFICATON NO. REF: N/A

PACKAGE OUTLINE, 8 LEAD SOP 5.24X7.80X2.10 N.M. SOD 008 REVISE

002-15858 \*\*



# 29. Major Changes In This Edition

Spansion Publication Number: DS702-00010

Page	Section	Details
		Changed the series name. MB95560H Series → MB95560H/570H/580H Series
_	_	Added information on the MB95570H Series.
		Added information on the MB95580H Series.
27	■ PIN CONNECTION • DBG pin	Revised details of "• DBG pin".
	• RST pin	Revised details of "• RST pin".
28	• C pin	Corrected the following statement. The decoupling capacitor for the Vcc pin must have a capacitance larger than Cs.  → The decoupling capacitor for the Vcc pin must have a capacitance equal to or larger than the capacitance of Cs.
39	■ I/O MAP (MB95570H Series)	Corrected the R/W attribute of the CMDR register. $R/W \rightarrow R$
		Corrected the R/W attribute of the WDTH register. $R/W \rightarrow R$
		Corrected the R/W attribute of the WDTL register. $R/W \rightarrow R$
42	■ I/O MAP (MB95580H Series)	Corrected the R/W attribute of the CMDR register. $R/W \rightarrow R$
		Corrected the R/W attribute of the WDTH register. $R/W \rightarrow R$
		Corrected the R/W attribute of the WDTL register. $R/W \rightarrow R$
46	■ ELECTRICAL CHARACTERISTICS  1. Absolute Maximum Ratings	Corrected the rating of the parameter "'L" level total maximum output current". $48 \rightarrow 100$
		Corrected the rating of the parameter "'H" level total maximum output current". $48 \rightarrow -100$



Page	Section	Details
48	2. Recommended Operating Conditions	Revised note *2.  The value is 2.88 V when the low-voltage detection reset is used.  The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used.
		Corrected the following statement in note *3.  The decoupling capacitor for the Vcc pin must have a capacitance larger than Cs.  →  The decoupling capacitor for the Vcc pin must have a capacitance equal to or larger than the capacitance of Cs.
		Revised the remark in "• DBG/RST/C pins connection diagram".
49	3. DC Characteristics	Revised the remark of the parameter "Input leak current (Hi-Z output leak current)".  When pull-up resistance is disabled  When the internal pull-up resistor is disabled
		Renamed the parameter "Pull-up resistance" to "Internal pull-up resistor".
		Revised the remark of the parameter "Internal pull-up resistor".  When pull-up resistance is enabled  →  When the internal pull-up resistor is enabled
53	AC Characteristics     (1) Clock Timing	Corrected the pin names of the parameter "Input clock rising time and falling time". $X0 \rightarrow X0$ , $X0A$ $X0$ , $X1$ $\rightarrow X0$ , $X1$ , $X0A$ , $X1A$



# • Major changes from third edition to fourth edition

Page	Section	Details
23 to 26	■ HANDLING PRECAUTIONS	New section
35	■ I/O MAP (MB95560H Series)	Corrected the R/W attribute of the CMDR register. $R/W \rightarrow R$
52	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Corrected the operating conditions of FCRH of the parameter "Clock frequency". $0 \text{ °C} \leq T_A < +70 \text{ °C} \rightarrow 0 \text{ °C} \leq T_A \leq +70 \text{ °C} \rightarrow 0 \text{ °C} \leq T_A \leq +85 \text{ °C} \rightarrow +70 \text{ °C} \leq T_A \leq +85 \text{ °C}$ Corrected the operating conditions of FMCRPLL of the parameter "Clock frequency". $0 \text{ °C} \leq T_A < +70 \text{ °C} \rightarrow 0 \text{ °C} \leq T_A \leq +70 \text{ °C} \rightarrow 0 \text{ °C} \leq T_A \leq +85 \text{ °C} \rightarrow +70 \text{ °C} \leq T_A \leq +85 \text{ °C} \rightarrow +70 \text{ °C} \leq T_A \leq +85 \text{ °C}$
68	A/D Converter     A/D Converter Electrical     Characteristics	Corrected the symbol of the parameter "Zero transition voltage". $Vo\tau \to Vo\tau$
69	<ul><li>5. A/D Converter</li><li>(2) Notes on Using A/D Converter</li><li>Analog input equivalent circuit</li></ul>	Corrected the range of Vcc. 2.7 V $\leq$ Vcc $<$ 5.5 V $\rightarrow$ 2.7 V $\leq$ Vcc $<$ 4.5 V Corrected the values of R. 3.3 k $\Omega \rightarrow$ 1.45 k $\Omega$ 5.7 k $\Omega \rightarrow$ 2.7 k $\Omega$
70, 71	A/D Converter     (3) Definitions of A/D Converter Terms	Corrected the symbol of the zero transition voltage. $V_{0T} \rightarrow V_{0T}$

NOTE: Please see "Document History" about later revised information.



# **Document History Page**

	Document Title: MB95560H Series/MB95570H Series/MB95580H Series, New 8FX 8-bit Microcontrollers Document Number: 002-04629			
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	05/27/2013	Migrated to Cypress and assigned document number 002-04629. No change to document contents or format.
*A	5193921	AKIH	03/29/2016	Updated 24.4.3 External Reset Added MB95F564KPF-G-UNE2, MB95F564KPFT-G-UNE2 in "Ordering Information". Updated to Cypress template.
*B	5420206	HTER	02/06/2017	Changed package code as the following in 1.Product Line-up (Page4, 6), 2.Packages And Corresponding Products (Page 7), 4.Pin Assignment (Page 9 to 10), 27.Ordering Information (Page 75 to 76) and 28.Package Dimensions (Page 77 to 83).  "LCC-32P-M19" to "WNP032"  "FPT-20P-M09" to "SOJ020"  "FPT-20P-M10" to "STG020"  "FPT-16P-M08" to "STB016"  "FPT-16P-M03" to "SO016"  "DIP-8P-M03" to "SO016"  "DIP-8P-M08" to "SOD008"  Added Part number "MB95F564KPFT-G-UNERE2, MB95F562KPFT-G-UNERE2, MB95F563KPFT-G-UNERE2" in 27.Ordering Information (Page 75).  Deleted Part number "MB95F564KPF-G-SNE2, MB95F564KPFT-G-SNE2" in 27.Ordering Information (Page 75).
*C	5761469	AESATP12	06/08/2017	Updated logo and copyright.
*D	5895915	HUAL	09/27/2017	Added Part number "MB95F563HPFT-G-UNERE2" and Packing information in 27.Ordering Information (Page 75).
*E	5972828	HUAL	11/21/2017	Updated Package Dimension: Updated Diagram corresponding to "SOP 20".



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