



## Frequency Generator & Integrated Buffers for PENTIUM/Pro™

### General Description

The ICS9148-36 generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

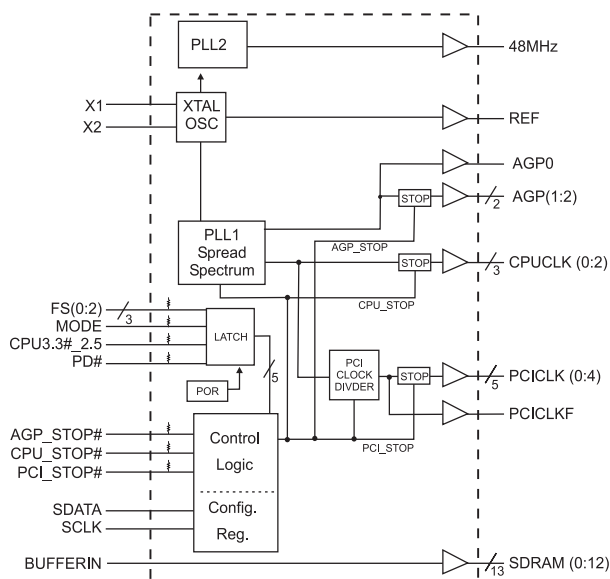
Spread spectrum may be enabled through I2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9148-36 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection. The SDRAM12 output may be used as a feed back into an off chip PLL.

### Features

- Generates the following system clocks:
  - 3 CPU(2.5V/3.3V) upto 100MHz.
  - 6 PCI(3.3V) @ 33.3MHz
  - 3 AGP(3.3V) @ 2x PCI
  - 13 SDRAMs(3.3V) up to 100MHz
  - 1 REF (3.3V) @ 14.318MHz
- Skew characteristics:
  - CPU – CPU ≤ 250ps
  - CPU(early) – PCI : 1-4ns, Center 2-6ns
  - AGP-PCI: 250ps
- Supports Spread Spectrum modulation & I<sup>2</sup>C programming for Power Management, Frequency Select
- Efficient Power management scheme through PCI and CPU STOPCLOCKs.
- Uses external 14.318MHz crystal
- 48 pin 300mil SSOP.

### Block Diagram



### Power Groups

VDD1 = REF (0:1), X1, X2

VDD2 = PCICLK\_F, PCICLK(0:5)

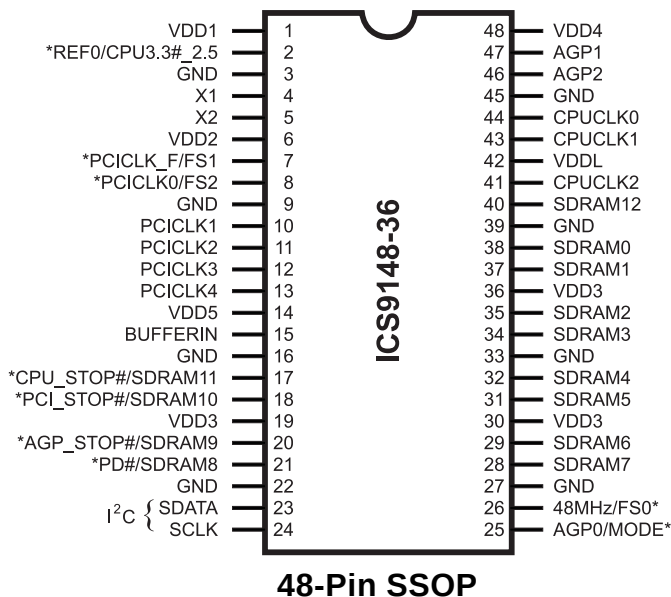
VDD3 = SDRAM (0:12), supply for PLL core

VDD4 = AGP (1:2)

VDD5 = Fixed PLL, 48MHz, AGP0

VDDL = CPUCLK (0:2)

### Pin Configuration



### 48-Pin SSOP

\* Internal Pull-up Resistor of  
240K to 3.3V on indicated inputs

Pentium is a trademark of Intel Corporation  
I<sup>2</sup>C is a trademark of Philips Corporation



## Pin Descriptions

| PIN NUMBER                      | PIN NAME                   | TYPE | DESCRIPTION                                                                                                                   |
|---------------------------------|----------------------------|------|-------------------------------------------------------------------------------------------------------------------------------|
| 1                               | VDD1                       | PWR  | Ref (0:2), XTAL power supply, nominal 3.3V                                                                                    |
| 2                               | REF0                       | OUT  | 14.318 Mhz reference clock.                                                                                                   |
|                                 | CPU3.3#_2.5 <sup>1,2</sup> | IN   | Indicates whether VDDL2 is 3.3V or 2.5V. High=2.5V CPU, LOW=3.3V CPU <sup>1</sup> . Latched input <sup>2</sup>                |
| 3,9,16,22,27,<br>33,39,45       | GND                        | PWR  | Ground                                                                                                                        |
| 4                               | X1                         | IN   | Crystal input, has internal load cap (33pF) and feedback resistor from X2                                                     |
| 5                               | X2                         | OUT  | Crystal output, nominally 14.318MHz. Has internal load cap (33pF)                                                             |
| 6                               | VDD2                       | PWR  | Supply for PCICLK_F and PCICLK (0:5), nominal 3.3V                                                                            |
| 7                               | PCICLK_F                   | OUT  | Free running PCI clock output. Synchronous with CPUCLKs with 1-4ns skew (CPU early) This is not affected by PCI_STOP#         |
|                                 | FS1 <sup>1, 2</sup>        | IN   | Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.               |
| 8                               | PCICLK0                    | OUT  | PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early)                                                            |
|                                 | FS2 <sup>1, 2</sup>        | IN   | Frequency select pin. Latched Input                                                                                           |
| 10, 11, 12, 13                  | PCICLK(1:4)                | OUT  | PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early)                                                            |
| 14                              | VDD5                       | PWR  | Supply for fixed PLL, 48MHz, AGP0                                                                                             |
| 15                              | BUFFERIN                   | IN   | Input pin for SDRAM buffers.                                                                                                  |
| 17                              | CPU_STOP# <sup>1</sup>     | IN   | Halts CPUCLK (0:3) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)                                           |
|                                 | SDRAM 11                   | OUT  | SDRAM clock output                                                                                                            |
| 18                              | PCI_STOP# <sup>1</sup>     | IN   | Halts PCICLK(0:5) clocks at logic 0 level, when input low (In mobile mode, MODE=0)                                            |
|                                 | SDRAM 10                   | OUT  | SDRAM clock output                                                                                                            |
| 28, 29, 31, 32, 34,<br>35,37,38 | SDRAM (0:9)                | OUT  | SDRAM clock outputs.                                                                                                          |
| 20                              | AGP_STOP#                  | IN   | This asynchronous input halts AGP(1:2) clocks at logic "0" level when input low (in Mobile Mode, MODE=0) Does not affect AGP0 |
|                                 | SDRAM9                     | OUT  | SDRAM clock output                                                                                                            |
| 21                              | PD#                        | IN   | This asynchronous Power Down input Stops the VCO, crystal & internal clocks when active, Low. (In Mobile Mode, MODE=0)        |
|                                 | SDRAM8                     | OUT  | SDRAM clock output                                                                                                            |
| 19,30,36                        | VDD3                       | PWR  | Supply for SDRAM (0:11), CPU Core, 48MHz clocks, nominal 3.3V.                                                                |
| 23                              | SDATA                      | IN   | Data input for I <sup>2</sup> C serial input.                                                                                 |
| 24                              | SCLK                       | IN   | Clock input of I <sup>2</sup> C input                                                                                         |
| 25                              | AGP0                       | OUT  | Advanced Graphic Port output, powered by VDD4. Not affected by AGP_STOP#                                                      |
|                                 | MODE <sup>1, 2</sup>       | IN   | Pin 17, 18, 20 & 21 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.                                        |
| 26                              | 48MHz                      | OUT  | 48MHz output clock for USB timing.                                                                                            |
|                                 | FS0 <sup>1, 2</sup>        | IN   | Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.               |
| 41, 43, 44                      | CPUCLK(0:3)                | OUT  | CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low                                                                     |
| 40                              | SDRAM12                    | OUT  | Feedback SDRAM clock output.                                                                                                  |
| 42                              | VDDL                       | PWR  | Supply for CPU (0:3), either 2.5V or 3.3V nominal                                                                             |
| 46, 47                          | AGP (1:2)                  | OUT  | Advanced Graphic Port outputs, powered by VDD4.                                                                               |
| 48                              | VDD4                       | PWR  | Supply for AGP (0:2)                                                                                                          |

### Notes:

- 1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



## Mode Pin - Power Management Input Control

| MODE, Pin 25<br>(Latched Input) | Pin 17               | Pin 18               | Pin 20               | Pin 21              |
|---------------------------------|----------------------|----------------------|----------------------|---------------------|
| 0                               | CPU_STOP#<br>(INPUT) | PCI_STOP#<br>(INPUT) | AGP_STOP#<br>(INPUT) | PD#<br>(INPUT)      |
| 1                               | SDRAM 11<br>(OUTPUT) | SDRAM 10<br>(OUTPUT) | SDRAM 9<br>(OUTPUT)  | SDRAM 8<br>(OUTPUT) |

## Power Management Functionality

| AGP_STOP# | CPU_STOP# | PCI_STOP# | AGP,<br>CPUCLK<br>Outputs | PCICLK<br>(0:5) | PCICLK_F,<br>REF, 48MHz<br>and SDRAM | Crystal<br>OSC | VCO     | AGP(1:2)    |
|-----------|-----------|-----------|---------------------------|-----------------|--------------------------------------|----------------|---------|-------------|
| 1         | 0         | 1         | Stopped Low               | Running         | Running                              | Running        | Running | Running     |
| 1         | 1         | 1         | Running                   | Running         | Running                              | Running        | Running | Running     |
| 1         | 1         | 0         | Running                   | Stopped Low     | Running                              | Running        | Running | Running     |
| 0         | 1         | 1         | Running                   | Running         | Running                              | Running        | Running | Stopped Low |

## CPU 3.3#\_2.5V Buffer selector for CPUCLK drivers.

| CPU3.3#_2.5<br>Input level<br>(Latched Data) | Buffer Selected for<br>operation at: |
|----------------------------------------------|--------------------------------------|
| 1                                            | 2.5V VDD                             |
| 0                                            | 3.3V VDD                             |

## Functionality

V<sub>DD1,2,3,4</sub> = 3.3V±5%, V<sub>DDL</sub> = 2.5V±5% or 3.3±5%, T<sub>A</sub> = 0 to 70°C  
 Crystal (X1, X2) = 14.31818MHz

| FS2 | FS1 | FS0 | CPU, SDRAM<br>(MHz) | PCI<br>(MHz) | AGP<br>(MHz) | REF, IOAPIC<br>(MHz) |
|-----|-----|-----|---------------------|--------------|--------------|----------------------|
| 1   | 1   | 1   | 100                 | 33.3         | 66.6         | 14.318               |
| 1   | 1   | 0   | 95.25               | 31.75        | 63.5         | 14.318               |
| 1   | 0   | 1   | 83.3                | 33.3         | 66.6         | 14.318               |
| 1   | 0   | 0   | 75                  | 30           | 60           | 14.318               |
| 0   | 1   | 1   | 75                  | 37.5         | 75           | 14.318               |
| 0   | 1   | 0   | 68.5                | 34.25        | 68.5         | 14.318               |
| 0   | 0   | 1   | 66.8                | 33.4         | 66.8         | 14.318               |
| 0   | 0   | 0   | 60                  | 30           | 60           | 14.318               |



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write:             |                      |
|---------------------------|----------------------|
| Controller (Host)         | ICS (Slave/Receiver) |
| Start Bit                 |                      |
| Address D2 <sub>(H)</sub> |                      |
|                           | <b>ACK</b>           |
| Dummy Command Code        |                      |
|                           | <b>ACK</b>           |
| Dummy Byte Count          |                      |
|                           | <b>ACK</b>           |
| Byte 0                    |                      |
|                           | <b>ACK</b>           |
| Byte 1                    |                      |
|                           | <b>ACK</b>           |
| Byte 2                    |                      |
|                           | <b>ACK</b>           |
| Byte 3                    |                      |
|                           | <b>ACK</b>           |
| Byte 4                    |                      |
|                           | <b>ACK</b>           |
| Byte 5                    |                      |
|                           | <b>ACK</b>           |
| Stop Bit                  |                      |

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read:              |                      |
|---------------------------|----------------------|
| Controller (Host)         | ICS (Slave/Receiver) |
| Start Bit                 |                      |
| Address D3 <sub>(H)</sub> |                      |
|                           | <b>ACK</b>           |
|                           | <b>Byte Count</b>    |
| ACK                       |                      |
|                           | <b>Byte 0</b>        |
| ACK                       |                      |
|                           | <b>Byte 1</b>        |
| ACK                       |                      |
|                           | <b>Byte 2</b>        |
| ACK                       |                      |
|                           | <b>Byte 3</b>        |
| ACK                       |                      |
|                           | <b>Byte 4</b>        |
| ACK                       |                      |
|                           | <b>Byte 5</b>        |
| ACK                       |                      |
| Stop Bit                  |                      |

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



## Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

| Bit     | Description                                                                                                  | PWD   |
|---------|--------------------------------------------------------------------------------------------------------------|-------|
| Bit 7   | Must be 0 for normal operation                                                                               | 0     |
|         | 0 - $\pm 0.25\%$ Spread Spectrum Modulation<br>1 - $\pm 0.6\%$ Spread Spectrum Modulation                    |       |
| Bit 6:4 | Bit6 Bit5 Bit4 CPU Clock PCI AGP                                                                             | Note1 |
|         | 111 100 33.3 66.6                                                                                            |       |
|         | 110 95.25 31.75 63.5                                                                                         |       |
|         | 101 83.3 33.3 66.6                                                                                           |       |
|         | 100 75 30 60                                                                                                 |       |
|         | 011 75 37.5 75                                                                                               |       |
|         | 010 68.5 34.25 68.5                                                                                          |       |
|         | 001 66.8 33.4 66.8                                                                                           |       |
|         | 000 60 30 60                                                                                                 |       |
| Bit 3   | 0 - Frequency is selected by hardware select, Latched Inputs<br>1 - Frequency is selected by Bit 6:4 (above) | 0     |
|         | Must be 0 for normal operation                                                                               |       |
| Bit 2   | 0 - Spread Spectrum center spread type.<br>1 - Spread Spectrum down spread type.                             | 0     |
|         | Must be 0 for normal operation                                                                               |       |
| Bit 1   | 0 - Normal<br>1 - Spread Spectrum Enabled                                                                    | 0     |
|         | Must be 0 for normal operation                                                                               |       |
| Bit 0   | 0 - Running<br>1 - Tristate all outputs                                                                      | 0     |
|         | Must be 0 for normal operation                                                                               |       |

**Note 1.** Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 000, and if bit 3 is written to a 1 to use Bits 6:4, then these should be defined to desired frequency at same write cycle.

**Note:** PWD = Power-Up Default

I<sup>2</sup>C is a trademark of Philips Corporation

Byte 1: CPU, Active/Inactive Register  
(1 = enable, 0 = disable)

| Bit   | Pin # | PWD | Description         |
|-------|-------|-----|---------------------|
| Bit 7 | -     | 1   | (Reserved)          |
| Bit 6 | -     | X   | FS2#                |
| Bit 5 | -     | X   | FS1#                |
| Bit 4 | 40    | 1   | SDRAM12 (Act/Inact) |
| Bit 3 | -     | 1   | (Reserved)          |
| Bit 2 | 41    | 1   | CPUCLK2 (Act/Inact) |
| Bit 1 | 43    | 1   | CPUCLK1 (Act/Inact) |
| Bit 0 | 44    | 1   | CPUCLK0 (Act/Inact) |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register  
(1 = enable, 0 = disable)

| Bit   | Pin # | PWD | Description          |
|-------|-------|-----|----------------------|
| Bit 7 | -     | X   | CPU3.3#_2.5          |
| Bit 6 | 7     | 1   | PCICLK_F (Act/Inact) |
| Bit 5 | -     | X   | FS0#                 |
| Bit 4 | 13    | 1   | PCICLK4 (Act/Inact)  |
| Bit 3 | 12    | 1   | PCICLK3 (Act/Inact)  |
| Bit 2 | 11    | 1   | PCICLK2 (Act/Inact)  |
| Bit 1 | 10    | 1   | PCICLK1 (Act/Inact)  |
| Bit 0 | 8     | 1   | PCICLK0(Act/Inact)   |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching.



## Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

| Bit   | Pin # | PWD | Description        |
|-------|-------|-----|--------------------|
| Bit 7 | 28    | 1   | SDRAM7 (Act/Inact) |
| Bit 6 | 29    | 1   | SDRAM6 (Act/Inact) |
| Bit 5 | 31    | 1   | SDRAM5 (Act/Inact) |
| Bit 4 | 32    | 1   | SDRAM4 (Act/Inact) |
| Bit 3 | 34    | 1   | SDRAM3 (Act/Inact) |
| Bit 2 | 35    | 1   | SDRAM2 (Act/Inact) |
| Bit 1 | 37    | 1   | SDRAM1 (Act/Inact) |
| Bit 0 | 38    | 1   | SDRAM0 (Act/Inact) |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

## Byte 4: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

| Bit   | Pin # | PWD | Description                                |
|-------|-------|-----|--------------------------------------------|
| Bit 7 | 25    | 1   | AGP0 (Active/Inactive)                     |
| Bit 6 | -     | 1   | (Reserved)                                 |
| Bit 5 | -     | 1   | (Reserved)                                 |
| Bit 4 | -     | 1   | (Reserved)                                 |
| Bit 3 | 17    | 1   | SDRAM11 (Act/Inact)<br>(Desktop Mode Only) |
| Bit 2 | 18    | 1   | SDRAM10 (Act/Inact)<br>(Desktop Mode Only) |
| Bit 1 | 20    | 1   | SDRAM9 (Act/Inact)                         |
| Bit 0 | 21    | 1   | SDRAM8 (Act/Inact)                         |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

## Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

| Bit   | Pin # | PWD | Description      |
|-------|-------|-----|------------------|
| Bit 7 | -     | 1   | (Reserved)       |
| Bit 6 | -     | 1   | (Reserved)       |
| Bit 5 | -     | 1   | (Reserved)       |
| Bit 4 | 47    | 1   | AGP1 (Act/Inact) |
| Bit 3 | -     | 1   | (Reserved)       |
| Bit 2 | -     | X   | MODE             |
| Bit 1 | 46    | 1   | AGP2 (Act/Inact) |
| Bit 0 | 2     | 1   | REF0 (Act/Inact) |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching.

## Byte 6: Optional Register for Possible Future Requirements

| Bit   | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | -     | 1   | (Reserved)  |
| Bit 6 | -     | 1   | (Reserved)  |
| Bit 5 | -     | 1   | (Reserved)  |
| Bit 4 | -     | 1   | (Reserved)  |
| Bit 3 | -     | 1   | (Reserved)  |
| Bit 2 | -     | 1   | (Reserved)  |
| Bit 1 | -     | 1   | (Reserved)  |
| Bit 0 | -     | 1   | (Reserved)  |

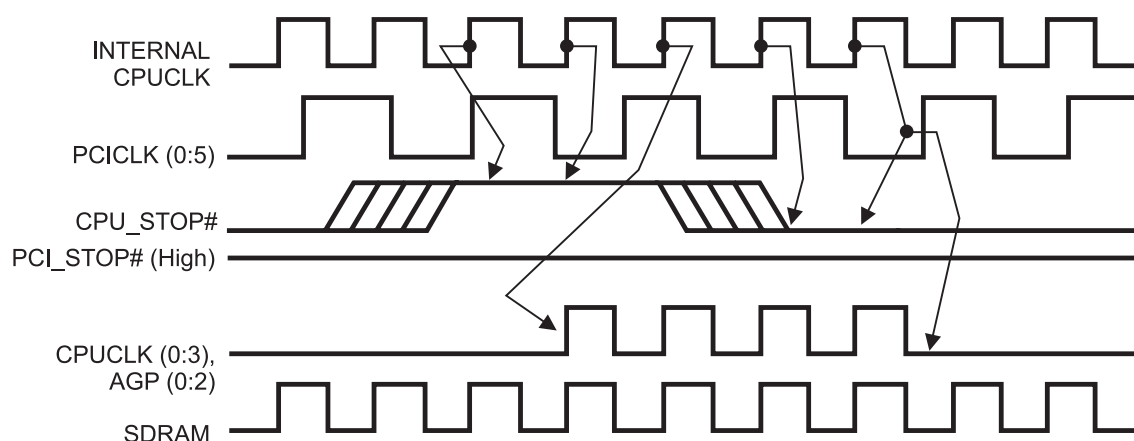
### Notes:

1. Byte 6 is reserved by Integrated Circuit Systems for future applications.



## CPU\_STOP# Timing Diagram

CPU\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU\_STOP# is synchronized by the **ICS9148-36**. The minimum that the CPU clock is enabled (CPU\_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



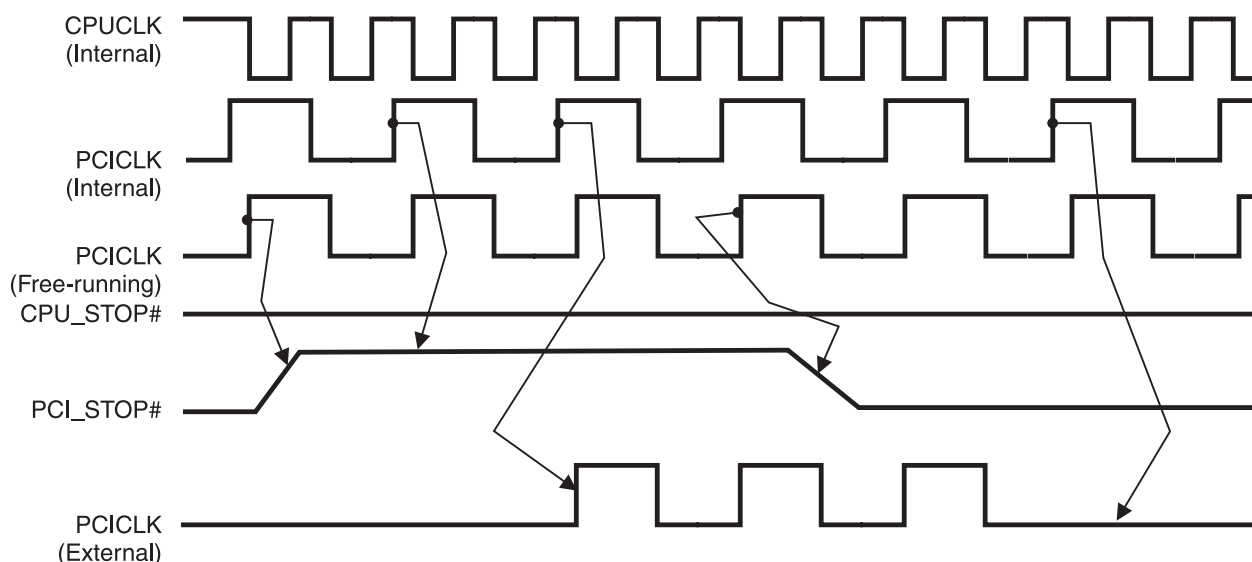
### Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9148-36.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).



## PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the **ICS9148-36**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI\_STOP# is synchronized by the **ICS9148-36** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. CPU\_STOP# is shown in a high (true) state.



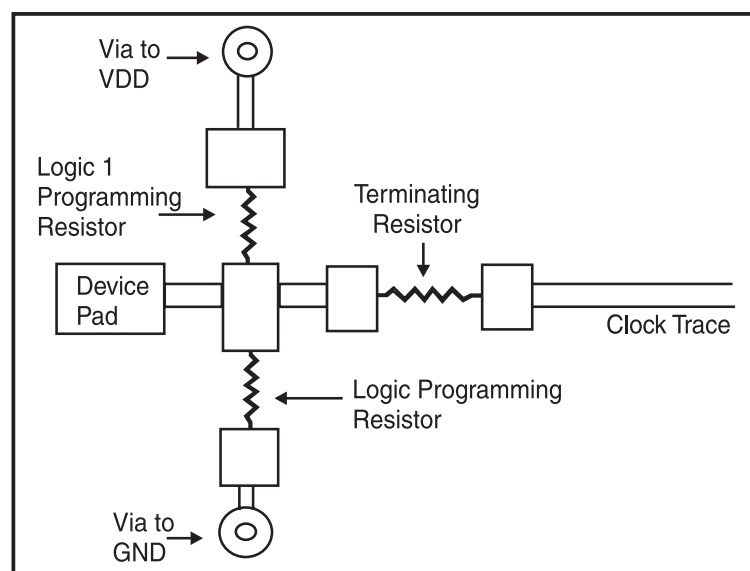
## Shared Pin Operation - Input/Output Pins

Pins 2, 7, 8, 25 & 26 on the **ICS9148-36** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

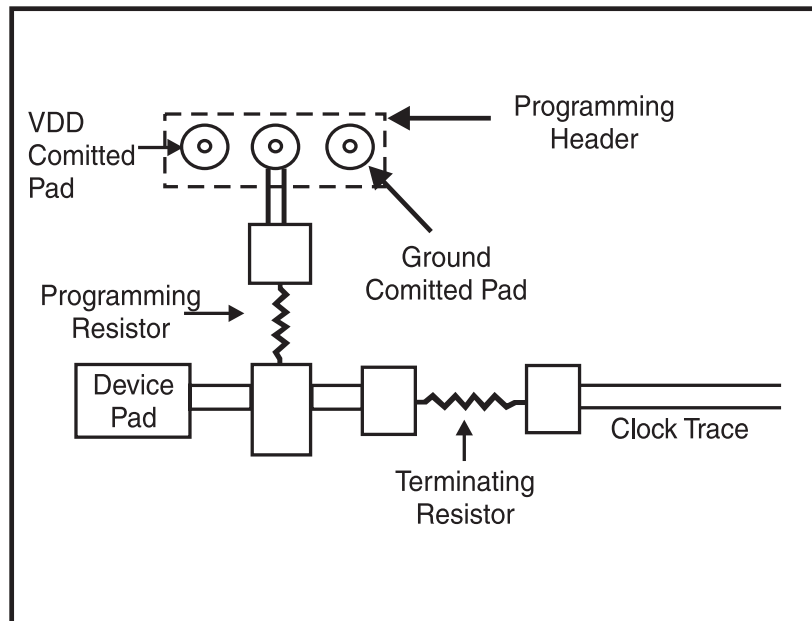
To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

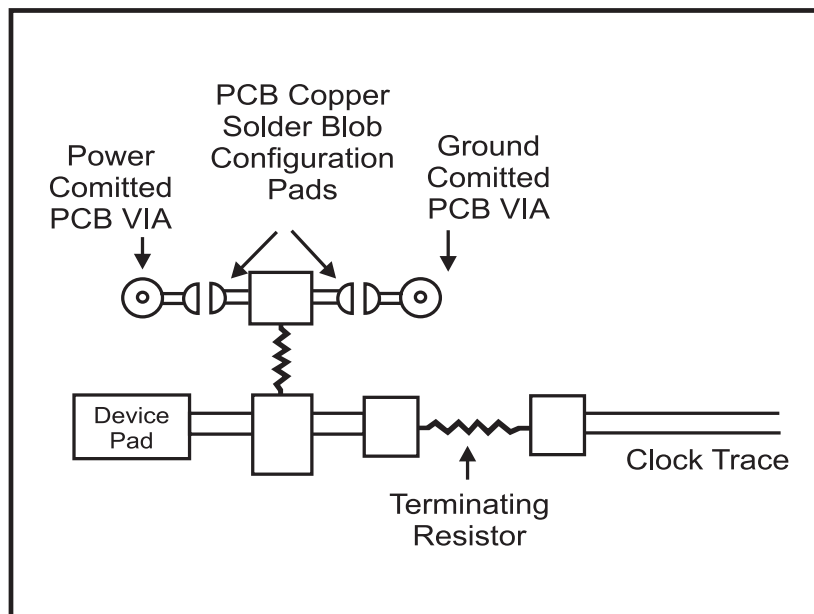
These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).



**Fig. 1**



**Fig. 2a**



**Fig. 2b**



## Absolute Maximum Ratings

|                               |                             |
|-------------------------------|-----------------------------|
| Supply Voltage                | 7.0 V                       |
| Logic Inputs                  | GND–0.5 V to $V_{DD}+0.5$ V |
| Ambient Operating Temperature | 0°C to +70°C                |
| Case Temperature              | 115°C                       |
| Storage Temperature           | –65°C to +150°C             |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = V_{DDL} = 3.3$  V  $\pm 5\%$  (unless otherwise stated)

| PARAMETER                      | SYMBOL         | CONDITIONS                                       | MIN          | TYP    | MAX          | UNITS         |
|--------------------------------|----------------|--------------------------------------------------|--------------|--------|--------------|---------------|
| Input High Voltage             | $V_{IH}$       |                                                  | 2            |        | $V_{DD}+0.3$ | V             |
| Input Low Voltage              | $V_{IL}$       |                                                  | $V_{SS}-0.3$ |        | 0.8          | V             |
| Input High Current             | $I_{IH}$       | $V_{IN} = V_{DD}$                                |              | 0.1    | 5            | $\mu\text{A}$ |
| Input Low Current              | $I_{IL1}$      | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5           | 2.0    |              | $\mu\text{A}$ |
| Input Low Current              | $I_{IL2}$      | $V_{IN} = 0$ V; Inputs with pull-up resistors    | -200         | -100   |              | $\mu\text{A}$ |
| Operating Supply Current       | $I_{DD3.3OP}$  | $C_L = 0$ pF; 66.8 MHz                           |              | 100    | 160          | mA            |
| Input frequency                | $F_i$          | $V_{DD} = 3.3$ V;                                |              | 14.318 |              | MHz           |
| Input Capacitance <sup>1</sup> | $C_{IN}$       | Logic Inputs                                     |              |        | 5            | pF            |
|                                | $C_{INX}$      | X1 & X2 pins                                     | 27           | 36     | 45           | pF            |
| Transition Time <sup>1</sup>   | $T_{trans}$    | To 1st crossing of target Freq.                  |              |        | 2            | ms            |
| Settling Time <sup>1</sup>     | $T_s$          | From 1st crossing to 1% target Freq.             |              |        |              | ms            |
| Clk Stabilization <sup>1</sup> | $T_{STAB}$     | From $V_{DD} = 3.3$ V to 1% target Freq.         |              |        | 2            | ms            |
| Skew <sup>1</sup>              | $T_{CPU-PCI1}$ | $V_T = 1.5$ V; $f = 66/100$ MHz; CPU leads       | 1            | 2.4    | 4            | ns            |
|                                | $T_{CPU-PCI1}$ | $V_T = 1.5$ V; $f = 83/75$ MHz; CPU leads        | 1            | 3.8    | 4            | ns            |
|                                | $T_{AGP-PCI1}$ | $V_T = 1.5$ V; AGP Leads                         |              | 220    | 500          | ps            |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V  $\pm 5\%$ ,  $V_{DDL} = 2.5$  V  $\pm 5\%$  (unless otherwise stated)

| PARAMETER                | SYMBOL         | CONDITIONS                                 | MIN | TYP | MAX | UNITS |
|--------------------------|----------------|--------------------------------------------|-----|-----|-----|-------|
| Operating Supply Current | $I_{DD2.5OP}$  | $C_L = 0$ pF; 66.8 MHz                     |     | 10  | 20  | mA    |
| Skew <sup>1</sup>        | $T_{CPU-PCI1}$ | $V_T = 1.5$ V; $f = 66/100$ MHz; CPU leads | 1   | 2.4 | 4   | ns    |
|                          | $T_{CPU-PCI1}$ | $V_T = 1.5$ V; $f = 83/75$ MHz; CPU leads  | 1   | 3.8 | 4   | ns    |
|                          | $T_{AGP-PCI1}$ | $V_T = 1.5$ V; AGP Leads                   |     | 220 | 500 | ps    |



## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER           | SYMBOL         | CONDITIONS                                          | MIN  | TYP  | MAX | UNITS |
|---------------------|----------------|-----------------------------------------------------|------|------|-----|-------|
| Output High Voltage | $V_{OH2A}$     | $I_{OH} = -28 \text{ mA}$                           | 2.5  | 2.6  |     | V     |
| Output Low Voltage  | $V_{OL2A}$     | $I_{OL} = 27 \text{ mA}$                            |      | 0.35 | 0.4 | V     |
| Output High Current | $I_{OH2A}$     | $V_{OH} = 2.0 \text{ V}$                            |      | -29  | -23 | mA    |
| Output Low Current  | $I_{OL2A}$     | $V_{OL} = 0.8 \text{ V}$                            | 33   | 37   |     | mA    |
| Rise Time           | $t_{r2A}^1$    | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ |      | 1.75 | 2   | ns    |
| Fall Time           | $t_{f2A}^1$    | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |      | 1.1  | 2   | ns    |
| Duty Cycle          | $d_{t2A}^1$    | $V_T = 1.5 \text{ V}$                               | 45   | 50   | 55  | %     |
| Skew                | $t_{sk2A}^1$   | $V_T = 1.5 \text{ V}$                               |      | 50   | 250 | ps    |
| Jitter, One Sigma   | $t_{j1s2A}^1$  | $V_T = 1.5 \text{ V}$                               |      | 65   | 150 | ps    |
| Jitter, Absolute    | $t_{jabs2A}^1$ | $V_T = 1.5 \text{ V}$                               | -250 | 165  | 250 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER                                     | SYMBOL         | CONDITIONS                                          | MIN  | TYP | MAX | UNITS |
|-----------------------------------------------|----------------|-----------------------------------------------------|------|-----|-----|-------|
| Output High Voltage                           | $VOH2B$        | $I_{OH} = -8 \text{ mA}$                            | 2    | 2.2 |     | V     |
| Output Low Voltage                            | $VOL2B$        | $I_{OL} = 12 \text{ mA}$                            |      | 0.3 | 0.4 | V     |
| Output High Current                           | $IOH2B$        | $V_{OH} = 1.7 \text{ V}$                            |      | -20 | -16 | mA    |
| Output Low Current                            | $IOL2B$        | $V_{OL} = 0.7 \text{ V}$                            | 19   | 26  |     | mA    |
| Rise Time                                     | $tr2B^1$       | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$ |      | 1.5 | 1.8 | ns    |
| Fall Time                                     | $tf2B^1$       | $V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |      | 1.6 | 1.8 | ns    |
| Duty Cycle                                    | $dt2B^1$       | $V_T = 1.25 \text{ V}$                              | 40   | 50  | 55  | %     |
| Skew                                          | $tsk2B^1$      | $V_T = 1.25 \text{ V}$                              |      | 60  | 250 | ps    |
| Jitter, Single Edge Displacement <sup>2</sup> | $t_{jsed2B}^1$ | $V_T = 1.25 \text{ V}$                              |      | 200 | 250 | ps    |
| Jitter, One Sigma                             | $t_{j1s2B}^1$  | $V_T = 1.25 \text{ V}$                              |      | 65  | 150 | ps    |
| Jitter, Absolute                              | $t_{jabs2B}^1$ | $V_T = 1.25 \text{ V}$                              | -250 | 160 | 250 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> Edge displacement of a period relative to a 10-clock-cycle rolling average period.



## Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$  (unless otherwise stated)

| PARAMETER                      | SYMBOL      | CONDITIONS                                       | MIN  | TYP | MAX | UNITS |
|--------------------------------|-------------|--------------------------------------------------|------|-----|-----|-------|
| Output High Voltage            | $V_{OH1}$   | $I_{OH} = -28 \text{ mA}$                        | 2.4  | 3   |     | V     |
| Output Low Voltage             | $V_{OL1}$   | $I_{OL} = 23 \text{ mA}$                         |      | 0.2 | 0.4 | V     |
| Output High Current            | $I_{OH1}$   | $V_{OH} = 2.0 \text{ V}$                         |      | -60 | -40 | mA    |
| Output Low Current             | $I_{OL1}$   | $V_{OL} = 0.8 \text{ V}$                         | 41   | 50  |     | mA    |
| Rise Time                      | $t_{r1}^1$  | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |      | 1.8 | 2   | ns    |
| Fall Time                      | $t_{f1}^1$  | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |      | 1.6 | 2   | ns    |
| Duty Cycle                     | $d_{t1}^1$  | $V_T = 1.5 \text{ V}$                            | 45   | 50  | 55  | %     |
| Skew                           | $t_{sk1}^1$ | $V_T = 1.5 \text{ V}$                            |      | 130 | 250 | ps    |
| Jitter, One Sigma <sup>1</sup> | $t_{j1s1a}$ | $V_T = 1.5 \text{ V}$ , synchronous              |      | 40  | 150 | ps    |
|                                | $t_{j1s1b}$ | $V_T = 1.5 \text{ V}$ , asynchronous             |      | 200 | 250 | ps    |
| Jitter, Absolute <sup>1</sup>  | $t_{abs1a}$ | $V_T = 1.5 \text{ V}$ , synchronous              | -250 | 135 | 250 | ps    |
|                                | $t_{abs1b}$ | $V_T = 1.5 \text{ V}$ , asynchronous             | -650 | 500 | 650 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$

| PARAMETER               | SYMBOL     | CONDITIONS                                       | MIN | TYP  | MAX | UNITS |
|-------------------------|------------|--------------------------------------------------|-----|------|-----|-------|
| Output High Voltage     | $V_{OH1}$  | $I_{OH} = -28 \text{ mA}$                        | 2.4 | 3    |     | V     |
| Output Low Voltage      | $V_{OL1}$  | $I_{OL} = 23 \text{ mA}$                         |     | 0.2  | 0.4 | V     |
| Output High Current     | $I_{OH1}$  | $V_{OH} = 2.0 \text{ V}$                         |     | -60  | -40 | mA    |
| Output Low Current      | $I_{OL1}$  | $V_{OL} = 0.8 \text{ V}$                         | 41  | 50   |     | mA    |
| Rise Time <sup>1</sup>  | $T_{r1}$   | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |     | 1.75 | 2   | ns    |
| Fall Time <sup>1</sup>  | $T_{f1}$   | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |     | 1.5  | 2   | ns    |
| Duty Cycle <sup>1</sup> | $D_{t1}$   | $V_T = 1.5 \text{ V}$                            | 45  | 50   | 55  | %     |
| Propagation Delay       | $T_{prop}$ | $V_T = 1.5 \text{ V}$                            |     | 4.2  | 6   | ns    |
| Skew <sup>1</sup>       | $T_{sk1}$  | $V_T = 1.5 \text{ V}$                            |     | 200  | 500 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - AGP

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$  (unless otherwise stated)

| PARAMETER                      | SYMBOL       | CONDITIONS                                          | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------|-----------------------------------------------------|-----|-----|-----|-------|
| Output High Voltage            | $V_{OH1}$    | $I_{OH} = -28 \text{ mA}$                           | 2.4 | 3   |     | V     |
| Output Low Voltage             | $V_{OL1}$    | $I_{OL} = 23 \text{ mA}$                            |     | 0.2 | 0.4 | V     |
| Output High Current            | $I_{OH1}$    | $V_{OH} = 2.0 \text{ V}$                            |     | -60 | -40 | mA    |
| Output Low Current             | $I_{OL1}$    | $V_{OL} = 0.8 \text{ V}$                            | 41  | 50  |     | mA    |
| Rise Time                      | $t_{r1}^1$   | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ |     | 1.1 | 2   | ns    |
| Fall Time                      | $t_{f1}^1$   | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |     | 1   | 2   | ns    |
| Duty Cycle                     | $d_{t1}^1$   | $V_T = 1.4 \text{ V}$                               | 45  | 50  | 55  | %     |
| Skew                           | $t_{sk1}^1$  | $V_T = 1.5 \text{ V}$                               |     | 130 | 250 | ps    |
| Jitter, One Sigma <sup>1</sup> | $t_{j1s1}$   | $V_T = 1.5 \text{ V}$                               |     | 2   | 3   | %     |
| Jitter, Absolute <sup>1</sup>  | $t_{abs1a}$  | $V_T = 1.5 \text{ V}$ , synchronous                 | -5  | 2.5 | 5   | %     |
|                                | $t_{jabs1b}$ | $V_T = 1.5 \text{ V}$ , asynchronous                | -6  | 4.5 | 6   | %     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 48MHz, REF

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER           | SYMBOL        | CONDITIONS                                          | MIN | TYP | MAX | UNITS |
|---------------------|---------------|-----------------------------------------------------|-----|-----|-----|-------|
| Output High Voltage | $V_{OH5}$     | $I_{OH} = -16 \text{ mA}$                           | 2.4 | 2.6 |     | V     |
| Output Low Voltage  | $V_{OL5}$     | $I_{OL} = 9 \text{ mA}$                             |     | 0.3 | 0.4 | V     |
| Output High Current | $I_{OH5}$     | $V_{OH} = 2.0 \text{ V}$                            |     | -32 | -22 | mA    |
| Output Low Current  | $I_{OL5}$     | $V_{OL} = 0.8 \text{ V}$                            | 16  | 25  |     | mA    |
| Rise Time           | $t_{r5}^1$    | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ |     | 2   | 4   | ns    |
| Fall Time           | $t_{f5}^1$    | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |     | 1.9 | 4   | ns    |
| Duty Cycle          | $d_{t5}^1$    | $V_T = 1.5 \text{ V}$                               | 45  | 50  | 57  | %     |
| Jitter, One Sigma   | $t_{j1s5}^1$  | $V_T = 1.5 \text{ V}$                               |     | 1   | 3   | %     |
| Jitter, Absolute    | $t_{jabs5}^1$ | $V_T = 1.5 \text{ V}$                               | -5  | -   | 5   | %     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

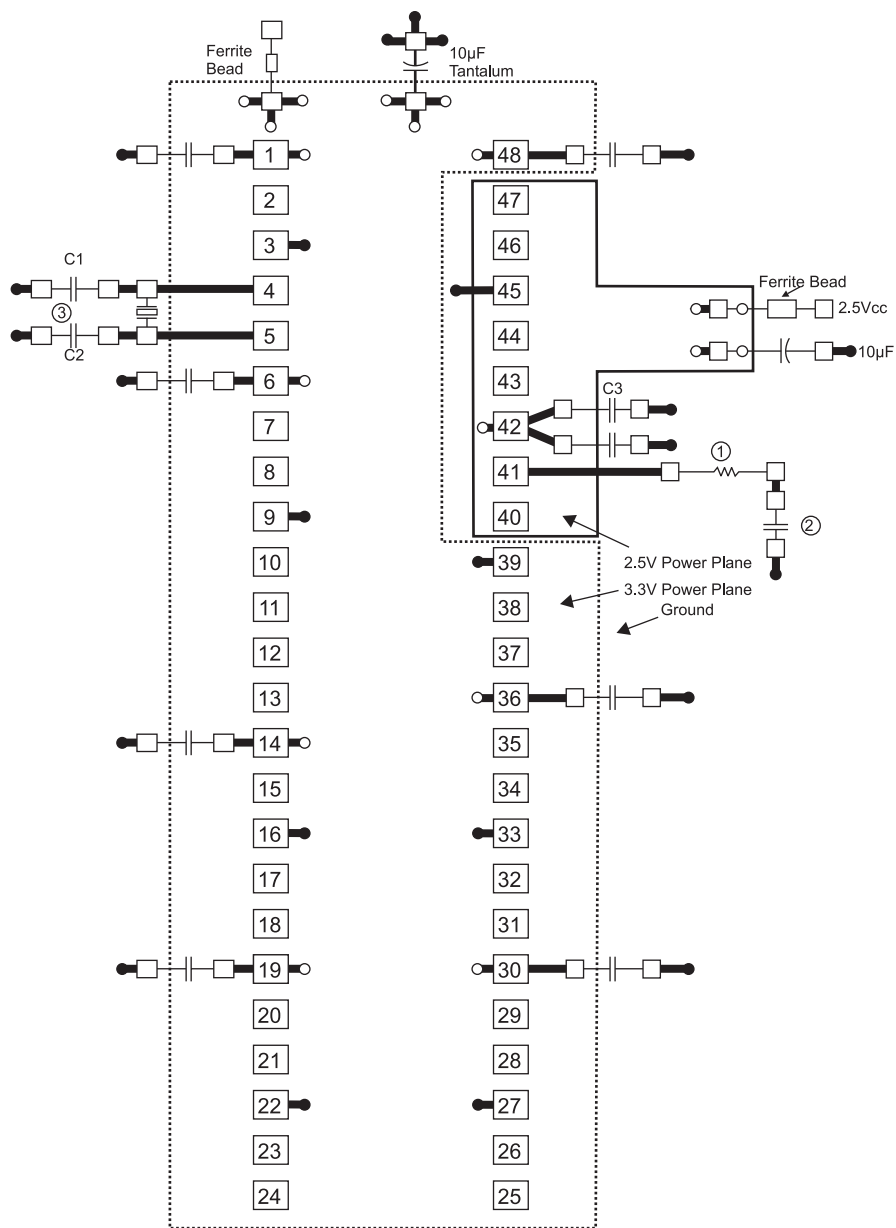


## General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

## Notes:

- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.



## Capacitor Values:

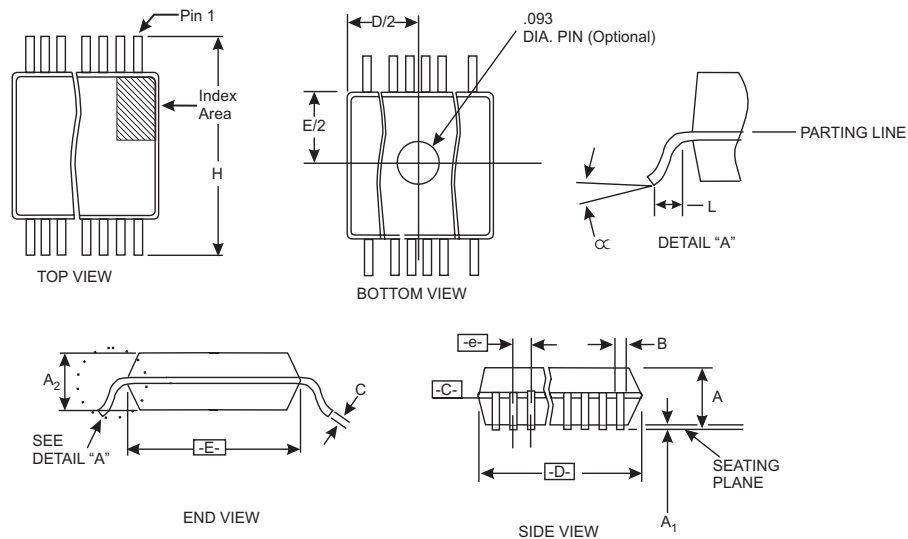
C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic



# ICS9148-36



| SYMBOL | COMMON DIMENSIONS |      |       | VARIATIONS                                              | D    |      |      | N  |
|--------|-------------------|------|-------|---------------------------------------------------------|------|------|------|----|
|        | MIN.              | NOM. | MAX.  |                                                         | MIN. | NOM. | MAX. |    |
| A      | .095              | .102 | .110  | AC                                                      | .620 | .625 | .630 | 48 |
| A1     | .008              | .012 | .016  | "For current dimensional specifications, see JEDEC 95." |      |      |      |    |
| A2     | .087              | .090 | .094  |                                                         |      |      |      |    |
| B      | .008              | -    | .0135 |                                                         |      |      |      |    |
| C      | .005              | -    | .0085 |                                                         |      |      |      |    |
| D      | See Variations    |      |       |                                                         |      |      |      |    |
| E      | .291              | .295 | .299  |                                                         |      |      |      |    |
| e      | 0.025 BSC         |      |       |                                                         |      |      |      |    |
| H      | .395              | -    | .420  |                                                         |      |      |      |    |
| h      | .010              | .013 | .016  |                                                         |      |      |      |    |
| L      | .020              | -    | .040  |                                                         |      |      |      |    |
| N      | See Variations    |      |       |                                                         |      |      |      |    |
| ∞      | 0°                | -    | 8°    |                                                         |      |      |      |    |

## 48 Pin 300 mil SSOP Package

## Ordering Information

### ICS9148yF-36

Example:

**ICS XXXX y F - PPP**

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type  
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.