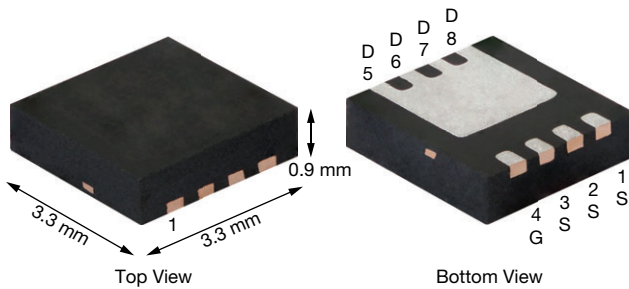


## N-Channel 20 V (D-S) Fast Switching MOSFET

**PowerPAK® 1212-8SH**


PRODUCT SUMMARY	
$V_{DS}$ (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0053
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0078
$Q_g$ typ. (nC)	14
$I_D$ (A)	21.1
Configuration	Single

### FEATURES

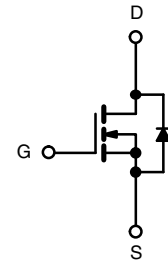
- TrenchFET® Gen II power MOSFET
- PWM optimized
- 100 %  $R_g$  tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- Synchronous buck



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH110DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	10 s	STEADY STATE	UNIT	
Drain-source voltage	$V_{DS}$	20	20	V	
Gate-source voltage	$V_{GS}$	$\pm 20$	$\pm 20$		
Continuous drain current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_A = 25$ °C	21.1	13.5	A
		$T_A = 70$ °C	16.9	10.8	
Pulsed drain current	$I_{DM}$	60	60		
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	3.2	1.3		
Single avalanche current	$I_{AS}$	L = 0.1 mH	35	35	mJ
Single avalanche energy			$E_{AS}$	61	
Maximum power dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	3.8	1.5	W
		$T_A = 70$ °C	2	0.8	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150			°C
Soldering recommendations (peak temperature) <sup>b, c</sup>		260			

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ s	24	33	°C/W
		Steady state	65	81	
Maximum junction-to-case (drain)	$R_{thJC}$	1.9	2.4		

#### Notes

- Surface mounted on 1" x 1" FR4 board
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5	-	2.5	V
Gate-body leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	5	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 21.1\text{ A}$	-	0.0044	0.0053	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 17.4\text{ A}$	-	0.0064	0.0078	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 21.1\text{ A}$	-	71	-	S
Diode forward voltage <sup>a</sup>	$V_{SD}$	$I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}$	-	0.8	1.2	V
<b>Dynamic <sup>b</sup></b>						
Total gate charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 21.1\text{ A}$	-	14	21	nC
Gate-source charge	$Q_{gs}$		-	7	-	
Gate-drain charge	$Q_{gd}$		-	4.5	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.7	1.4	2.1	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$	-	12	20	ns
Rise time	$t_r$		-	10	15	
Turn-off delay time	$t_{d(off)}$		-	36	55	
Fall time	$t_f$		-	10	15	
Body diode reverse recovery time	$t_{rr}$	$I_F = 3.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	30	60	nC
Body diode reverse recovery charge	$Q_{rr}$		-	25	50	
Reverse recovery fall time	$t_a$		-	14	-	
Reverse recovery rise time	$t_b$		-	16	-	

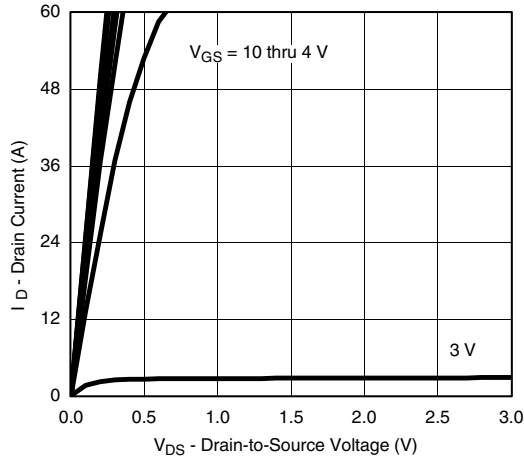
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

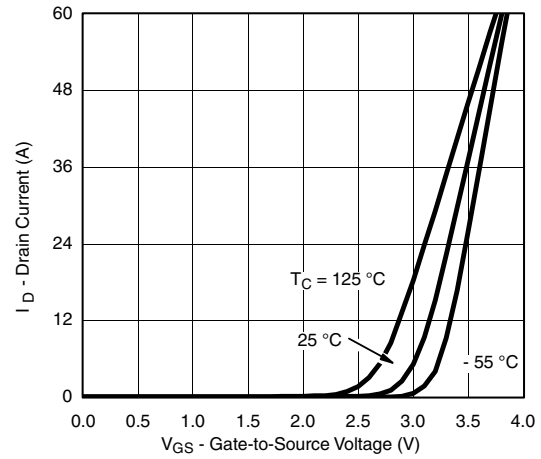
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



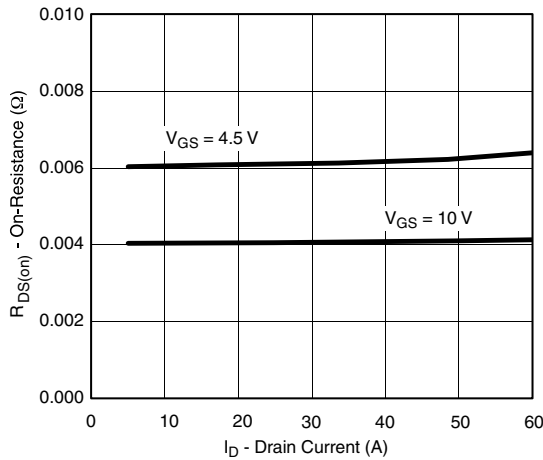
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



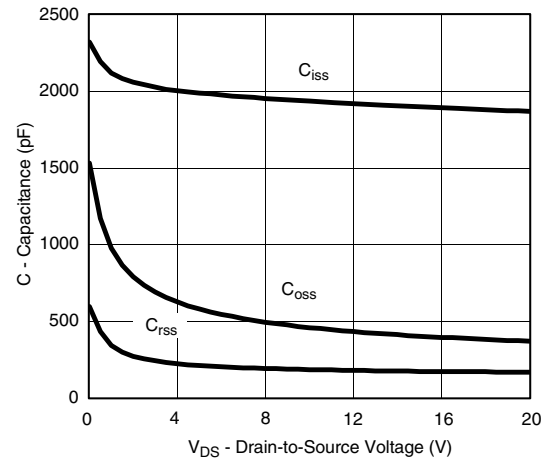
Output Characteristics



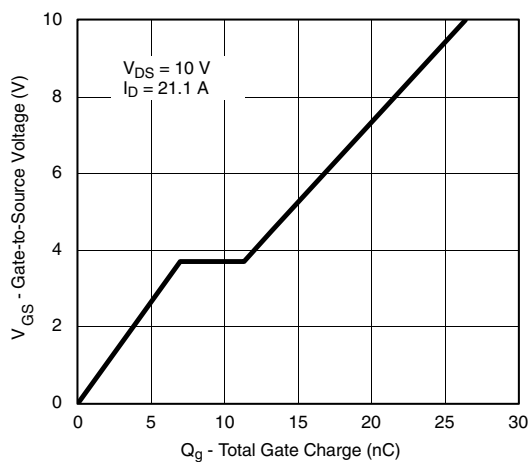
Transfer Characteristics



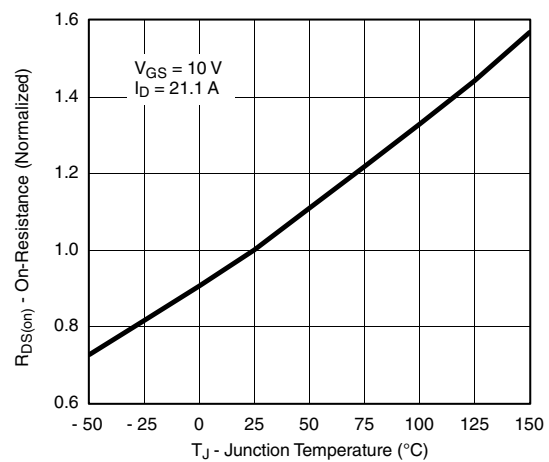
On-Resistance vs. Drain Current



Capacitance



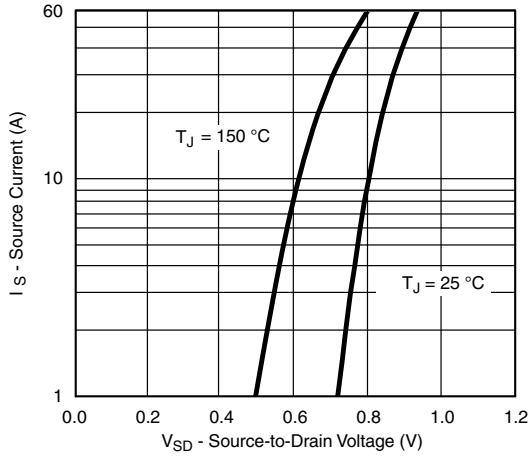
Gate Charge



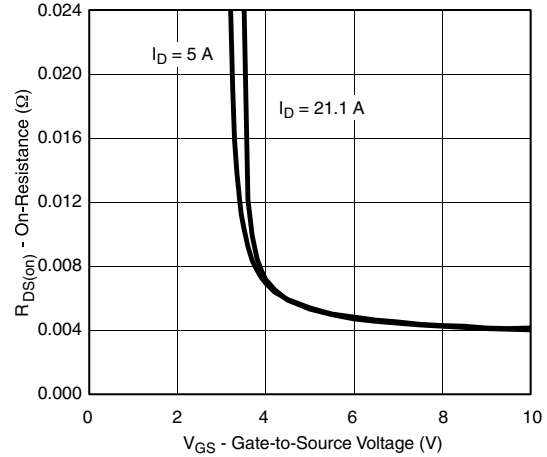
On-Resistance vs. Junction Temperature



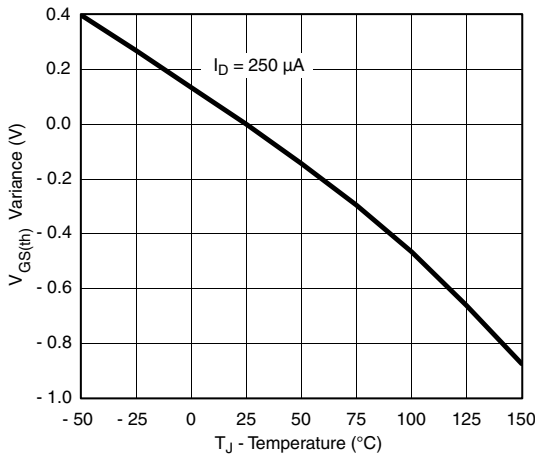
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



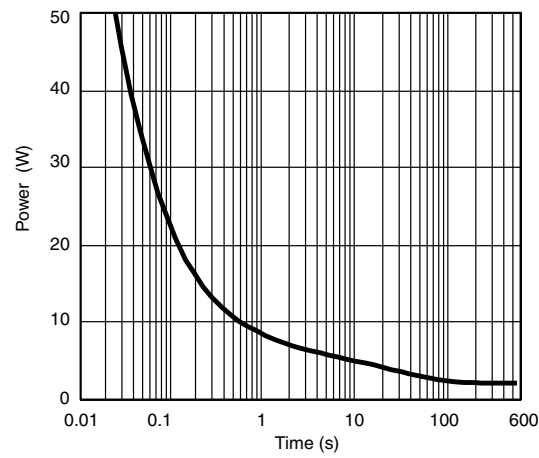
**Source-Drain Diode Forward Voltage**



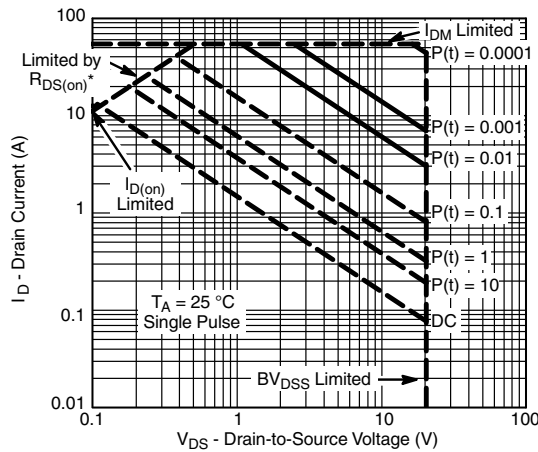
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



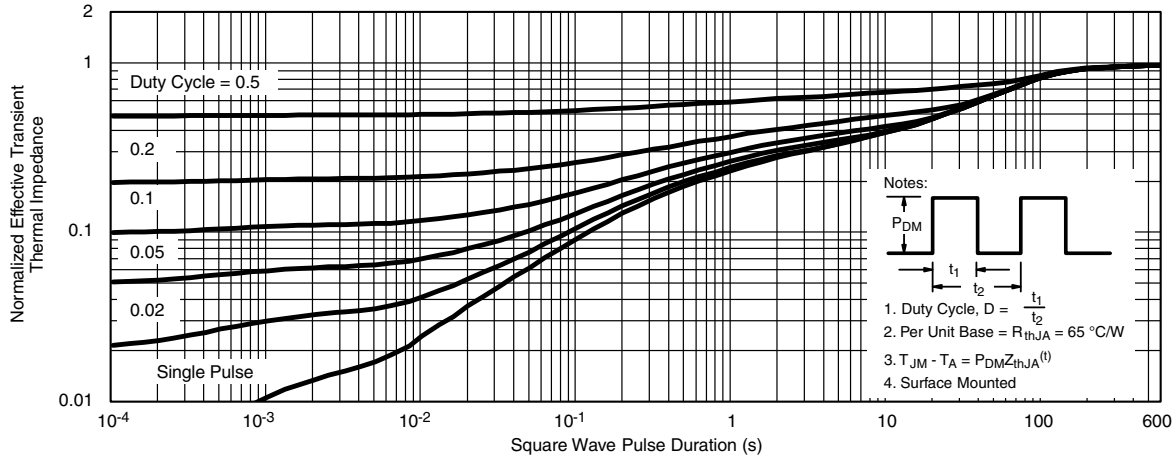
**Single Pulse Power, Junction-to-Ambient**



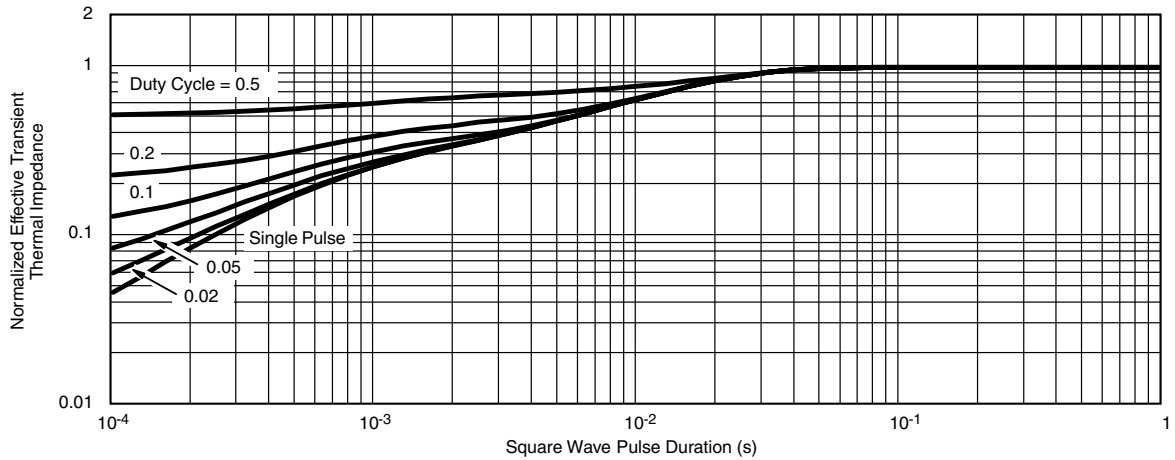
**Safe Operating Area**



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

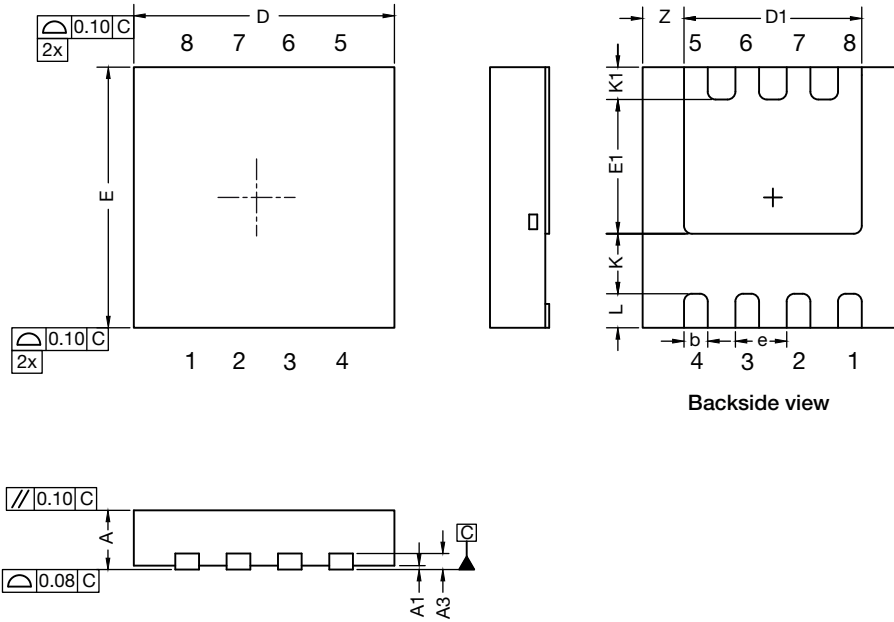


Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® 1212-SWLH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.30 BSC			0.012 BSC		
D	3.30 BSC			0.130 BSC		
D1	2.15	2.25	2.35	0.084	0.088	0.092
E	3.30 BSC			0.130 BSC		
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 BSC			0.026 BSC		
K	0.76 typ.			0.030 typ.		
K1	0.41 typ.			0.016 typ.		
L	0.43 BSC			0.017 BSC		
Z	0.525 typ.			0.021 typ.		

ECN: C18-0001-Rev. A, 15-Jan-18  
 DWG: 6062



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- Техническая поддержка проекта;
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