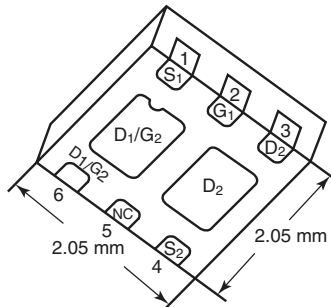




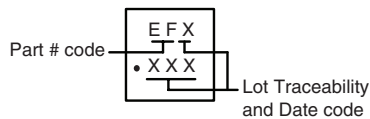
N- and P-Channel for Level Shift Load Switch

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	20	0.225 at V _{GS} = 4.5 V	1.5 ^a	1.1 nC
		0.270 at V _{GS} = 2.5 V	1.5 ^a	
		0.345 at V _{GS} = 1.8 V	1.5 ^a	
		0.960 at V _{GS} = 1.5 V	0.5	
P-Channel	- 12	0.057 at V _{GS} = - 4.5 V	- 4.5 ^a	5 nC
		0.077 at V _{GS} = - 2.5 V	- 4.5 ^a	
		0.115 at V _{GS} = - 1.8 V	- 4.5 ^a	
		0.200 at V _{GS} = - 1.5 V	- 1.5	

PowerPAK® SC-70-6 Dual



Marking Code



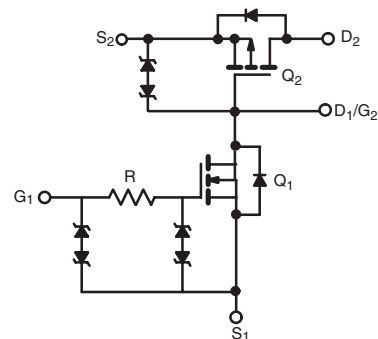
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Typical ESD Protection: N-Channel 2800 V
P-Channel 1900 V
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Load Switch with Level Shift for Portable Devices
 - N-Channel for Level Shift Drive
 - P-Channel for Main Switch



Ordering Information: SiA777EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	20	- 12	V	
Gate-Source Voltage	V _{GS}	± 6	± 8		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	1.5 ^a	- 4.5 ^a	A
		T _C = 70 °C	1.5 ^a	- 4.5 ^a	
		T _A = 25 °C	1.5 ^{a, b, c}	- 4.5 ^{a, b, c}	
		T _A = 70 °C	1.5 ^{a, b, c}	- 3.9 ^{b, c}	
Pulsed Drain Current	I _{DM}	4	- 15		
Source Drain Current Diode Current	I _S	T _C = 25 °C	1.5 ^a	- 4.5 ^a	
		T _A = 25 °C	1.6 ^{b, c}	- 1.6 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	5	7.8	W
		T _C = 70 °C	3.2	5	
		T _A = 25 °C	1.9 ^{b, c}	1.9 ^{b, c}	
		T _A = 70 °C	1.2 ^{b, c}	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	20	25	12.5	16	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions for channel 1 and channel 2 is 110 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	20			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-12			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		21		mV/°C
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-3		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-2.3		mV/°C
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		2.3		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.4		1.0	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.4		-1	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 3\text{ V}$	N-Ch			± 1	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$	P-Ch			± 0.5	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 6\text{ V}$	N-Ch			± 1	mA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	P-Ch			± 3	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	4			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-10			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 1.6\text{ A}$	N-Ch		0.183	0.225	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -3.8\text{ A}$	P-Ch		0.047	0.057	
		$V_{GS} = 2.5\text{ V}, I_D = 1.5\text{ A}$	N-Ch		0.220	0.270	
		$V_{GS} = -2.5\text{ V}, I_D = -3.3\text{ A}$	P-Ch		0.063	0.077	
		$V_{GS} = 1.8\text{ V}, I_D = 1.3\text{ A}$	N-Ch		0.275	0.345	
		$V_{GS} = -1.8\text{ V}, I_D = 2.6\text{ A}$	P-Ch		0.095	0.115	
		$V_{GS} = 1.5\text{ V}, I_D = 0.3\text{ A}$	N-Ch		0.320	0.960	
		$V_{GS} = -1.5\text{ V}, I_D = 1\text{ A}$	P-Ch		0.125	0.200	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 1.6\text{ A}$	N-Ch		3.5		S
		$V_{DS} = -10\text{ V}, I_D = -3.8\text{ A}$	P-Ch		11		
Dynamic^a							
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 5\text{ V}, I_D = 1.7\text{ A}$	N-Ch		1.3	2.2	nC
		$V_{DS} = -6\text{ V}, V_{GS} = -8\text{ V}, I_D = -4.9\text{ A}$	P-Ch		7.5	12	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1.7\text{ A}$	N-Ch		1.1	1.7	
			P-Ch		5	8	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.9\text{ A}$	N-Ch		0.2		
			P-Ch		0.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch	40	200	400	Ω
			P-Ch	2	10	20	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 7.7\ \Omega$ $I_D \cong 1.3\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		20	30	ns
Rise Time	t_r		P-Ch		20	30	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -6\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong -3.9\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		12	20	
			P-Ch		20	30	
Fall Time	t_f		N-Ch		70	105	
			P-Ch		32	50	
			N-Ch		20	30	
			P-Ch		16	25	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			1.5	A
			P-Ch			-4.5	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			4	A
			P-Ch			-15	
Body Diode Voltage	V_{SD}	$I_S = 1.3\text{ A}$, $V_{GS} = 0\text{ V}$	N-Ch		0.9	1.2	V
		$I_S = -3.9\text{ A}$, $V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 1.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		50	75	ns
			P-Ch		45	70	
Body Diode Reverse Recovery Charge	Q_{rr}	P-Channel $I_F = -3.9\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		30	45	nC
			P-Ch		25	40	
Reverse Recovery Fall Time	t_a		N-Ch		15		ns
			P-Ch		15		
Reverse Recovery Rise Time	t_b	N-Ch		35			
		P-Ch		30			

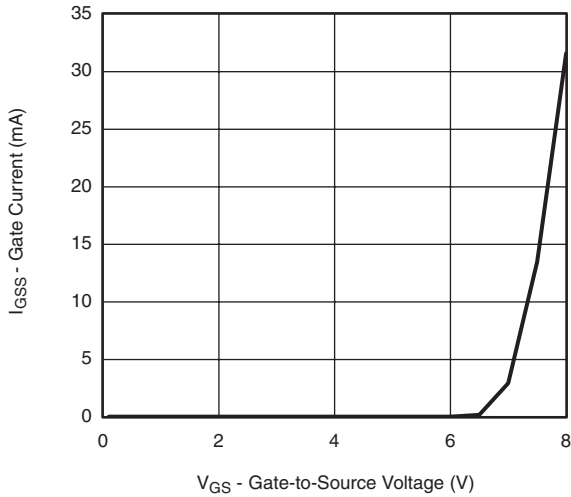
Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

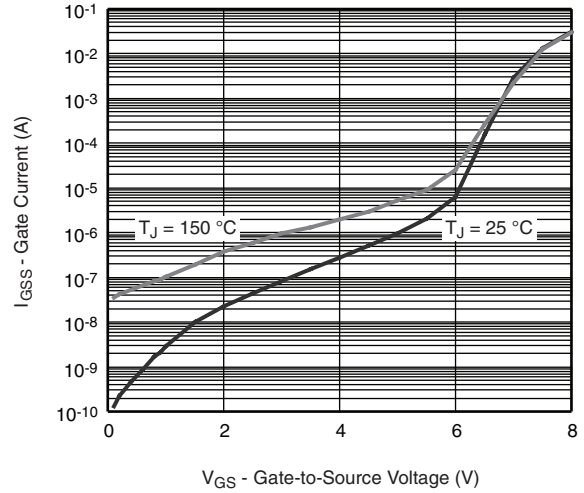
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



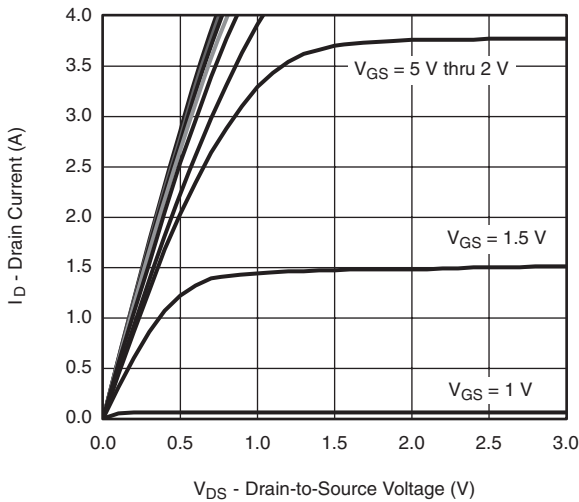
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



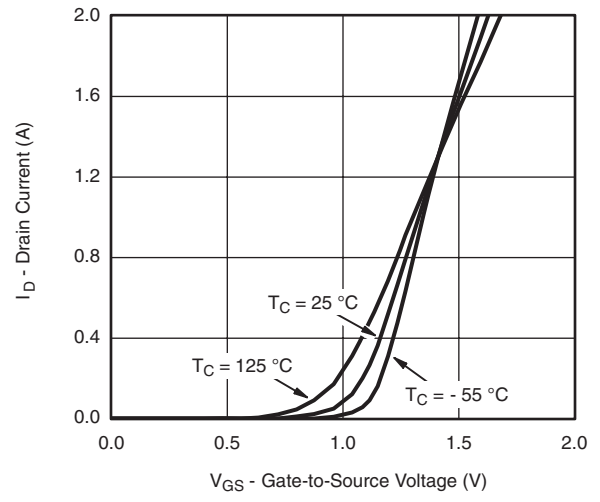
Gate Current vs. Gate-to-Source Voltage



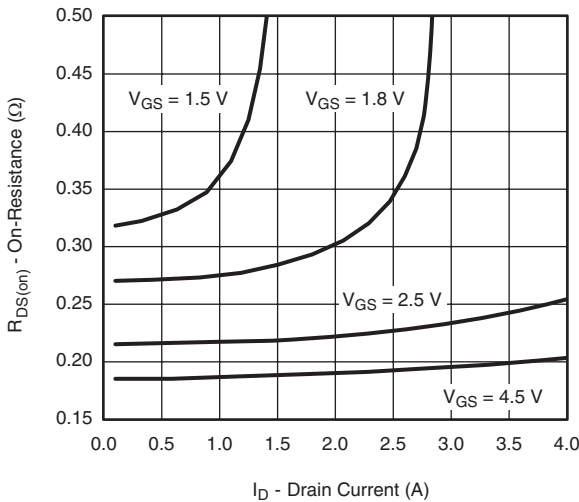
Gate Current vs. Gate-to-Source Voltage



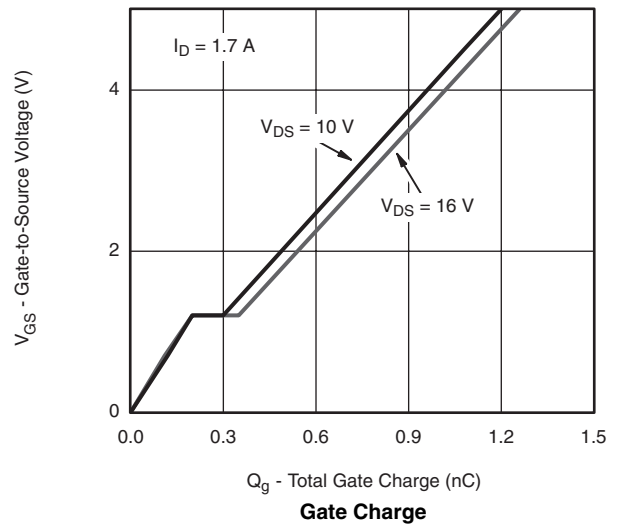
Output Characteristics



Transfer Characteristics



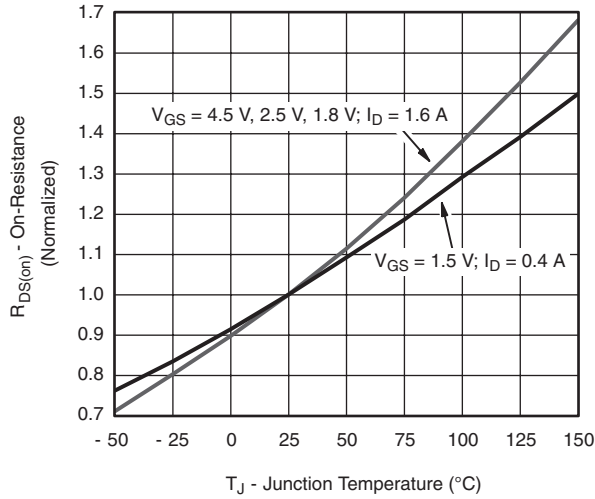
On-Resistance vs. Drain Current



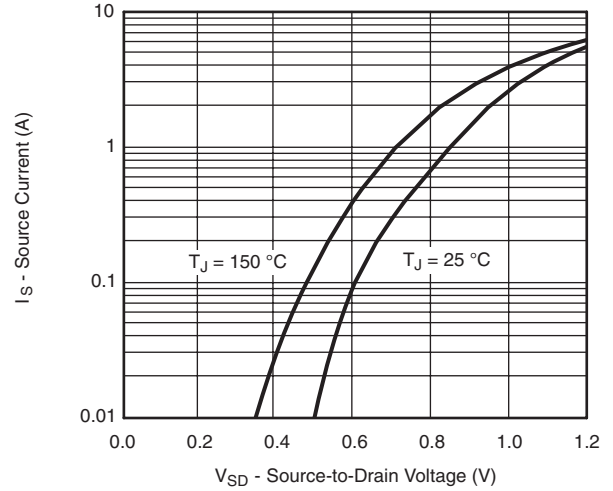
Gate Charge



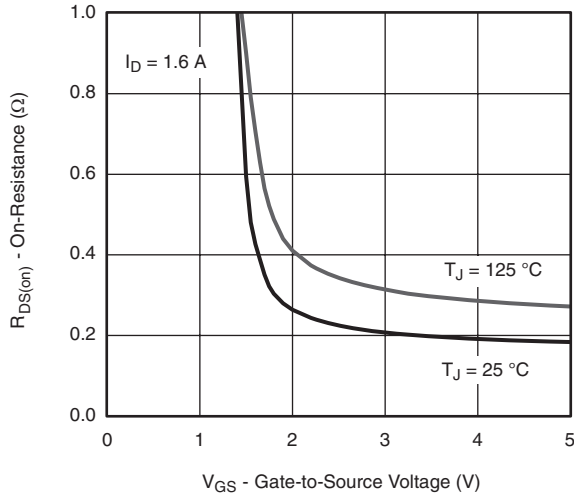
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



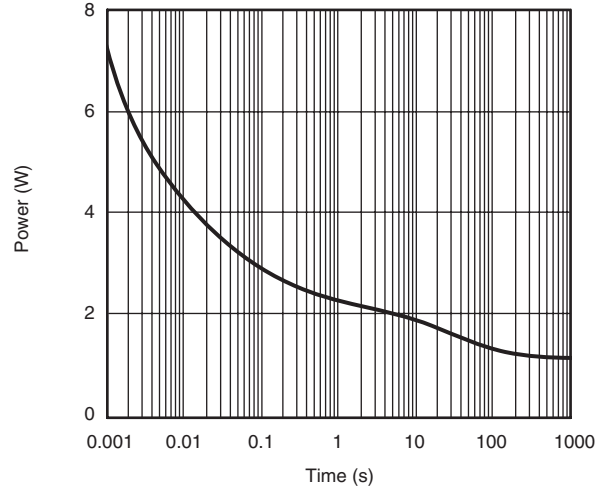
Normalized On-Resistance vs. Junction Temperature



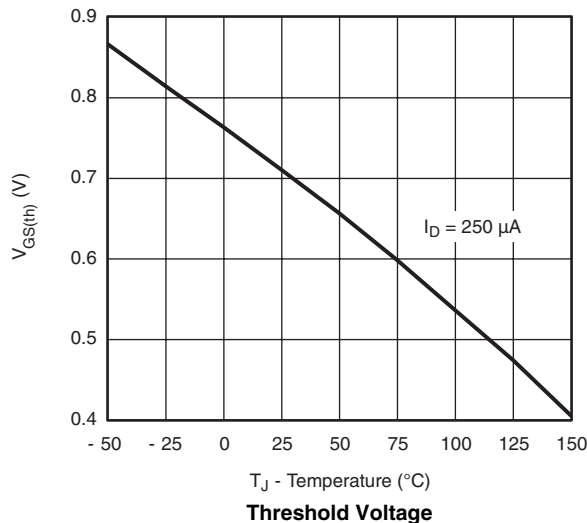
Source-Drain Diode Forward Voltage



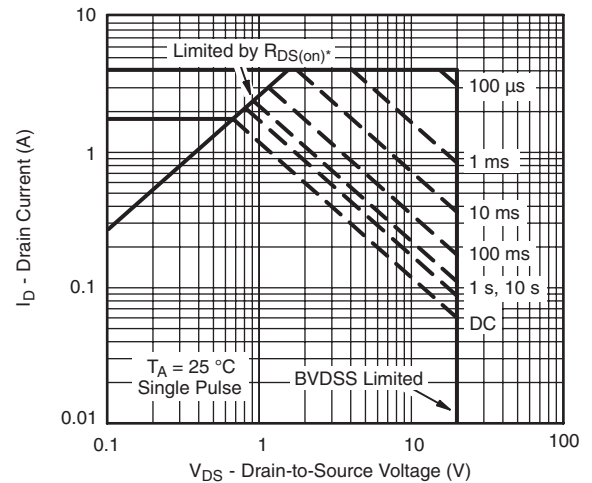
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

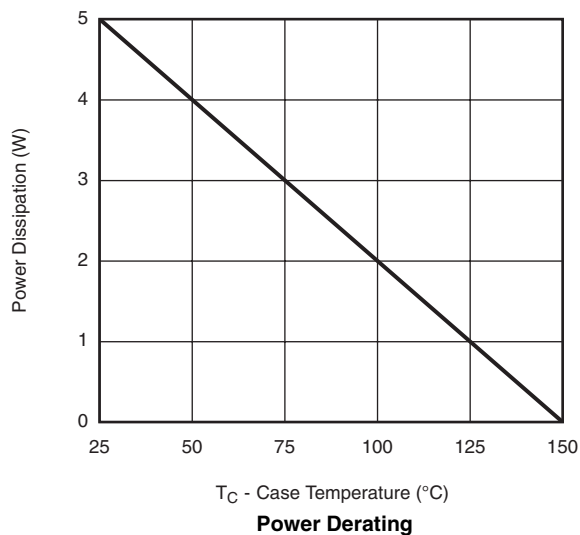
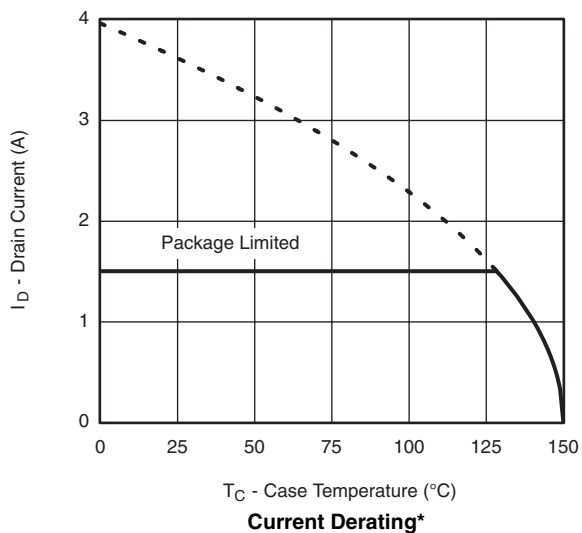


Threshold Voltage



Safe Operating Area, Junction-to-Ambient
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

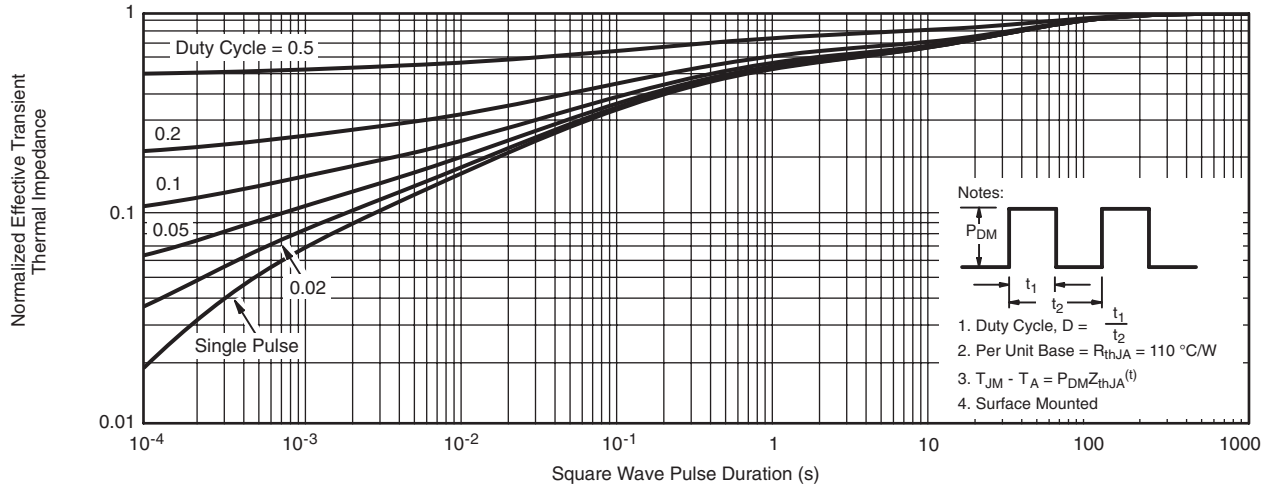
N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



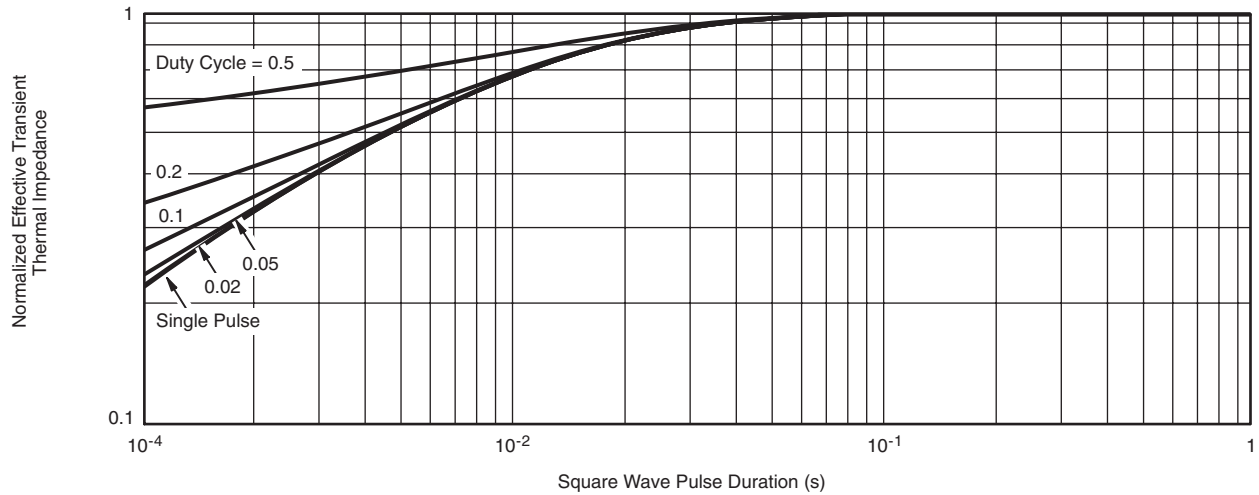
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



N-CHANNEL TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted

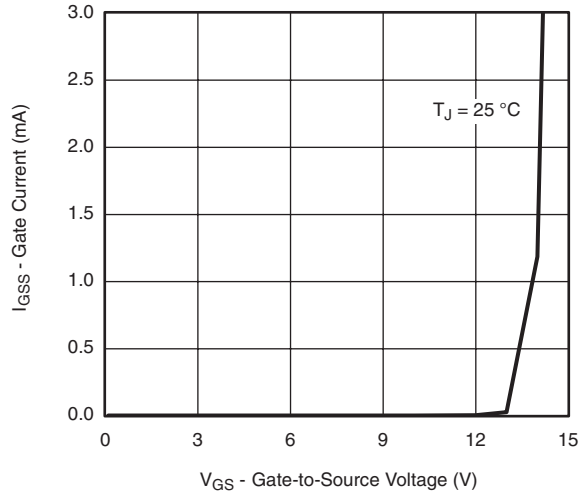


Normalized Thermal Transient Impedance, Junction-to-Ambient

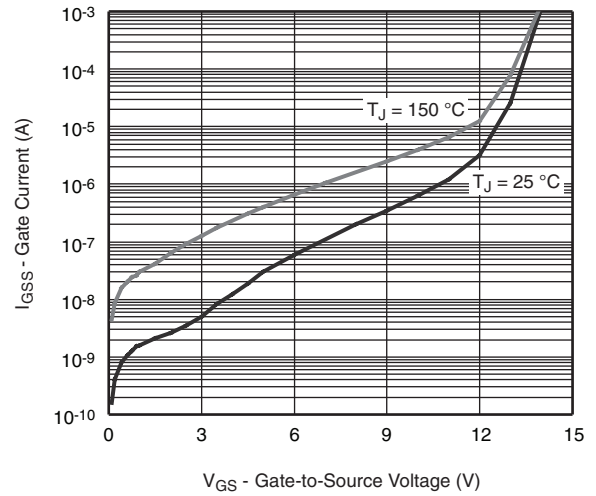


Normalized Thermal Transient Impedance, Junction-to-Case

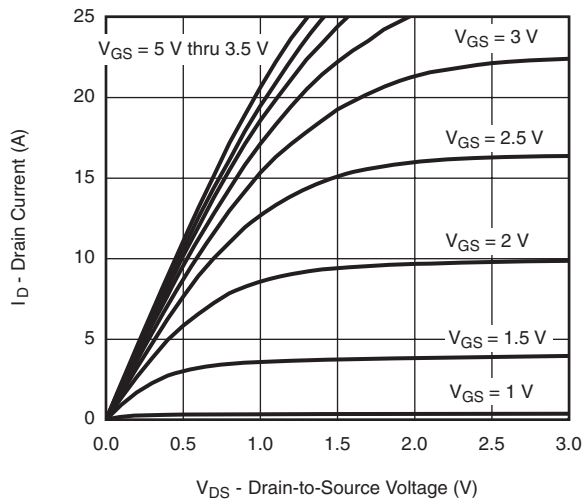
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



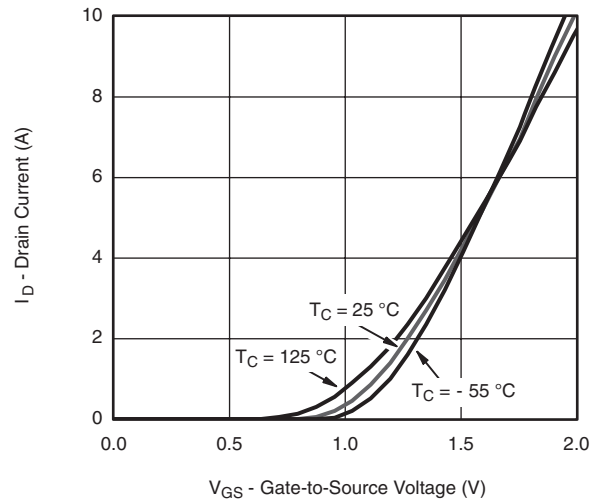
Gate Current vs. Gate-Source Voltage



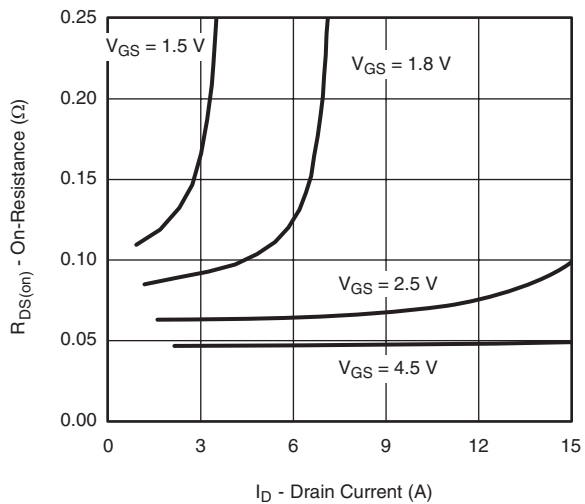
Gate Current vs. Gate-Source Voltage



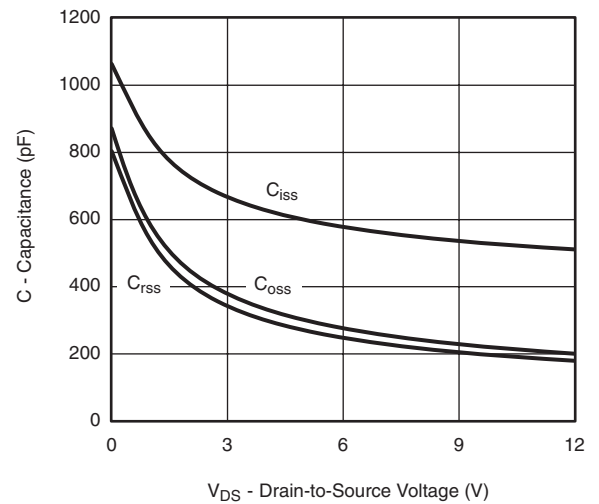
Output Characteristics



Transfer Characteristics



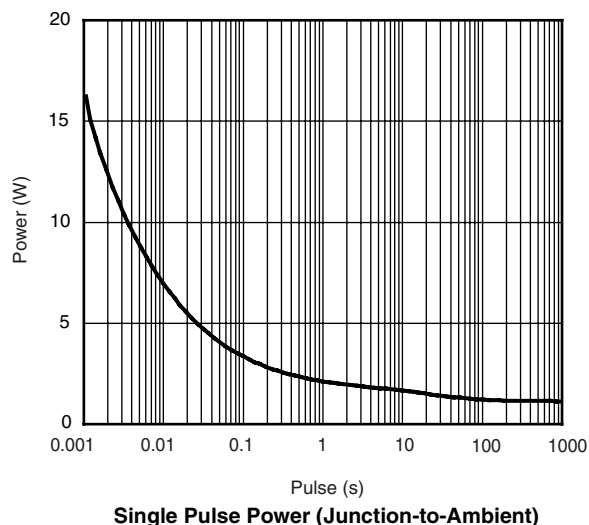
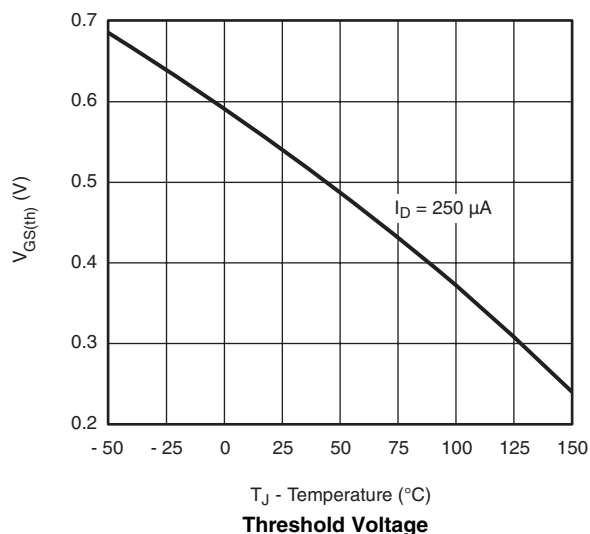
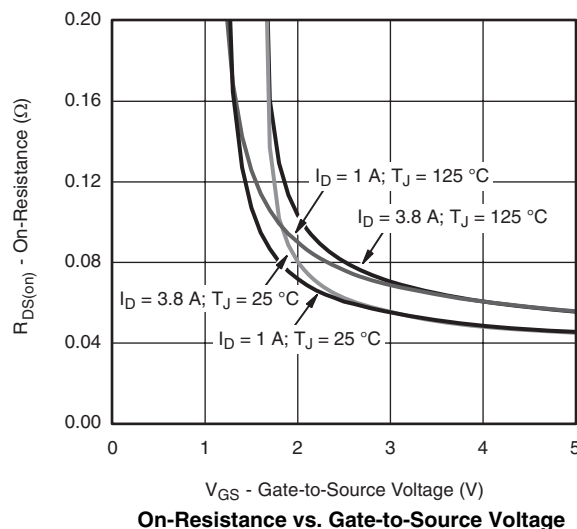
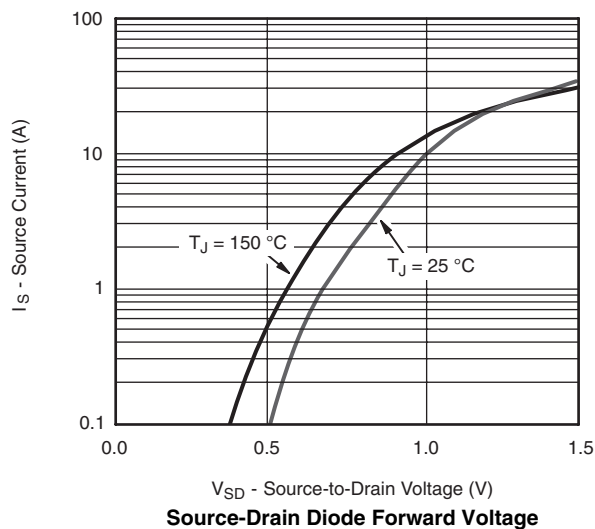
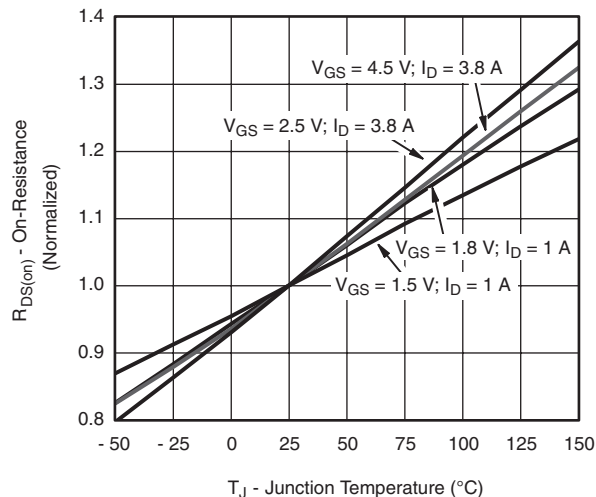
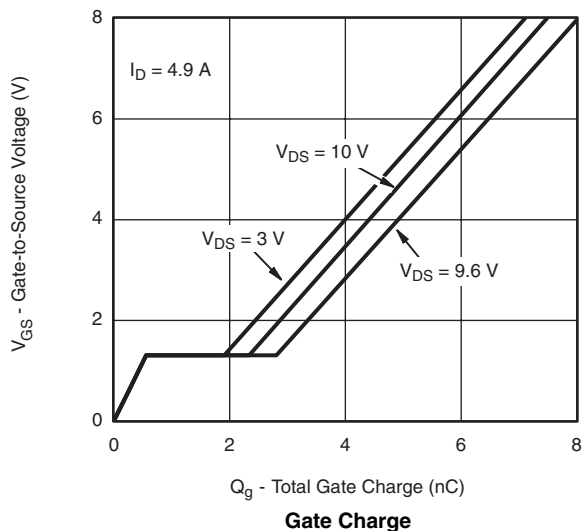
On-Resistance vs. Drain Current and Gate Voltage



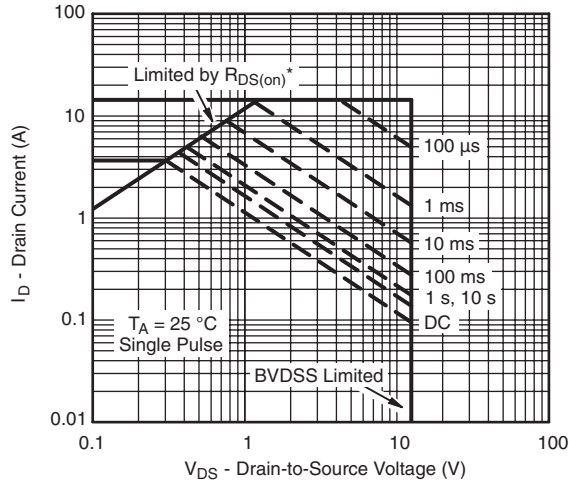
Capacitance



P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

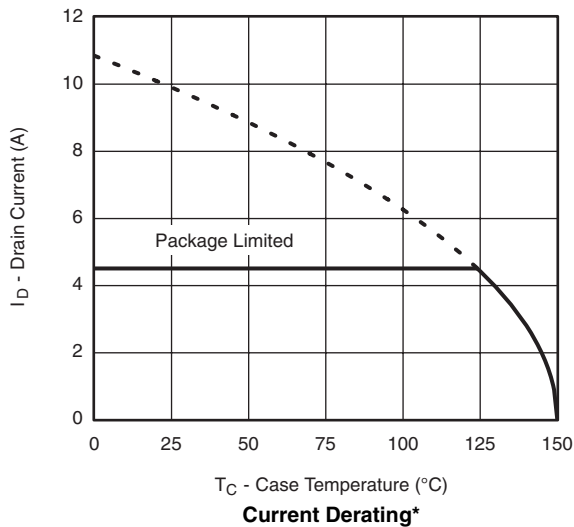


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

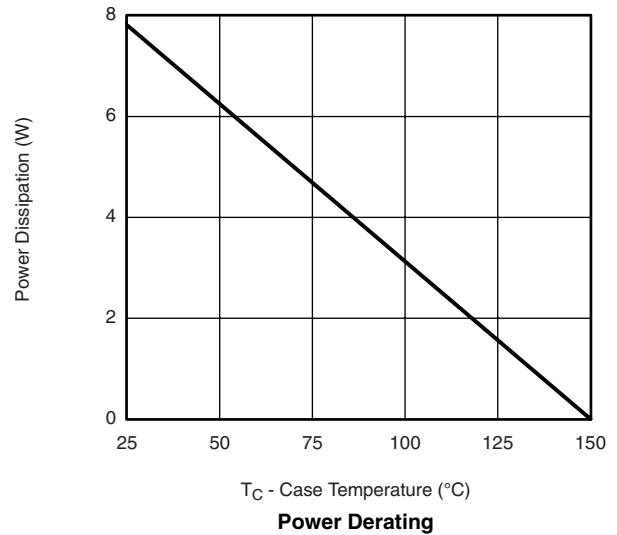


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



Current Derating*

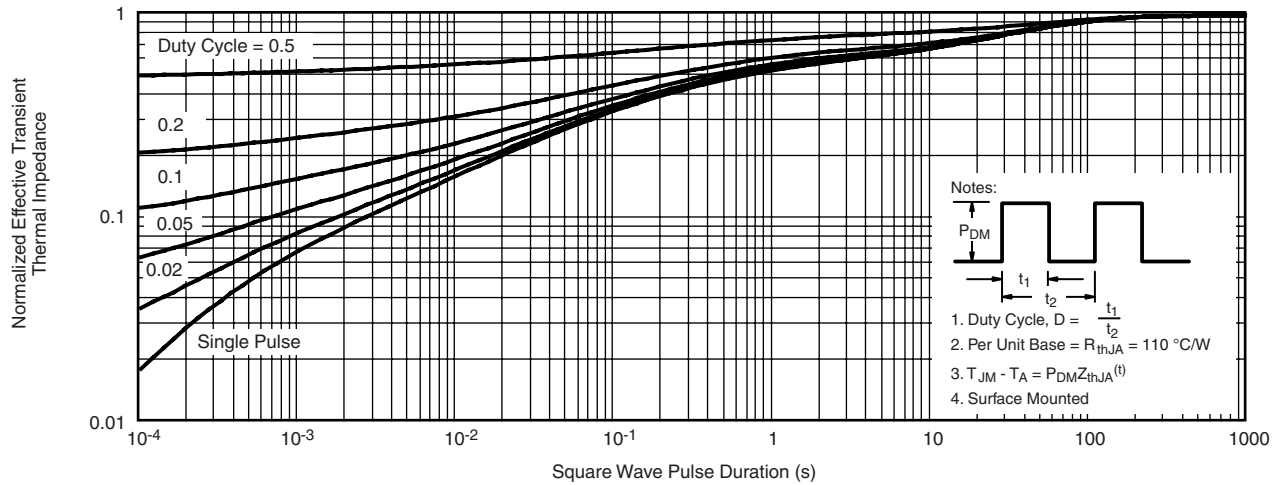


Power Derating

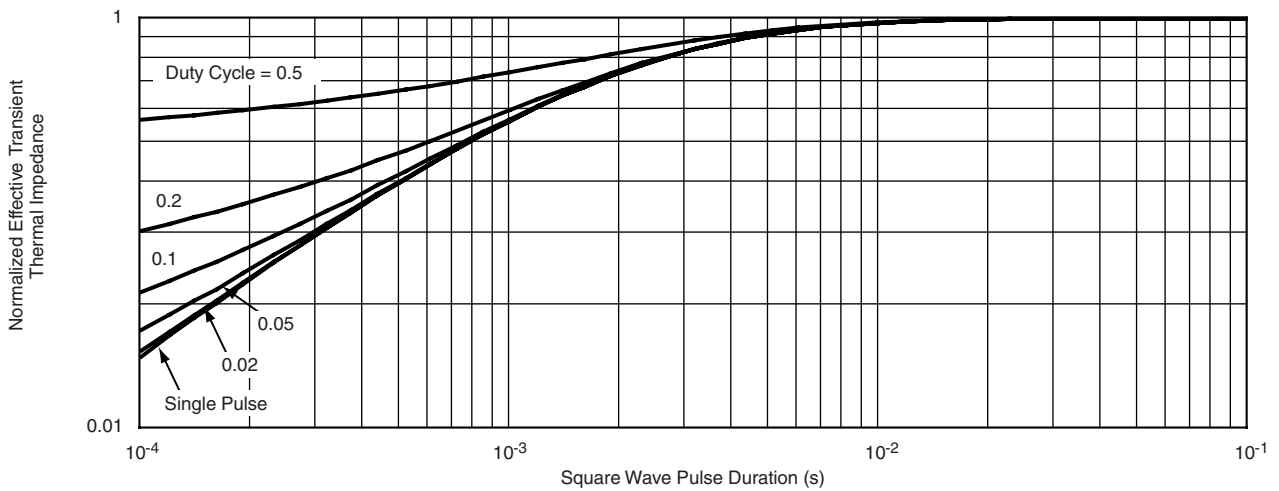
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

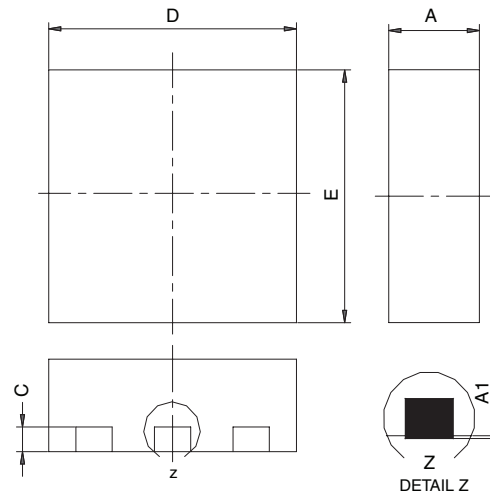
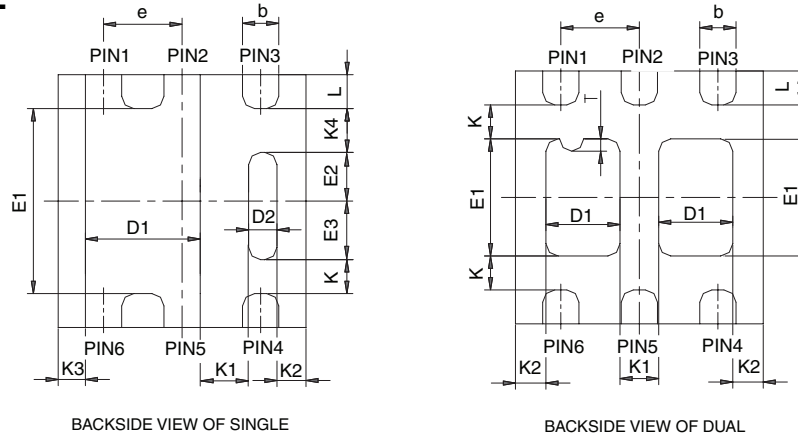


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65371.



PowerPAK® SC70-6L

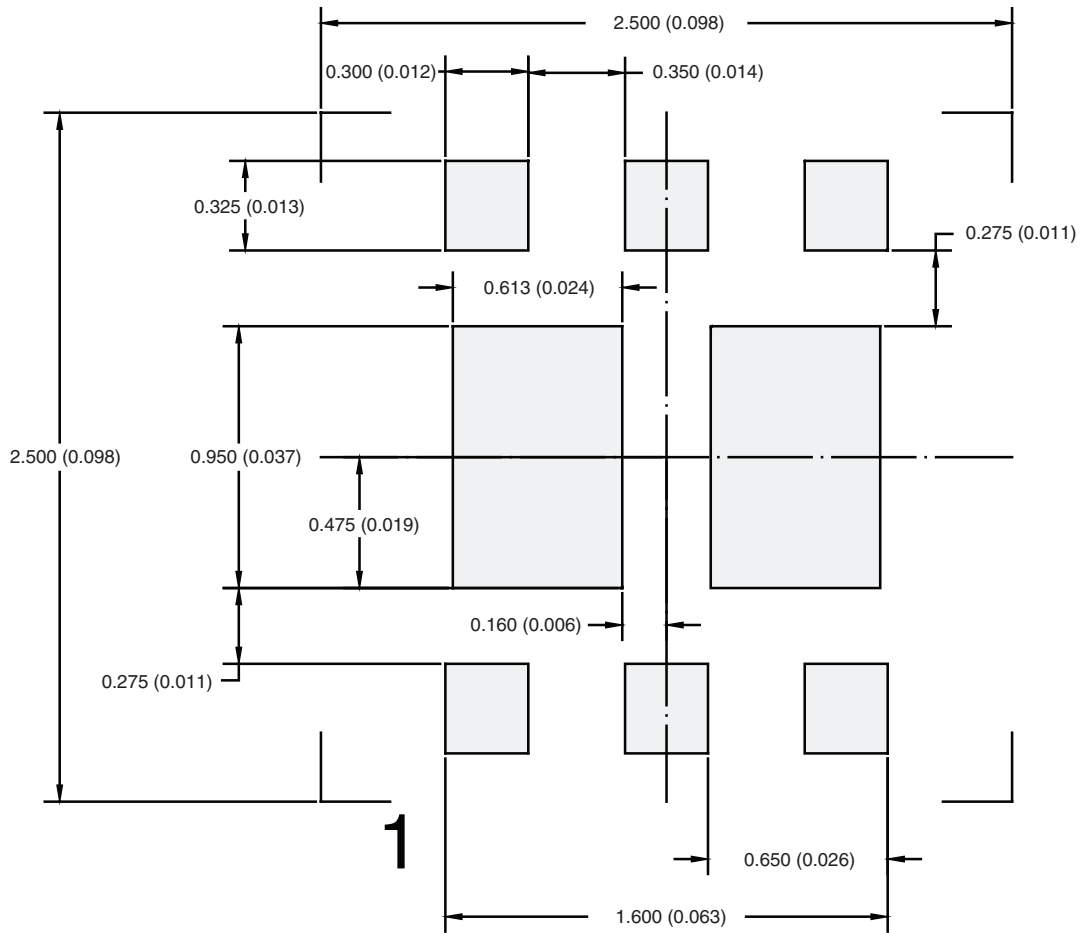


- Notes:
 1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

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 DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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