SID1102K
SCALE-iDriver Family

Up to 5 A Single Channel IGBT/MOSFET Gate Driver Providing Reinforced Galvanic Isolation up to 1200 V Blocking Voltage

Product Highlights

Highly Integrated, Compact Footprint

- Single channel providing up to 5 A peak gate drive current
- Auxiliary outputs for external booster stage for increased peak drive current
- Integrated FluxLink™ technology providing safe isolation between primary-side and secondary-side
- Rail-to-rail stabilized output voltage
- Unipolar supply voltage for secondary-side
- Suitable for 600 V / 650 V / 1200 V IGBT and MOSFET switches
- Up to 75 kHz switching frequency
- Propagation delay jitter ±5 ns
- -40 °C to 125 °C operating ambient temperature
- High common-mode transient immunity
- eSOP package with 9.5 mm creepage and clearance

Protection / Safety Features

- Undervoltage lock-out protection for primary and secondary-side (UVLO)

Full Safety and Regulatory Compliance

- 100% production partial discharge test
- 100% production HIPOT compliance testing at 6 kV RMS 1 s
- Reinforced insulation meets VDE V 0884-10

Green Package

- Halogen free and RoHS compliant

Applications

- General purpose and servo drives
- UPS, solar, welding inverters and power supplies

Description

The SID1102K is a single channel IGBT and MOSFET gate driver in an eSOP package. Reinforced galvanic isolation is provided by Power Integrations' revolutionary solid insulator FluxLink technology. Up to 5 A peak output drive current enables the product to drive devices with nominal currents of up to 300 A. For gate drive requirements that exceed the stand-alone capability of SID1102K, additionally AUXGL and AUXGH output pins can drive external n-channel MOSFETs as a booster stage, giving customers full freedom and control of their system design.

Controller (PWM) signals are compatible with 5 V CMOS logic, which may also be adjusted to 15 V levels by using external resistor divider.

Product Portfolio

Product[1]	Peak Output Drive Current
SID1102K	5 A without external booster

Table 1. SCALE-iDriver Portfolio.
Notes:
1. Package: eSOP-R16B.

Figure 2. eSOP-R16B Package.

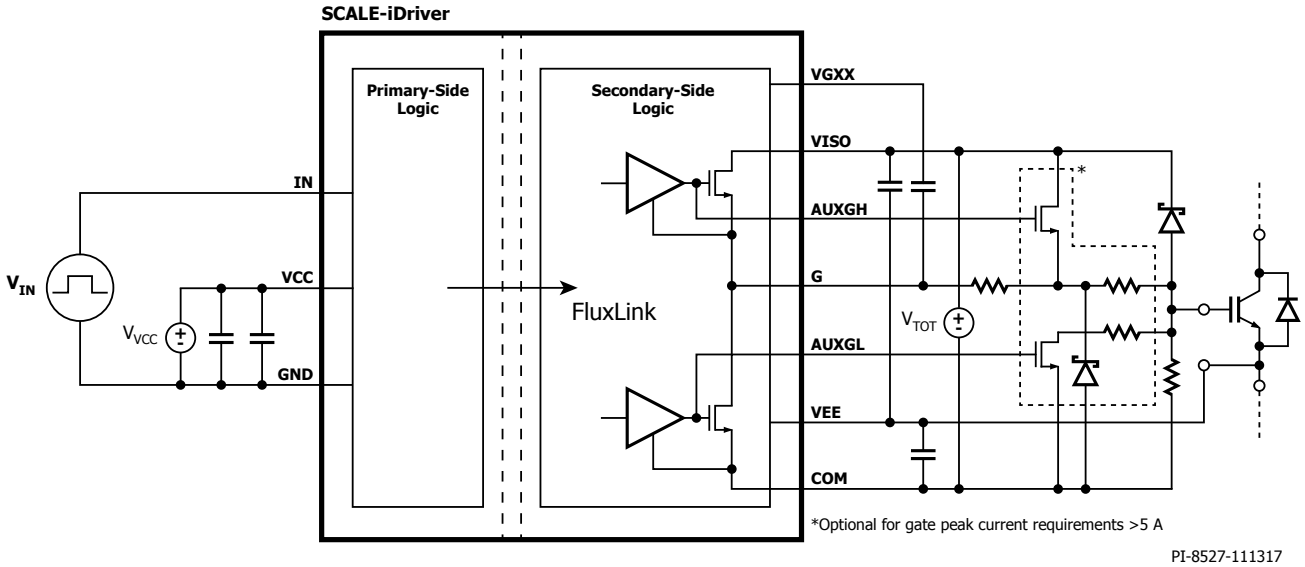


Figure 1. Typical Application Schematic with External n-Channel MOSFET Booster Stage.

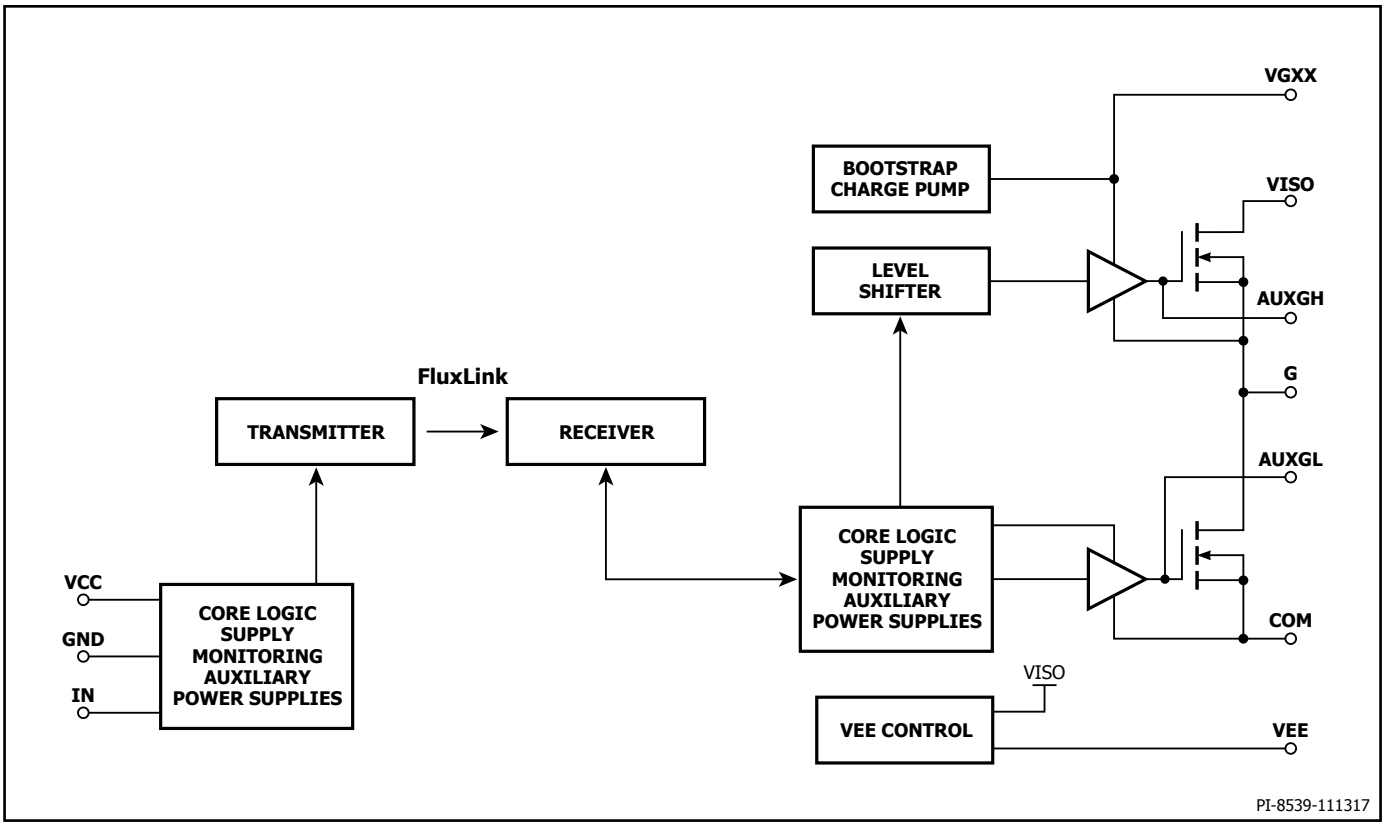


Figure 3. Functional Block Diagram.

Pin Functional Description

VCC Pin (Pin 1)
This pin is the primary-side supply voltage connection.

GND Pin (Pin 3-6)
This pin is the connection for the primary-side ground potential. All primary-side voltages refer to the pin.

IN Pin (Pin 7)
This pin is the input for the logic command signal.

NC Pins (Pin 8, Pin 9)
These pins must be un-connected. Minimum PCB pad size for soldering is required.

VEE Pin (Pin 10)
Common (IGBT emitter/MOSFET source) output supply voltage.

AUXGH Pin (Pin 11)
This pin is the high side driver signal for external n-channel MOSFET booster stage.

VGXX Pin (Pin 12)
This pin is the bootstrap and charge pump supply voltage source.

G Pin (Pin 13)
This pin is the driver output (turn-on/turn-off) connection.

VISO Pin (Pin 14)
This pin is the input for the secondary-side positive supply voltage.

COM Pin (Pin 15)
This pin provides the secondary-side reference potential.

AUXGL Pin (Pin 16)
This pin is the low side driver signal for external n-channel MOSFET booster stage.

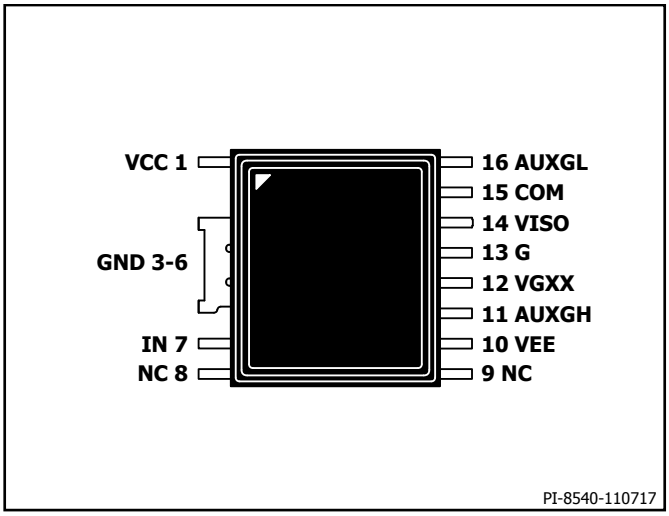


Figure 4. Pin Configuration.

SCALE-iDriver Functional Description

The single channel SCALE-iDriver™ SID1102K drives IGBTs and MOSFETs or other semiconductor power switches with a blocking voltage of up to 1200 V and provides reinforced isolation between micro-controller and the power semiconductor switch.

Command signals are transferred from the primary (IN) to secondary-side via FluxLink isolation technology. The G pin supplies a positive gate voltage and charges the semiconductor gate during the turn-on process. During the turn-off process the G pin supplies the negative voltage and discharges the gate.

Additionally, dedicated AUXGL and AUXGH output pins are available to drive external n-channel MOSFETs as booster stage that can be configured to provide increased peak output gate drive current.

Power Supplies

The SID1102K requires two power supplies. One for the primary-side (V_{VCC}), which powers the primary-side logic and communication with the secondary (insulated) side. The other supply voltage (V_{TOT}) is required for the secondary-side. V_{TOT} is applied between VISO pin and COM pin. V_{TOT} should be insulated from the primary-side and should provide at least the same insulation capabilities as the SCALE-iDriver. V_{TOT} should have a low capacitive coupling to the primary or any other secondary-side. The positive gate-emitter source voltage is provided by V_{VISO}, which is internally generated and stabilized to 15 V (typically) with respect to VEE. The negative gate-emitter source voltage is provided by VEE with respect to COM. Due to the limited current sourcing/sinking capabilities of the VEE pin, any additional load needs to be applied between the VISO and COM pins. No additional load between VISO and VEE pins or between VEE and COM pins is allowed.

Input (Primary-Side)

The input (IN) logic is designed to work directly with micro-controllers using 5 V CMOS logic. If the physical distance between the controller and the SCALE-iDriver is large or if a different logic level is required, the resistive divider in Figure 6 is recommended. This solution adjusts the logic level as necessary and will also improve the driver's noise immunity.

Gate driver commands are transferred from the IN pin to the G pin with a propagation delay $t_{P(LH)}$ and $t_{P(HL)}$.

Output (Secondary-Side)

The gate of the power semiconductor switch should be connected to the SCALE-iDriver output via pin G, using suitable gate resistor R_G as shown in Figure 7.

Note that most power semiconductor data sheets specify an internal gate resistor R_{GINT}, which is already integrated into power semiconductor switch. In addition to R_{GINT}, external resistor device R_G is specified to set-up the gate current level to the application requirements. Careful consideration should be given to the power dissipation and peak current associated with the external gate resistor.

The G pin output current source ($I_{G(H)}$, $I_{G(L)}$) of SID1102K is capable of sinking and sourcing (typically) 5 A at 25 °C. The SCALE-iDriver's internal resistances are described as R_{GHI} and R_{GLI} respectively. If the gate resistor attempts to draw a higher peak current, the peak current will be internally limited to a safe value.

Safe Power-Up and Power-Down

It is recommended during power-up and power-down that the IN pin stays at logic low. Any supply voltage related to VCC, VISO, VEE and VGXX pins should be stabilized using ceramic capacitors C_1, C_2, C_{S1}, C_{S2}, and C_{GXX} respectively as shown in Figure 5 and Figure 7. After supply voltages reach their nominal values, the driver will begin to function after a time delay t_{START}.

Short-Pulse Operation

If command signals applied to the IN pin are shorter than the minimum specified by $t_{GE(MIN)}$, then SID1102K output signals at G, AUXGH, and AUXGL pins will extend to value $t_{GE(MIN)}$. The duration of pulses longer than $t_{GE(MIN)}$ will not be changed.

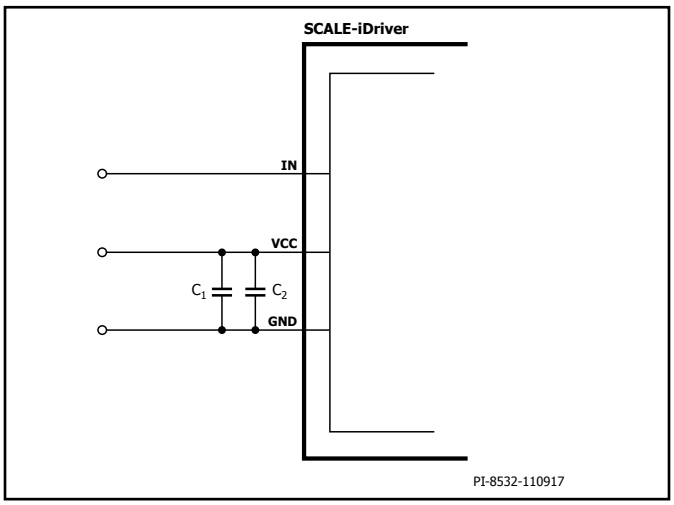


Figure 5. Recommended Circuitry for Standard 5 V IN Logic Level.

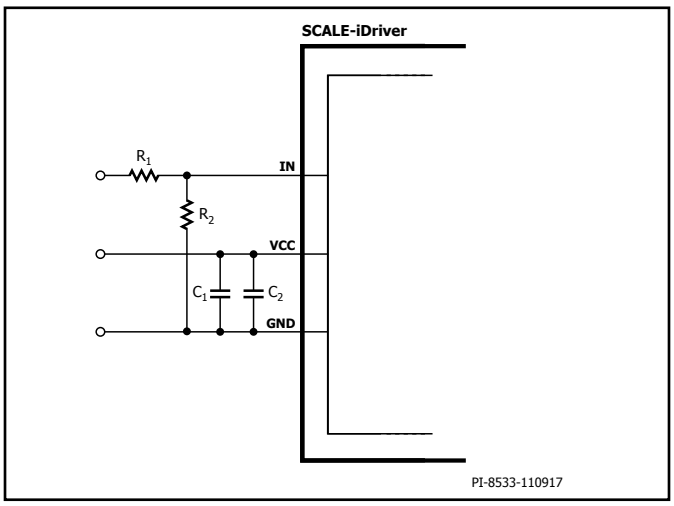


Figure 6. Recommended Circuitry for Increased IN Logic Levels. For R_1 = 3.3 kΩ and R_2 = 1 kΩ the IN Logic Level is 15 V.

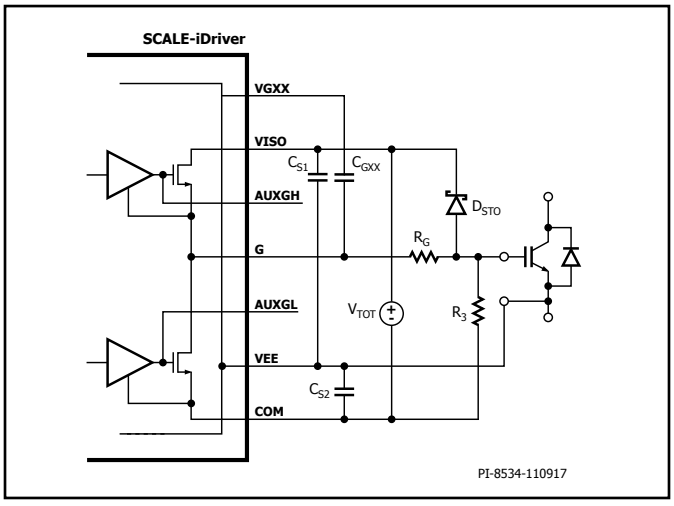


Figure 7. SID1102K without External Booster Stage.

Application Example and Components Selection Without Booster

Figure 5 and Figure 7 show the primary-side and secondary-side schematic and typical components used for SID1102K design without a booster stage, in which the primary-side supply voltage (V_{VCC}) will be connected between VCC and GND pins and supported through supply bypass ceramic capacitors C_1 (4.7 µF typically) and C_2 (470 nF typically). If the command signal voltage level is higher than the rated IN pin voltage, a resistive voltage divider should be used (Figure 6). Additional capacitor C_F can be used to provide input signal filtering as shown in Figure 8. The filter time τ can be calculated according to equation (1):

$$\tau = \frac{R_1 \times R_2}{R_1 + R_2} \times C_F \quad (1)$$

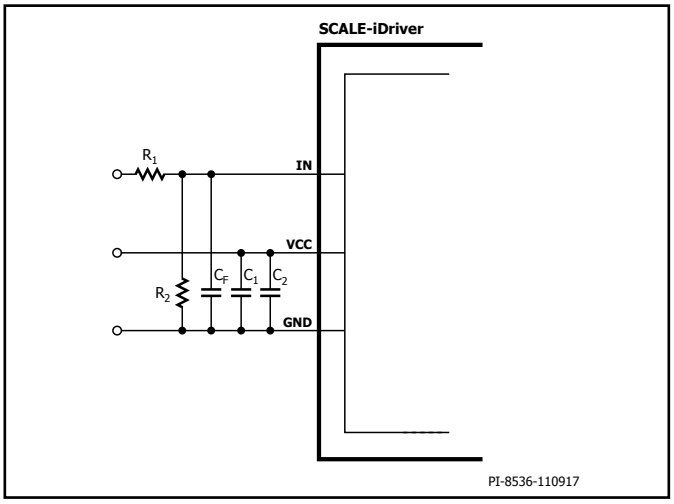


Figure 8. Optional Input Signal Filtering.

The secondary-side isolated power supply (V_{TOT}) is connected between VISO and COM. The positive voltage rail (V_{VISO}) is supported through ceramic capacitor C_{S1}. The negative voltage rail (V_{VEE}) is similarly supported through capacitor C_{S2}. Typically, C_{S1} and C_{S2} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. A 10 nF capacitor C_{GXX} is connected between the G and VGXX pins.

To ensure gate voltage stabilization and collector current limitation during short-circuit the gate is connected to V_{VISO} through Schottky diode D_{STO}.

To avoid parasitic power-switch-conduction during system power-on the gate is connected to COM through 22 kΩ resistor R_3 as shown in Figure 7.

Gate resistors are located physically close to the power semiconductor switch. As these components can get hot, it is recommended that they are placed away from the SCALE-iDriver.

Application Example and Components Selection With Booster

The primary-side can be setup identical as described in the previous section refering to Figure 5 or Figure 6 or Figure 8.

The secondary-side is slightly extended by the booster MOSFETs T_1 and T_2 (BSO220N03MD G for example) and the addition of discrete gate resistors R_{GON} and R_{GOFF} as well as diode D_2 (PMEG4010CEJ for example). All other components can be kept, values might be adapted to the relevant target power semiconductor switching device, such as gate resistors and the supply bypass capacitors C_{S1}, C_{S2}.

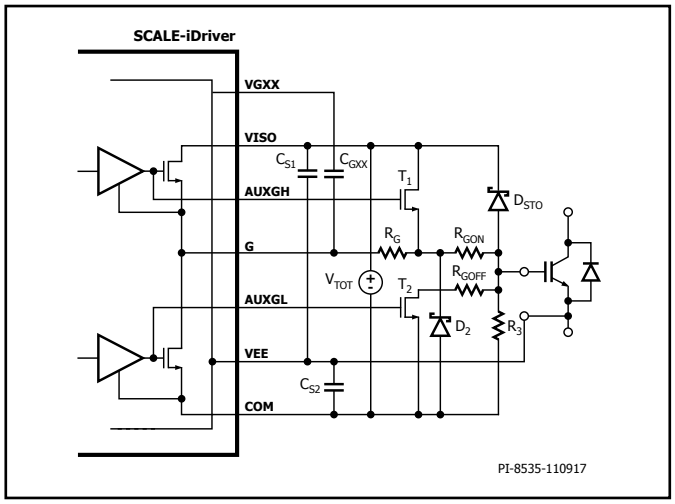


Figure 9. SID1102K with External Boosterstage.

In Off-state (VIN = 0 V) the AUXGL pin provides a positive voltage to the gate terminal of T_2 with reference to the MOSFETs source potential e.g. COM. T_2 conducts the semiconductors gate terminal to COM via R_{GOFF}, providing a negative voltage with reference to VEE to the semiconductors gate (IGBT in this case). The power semiconductor device is off.

When VIN changes from 0 V to 5 V, T_2 is turned off by applying 0 V to the AUXGL pin with reference to COM. At the same time T_1 is turned on by providing a positive gate voltage via AUXGH to the gate of T_1 with reference to G. Since the G pin is connected to V_{TOT} in On-state, the potential of the AUXGH pin needs to be higher than V_{TOT}. This is achieved via SCALE-iDriver's internal charge pump / bootstrap. When T_1 conducts, it provides a positive gate voltage to the power semiconductors gate with reference to VEE. The power semiconductor device is on.

When VIN changes from 5 V to 0 V, it has to be considered, that R_{GON} and R_{GOFF} are paralleled, consequently resulting in a $R_{GOFF} < R_{GON}$ for all chosen. R_G is placed in series to R_{GON} to allow $R_{GOFF} > R_{GON}$.

To ensure that no parasitic turn-on of the power semiconductor switching device occurs when used on the high-side of a half-bridge topology and under worst case switching conditions, the use of the Schottky diode D_2 (PMEG4010CEJ for example) is recommended.

Since the current capability of the VGXX pin is limited, it is recommended to restrict the applicable external N-Channel Booster MOSFETs to those with a gate charge $Q_G \leq 9$ nC for T_1 and $Q_G \leq 5$ nC for T_2.

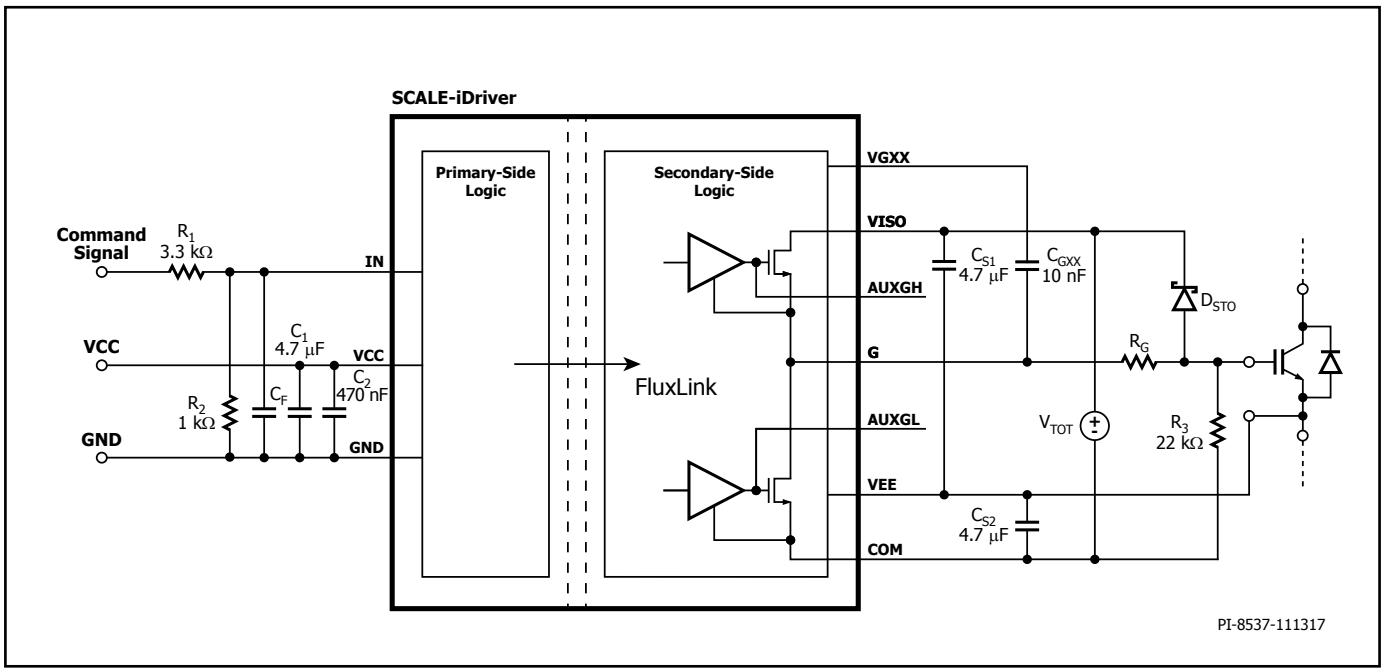


Figure 10. Exemplary Schematic without Booster.

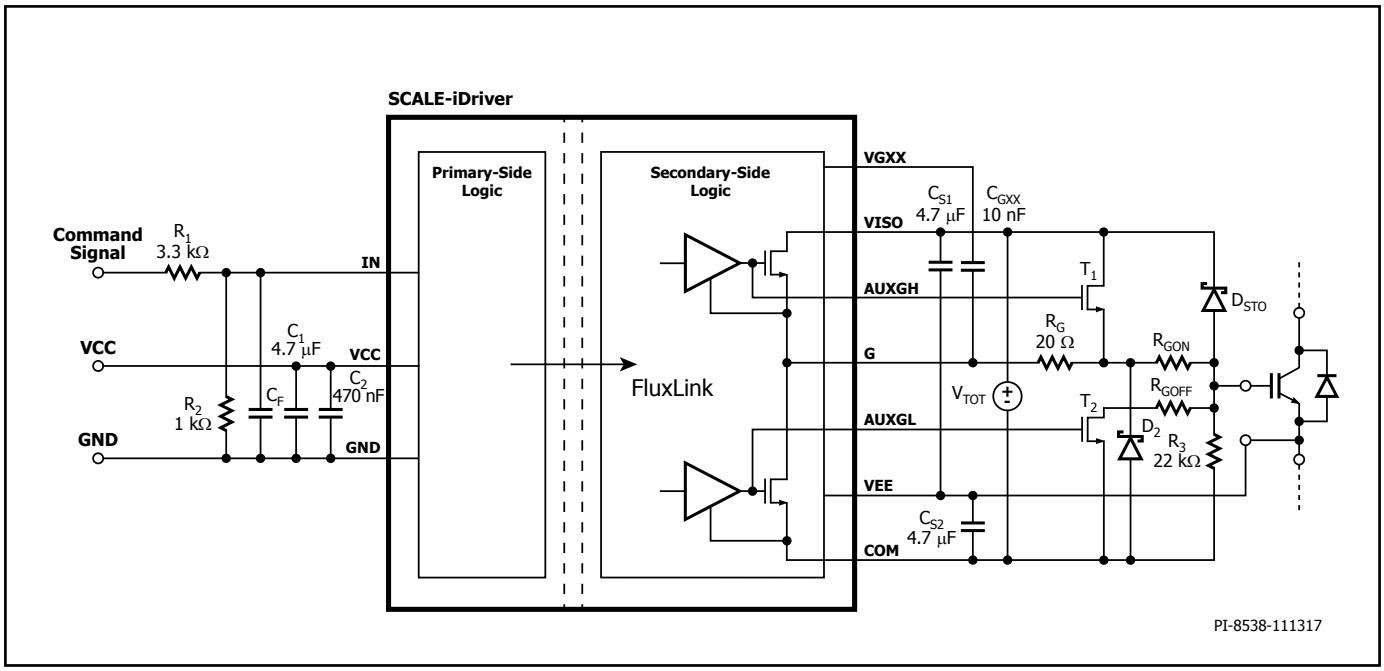


Figure 11. Exemplary Schematic with Booster.

Power Dissipation and IC Junction Temperature Estimation

The following scheme is valid for the SCALE-iDriver without external booster stage. With external booster stage, the majority of losses will be consumed by the MOSFETs of the booster.

First calculation in designing the power semiconductor switch gate driver stage is to calculate the required gate power P_{DRV}. The power is calculated based on equation (2):

$$P_{DRV} = Q_{GATE} \times f_S \times V_{TOT} \quad (2)$$

where,

Q_{GATE} – Controlled power semiconductor switch gate charge (derived for the particular gate potential range defined by V_{TOT}). See semiconductor manufacturer data sheet.

f_S – Switching frequency which is the same as applied to the IN pin of SCALE-iDriver.

V_{TOT} – SCALE-iDriver secondary-side supply voltage.

In addition to P_{DRV}, P_P (primary-side IC power dissipation) and P_{SNL} (secondary-side IC power dissipation without capacitive load) must be considered. Both are ambient temperature and switching frequency dependent (see typical performance characteristics).

$$P_P = V_{VCC} \times I_{VCC} \quad (3)$$

$$P_{SNL} = V_{TOT} \times I_{VISO} \quad (4)$$

During operation, the P_{DRV} power is shared between the external gate resistor R_G, the internal gate resistor R_{GINT}, of the power switch (if available) and internal driver resistances R_{GHI} and R_{GLI}. For junction temperature estimation purposes, the dissipated power under load (P_{OL}) inside the IC can be calculated according to equation (5):

$$P_{OL} = 0.5 \times Q_{GATE} \times f_S \times V_{TOT} \times \left(\frac{R_{GHI}}{R_{GHI} + R_{GX}} + \frac{R_{GLI}}{R_{GLI} + R_{GX}} \right) \quad (5)$$

R_{GX} represents the sum of external (R_G) and power semiconductor internal gate resistance (R_{GINT}):

$$R_{GX} = R_G + R_{GINT} \quad (6)$$

Total power dissipation (P_{DIS}) is estimated as sum of equations (3), (4) and (5):

$$P_{DIS} = P_P + P_{SNL} + P_{OL} \quad (7)$$

The operating junction temperature (T_J) for given ambient temperature (T_A) can be estimated according to equation (8):

$$T_J = \theta_{JA} \times P_{DIS} + T_A \quad (8)$$

Table 2 describes the recommended component characteristics and layout requirements to achieve optimum performances of SCALE-iDriver without external n-channel MOSFET booster.

Pin	Return to Pin	Recommended Value	Symbol	Notes
VCC	GND	4.7 µF 470 nF	C_1 C_2	VCC blocking capacitors C_1 and C_2 must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C_1 X7R / 25 V / 10% in a 1206 package is recommended. For C_2 X7R / 25 V / 10% in a 0608 package is recommended.
Command Signal	IN	Application specific	R_1	Needed if command signals >5 V are used. For 15 V input logic the value of Figure 10 e.g. 3.3 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
IN	GND	Application specific	R_2	Needed if command signals >5 V are used. For 15 V input logic the value of Figure 10 e.g. 1 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
IN	GND	Application specific	C_F	See equation 1. The use of NP0, C0G / 50 V / 5% in 0603 package is recommended.
VISO	VEE	Application specific	C_{S1}	C_{S1} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VEE	COM	Application specific	C_{S2}	C_{S2} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VGXX	G	10 nF	C_{GXX}	To avoid misoperation, this pin should not be connected to anything else. This capacitor needs to be as close to IC pins as possible. The use of X7R / 25 V / 10% in 0603 package is recommended.
VISO	Power semiconductor gate	Schottky diode	D_{STO}	To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to the VISO pin through the Schottky diode D_{STO}. D_{STO} should be connected close to capacitor C_{S1} as well as the power semiconductor gate. Enlarged loop could result in increased short-circuit current. The use of NXP PMEG4050ETP is recommended
G	Power semiconductor gate	Application specific	R_G	As this component gets hot, it shall be ensured that it is placed not too close to SID1102K.
COM	Power semiconductor gate	22 kΩ	R_3	To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 22 kΩ. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.

Table 2. PCB Layout and Component Guidelines without External n-Channel MOSFET Booster.

Table 3 describes the recommended component characteristics and layout requirements to achieve optimum performances of SCALE-iDriver with external n-channel MOSFET booster.

Pin	Return to Pin	Recommended Value	Symbol	Notes
VCC	GND	4.7 µF 470 nF	C_1 C_2	VCC blocking capacitors C_1 and C_2 must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C_1 X7R / 25 V / 10% in a 1206 package is recommended. For C_2 X7R / 25 V / 10% in a 0608 package is recommended.
Command Signal	IN	Application specific	R_1	Needed if command signals >5 V are used. For 15 V input logic the value of Figure 11 e.g. 3.3 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
IN	GND	Application specific	R_2	Needed if command signals >5 V are used. For 15 V input logic the value of Figure 11 e.g. 1 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
IN	GND	Application specific	C_F	See equation 1. The use of NP0, C0G / 50 V / 5% in 0603 package is recommended.
VISO	VEE	Application specific	C_{S1}	C_{S1} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VEE	COM	Application specific	C_{S2}	C_{S2} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. The use of X7R / 25 V /10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VGXX	G	10 nF	C_{GXX}	To avoid misoperation, this pin should not be connected to anything else. This capacitor needs to be as close to IC pins as possible. The use of X7R / 25 V / 10% in 0603 package is recommended.
VISO	Power semiconductor gate	Schottky diode	D_{STO}	To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to the VISO pin through the Schottky diode D_{STO}. D_{STO} should be connected close to capacitor C_{S1} as well as the power semiconductor gate. Enlarged loop could result in increased short-circuit current. The use of NXP PMEG4050ETP is recommended.
G	Source Terminal T_1	20 Ω	R_G	Gate Resistor needed to provide a higher gate resistance for turn-off than for turn-on 20 Ω is recommended also to avoid oscillations. The use of 1% / 0.25 W / 200 V / CRCWe3 in 1206 package is recommended.

Table 3. PCB Layout and Component Guidelines with External n-Channel MOSFET Booster.

VISO	R_{GON}	n-channel MOSFET	T_1	Turn-on switch of external booster stage.
R_{GOFF}	COM	n-channel MOSFET	T_2	Turn-off switch of external booster stage.
R_{GON}	COM	Schottky diode	D_2	To ensure that no parasitic turn-on of the power semiconductor switching device occurs when used on the high-side of a half-bridge under worst-case switching conditions. The use of NXP PMEG4010CEJ is recommended.
Source Terminal T_1	Power semiconductor gate	Application specific	R_{GON}	As this component gets hot, it shall be ensured that it is placed not too close to SID1102K.
Drain Terminal T_2	Power semiconductor gate	Application specific	R_{GOFF}	As this component gets hot, it shall be ensured that it is placed not too close to SID1102K.
COM	Power semiconductor gate	22 kΩ	R_3	To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 22 kΩ resistor. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.

Table 3. PCB Layout and Component Guidelines with External n-Channel MOSFET Booster (cont.).

Parameter	Symbol	Conditions	Min	Max	Units
Absolute Maximum Ratings[1]					
Primary-Side Supply Voltage[2]	V_{VCC}	VCC to GND	-0.5	6.5	V
Secondary-Side Total Supply Voltage	V_{TOT}	VISO to COM	-0.5	30	V
Secondary-Side Positive Supply Voltage	V_{VISO}	VISO to VEE	-0.5	17.5	V
Secondary-Side Negative Supply Voltage	V_{VEE}	VEE to COM	-0.5	15	V
Logic Input Voltage (command signal)	V_{IN}	IN to GND	-0.5	V_{VCC} + 0.5	V
Switching Frequency	f_S			75	kHz
Storage Temperature	T_S		-65	150	°C
Operating Junction Temperature	T_J		-40	150[3]	°C
Operating Ambient Temperature	T_A		-40	125	°C
Operating Case Temperature	T_C		-40	125	°C
Input Power Dissipation[4]	P_P	V_{VCC} = 5 V, V_{TOT} = 28 V, T_A = 25 °C f_S = 75 kHz		115	mW
Output Power Dissipation[4]	P_S			1675	
Total IC Power Dissipation	P_{DJS}			1790	mW

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Defined as peak voltage measured directly on VCC pin.
3. Transmission of command signals could be affected by PCB layout parasitic inductances at junction temperatures higher than recommended.
4. Input Power Dissipation refers to equation (3). Output Power Dissipation is secondary-side IC power dissipation without capacitive load (P_{SNL}, equation (4)) and dissipated power under load (P_{OL}, equation (5)). Total IC power dissipation is sum of P_P and P_S.

Thermal Resistance

Thermal Resistance: eSOP-R16B Package:

(θ_{JA}) ..... 67 °C/W[1]

(θ_{JC}) ..... 34 °C/W[2]

Notes:

1. 2 oz. (610 g/m^2) copper clad.
2. The case temperature is measured at the plastic surface at the top of the package.

Parameter	Symbol	Conditions T_J = -40 °C to 125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Recommended Operation Conditions						
Primary-Side Supply Voltage	V_{VCC}	VCC - GND	4.75		5.25	V
Secondary-Side Total Supply Voltage	V_{TOT}	VISO - COM	22		28	V
Logic Low Input Voltage	V_{IL}				0.5	V
Logic High Input Voltage	V_{IH}		3.3			V
Switching Frequency	f_S		0		75	kHz
Operating IC Junction Temperature	T_J		-40		125	°C
Gate Charge of External Turn-On N-Channel-MOSFET T_1	$Q_{G,AUXGH}$	0 V ≤ V_{AUXGH} ≤ 10 V referenced to G See Note 8			9	nC
Gate Charge of External Turn-Off N-Channel-MOSFET T_2	$Q_{G,AUXGL}$	0 V ≤ V_{AUXGL} ≤ 6 V referenced to COM See Note 8			5	nC
Electrical Characteristics						
Logic Low Input Threshold Voltage (Referenced to GND)	V_{IN+LT}		0.6	1.25	1.8	V
Logic High Input Threshold Voltage (Referenced to GND)	V_{IN+HT}		1.7	2.2	3.05	V
Logic Input Voltage Hysteresis	V_{IN+HS}		0.1			V
Input Bias Current	I_{IN}	V_{IN} = 5 V	56	113	165	µA
Supply Current (Primary-Side)	I_{VCC}	V_{IN} = 0 V			17	mA
		V_{IN} = 5 V			23	
		f_S = 20 kHz			20	
		f_S = 75 kHz			23	
Supply Current (Secondary-Side)	I_{VISO}	V_{IN} = 0 V			8	mA
		V_{IN} = 5 V			9	
		f_S = 20 kHz			10	
		f_S = 75 kHz			14	
Power Supply Monitoring Threshold (Primary-Side) (Referenced to GND)	$UVLO_{VCC}$	Clear Fault		4.28	4.65	V
		Set Fault	3.85	4.12		
		Hysteresis	0.02			
Power Supply Monitoring Threshold (Secondary-Side, Positive Rail V_{VISO}) (Referenced to VEE)	$UVLO_{VISO}$	Clear Fault		12.85	13.5	V
		Set Fault	11.7	12.35		
		Hysteresis	0.3			

Parameter	Symbol	Conditions T_J = -40 °C to 125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
Power Supply Monitoring Threshold (Secondary-Side, Negative Rail V_{VEE}) (Referenced to COM)	$UVLO_{VEE}$	Clear Fault, V_{TOT} = 20 V		5.15	5.5	V
		Set Fault, V_{TOT} = 20 V	4.67	4.93		
		Hysteresis	0.1			
Secondary-Side Positive Supply Voltage Regulation (Referenced to VEE)	$V_{VISO(HS)}$	22 V ≤ V_{TOT} ≤ 28 V, |i(VEE)| ≤ 1.5 mA	14.4	15.07	15.75	V
VEE Source Capability	$I_{VEE(SO)}$	V_{TOT} = 15 V, V_{VEE} set to 0 V	0.1			mA
		V_{TOT} = 25 V, V_{VEE} set to 7.5 V See Note 9	1.85	3.3	4.5	
VEE Sink Capability	$I_{VEE(SI)}$	V_{TOT} = 25 V, V_{VEE} set to 12.5 V	1.74	3.1	4.5	mA
Turn-On Propagation Delay	$t_{P(LH)}$	T_J = 25 °C See Note 3	190	262	350	ns
		T_J = 125 °C See Note 3	210	285	364	
Turn-Off Propagation Delay	$t_{P(HL)}$	T_J = 25 °C See Note 4	190	262	350	ns
		T_J = 125 °C See Note 4	211	289	359	
Minimum Turn-On and Off Pulses	$t_{GE(MIN)}$	See Note 8			650	ns
Output Rise Time	t_R	No C_G See Note 5		29	45	ns
		C_G = 10 nF See Note 5	120	145	175	
		C_G = 47 nF See Note 5	600	675	790	
Output Fall Time	t_F	No C_G See Note 6		14	45	ns
		C_G = 10 nF See Note 6	113	138	163	
		C_G = 47 nF See Note 6	580	655	790	

Parameter	Symbol	Conditions T_J = -40 °C to 125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
Propagation Delay Jitter		See Note 8		±5		ns
Power-On Start-Up Time	t_{START}	See Note 7			10	ms
Gate Sourcing Peak Current	$I_{G(H)}$	$V_{GH} \geq V_{TOT}$ - 8.8 V C_G = 470 nF See Note 9	2.7	3.3	4	A
		R_G = 0 Ω, C_G = 47 nF T_J = 25 °C See Notes 2, 8, 9		5		
Gate Sinking Peak Current	I_{GL}	$V_{GL} \leq$ 7.5 V C_G = 470 nF V_{GL} is Referenced to COM	3	3.55	4	A
		R_G = 0 Ω, C_G = 47 nF T_J = 25 °C See Notes 2, 8		5		
Turn-On Internal Gate Resistance	R_{GHI}	I_G = -250 mA V_{IN}= 5 V See Note 9		1.05	1.7	Ω
Turn-Off Internal Gate Resistance	R_{GLI}	I_G = 250 mA V_{IN} = 0 V See Note 9		1	1.7	Ω
Turn-On Gate Output Voltage (Referenced to COM)	V_{GH}	I_G = 20 mA V_{IN} = 5 V	V_{TOT}-0.05			V
Turn-Off Gate Output Voltage (Referenced to COM)	V_{GL}	I_G = 20 mA V_{IN} = 0 V			0.05	V
Auxiliary High-Side Gate High Level Output Voltage (Referenced to G)	V_{AUXGH}	IN = 5 V, V_{TOT} = 25 V	7	9.5	12.5	V
Auxiliary Low-Side Gate High Level Output Voltage (Referenced to COM)	V_{AUXGL}	IN = 0 V, V_{TOT} = 25 V	4	5.25	6.75	V

Parameter	Symbol	Conditions T_J = -40 °C to 125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Package Characteristics (See Notes 8, 10)						
Distance Through the Insulation	DTI	Minimum Internal Gap (Internal Clearance)	0.4			mm
Minimum Air Gap (Clearance)	L1 (IO1)	Shortest Terminal-to-Terminal Distance Through Air	9.5			mm
Minimum External Tracking (Creepage)	L2 (IO2)	Shortest Terminal-to-Terminal Distance Across the Package Surface	9.5			mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN EN 60112 (VDE 0303-11): 2010-05 EN / IEC 60112:2033 + A1:2009	600			
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C	10^{12}			Ω
		V_{IO} = 500 V 100 °C ≤ T_J ≤ $T_{C(MAX)}$ See Note 12	10^{11}			
Isolation Capacitance, Input to Output	C_{IO}	See Note 12		1		pF
Package Insulation Characteristics						
Maximum Working Isolation Voltage	V_{IOWM}				1000	V_{RMS}
Maximum Repetitive Peak Isolation Voltage	V_{IORM}				1414	V_{PEAK}
Input to Output Test Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PR} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC			2263	V_{PEAK}
		Method A, After Input/Output Safety Test Subgroup 2/3, V_{PR} = 1.2 x V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC			1697	
		Method B1, 100% Production Test, V_{PR} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC			2652	
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification), t = 1 s (100% production)			8000	V_{PEAK}
Insulation Resistance	R_S	V_{IO} = 500 V at T_S			>10^9	Ω
Maximum Case Temperature	T_S				150	°C
Safety Total Dissipated Power	P_S	T_J = 25 °C			1.79	W
Pollution Degree				2		
Climatic Classification				40/125/21		
Withstanding Isolation Voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production)		5000		V_{RMS}

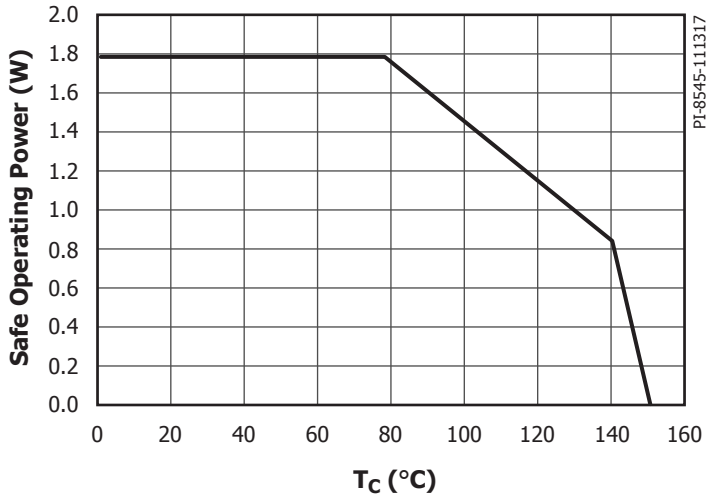


Figure 12. Thermal Derating Curve Showing Dependence of Limited Dissipated Power on Case Temperature (DIN V VDE V 0884-10).

Operation is allowed until T_J and/or T_C of 125 °C are reached. Thermal stress beyond those values but below thermal derating curve may lead to permanent functional product damage. Operating beyond thermal SOP derating curve may affect product reliability.

NOTES:

1. V_{VCC} = 5 V, V_{TOT} = 25 V. R_G = 5.6 Ω, no C_G, without external booster stage. The VGXX pin is connected to the G pin through a 10 nF capacitor. Typical values are defined at T_A = 25 °C; f_S = 20 kHz, Duty Cycle = 50%. Positive currents are assumed to be flowing into pins.
2. Pulse width ≤ 10 µs, duty cycle ≤ 1%. The maximum value is controlled by the ASIC to a safe level. The internal peak power is safely controlled for R_G ≥ 0 and power semiconductor module input gate capacitance C_{IES} ≤ 47 nF.
3. V_{IN} potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on IN pin to 10% voltage increase on G pin.
4. V_{IN} potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on IN pin to 10% voltage decrease on G pin.
5. Measured from 10% to 90% of V_{GE} (C_G simulates semiconductor gate capacitance). The V_{GE} is measured across C_G.
6. Measured from 90% to 10% of V_{GE} (C_G simulates semiconductor gate capacitance). The V_{GE} is measured across C_G.
7. The amount of time after primary and secondary-side supply voltages (V_{VCC} and V_{TOT}) reach minimal required level for driver proper operation. No signal is transferred from primary to secondary-side during that time.
8. Guaranteed by design.
9. Positive current is flowing out of the pin.
10. Safety distances are application dependent and the creepage and clearance requirements should follow specific equipment isolation standards of an application. Board design should ensure that the soldering pads of an IC maintain required safety relevant distances.
11. Measured accordingly to IEC 61000-4-8 (f_S = 50 Hz, and 60 Hz) and IEC 61000-4-9.
12. All pins on each side of the barrier tied together creating a two-terminal device.

Typical Performance Characteristics

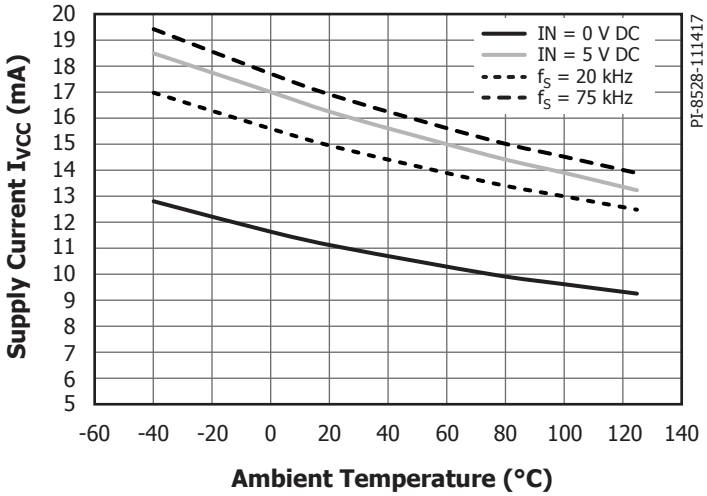


Figure 13. Supply Current Primary-Side I_{VCC} vs. Ambient Temperature. Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, No-Load.

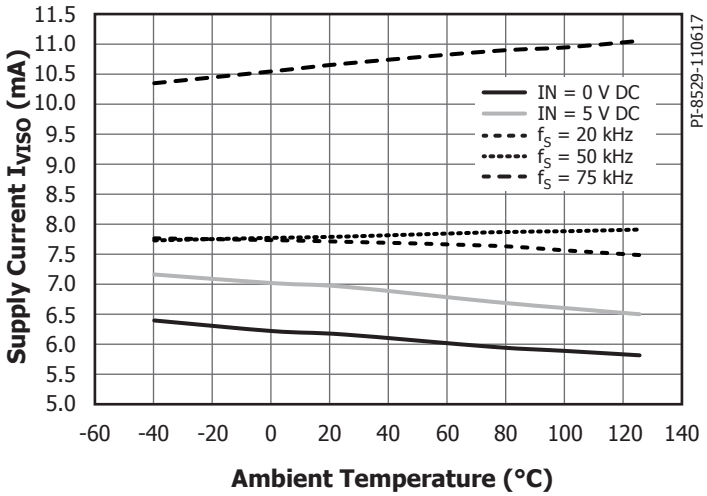


Figure 14. Supply Current Secondary-Side I_{VISO} vs. Ambient Temperature Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, No-Load.

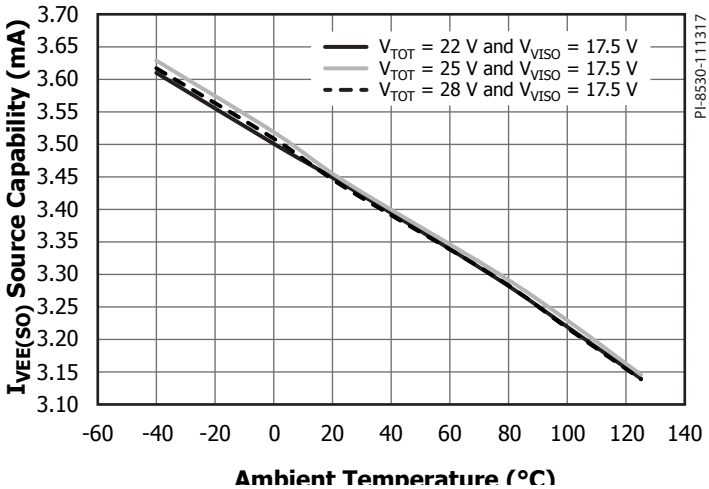


Figure 15. VEE Source Capability $I_{VEE(SO)}$ vs. Ambient Temperature and V_{TOT}. Conditions: V_{VCC} = 5 V, f_S = 20 kHz, Duty Cycle = 50%.

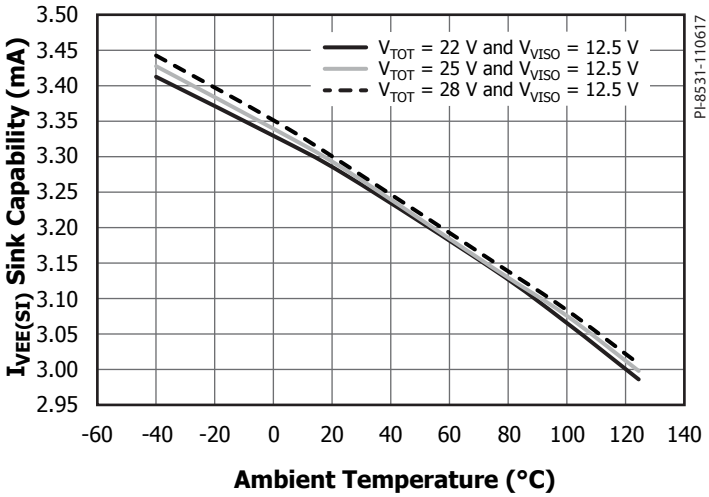
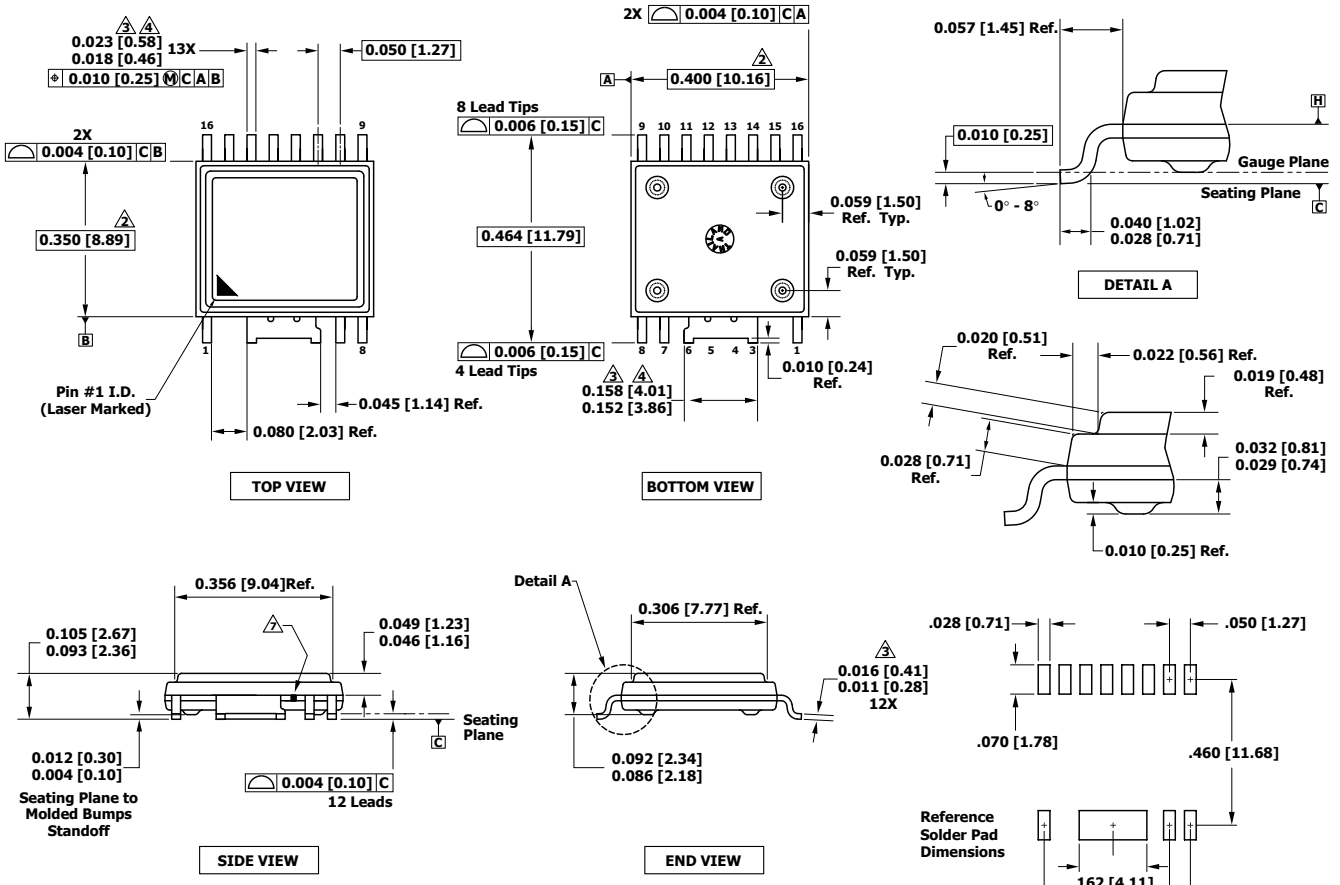


Figure 16. VEE Sink Capability $I_{VEE(SI)}$ vs. Ambient Temperature and V_{TOT}. Conditions: V_{VCC} = 5 V, f_S = 20 kHz, Duty Cycle = 50%.

eSOP-R16B



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

PI-6995-051716
POD-eSOP-R16B Rev B

MSL Table

Part Number	MSL Rating
SID1102K	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	JESD22-A114F	> ±2000 V on all pins
Charged Device Model ESD	JESD22-C101	> ±500 V on all pins

IEC 60664-1 Rating Table

Parameter	Conditions	Specifications
Basic Isolation Group	Material Group	I
Installation Classification	Rated mains voltage ≤ 150 V_{RMS}	I - IV
	Rated mains voltage ≤ 300 V_{RMS}	I - IV
	Rated mains voltage ≤ 600 V_{RMS}	I - IV
	Rated mains voltage ≤ 1000 V_{RMS}	I - III

Electrical Characteristics (EMI) Table

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Common-Mode Transient Immunity, Logic High	CM_H	Typical values measured according to Figure 17 and Figure 18. Maximum values are design values assuming trapezoid waveforms.		-35 / 50	-100 / 100	kV/µs
Common-Mode Transient Immunity, Logic Low	CM_L	Typical values measured according to Figure 17 and Figure 18. Maximum values are design values assuming trapezoid waveforms.		-35 / 50	-100 / 100	kV/µs
Variable Magnetic Field Immunity	H_{HPEAK}	See Note 11		1000		A/m
	H_{LPEAK}	See Note 11		1000		

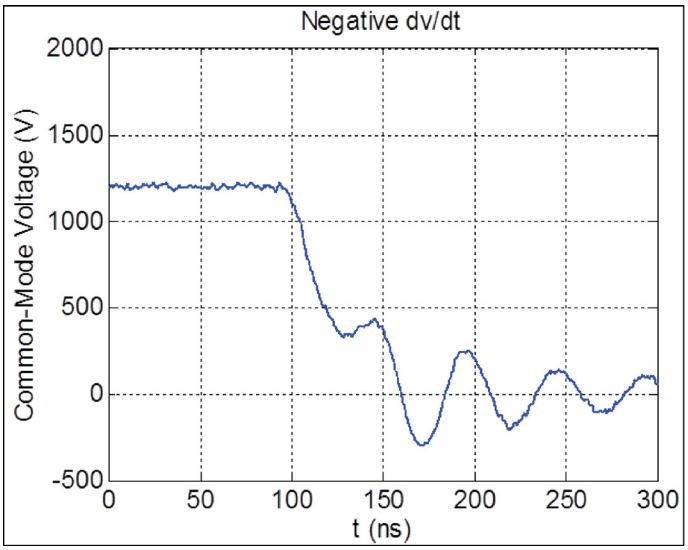


Figure 17. Applied Common Mode Pulses for Generating Negative dv/dt.

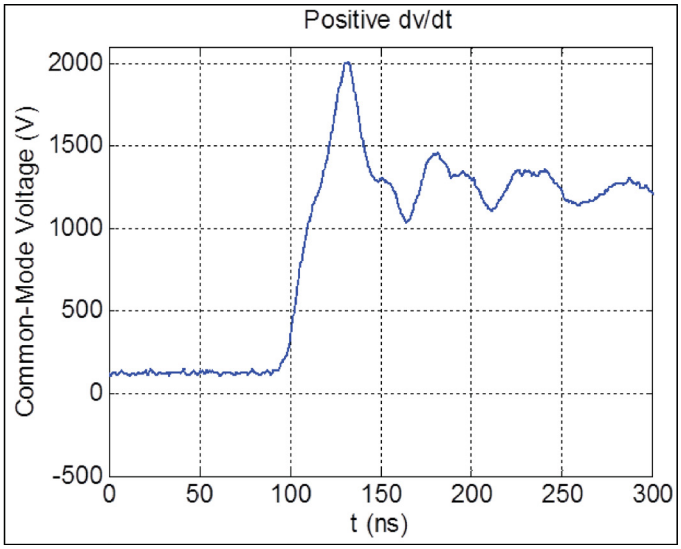
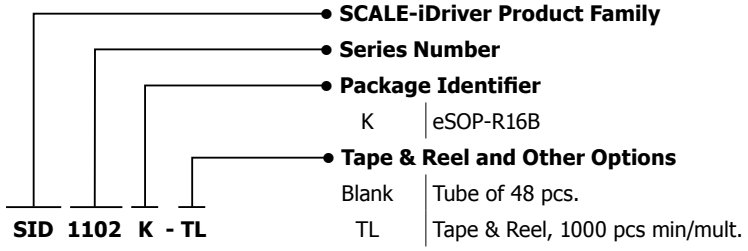


Figure 18. Applied Common Mode Pulses for Generating Positive dv/dt.

Regulatory Information Table

VDE	UL	CSA
Certified to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	UR recognized under UL1577 Component Recognition Program	UR recognized to CSA Component Acceptance Notice 5A
Reinforced insulation for Max. Transient Isolation voltage 8 kV_{PEAK}, Max. Surge Isolation voltage 8 kV_{PEAK}, Max. Repetitive Peak Isolation voltage 1414 V_{PEAK}	Single protection, 5000 V_{RMS} dielectric voltage withstand	Single protection, 5000 V_{RMS} dielectric voltage withstand
File No. 40044363	File No. E358471	File No. E358471

Part Ordering Information



Revision	Notes	Date
C	Code A.	11/17
D	Updated with UL approval information on page 1 and Regulatory Information table on page 19.	05/18

For the latest updates, visit our website: www.power.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at www.power.com/ip.htm.

Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Lindwurmstrasse 114
D-80337 München
Germany
Phone: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com

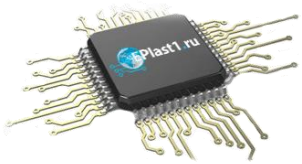
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.