IS61LF102436A IS61VF102436A
IS61LF204818A IS61VF204818A

1M x 36, 2M x 18
36Mb SYNCHRONOUS FLOW-THROUGH STATIC RAM

APRIL 2008

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply

  LF: V_{DD} 3.3V ± 5%, V_{DDQ} 3.3V/2.5V ± 5%

  VF: V_{DD} 2.5V ± 5%, V_{DDQ} 2.5V ± 5%
- JEDEC 100-Pin TQFP and 165-pin PBGA packages.
- Lead-free available

DESCRIPTION

The *ISSI* IS61LF/VF102436A and IS61LF/VF204818A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LF/VF102436A is organized as 1,048,476 words by 36 bits. The IS61LF/VF204818A is organized as 2M-words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$) input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

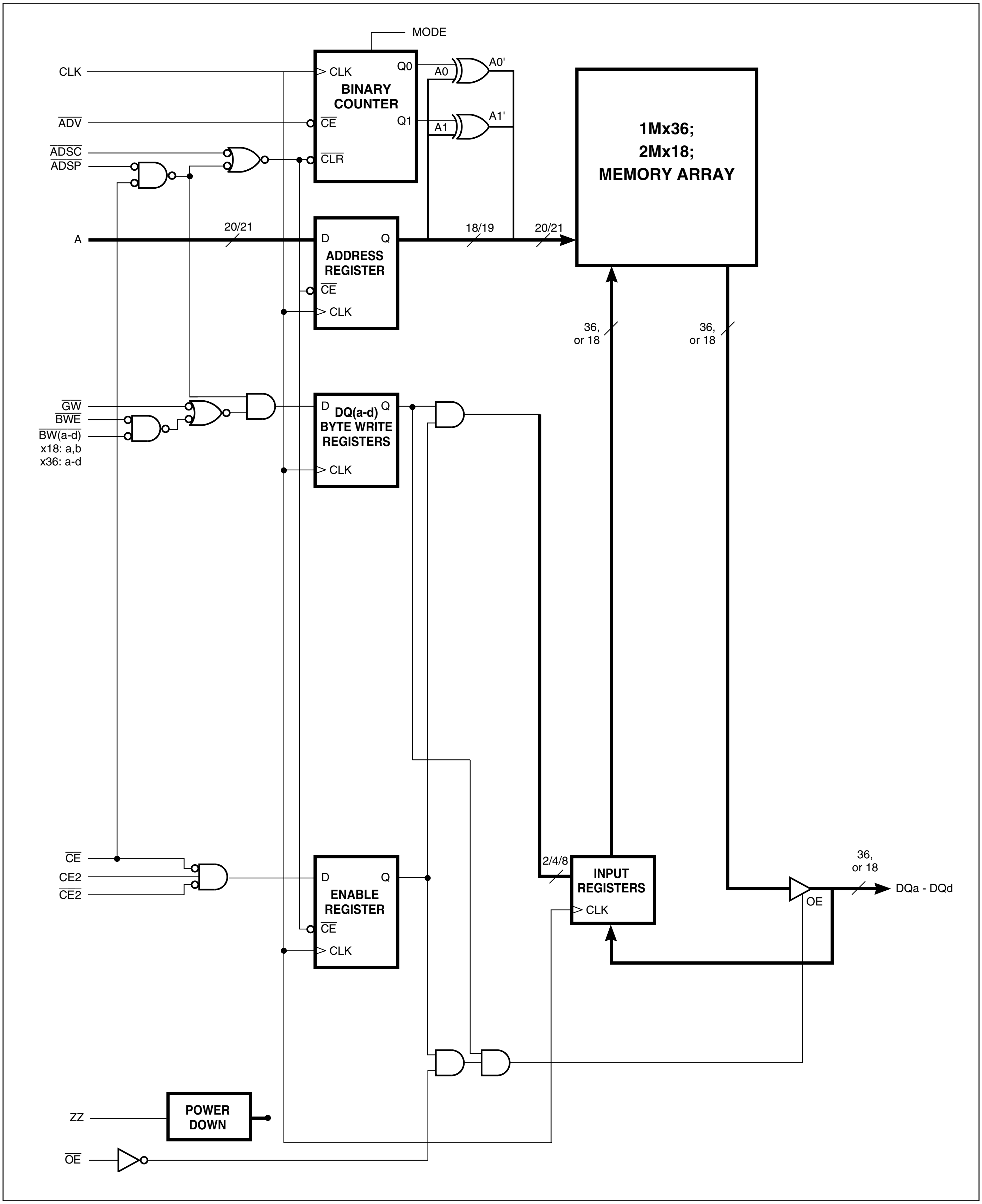
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

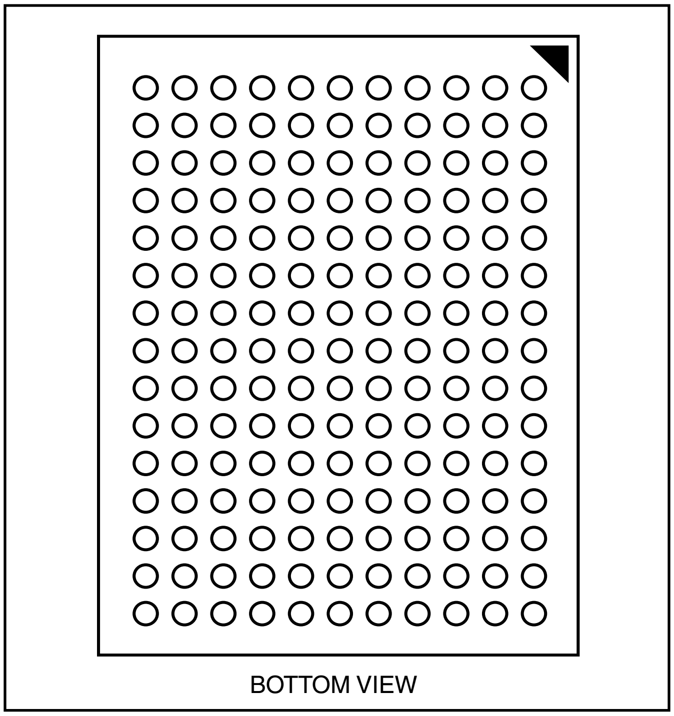
Symbol	Parameter	-6.5	-7.5	Units
t_{KQ}	Clock Access Time	6.5	7.5	ns
t_{KC}	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

BLOCK DIAGRAM



165-PIN BGA

165-Ball, 13x15 mm BGA



165 PBGA PACKAGE PIN CONFIGURATION

1M x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CE}}$	$\overline{\text{BWc}}$	$\overline{\text{BWb}}$	$\overline{\text{CE2}}$	$\overline{\text{BWE}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	NC
B	NC	A	CE2	$\overline{\text{BWd}}$	$\overline{\text{BWa}}$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC
C	DQPc	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
H	NC	NC	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	Vss	NC	A	NC	Vss	VDDQ	NC	DQPa
P	NC	NC	A	A	NC	A1*	NC	A	A	A	A
R	MODE	A	A	A	NC	A0*	NC	A	A	A	A

Note: * A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
(Under Evaluation)

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{\text{ADV}}$	Synchronous Burst Address Advance.
$\overline{\text{ADSP}}$	Address Status Processor
$\overline{\text{ADSC}}$	Address Status Controller
$\overline{\text{GW}}$	Global Write Enable
CLK	Synchronous Clock
$\overline{\text{CE}}$, $\overline{\text{CE2}}$, CE2	Synchronous Chip Select
$\overline{\text{BW}}$x (x=a,b,c,d)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{\text{BWE}}$	Byte Write Enable
$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Data Inputs/Outputs
VDD	Power Supply
VDDQ	Output Power Supply
Vss	Ground

165 PBGA PACKAGE PIN CONFIGURATION

2M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CE}}$	$\overline{\text{BWb}}$	NC	$\overline{\text{CE2}}$	$\overline{\text{BWE}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	A
B	NC	A	CE2	NC	$\overline{\text{BWa}}$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
H	NC	NC	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	A	NC	Vss	VDDQ	NC	NC
P	NC	NC	A	A	NC	A1*	NC	A	A	A	A
R	MODE	A	A	A	NC	A0*	NC	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired. (Under Evaluation)

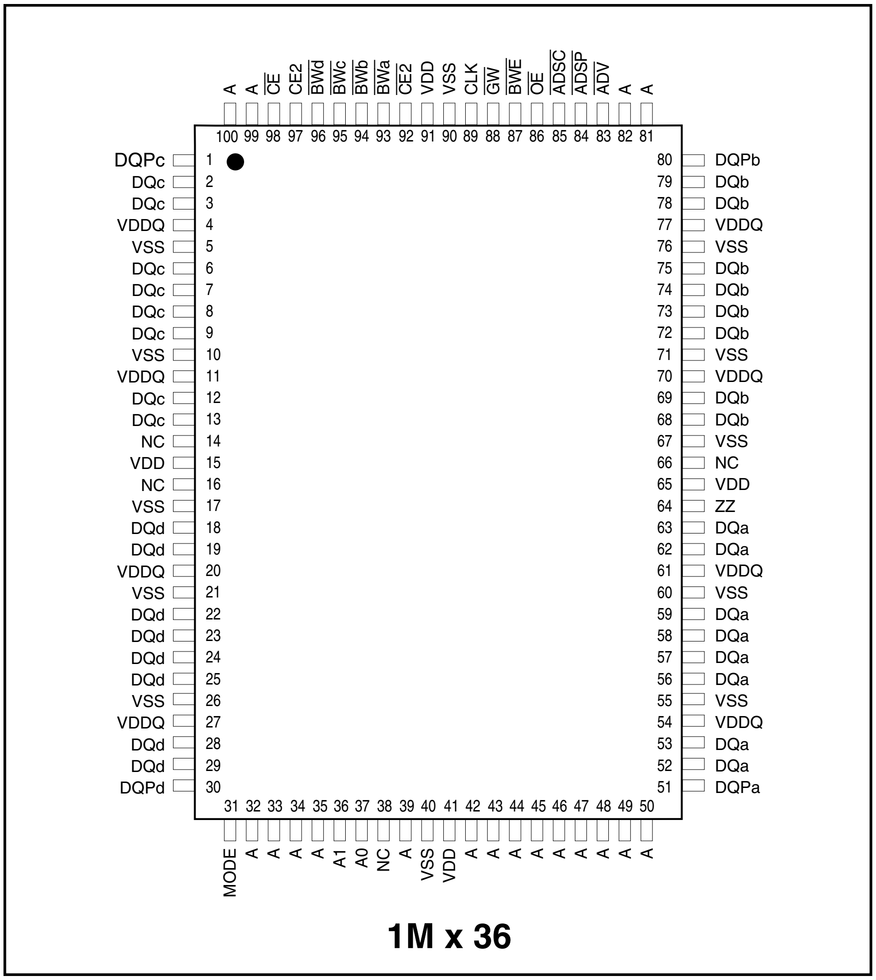
PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{\text{ADV}}$	Synchronous Burst Address Advance.
$\overline{\text{ADSP}}$	Address Status Processor
$\overline{\text{ADSC}}$	Address Status Controller
$\overline{\text{GW}}$	Global Write Enable
CLK	Synchronous Clock
$\overline{\text{CE}}$, $\overline{\text{CE2}}$, CE2	Synchronous Chip Select
$\overline{\text{BWx}}$ (x=a,b)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{\text{BWE}}$	Byte Write Enable
$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Data Inputs/Outputs
VDD	Power Supply
VDDQ	Output Power Supply
Vss	Ground

PIN CONFIGURATION

100-Pin TQFP



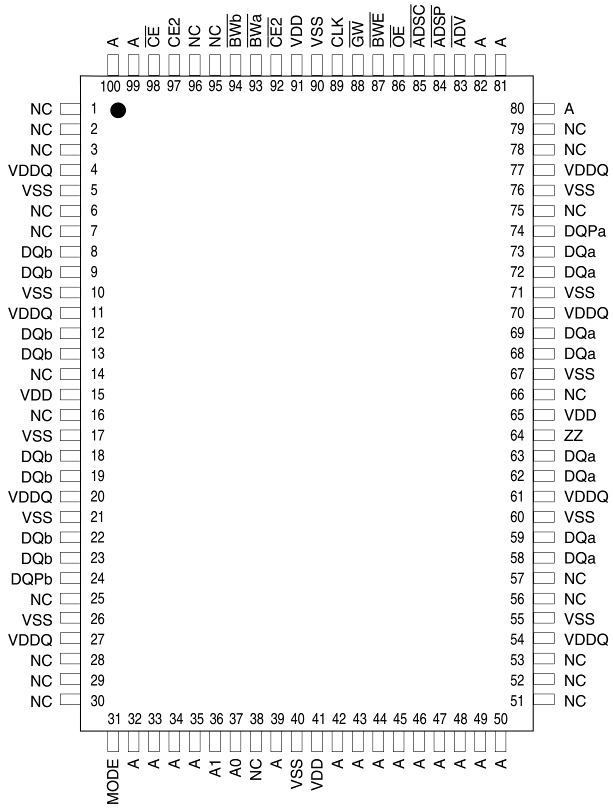
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWa}}$-$\overline{\text{BWd}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable
$\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQd	Synchronous Data Input/Output

DQPa-DQPd	Parity Data Input/Output
Vss	Ground
$\overline{\text{GW}}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{\text{OE}}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

100-Pin TQFP



2M x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWa}}$-$\overline{\text{BWb}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable
$\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Input/Output
DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
V_{SS}	Ground
$\overline{\text{GW}}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{\text{OE}}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
ZZ	Snooze Enable

TRUTH TABLE[1-8] (3CE option)

OPERATION	ADDRESS	$\overline{\text{CE}}$	$\overline{\text{CE2}}$	CE2	ZZ	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

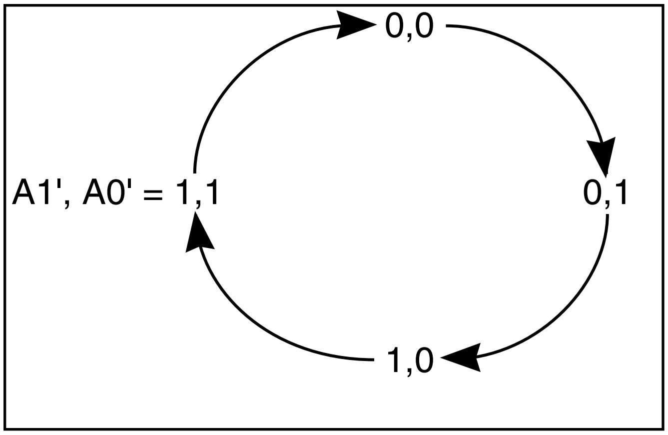
NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{\text{WRITE}}$, L means one or more byte write enable signals ($\overline{\text{BWa-h}}$) and $\overline{\text{BWE}}$ are LOW or $\overline{\text{GW}}$ is LOW. $\overline{\text{WRITE}}$ = H for all $\overline{\text{BWx}}$, $\overline{\text{BWE}}$, $\overline{\text{GW}}$ HIGH.
3. $\overline{\text{BWa}}$ enables WRITEs to DQa's and DQPa. $\overline{\text{BWb}}$ enables WRITEs to DQb's and DQPb. $\overline{\text{BWc}}$ enables WRITEs to DQc's and DQPc. $\overline{\text{BWd}}$ enables WRITEs to DQd's and DQPd. $\overline{\text{BWe}}$ enables WRITEs to DQe's and DQPe. $\overline{\text{BWf}}$ enables WRITEs to DQf's and DQPf. $\overline{\text{BWg}}$ enables WRITEs to DQg's and DQPg. $\overline{\text{BWh}}$ enables WRITEs to DQh's and DQPh. DQPa-DQPh are available on the x72 version. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{\text{OE}}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{\text{OE}}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{\text{ADSP}}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{\text{BWE}}$ LOW or $\overline{\text{GW}}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = VSS)



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ} + 0.5	V
V_{IN}	Voltage Relative to Vss for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61LFxxxxx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V/2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V/2.5V ± 5%

OPERATING RANGE (IS61VFxxxxx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			3.3V		2.5V		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V)	2.4	—	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
I_{LI}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$(1)	–5	5	–5	5	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{DDQ}$, $\overline{OE} = V_{IH}$	–5	5	–5	5	μA

Note:

1. V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

				6.5 MAX		7.5 MAX		
Symbol	Parameter	Test Conditions	Temp. range	x18	x36	x18	x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected,	Com.	360	360	340	340	mA
		$\overline{OE} = V_{IH}$, $ZZ \leq V_{IL}$,	Ind.	375	375	350	350	
		All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V,	typ.(2)	295		295		
		Cycle Time ≥ t_{KC} min.						
I_{SB}	Standby Current TTL Input	Device Deselected,	Com.	155	155	155	155	mA
		V_{DD} = Max.,	Ind.	160	160	160	160	
		All Inputs ≤ V_{IL} or ≥ V_{IH},						
		$ZZ \leq V_{IL}$, f = Max.						
I_{SBI}	Standby Current CMOS Input	Device Deselected,	Com.	140	140	140	140	mA
		V_{DD} = Max.,	Ind.	145	145	145	145	
		$V_{IN} \leq V_{SS}$ + 0.2V or ≥V_{DD} – 0.2V	typ.(2)	80		80		
		f = 0						

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100 μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V.
2. Typical values are measured at Vcc = 3.3V, TA = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{OUT}	Input/Output Capacitance	$V_{OUT} = 0V$	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25°C$, f = 1 MHz, $V_{DD} = 3.3V$.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

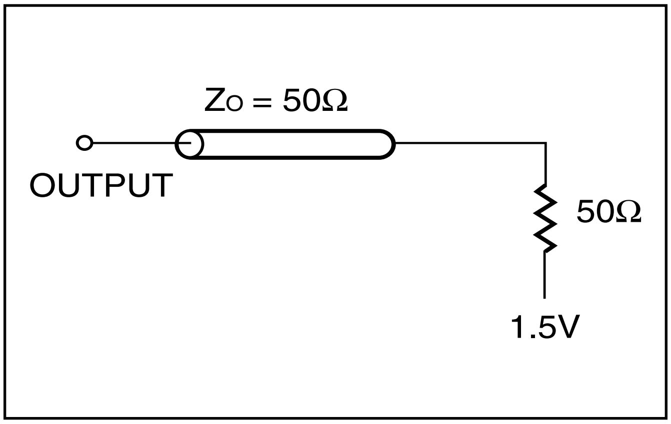


Figure 1

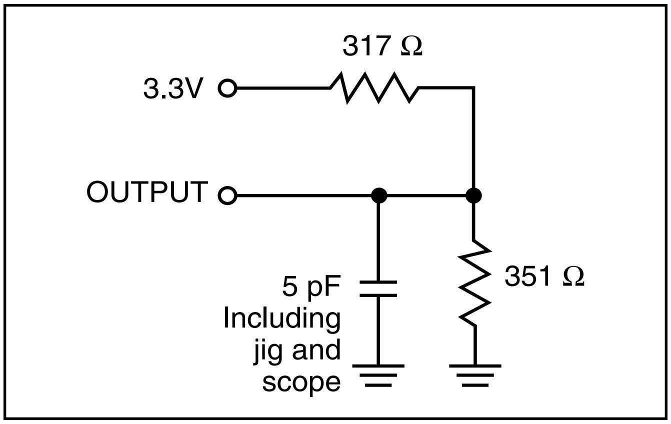


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

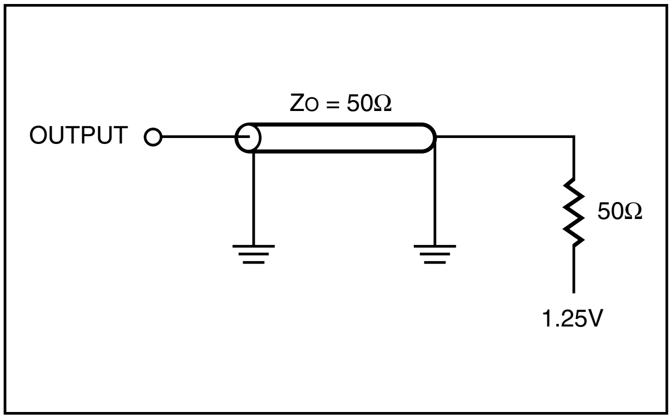


Figure 3

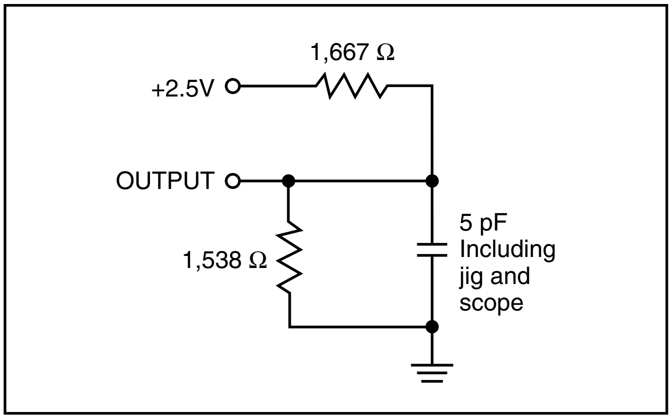


Figure 4

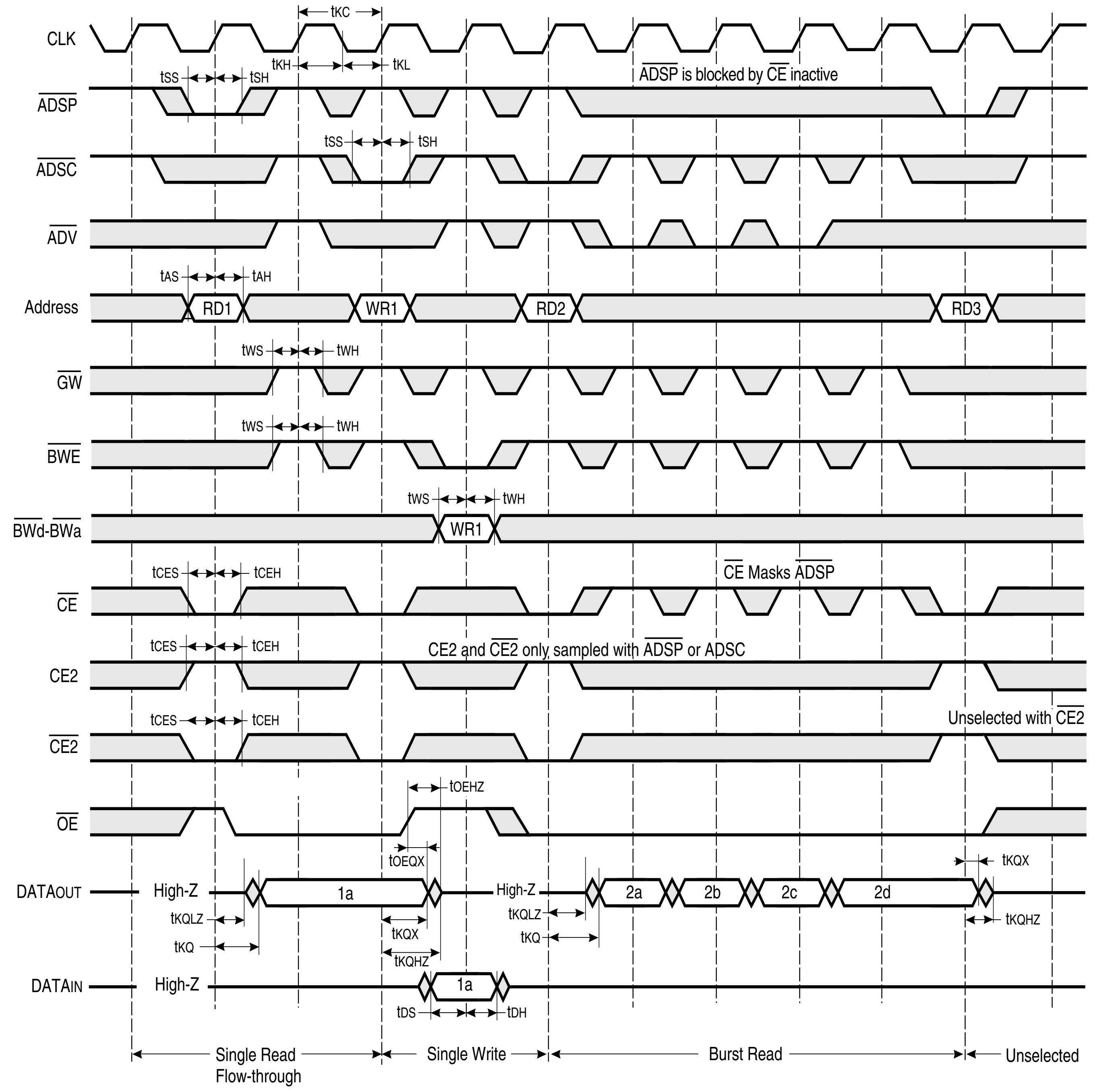
READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		6.5		7.5		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fmax	Clock Frequency	—	133	—	117	MHz
t_{KC}	Cycle Time	7.5	—	8.5	—	ns
t_{KH}	Clock High Time	2.2	—	2.5	—	ns
t_{KL}	Clock Low Time	2.2	—	2.5	—	ns
t_{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t_{KQX}[2]	Clock High to Output Invalid	2.5	—	2.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	2.5	—	2.5	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	3.8	—	4.0	ns
t_{OEQ}	Output Enable to Output Valid	—	3.2	—	3.4	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	3.5	—	3.5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{DS}	Data Setup Time	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

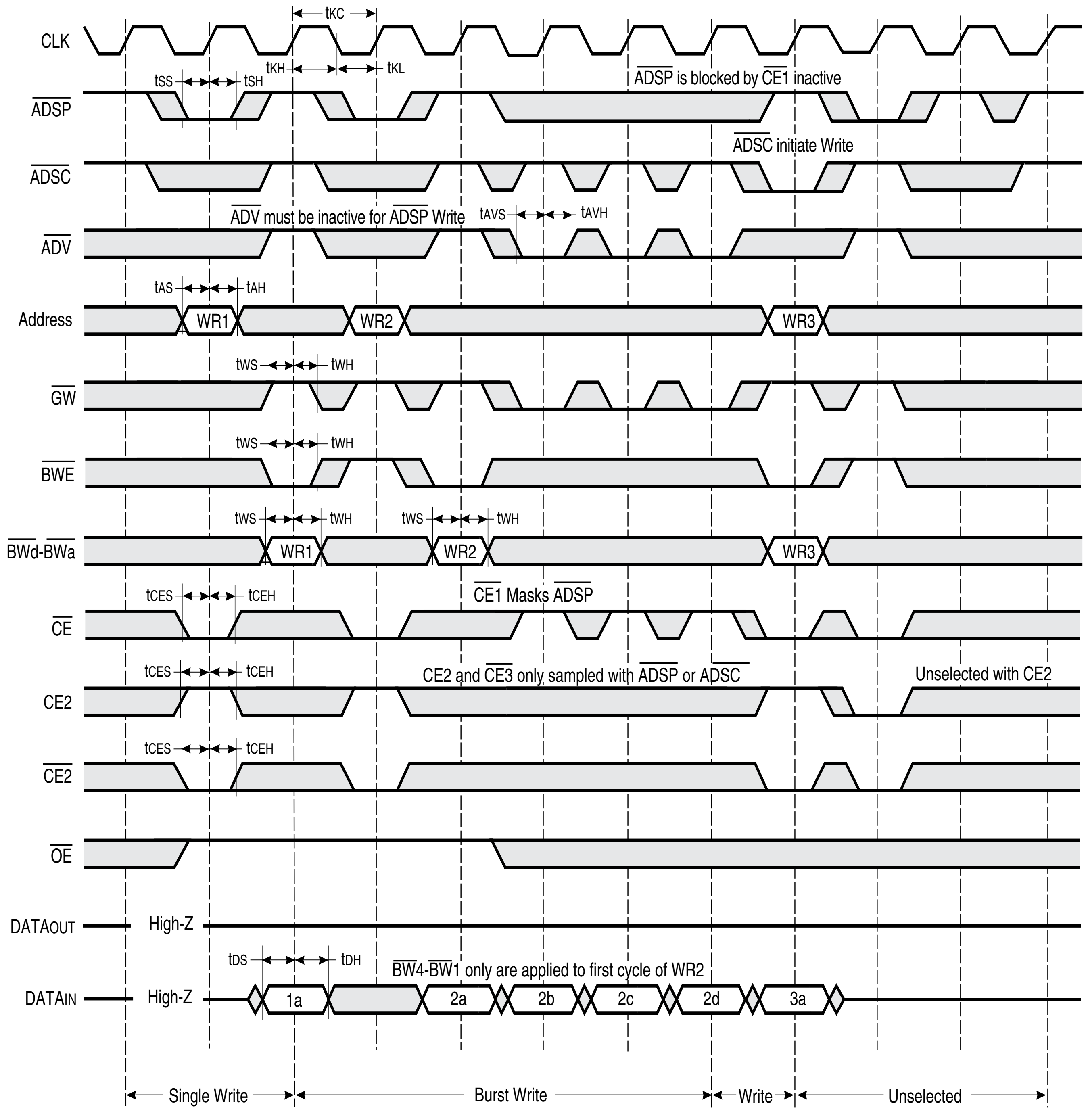
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



WRITE CYCLE TIMING

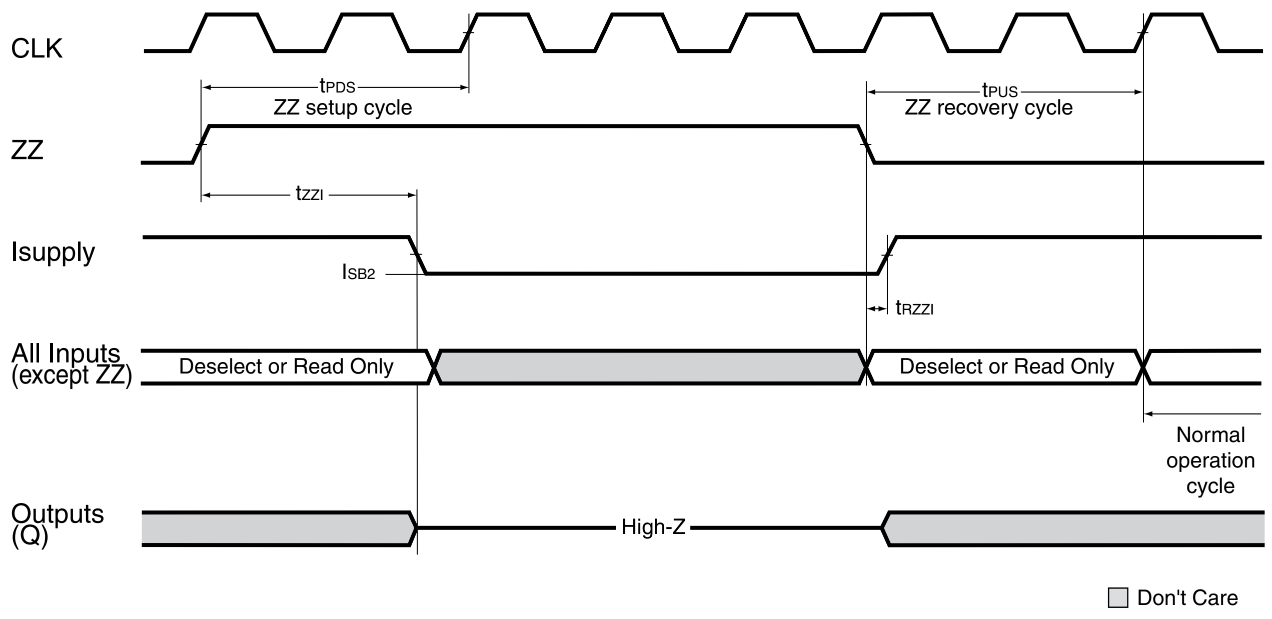


SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	typ. (1)	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ Vih	—	27	90	mA
t_{PDS}	ZZ active to input ignored		—		2	cycle
t_{PUS}	ZZ inactive to input sampled		2		—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—		2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0		—	ns

1. Typical values are measured at Vcc = 3.3V, TA = 25°C and not 100% tested.

SNOOZE MODE TIMING



ORDERING INFORMATION (VDD = 3.3V/VDDQ = 2.5V/3.3V)

Commercial Range: 0°C to +70°C

Configuration	Access Time	Order Part Number	Package
1Mx36	6.5	IS61LF102436A-6.5TQL IS61LF102436A-6.5B3	100 TQFP, Lead-free 165 PBGA
2Mx18	6.5	IS61LF204818A-6.5TQ IS61LF204818A-6.5TQL IS61LF204818A-6.5B3	100 TQFP 100 TQFP, Lead-free 165 PBGA

Industrial Range: -40°C to +85°C

Configuration	Access Time	Order Part Number	Package
1Mx36	6.5	IS61LF102436A-6.5TQLI IS61LF102436A-6.5B3I	100 TQFP, Lead-free 165 PBGA
1Mx36	7.5	IS61LF102436A-7.5TQI IS61LF102436A-7.5TQLI IS61LF102436A-7.5B3I IS61LF102436A-7.5B3LI	100 TQFP 100 TQFP, Lead-free 165 PBGA 165 PBGA, Lead-free
2Mx18	6.5	IS61LF204818A-6.5TQI IS61LF204818A-6.5B3I	100 TQFP 165 PBGA
2Mx18	7.5	IS61LF204818A-7.5TQI IS61LF204818A-7.5TQLI IS61LF204818A-7.5B3I	100 TQFP 100 TQFP, Lead-free 165 PBGA

ORDERING INFORMATION (VDD = 2.5V /VDDQ = 2.5V)

Commercial Range: 0°C to +70°C

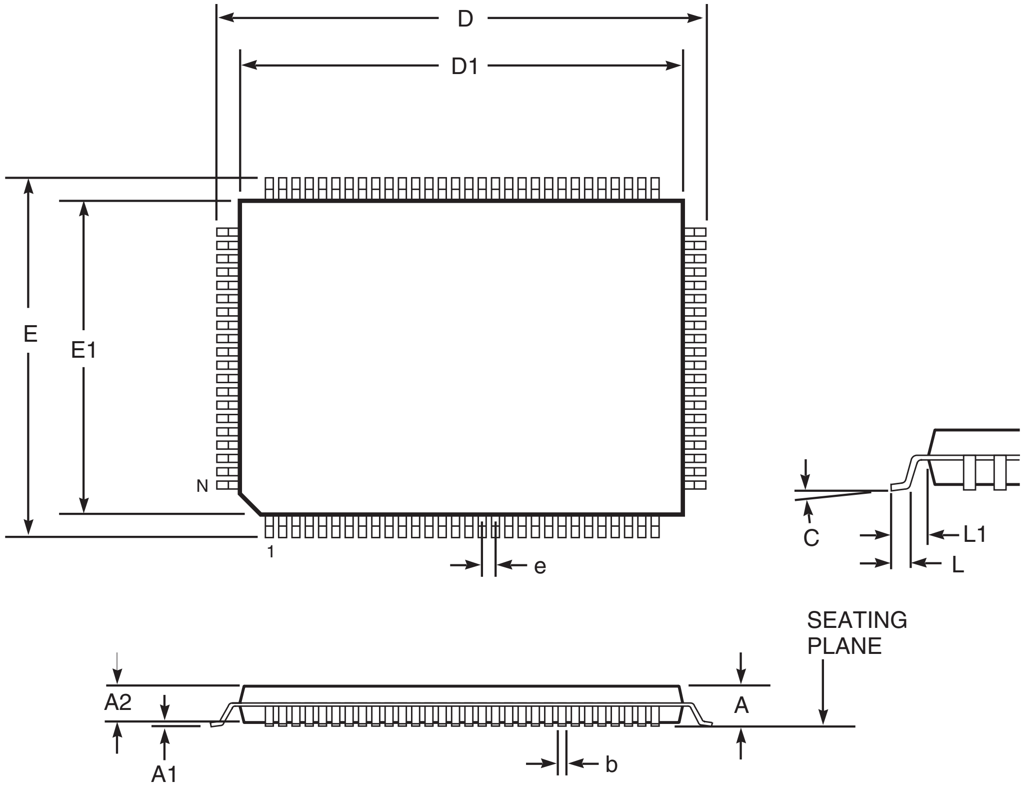
Configuration	Access Time	Order Part Number	Package
1Mx36	6.5	IS61VF102436A-6.5TQ IS61VF102436A-6.5B3	100 TQFP 165 PBGA
1Mx36	7.5	IS61VF102436A-7.5TQ IS61VF102436A-7.5B3	100 TQFP 165 PBGA
2Mx18	6.5	IS61VF204818A-6.5TQ IS61VF204818A-6.5B3	100 TQFP 165 PBGA
2Mx18	7.5	IS61VF204818A-7.5TQ IS61VF204818A-7.5B3	100 TQFP 165 PBGA

Industrial Range: -40°C to +85°C

Configuration	Access Time	Order Part Number	Package
1Mx36	6.5	IS61VF102436A-6.5TQI IS61VF102436A-6.5B3I	100 TQFP 165 PBGA
1Mx36	7.5	IS61VF102436A-7.5TQI IS61VF102436A-7.5TQLI IS61VF102436A-7.5B3I	100 TQFP 100 TQFP, Lead-free 165 PBGA
2Mx18	6.5	IS61VF204818A-6.5TQI IS61VF204818A-6.5B3I	100 TQFP 165 PBGA
2Mx18	7.5	IS61VF204818A-7.5TQI IS61VF204818A-7.5B3I	100 TQFP 165 PBGA

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flat Pack (TQ)

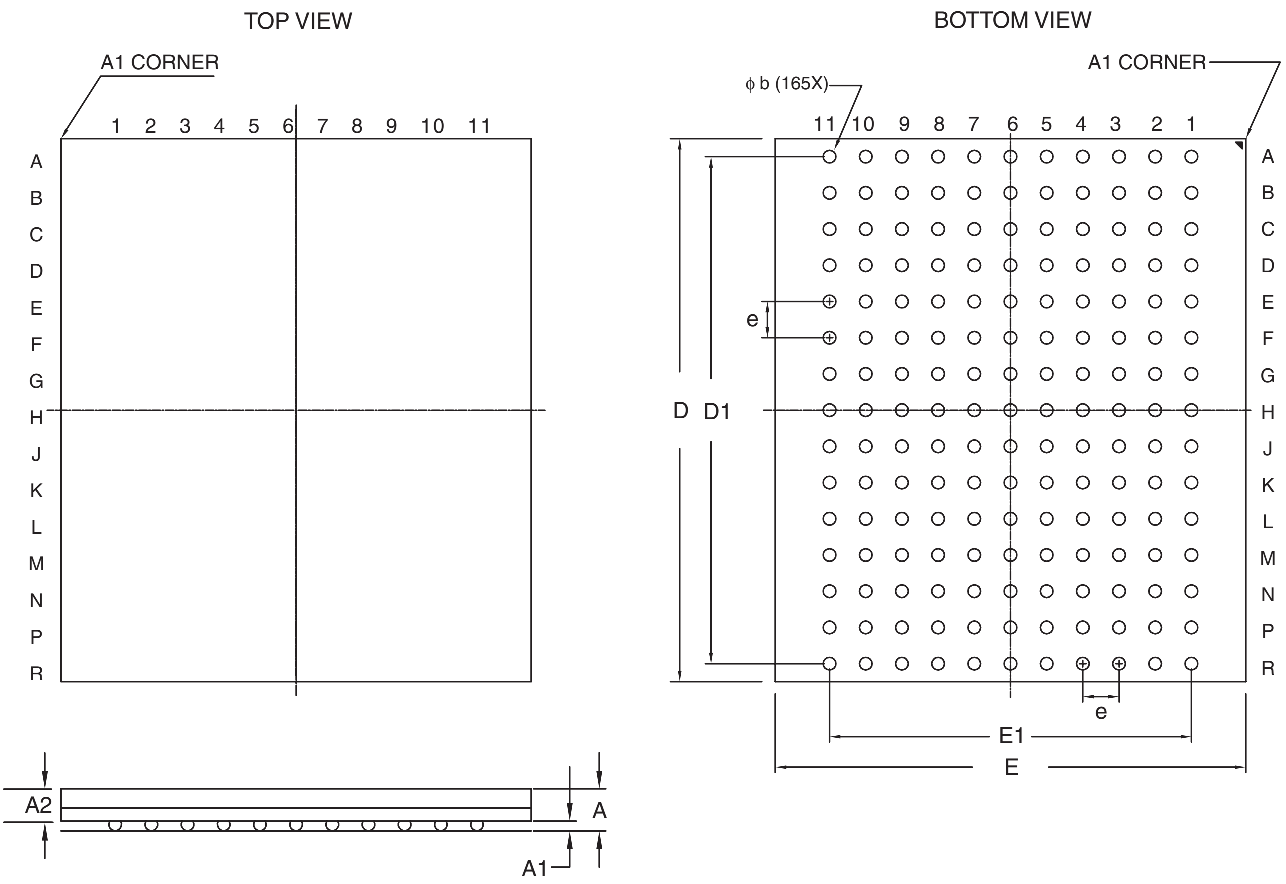
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads (N)	100				128			
A	—	1.60	—	0.063	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°	0°	7°	0°	7°

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.

PACKAGING INFORMATION

Ball Grid Array
Package Code: B (165-pin)



BGA - 13mm x 15mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
N0. Leads		**165**			**165**	
A	—	—	1.20	—	—	0.047
A1	0.25	0.33	0.40	0.010	0.013	0.016
A2	—	0.79	—	—	0.031	—
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	—	1.00	—	—	0.039	—
b	0.40	0.45	0.50	0.016	0.018	0.020

Notes:

1. Controlling dimensions are in millimeters.

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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