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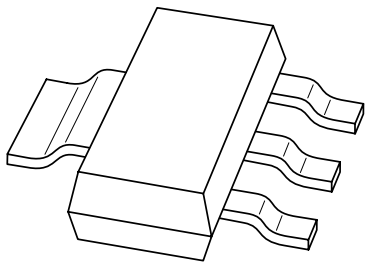
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Kind regards,

Team Nexperia

DATA SHEET



BSP122

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
Supersedes data of 1997 Jun 23

2001 May 18

N-channel enhancement mode vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

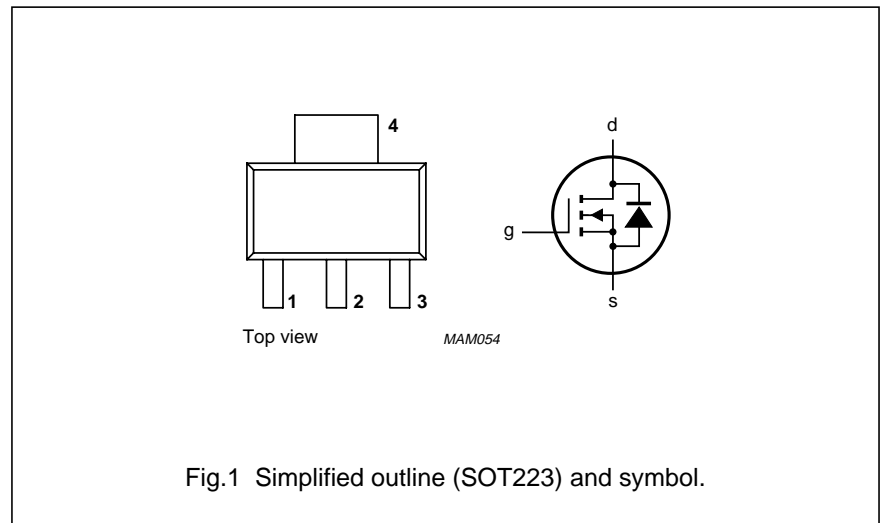
N-channel enhancement mode vertical D-MOS transistor in a SOT223 package and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| 4 | drain |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|------------|----------------------------------|------|----------|
| V_{DS} | drain-source voltage (DC) | 200 | V |
| I_D | drain current (DC) | 550 | mA |
| R_{DSon} | drain-source on-state resistance | 2.5 | Ω |
| V_{GSth} | gate-source threshold voltage | 2 | V |



LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|---------------------------|--|------|----------|------------------|
| V_{DS} | drain-source voltage (DC) | | – | 200 | V |
| V_{GSO} | gate-source voltage (DC) | open drain | – | ± 20 | V |
| I_D | drain current (DC) | | – | 550 | mA |
| I_{DM} | peak drain current | | – | 3 | A |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1 | – | 1.5 | W |
| T_{stg} | storage temperature | | –55 | +150 | $^\circ\text{C}$ |
| T_j | junction temperature | | – | 150 | $^\circ\text{C}$ |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient; note 1 | 83.3 | K/W |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

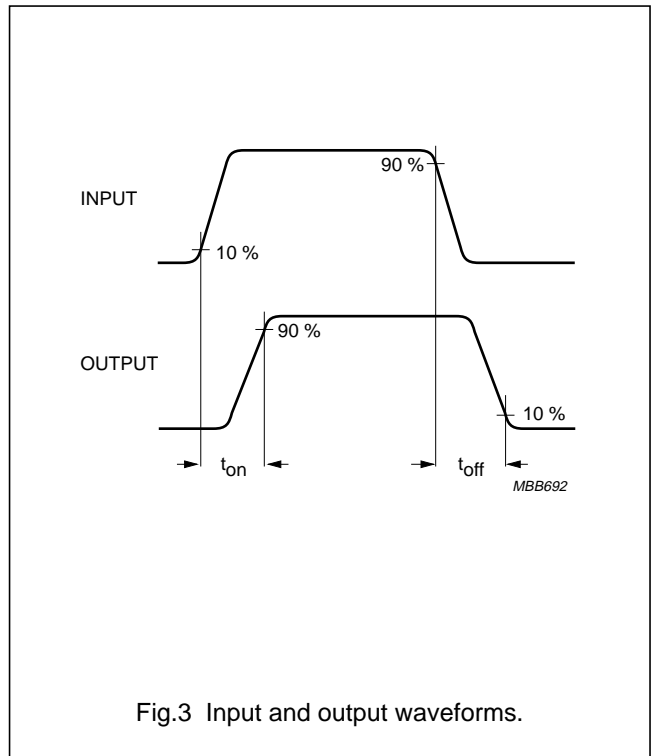
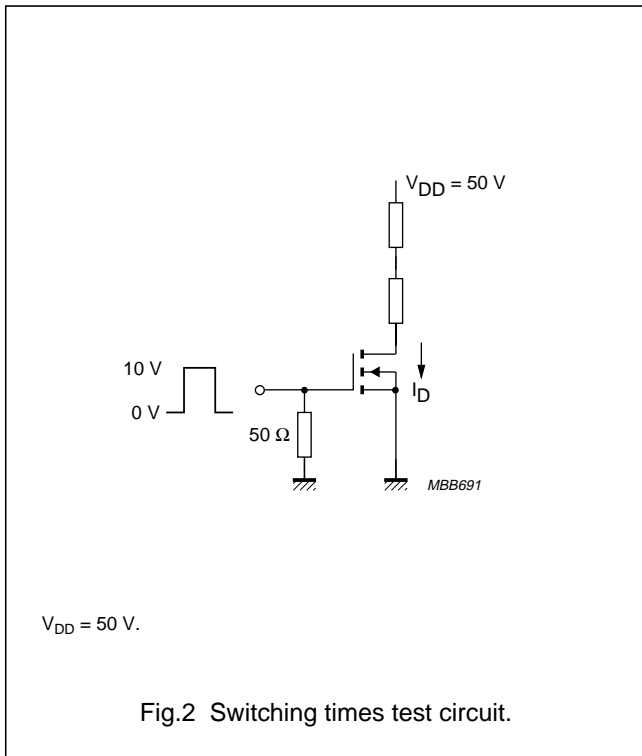
N-channel enhancement mode vertical D-MOS transistor

BSP122

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--------------------------------|--|------|------|------|------|
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 10 μA; V _{GS} = 0 | 200 | – | – | V |
| I _{DSS} | drain-source leakage current | V _{DS} = 160 V; V _{GS} = 0 | – | – | 1 | μA |
| I _{GSS} | gate-source leakage current | V _{GS} = ±20 V; V _{DS} = 0 | – | – | 100 | nA |
| V _{GSth} | gate-source threshold voltage | I _D = 1 mA; V _{GS} = V _{DS} | 0.4 | – | 2 | V |
| R _{DSon} | drain-source on-resistance | I _D = 750 mA; V _{GS} = 10 V | – | 1.7 | 2.5 | Ω |
| | | I _D = 20 mA; V _{GS} = 2.4 V | – | 3 | – | Ω |
| Y _{fs} | transfer admittance | I _D = 750 mA; V _{DS} = 25 V | 400 | 900 | – | mS |
| C _{iSS} | input capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | – | 100 | – | pF |
| C _{oSS} | output capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | – | 20 | – | pF |
| C _{rSS} | reverse transfer capacitance | V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz | – | 10 | – | pF |
| Switching times (see Figs 2 and 3) | | | | | | |
| t _{on} | turn-on time | I _D = 750 mA; V _{DD} = 50 V; V _{GS} = 0 to 10 V | – | 10 | 20 | ns |
| t _{off} | turn-off time | I _D = 750 mA; V _{DD} = 50 V; V _{GS} = 0 to 10 V | – | 45 | 60 | ns |



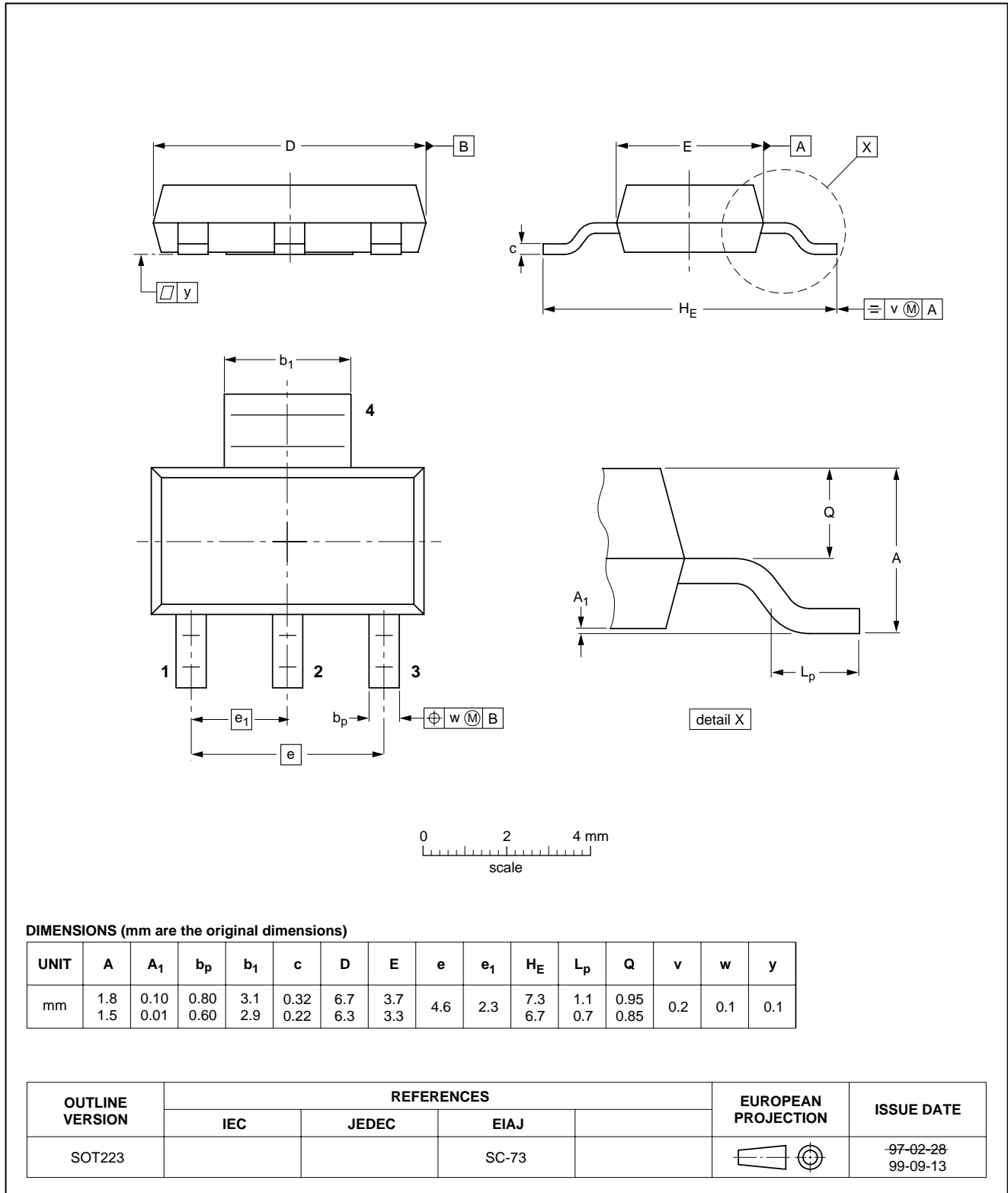
N-channel enhancement mode
vertical D-MOS transistor

BSP122

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



N-channel enhancement mode vertical D-MOS transistor

BSP122

DATA SHEET STATUS

| DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾ | DEFINITIONS |
|----------------------------------|-------------------------------|--|
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vertical D-MOS transistor

BSP122

NOTES

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vertical D-MOS transistor

BSP122

NOTES

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