



16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
 - Typical standby current: 5.5 μ A
 - Maximum standby current: 16 μ A
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-ball VFBGA package

Functional Description

CY62168G and CY62168GE are high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62168GE device includes an error indication pin that signals a single-bit error-detection and correction event during a read cycle.

Devices with a single chip enable input are accessed by asserting the chip enable input (CE) LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – CE₁ as LOW and CE₂ as HIGH.

Write to the device by taking Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (CE₂) HIGH and the Write Enable (WE) input LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₂₀).

Read from the device by taking Chip Enable 1 (\overline{CE}_1) and Output Enable (\overline{OE}) LOW and Chip Enable 2 (CE₂) HIGH while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins (I/O₀ through I/O₇) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE₂ LOW), the outputs are disabled (\overline{OE} HIGH), or a write operation is in progress (\overline{CE}_1 LOW and CE₂ HIGH and WE LOW). See the [Truth Table – CY62168G/CY62168GE on page 14](#) for a complete description of read and write modes.

On CY62168GE devices, the detection and correction of a single bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH) ^[1].

The CY62168G and CY62168GE devices are available in a Pb-free 48-pin VFBGA package. The logic block diagrams are on page 2.

For a complete list of related resources, [click here](#).

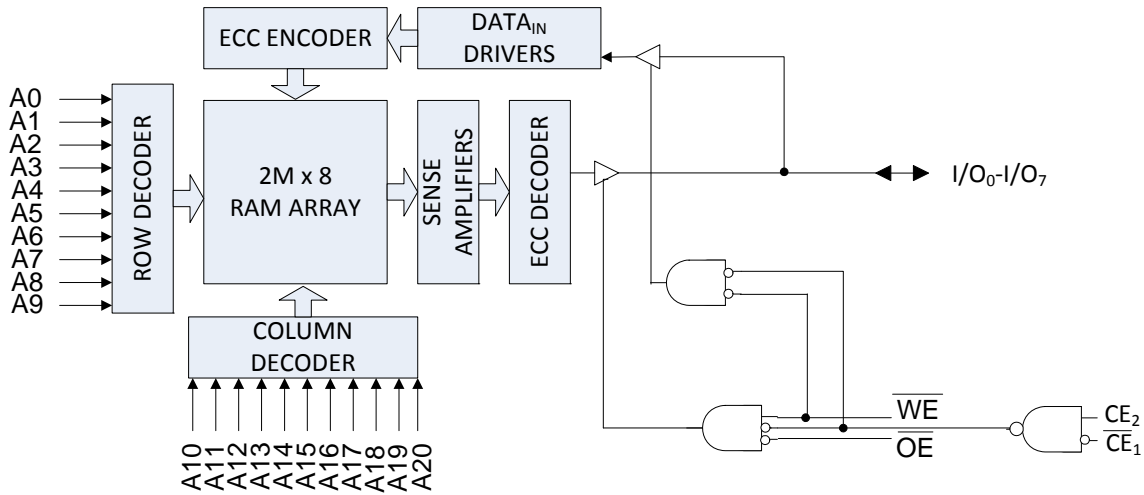
Product Portfolio

| Product | Features and Options (see Pin Configurations section) | Range | V _{CC} Range (V) | Speed (ns) | Power Dissipation | | | |
|---------------|--|------------|---------------------------|------------|----------------------------------|-----|--------------------------------------|-----|
| | | | | | Operating I _{CC} , (mA) | | Standby, I _{SB2} (μ A) | |
| | | | | | f = f _{max} | | | |
| | | | | | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62168G(E)18 | Single or dual Chip Enables | Industrial | 1.65 V–2.2 V | 55 | 29 | 32 | 7 | 26 |
| CY62168G(E)30 | | | 2.2 V–3.6 V | 45 | 29 | 36 | 5.5 | 16 |
| CY62168G(E) | Optional ERR pin | | 4.5 V–5.5 V | | | | | |

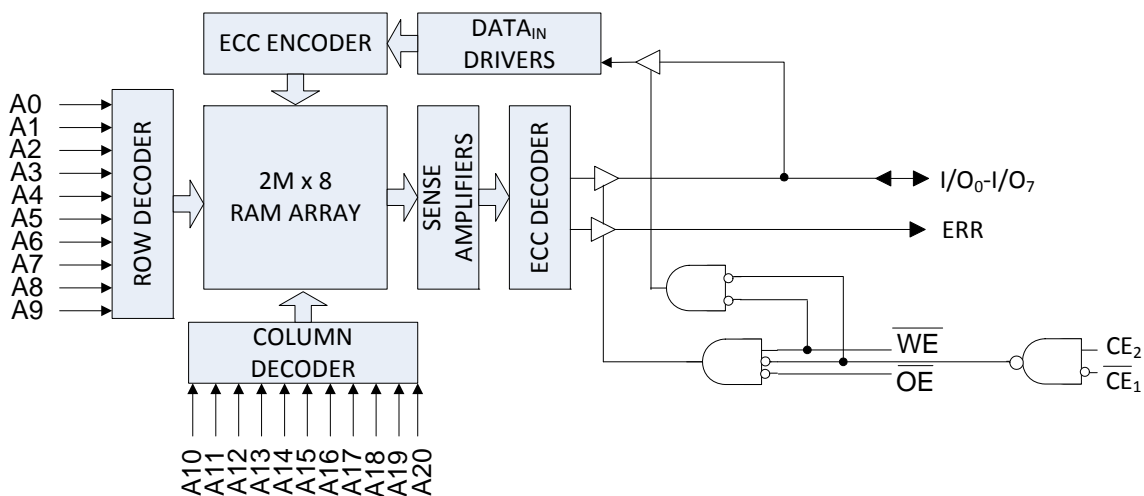
Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY62168G



Logic Block Diagram – CY62168GE



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Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1 mm) pinout^[3]
CY62168G

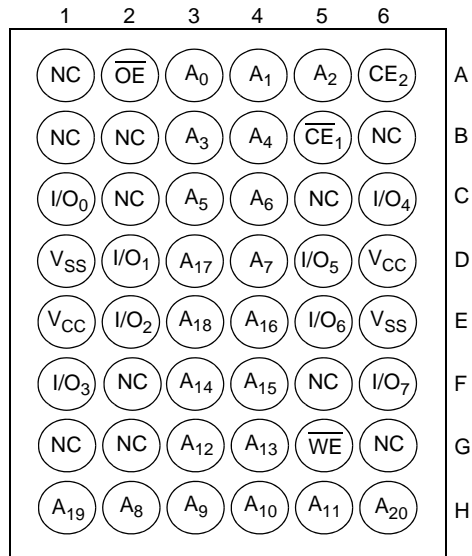
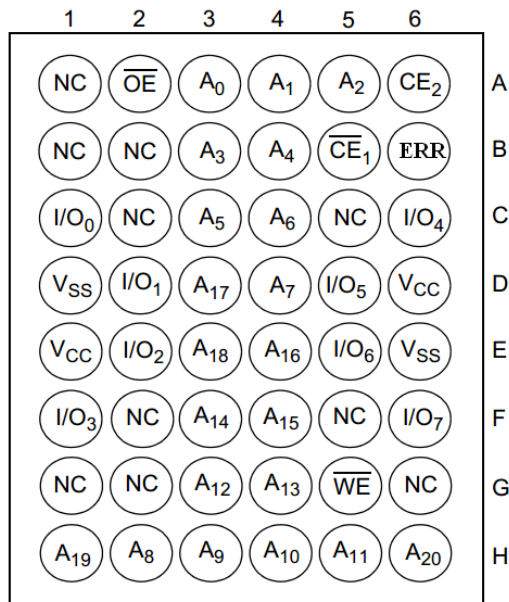


Figure 2. 48-ball VFBGA (6 × 8 × 1 mm) pinout^[3, 4]
CY62168GE



Note

3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
4. ERR is an Output pin. If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.5 V to 6 V

DC voltage applied to outputs
in High Z state^[5] -0.5 V to $V_{CC} + 0.5 V$

DC input voltage^[5] -0.5 V to $V_{CC} + 0.5 V$

Output current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) >2001 V

Latch up current >140 mA

Operating Range

| Grade | Ambient Temperature | V_{CC} ^[6] |
|------------|---------------------|---|
| Industrial | -40 °C to +85 °C | 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V |

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Test Conditions | 45 ns/55 ns | | | Unit | |
|-----------|----------------------------------|--|---|-------------------------------|------|----------------|---|
| | | | Min | Typ ^[7] | Max | | |
| V_{OH} | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$ | 1.4 | - | - | V |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$ | 2.0 | - | - | V |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$ | 2.4 | - | - | V |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$ | 2.4 | - | - | V |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$ | $V_{CC} - 0.4$ ^[8] | - | - | V |
| V_{OL} | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$ | - | - | 0.2 | V |
| | | 2.2 V to 2.7 V | $V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$ | - | - | 0.4 | V |
| | | 2.7 V to 3.6 V | $V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$ | - | - | 0.4 | V |
| | | 4.5 V to 5.5 V | $V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$ | - | - | 0.4 | V |
| V_{IH} | Input HIGH voltage | 1.65 V to 2.2 V | - | 1.4 | - | $V_{CC} + 0.2$ | V |
| | | 2.2 V to 2.7 V | - | 1.8 | - | $V_{CC} + 0.3$ | V |
| | | 2.7 V to 3.6 V | - | 2.0 | - | $V_{CC} + 0.3$ | V |
| | | 4.5 V to 5.5 V | - | 2.2 | - | $V_{CC} + 0.5$ | V |
| V_{IL} | Input LOW voltage ^[9] | 1.65 V to 2.2 V | - | -0.2 | - | 0.4 | V |
| | | 2.2 V to 2.7 V | - | -0.3 | - | 0.6 | V |
| | | 2.7 V to 3.6 V | - | -0.3 | - | 0.8 | V |
| | | 4.5 V to 5.5 V | - | -0.5 | - | 0.8 | V |
| I_{IX} | Input leakage current | $GND \leq V_{IN} \leq V_{CC}$ | -1.0 | - | +1.0 | μA | |
| I_{OZ} | Output leakage current | $GND \leq V_{OUT} \leq V_{CC}$, Output disabled | -1.0 | - | +1.0 | μA | |

Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(\text{min})}$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25 \text{ }^\circ\text{C}$.
- This parameter is guaranteed by design and is not tested.
- $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

| Parameter | Description | Test Conditions | 45 ns/55 ns | | | Unit | |
|----------------------------------|---|--|--------------------------|--------------------|----------------------|------|----|
| | | | Min | Typ ^[7] | Max | | |
| I _{CC} | V _{CC} operating supply current | V _{CC} = Max, I _{OUT} = 0 mA, CMOS levels | f = 22.22 MHz (45 ns) | – | 29.0 | 36.0 | mA |
| | | | f = 18.18 MHz (55 ns) | – | 29.0 | 32.0 | mA |
| | | | f = 1 MHz | – | 7.0 | 9.0 | mA |
| I _{SB1} ^[10] | Automatic power down current – CMOS inputs; V _{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, f = f _{max} (address and data only), | – | 5.5 | 16.0 | μA | |
| | Automatic power down current – CMOS inputs; V _{CC} = 1.65 to 2.2 V | f = 0 (\overline{OE} , and \overline{WE}), V _{CC} = V _{CC(max)} | – | 7 | 26.0 | μA | |
| I _{SB2} ^[10] | Automatic power down current – CMOS inputs; V _{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, | 25 °C ^[11] | – | 5.5 | 6.5 | μA |
| | | | 40 °C ^[11] | – | 6.3 | 8.0 | μA |
| | | $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, | 70 °C ^[11] | – | 8.4 | 12.0 | μA |
| | | f = 0, V _{CC} = V _{CC(max)} | 85 °C | – | 12.0 ^[11] | 16.0 | μA |
| | Automatic power down current – CMOS inputs; V _{CC} = 1.65 to 2.2 V | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = 0, V _{CC} = V _{CC(max)} | – | 7.0 | 26.0 | μA | |

Notes

10. Chip enables (\overline{CE}_1 and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
 11. The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

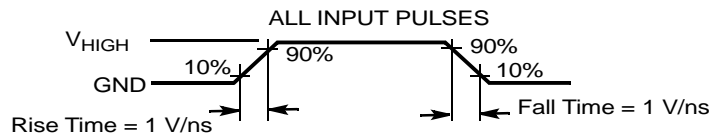
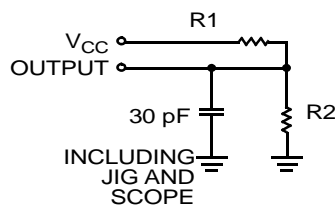
| Parameter ^[12] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

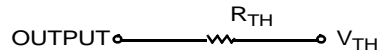
| Parameter ^[12] | Description | Test Conditions | 48-ball VFBGA | Unit |
|---------------------------|--|---|---------------|------|
| θ _{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 31.50 | °C/W |
| θ _{JC} | Thermal resistance (junction to case) | | 15.75 | °C/W |

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameters | 1.8 V | 2.5 V | 3.0 V | 5.0 V | Unit |
|-------------------|-------|-------|-------|-------|------|
| R1 | 13500 | 16667 | 1103 | 1800 | Ω |
| R2 | 10800 | 15385 | 1554 | 990 | Ω |
| R _{TH} | 6000 | 8000 | 645 | 639 | Ω |
| V _{TH} | 0.8 | 1.2 | 1.75 | 1.77 | V |
| V _{HIGH} | 1.8 | 2.5 | 3.0 | 5.0 | V |

Note

12. Tested initially and after any design or process changes that may affect these parameters.

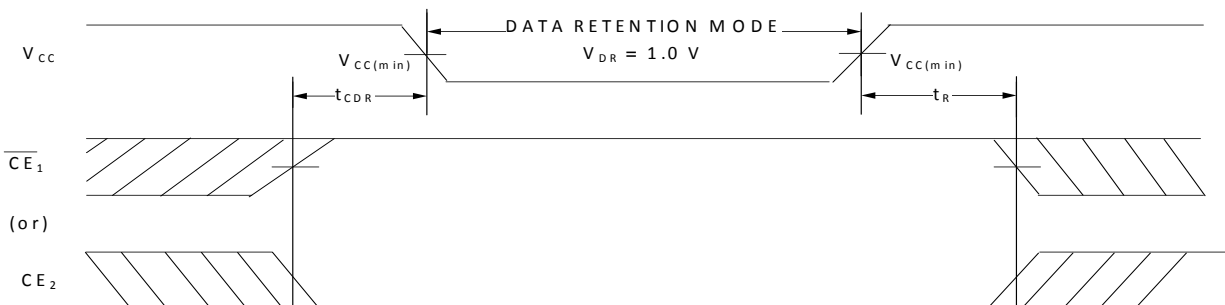
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[13] | Max | Unit |
|--------------------------------|--------------------------------------|--|-------|---------------------|------|---------------|
| V_{DR} | V_{CC} for data retention | | 1.0 | – | – | V |
| I_{CCDR} ^[14, 15] | Data retention current | $1.2\text{ V} \leq V_{CC} \leq 2.2\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 7.0 | 26.0 | μA |
| | | $2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ or $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 5.5 | 16.0 | μA |
| t_{CDR} ^[16] | Chip deselect to data retention time | | 0 | – | – | – |
| t_R ^[16, 17] | Operation recovery time | | 45/55 | – | – | ns |

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8\text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3\text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5\text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25\text{ }^\circ\text{C}$.

14. Chip enables (\overline{CE}_1 and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

15. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and brought down to V_{DR} .

16. These parameters are guaranteed by design.

17. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

| Parameter ^[18, 19] | Description | 45 ns | | 55 ns | | Unit |
|--|--|-------|------|-------|------|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read cycle time | 45.0 | – | 55.0 | – | ns |
| t_{AA} | Address to data valid / Address to ERR valid | – | 45.0 | – | 55.0 | ns |
| t_{OHA} | Data hold from address change / ERR hold from address change | 10.0 | – | 10.0 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid / \overline{CE} LOW to ERR valid | – | 45.0 | – | 55.0 | ns |
| t_{DOE} | \overline{OE} LOW to data valid / \overline{OE} LOW to ERR valid | – | 22.0 | – | 25.0 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[19, 20] | 5.0 | – | 5.0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[19, 20, 21] | – | 18.0 | – | 18.0 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[19, 20] | 10.0 | – | 10.0 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[19, 20, 21] | – | 18.0 | – | 18.0 | ns |
| t_{PU} ^[22] | \overline{CE}_1 LOW and CE_2 HIGH to power-up | 0 | – | 0 | – | ns |
| t_{PD} ^[22] | \overline{CE}_1 HIGH and CE_2 LOW to power-down | – | 45.0 | – | 55.0 | ns |
| Write Cycle ^[23, 24] | | | | | | |
| t_{WC} | Write cycle time | 45.0 | – | 55.0 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35.0 | – | 40.0 | – | ns |
| t_{AW} | Address setup to write end | 35.0 | – | 40.0 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35.0 | – | 40.0 | – | ns |
| t_{SD} | Data setup to write end | 25.0 | – | 25.0 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[19, 21, 20] | – | 18.0 | – | 20.0 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[19, 20] | 10.0 | – | 10.0 | – | ns |

Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.

20. Tested initially and after any design or process changes that may affect these parameters.

21. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

22. These parameters are guaranteed by design and are not tested.

23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

24. The minimum write cycle pulse width for write cycle No. 2 (\overline{WE} Controlled, \overline{OE} Low) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62168G (Address Transition Controlled)^[25, 26]

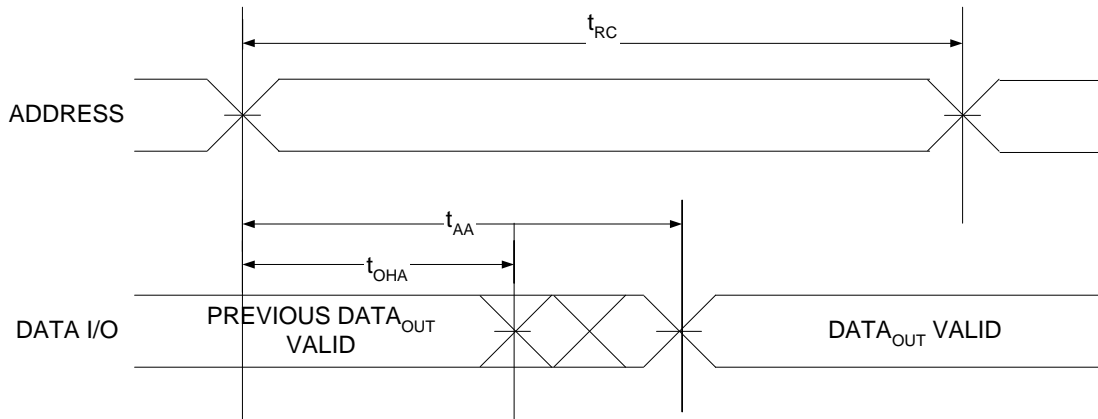
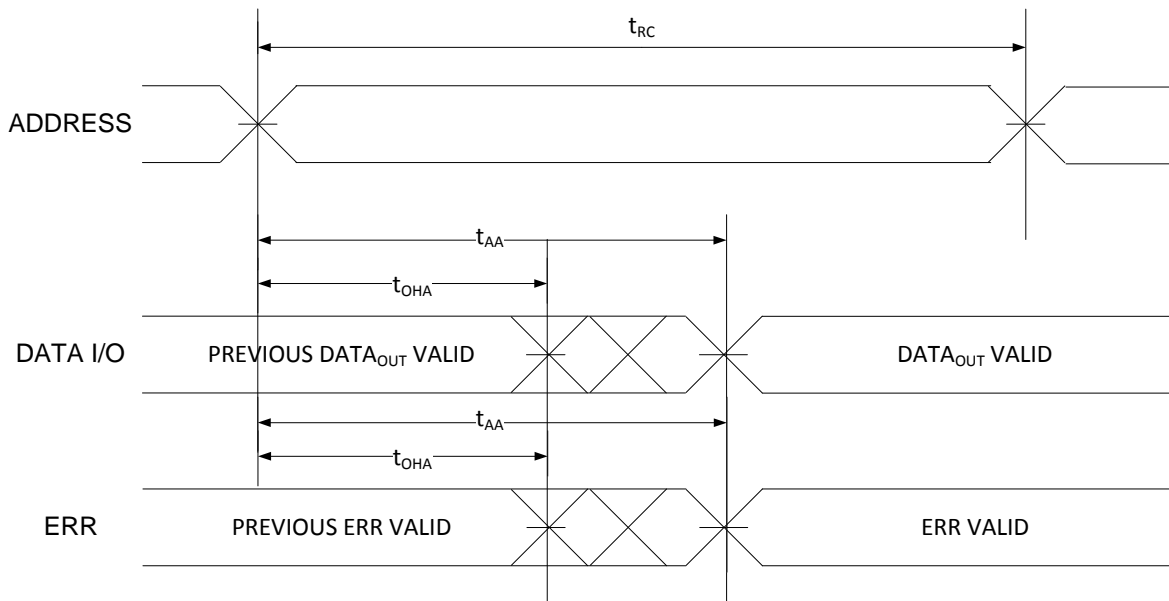


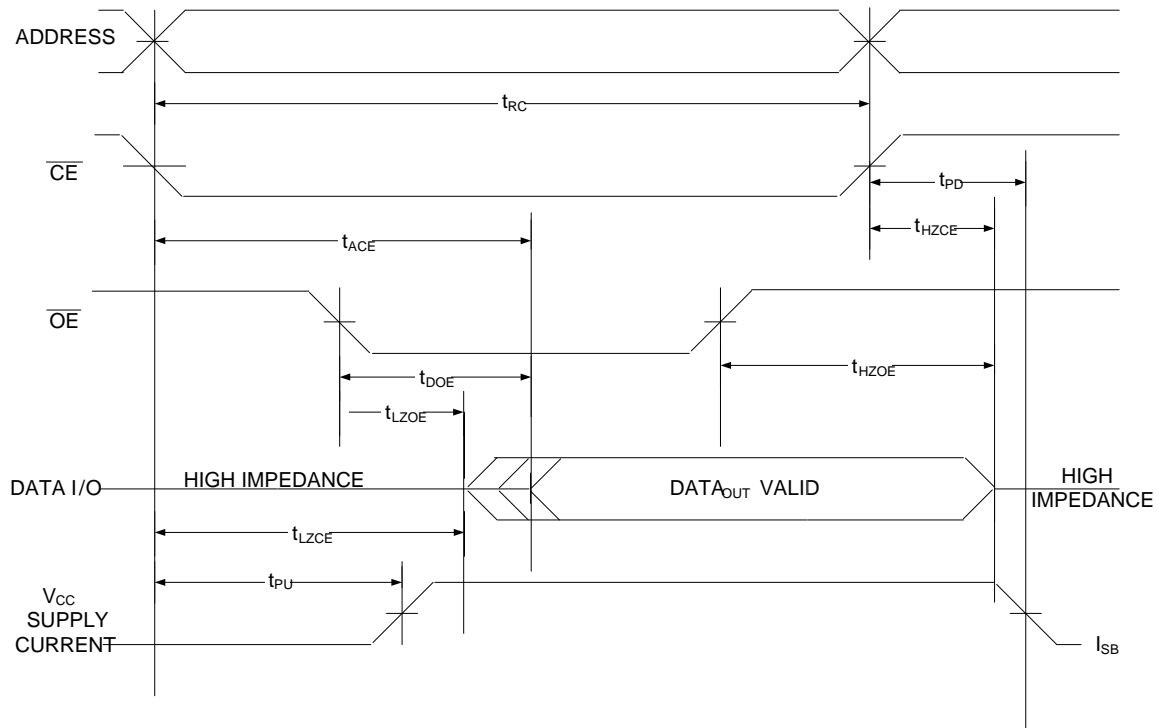
Figure 6. Read Cycle No. 1 of CY62168GE (Address Transition Controlled)^[25, 26]



Notes

- 25. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
- 26. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[27, 28, 29]

Notes

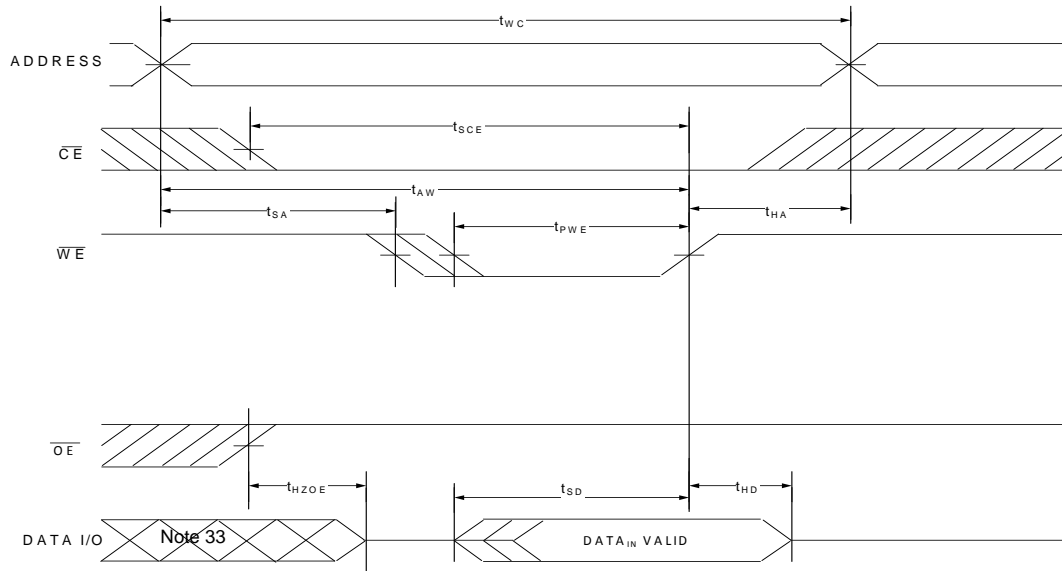
27. $\overline{\text{WE}}$ is HIGH for read cycle.

28. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.

29. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (\overline{WE} Controlled)^[30, 31, 32]



Notes

- 30. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 31. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 32. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
- 33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} Low)^[34, 35, 36, 37]

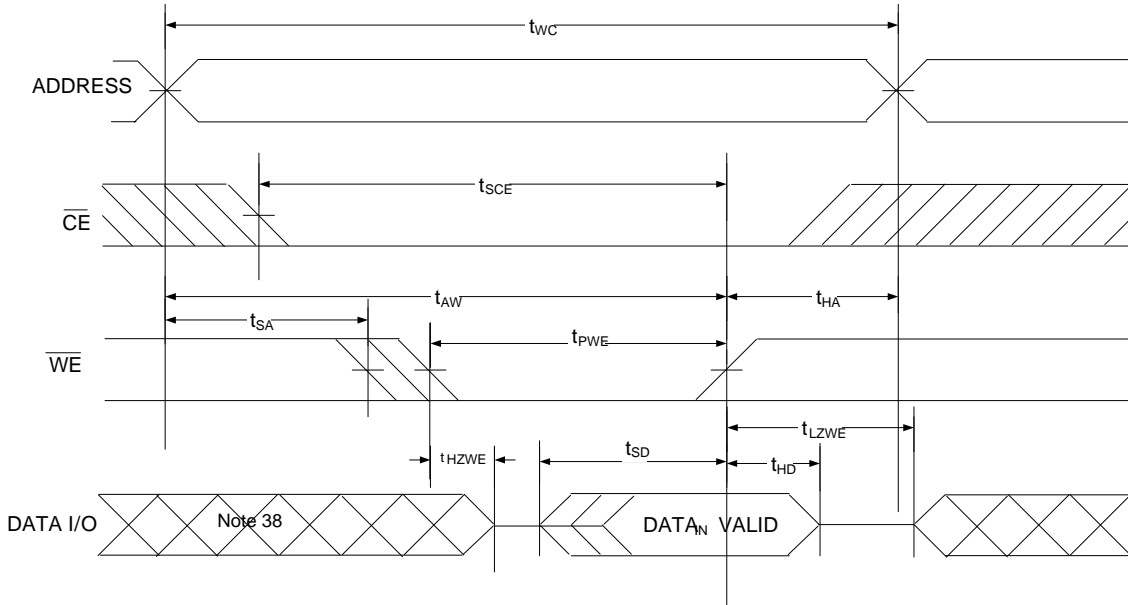
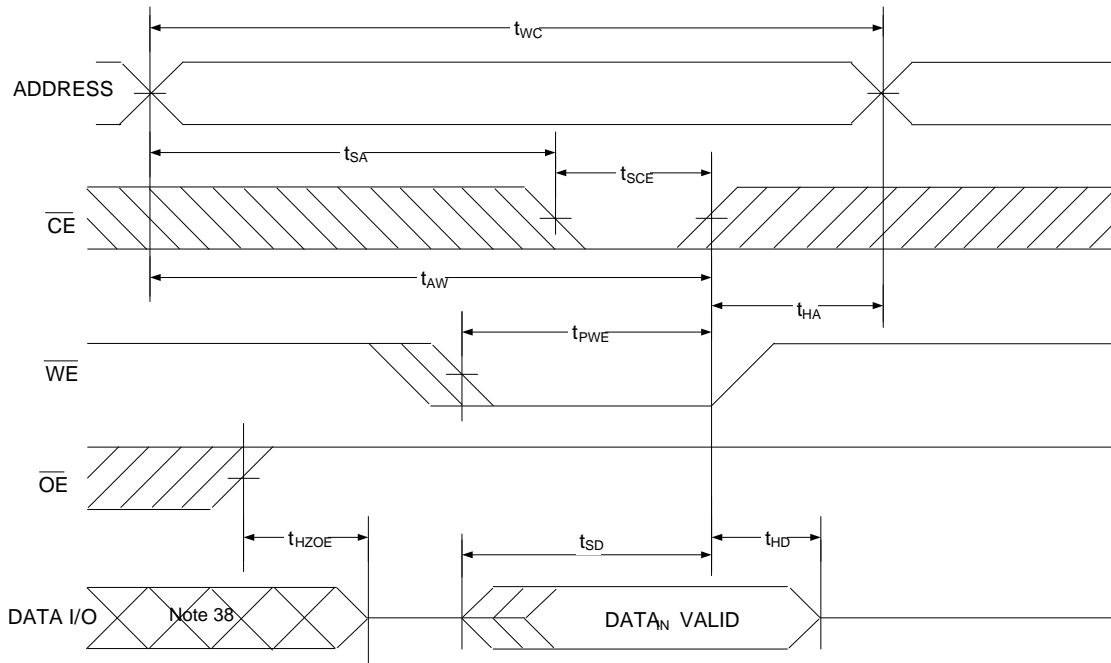


Figure 10. Write Cycle No. 3 (\overline{CE} Controlled)^[34, 35, 36]



Notes

- 34. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 35. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 36. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$.
- 37. The minimum write cycle pulse width should be equal to the sum of the t_{HZWE} and t_{SD} .
- 38. During this period I/O are in the output state. Do not apply input signals.

Truth Table – CY62168G/CY62168GE

| \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | I/Os | Mode | Power |
|-------------------|-------------------|-------------------|-------------------|--|-----------------------|-----------------------------|
| H | X ^[39] | X ^[39] | X ^[39] | High Z | Deselect / Power down | Standby (I _{SB2}) |
| X ^[39] | L | X ^[39] | X ^[39] | High Z | Deselect / Power down | Standby (I _{SB2}) |
| L | H | H | L | Data Out (I/O ₀ –I/O ₇) | Read | Active (I _{CC}) |
| L | H | H | H | High Z | Output disabled | Active (I _{CC}) |
| L | H | L | X | Data In (I/O ₀ –I/O ₇) | Write | Active (I _{CC}) |

ERR Output – CY62168GE

| Output ^[40] | Mode |
|------------------------|--|
| 0 | Read Operation, no single-bit error in the stored data. |
| 1 | Read Operation, single-bit error detected and corrected. |
| High Z | Device deselected / Outputs disabled / Write Operation. |

Note

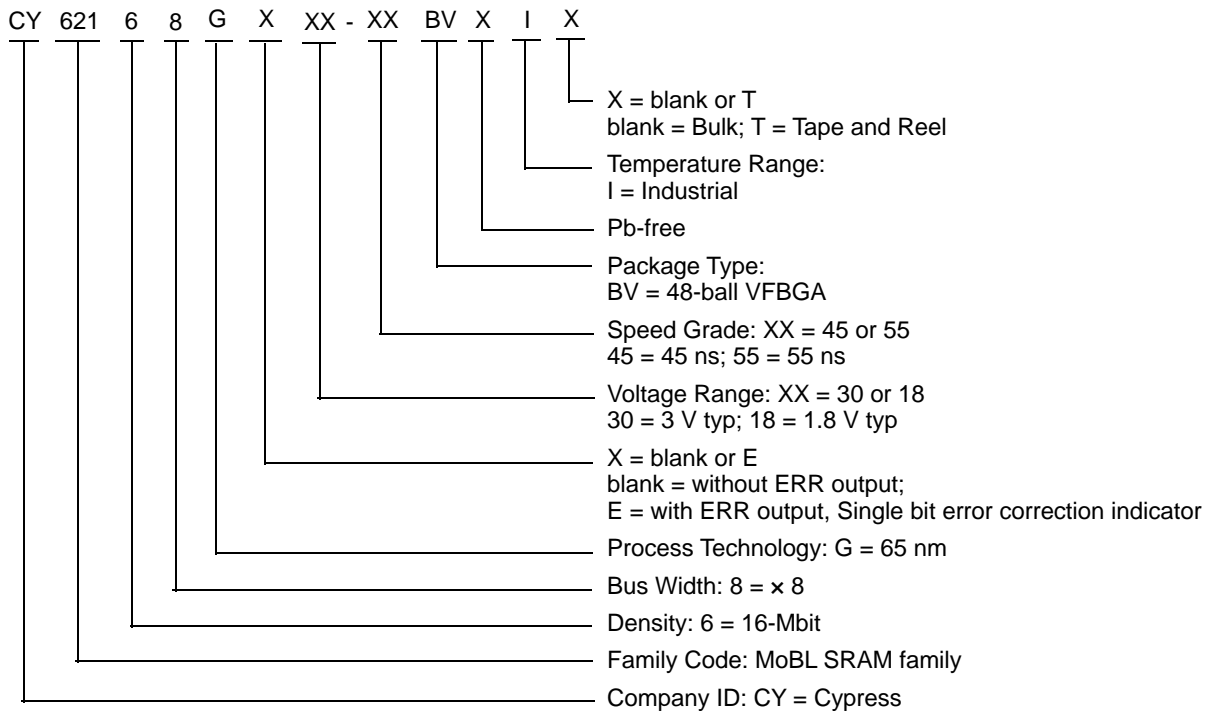
39. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

40. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

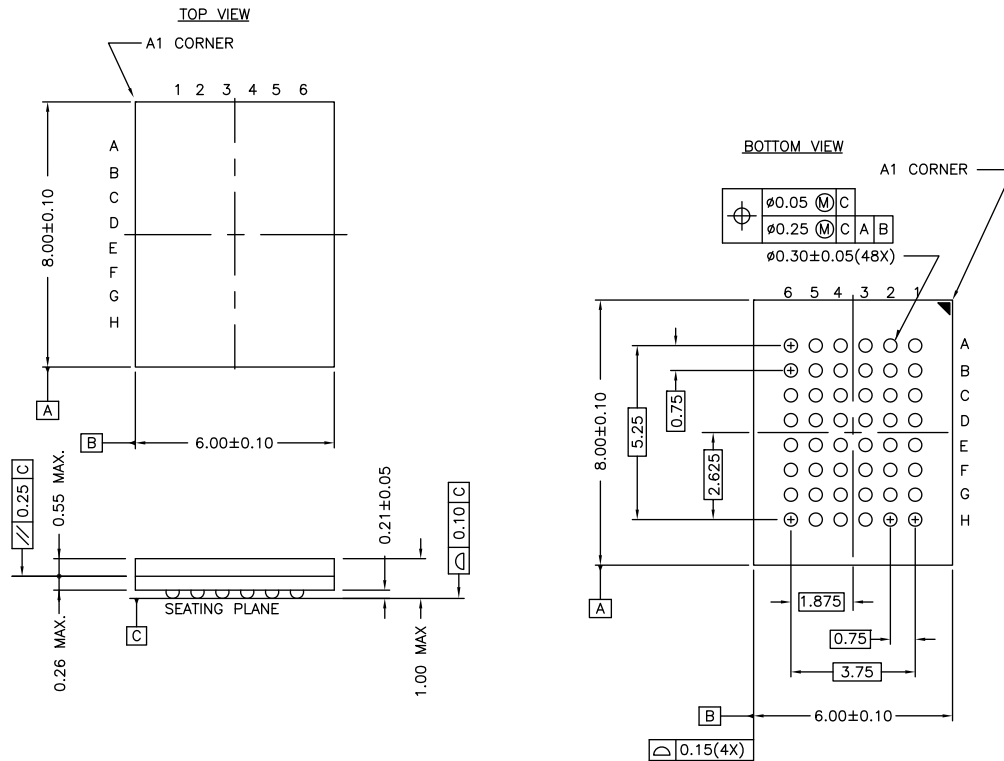
| Speed (ns) | Ordering Code | Package Diagram | Package Type (all Pb-free) | Operating Range |
|------------|---------------------|-----------------|------------------------------|-----------------|
| 45 | CY62168GE30-45BVXI | 51-85150 | 48-ball VFBGA | Industrial |
| | CY62168GE30-45BVXIT | | 48-ball VFBGA, Tape and Reel | |
| | CY62168G30-45BVXI | 51-85150 | 48-ball VFBGA | Industrial |
| | CY62168G30-45BVXIT | | 48-ball VFBGA, Tape and Reel | |
| 55 | CY62168G18-55BVXI | 51-85150 | 48-ball VFBGA | Industrial |
| | CY62168G18-55BVXIT | | 48-ball VFBGA, Tape and Reel | |

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| \overline{OE} | Output Enable |
| SRAM | Static Random Access Memory |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| \overline{WE} | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62168G/CY62168GE MoBL [®] , 16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84771 | | | | |
|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *G | 4800984 | VINI | 07/31/2015 | Changed status from Preliminary to Final. |
| *H | 5449003 | VINI | 11/03/2016 | Updated Maximum Ratings : Updated Note 5 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Changed minimum value of V _{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V”. Changed minimum value of V _{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Thermal Resistance : Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated Ordering Information : Updated part numbers. Updated Ordering Code Definitions . Updated to new template. Completing Sunset Review. |
| *I | 6003639 | AESATP12 | 12/22/2017 | Updated logo and copyright. |

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.