LF442 Dual Low Power JFET Input Operational Amplifier

Check for Samples: LF442

FEATURES

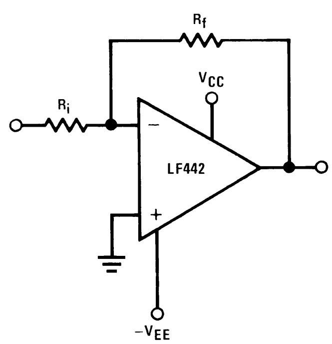
- **1/10 Supply Current of a LM1458: 400 μA (max)**
- **Low Input Bias Current: 50 pA (max)**
- **Low Input Offset Voltage: 1 mV (max)**
- **Low Input Offset Voltage Drift: 10 μV/°C (max)**
- **High Gain Bandwidth: 1 MHz**
- **High Slew Rate: 1 V/μs**
- **Low Noise Voltage for Low Power: 35 nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **High Input Impedance: $10^{12}\Omega$**
- **High Gain V_O = ±10V, R_L = 10k: 50k (min)**

DESCRIPTION

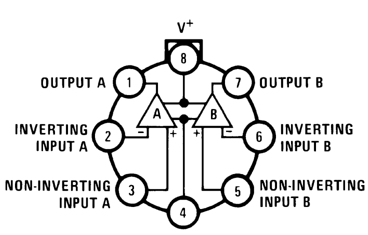
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming ensures very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Typical Connection

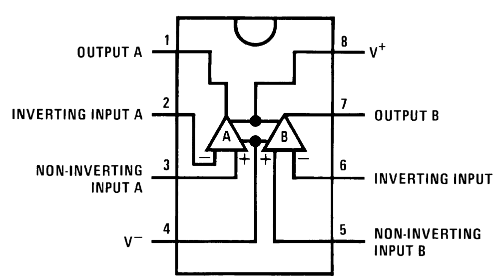


Connection Diagrams



Pin 4 connected to case

TO Package Top View
Package Number LMC0008C



PDIP Package Top View
Package Number P0008E

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

	LF442A	LF442
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range(3)	±19V	±15V
Output Short Circuit Duration(4)	Continuous	Continuous

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) Refer to RETS442X for LF442MH military specifications.
(3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

ABSOLUTE MAXIMUM RATINGS(1)(2)

		LMC0008C Package	P0008E Package
T_j max		150°C	115°C
θ_{JA} (Typical)	See(3)	65°C/W	114°C/W
	See(4)	165°C/W	152°C/W
θ_{JC} (Typical)		21°C/W	
Operating Temperature Range		See(5)(4)	See(5)(4)
Storage Temperature Range		$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
Lead Temperature (Soldering, 10 sec.)		260°C	260°C
ESD Tolerance		Rating to be determined	

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) Refer to RETS442X for LF442MH military specifications.
(3) The value given is in 400 linear feet/min air flow.
(4) The value given is in static air.
(5) These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in “H” package only.

DC Electrical Characteristics[1][2]

Symbol	Parameter	Conditions		LF442A			LF442			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			7	10		7		μV/°C
I_{OS}	Input Offset Current	V_S = ±15V[1][3]	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA
I_B	Input Bias Current	V_S = ±15V[1][3]	T_j = 25°C		10	50		10	100	pA
			T_j = 70°C			3			3	nA
			T_j = 125°C			20				nA
R_{IN}	Input Resistance	T_j = 25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_O = ±10V, R_L = 10 kΩ, T_A = 25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode			±16	+18		±11	+14		V
	Voltage Range				−17			−12		V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	See[4]		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±20V for the LF442A and for V_S = ±15V for the LF442. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.
(2) Refer to RETS442X for LF442MH military specifications.
(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

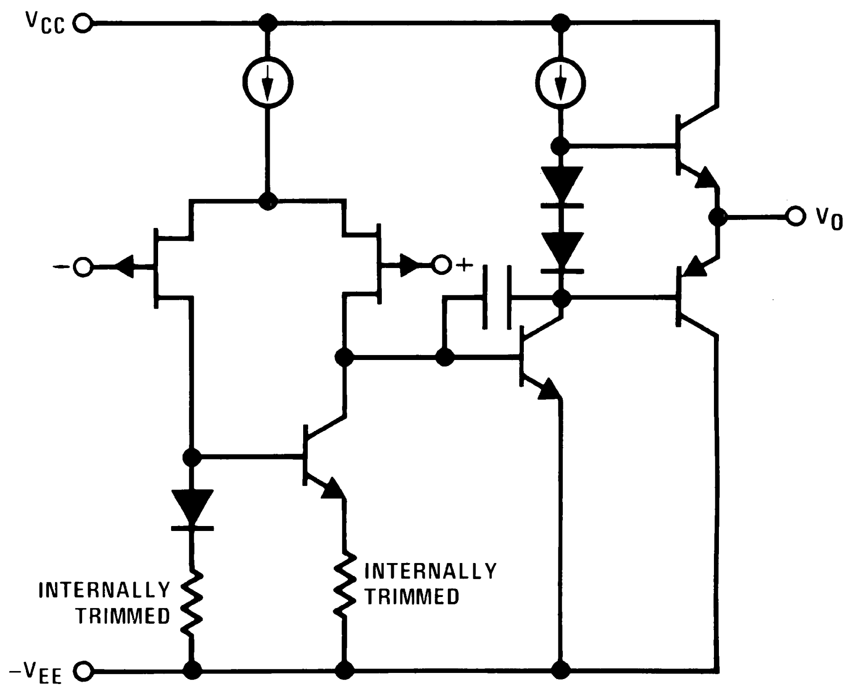
AC Electrical Characteristics[1][2]

Symbol	Parameter	Conditions	LF442A			LF442			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		pA/√Hz
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		pA/√Hz

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±20V for the LF442A and for V_S = ±15V for the LF442. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.
(2) Refer to RETS442X for LF442MH military specifications.

SIMPLIFIED SCHEMATIC

1/2 Dual



Typical Performance Characteristics

Input Bias Current

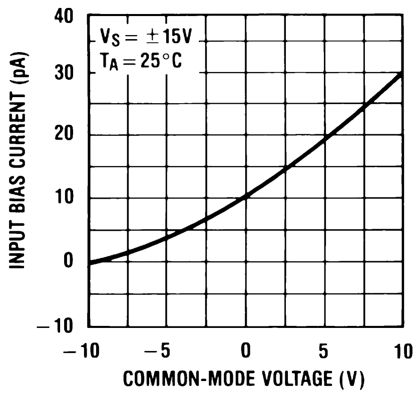


Figure 1.

Input Bias Current

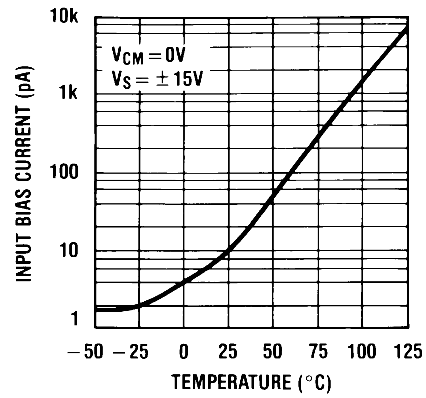


Figure 2.

Supply Current

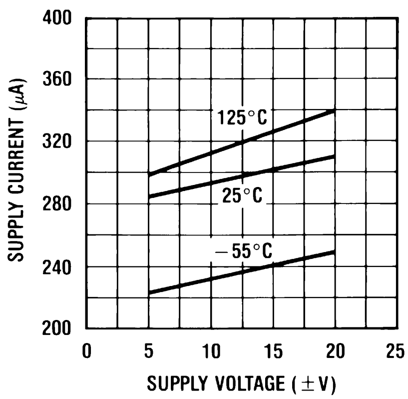


Figure 3.

Positive Common-Mode Input Voltage Limit

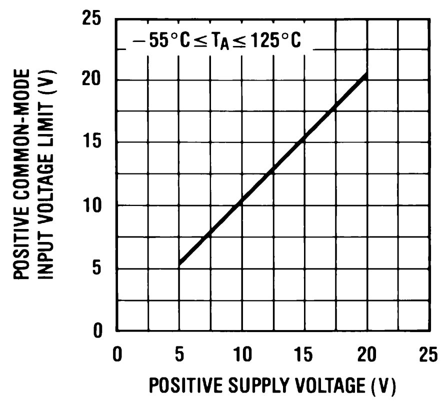


Figure 4.

Negative Common-Mode Input Voltage Limit

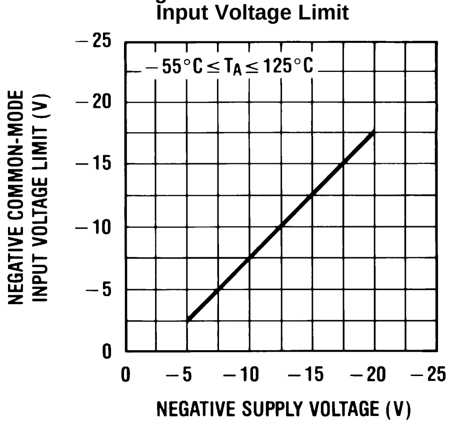


Figure 5.

Positive Current Limit

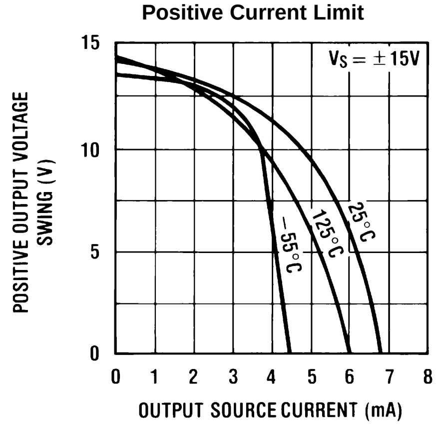


Figure 6.

Typical Performance Characteristics (continued)

Negative Current Limit

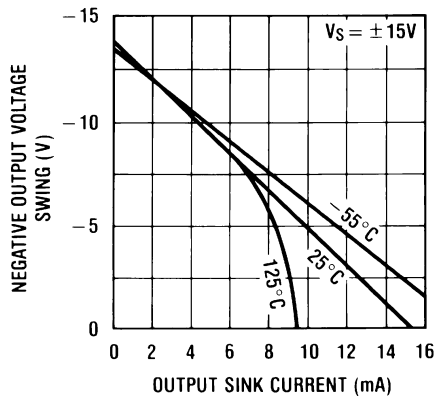


Figure 7.

Output Voltage Swing

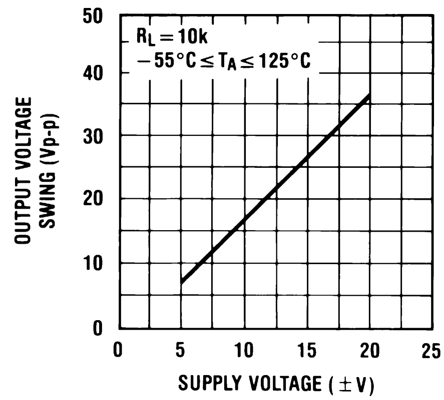


Figure 8.

Output Voltage Swing

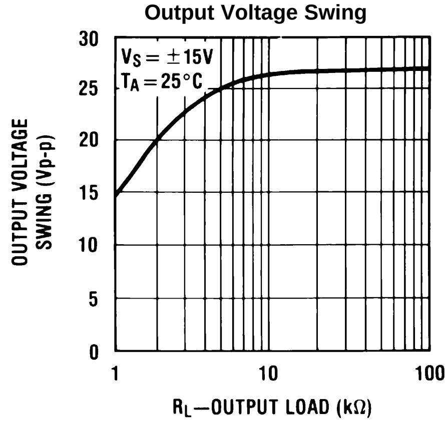


Figure 9.

Gain Bandwidth

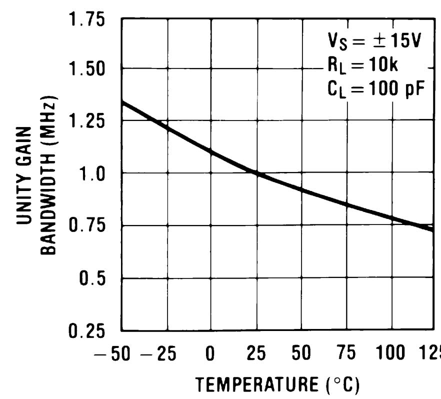


Figure 10.

Bode Plot

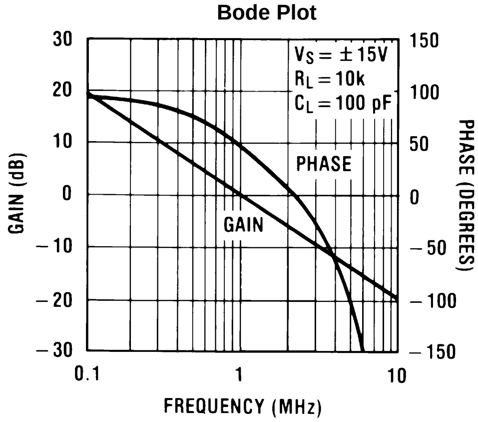


Figure 11.

Slew Rate

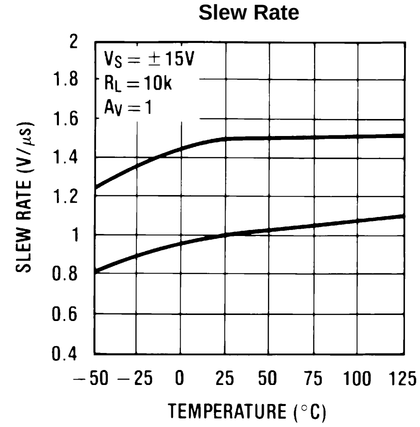


Figure 12.

Typical Performance Characteristics (continued)

Distortion vs Frequency

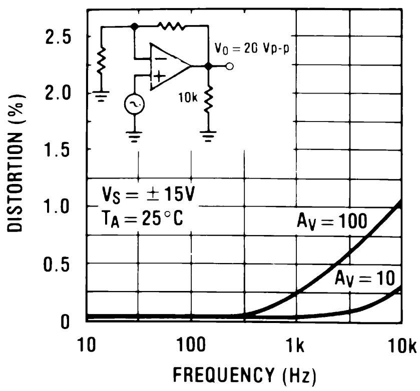


Figure 13.

Undistorted Output Voltage Swing

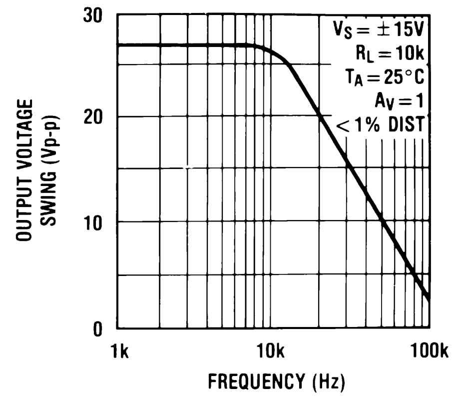


Figure 14.

Open Loop Frequency Response

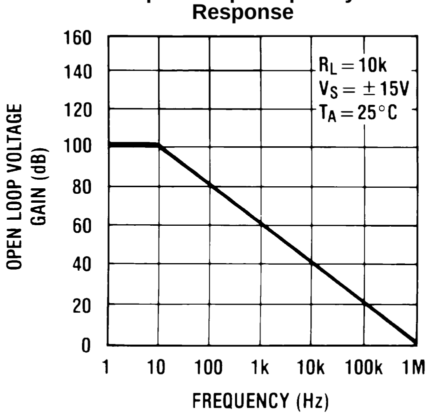


Figure 15.

Common-Mode Rejection Ratio

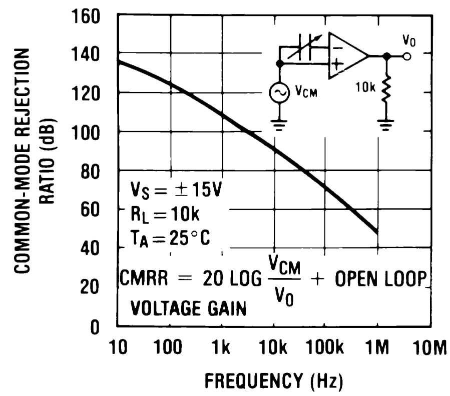


Figure 16.

Power Supply Rejection Ratio

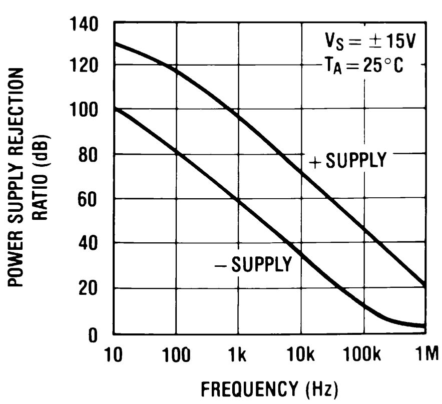


Figure 17.

Equivalent Input Noise Voltage

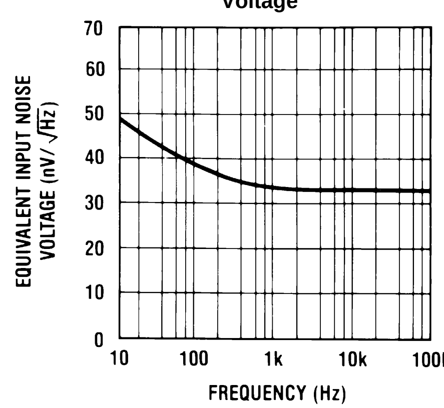


Figure 18.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain

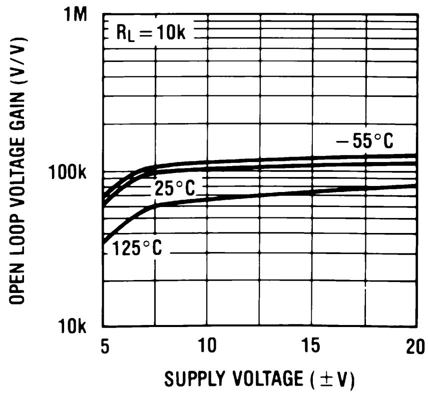


Figure 19.

Output Impedance

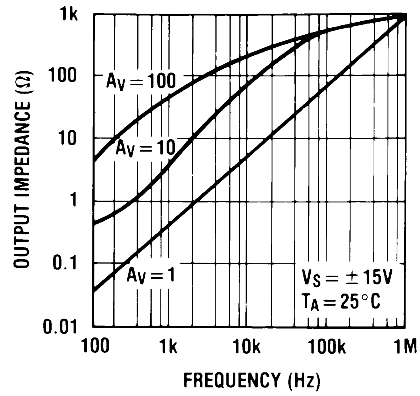


Figure 20.

Inverter Settling Time

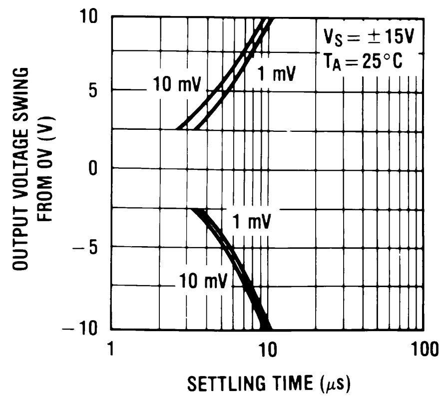


Figure 21.

Typical Performance Characteristics (continued)

Pulse Response

R_L = 10 kΩ, C_L = 10 pF

Small Signal Inverting

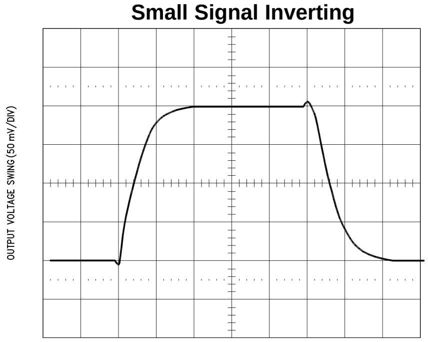


Figure 22.

Small Signal Non-Inverting

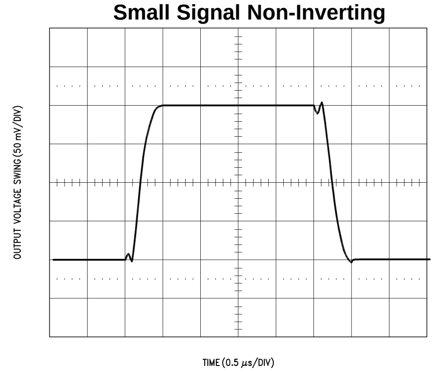


Figure 23.

Large Signal Inverting

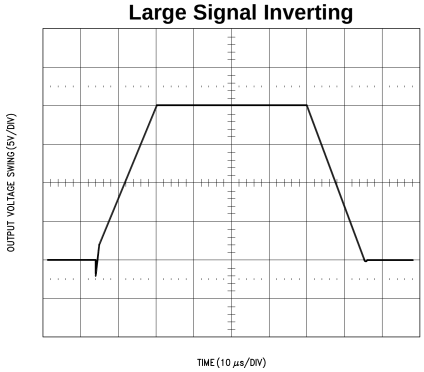


Figure 24.

Large Signal Non-Inverting

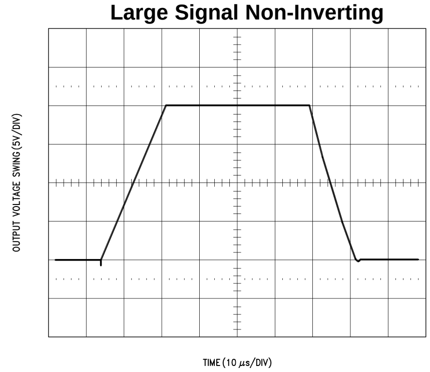


Figure 25.

APPLICATION HINTS

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

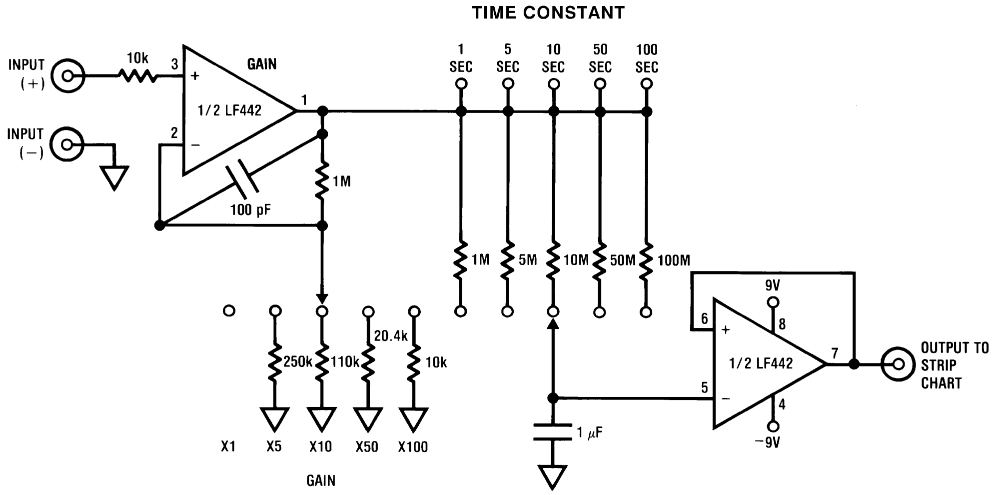
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

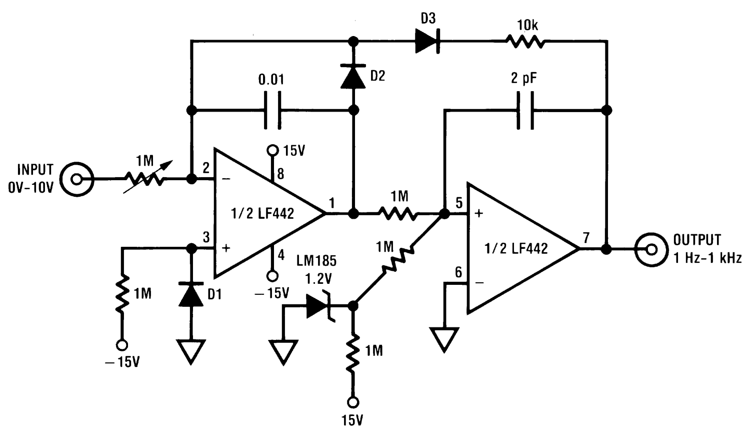
Typical Applications

Battery Powered Strip Chart Preamplifier



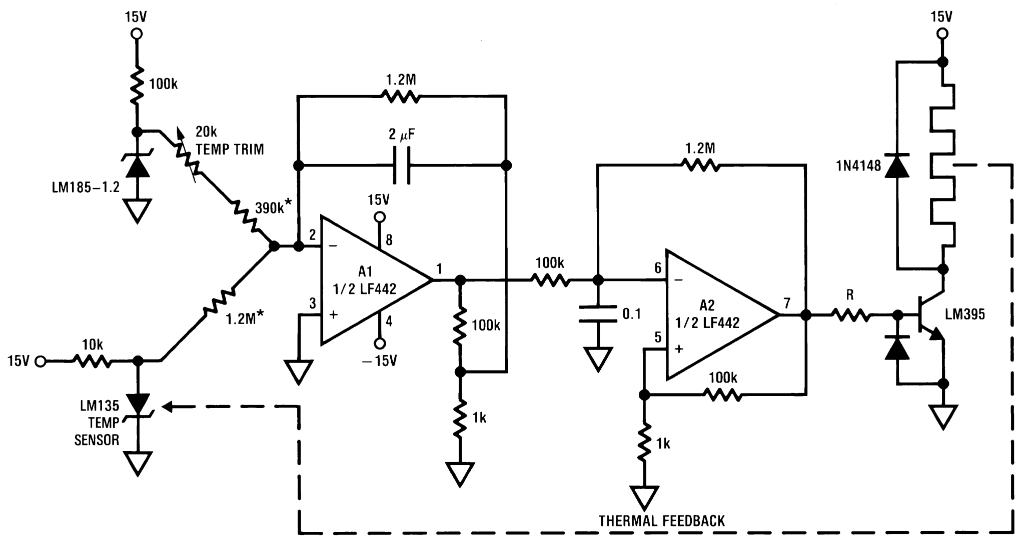
Runs from 9v batteries (±9V supplies)
Fully settable gain and time constant
Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

"No FET" Low Power V→F Converter



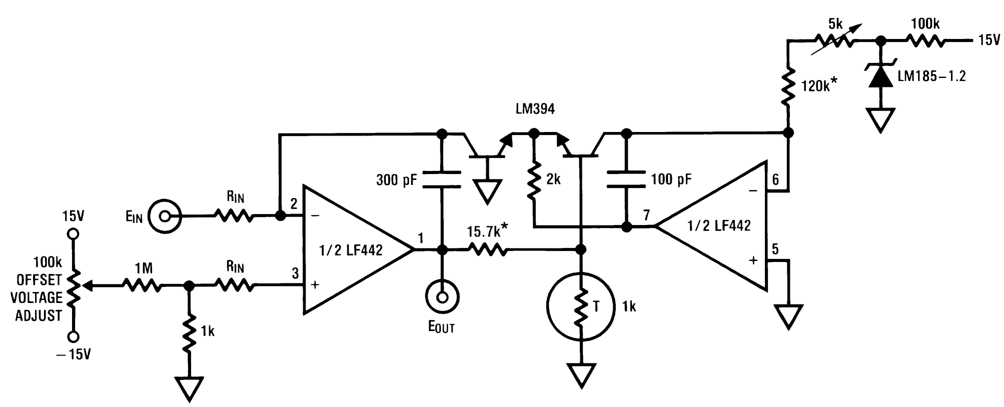
Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

High Efficiency Crystal Oven Controller



- $T_{control}$= 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor

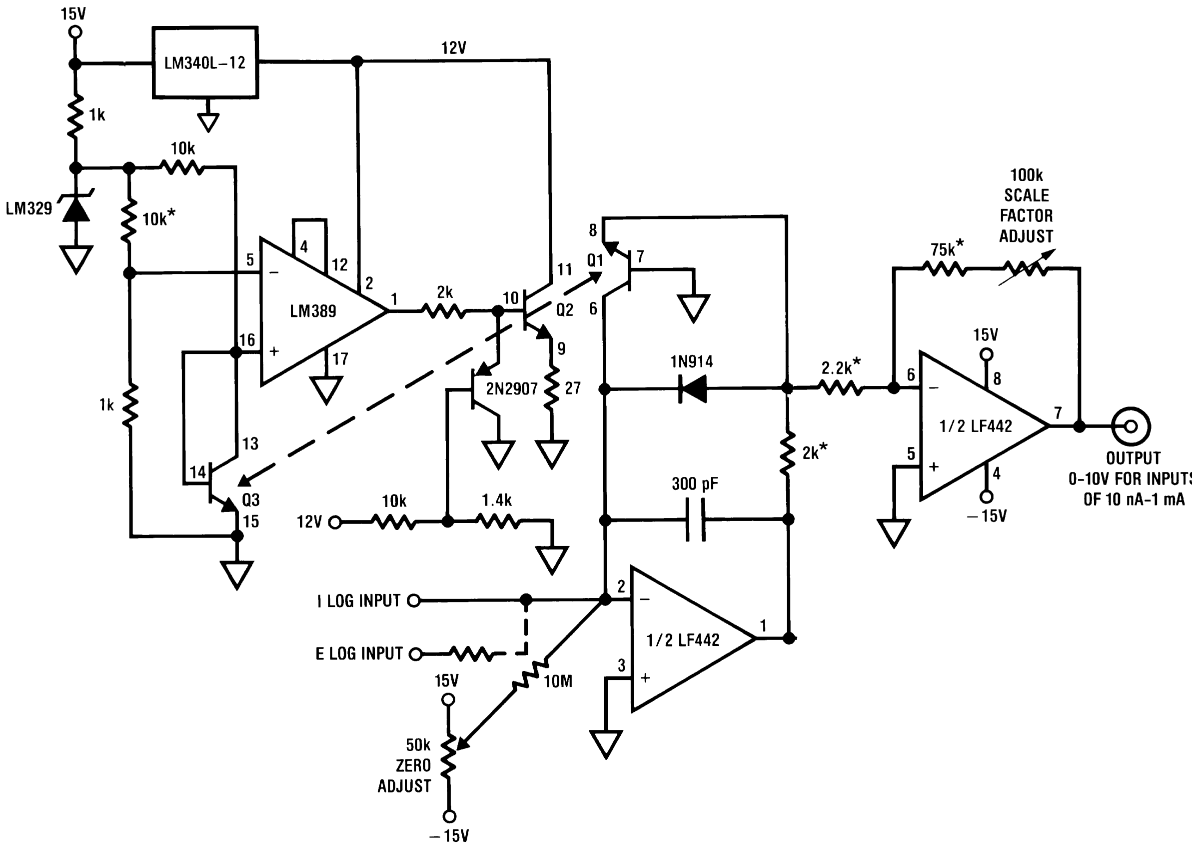
Conventional Log Amplifier



$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81
Trim 5k for 10 µA through the 5k–120k combination
*1% film resistor

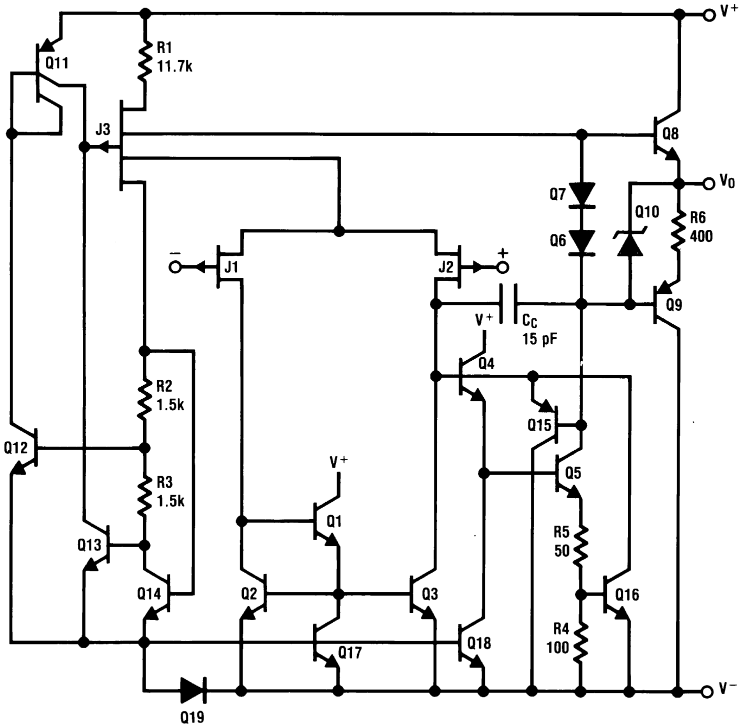
Unconventional Log Amplifier



Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

Detailed Schematic

1/2 Dual



REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LF442ACN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LF 442ACN	Samples
LF442ACN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 70	LF 442ACN	Samples
LF442AMH	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	LF442AMH	Samples
LF442AMH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LF442AMH	Samples
LF442CN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LF 442CN	Samples
LF442CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	LF 442CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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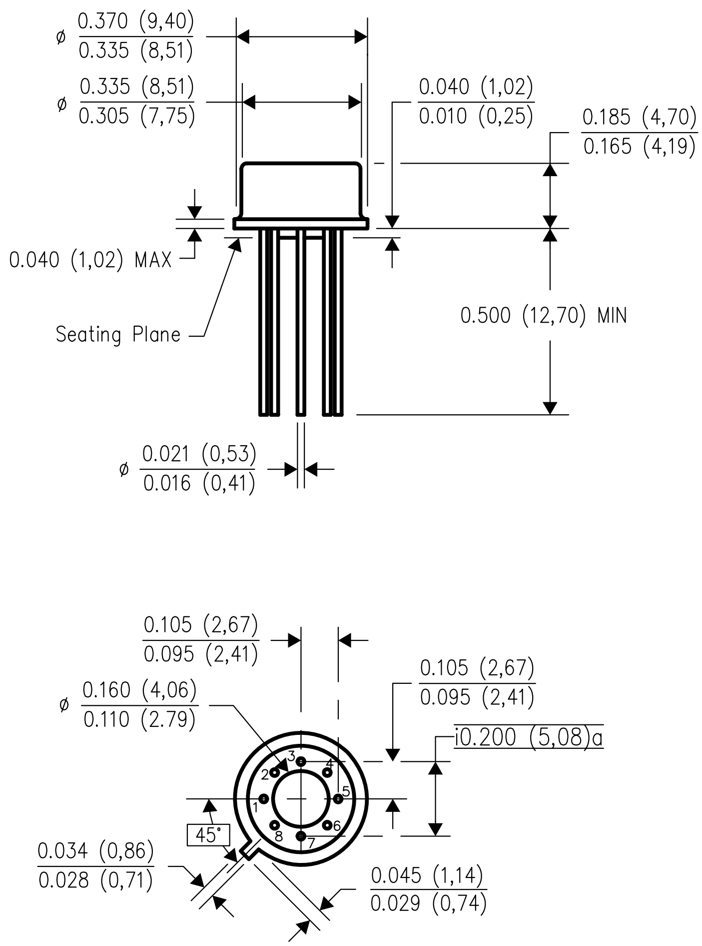
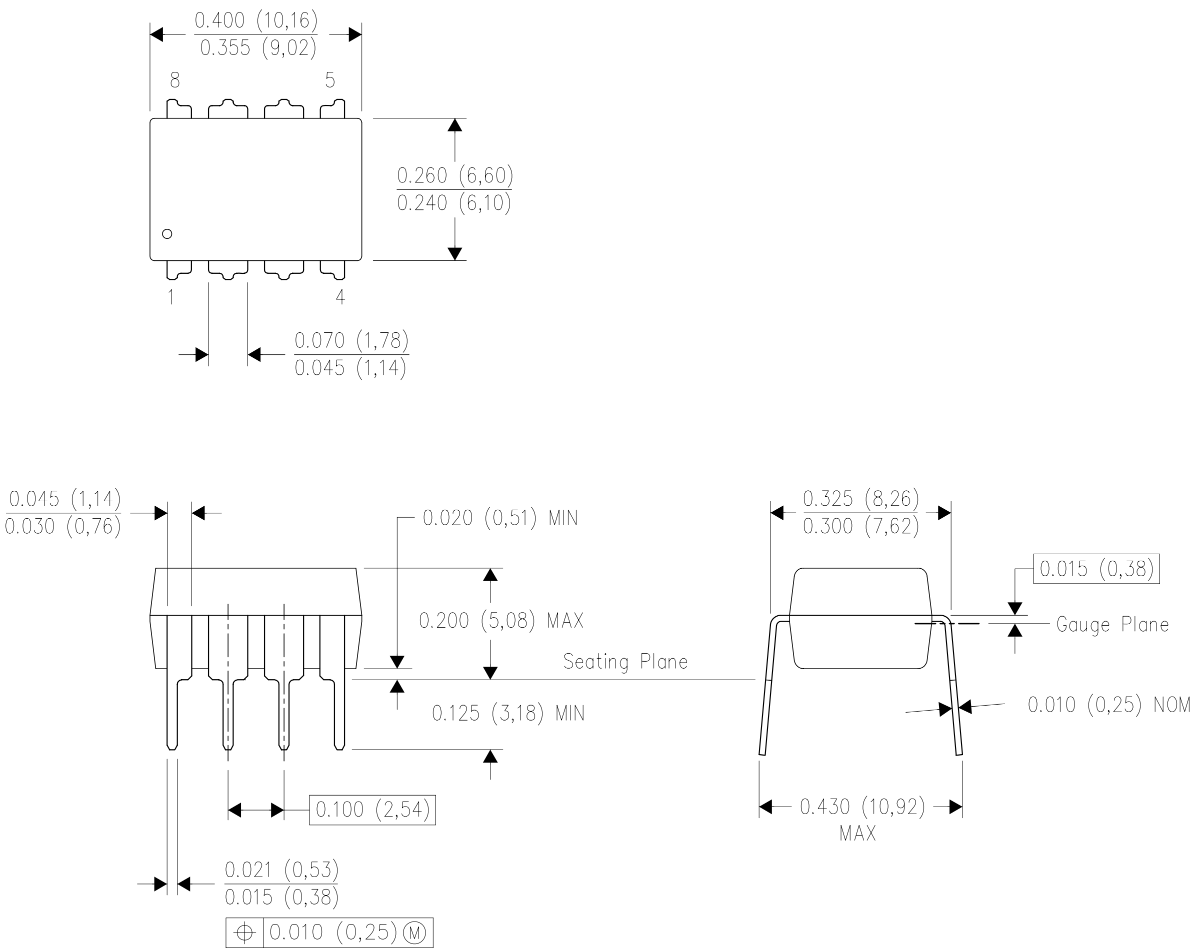
LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO-002/TO-99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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