REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case 2 for vendor CAGE 06665 and vendor CAGE 24355. Change to Standardized Military Drawing CAGE code 67268. Add testing at temperature for dynamic and ac tests. Editorial changes throughout.	90-01-30	M. A. Frye
B	Changes in accordance with NOR 5962-R006-94.	93-10-15	M. A. Frye
C	Drawing updated to reflect current requirements. Editorial changes throughout. – drw	01-02-21	Raymond Monnin
D	Redraw. Update paragraphs to new boilerplate requirements. - drw	11-11-07	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D								
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10								

PMIC N/A

PREPARED BY
Joseph A. Kerby

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-06-01

REVISION LEVEL
D

MICROCIRCUIT, LINEAR, 8-BIT QUAD DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-87802**

SHEET 1 OF 10

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87802	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	7226	Four 8-bit digital-to-analog converters with output amplifiers

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND or DGND	-0.3 V dc to +17.0 V dc
V_{DD} to V_{SS}	-0.3 V dc to +24.0 V dc
AGND to DGND	-0.3 V dc to V_{DD}
Digital input voltage to DGND	-0.3 V dc to V_{DD}
V_{REF} to AGND	-0.3 V dc to V_{DD}
V_{OUT} to AGND 2/	V_{SS} to V_{DD}
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 3/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R and 2	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Power supply range (V_{DD})	+11.4 V dc to +16.5 V dc
Input reference voltages:	
Dual supply operation	+2.0 V dc to V_{DD}-4 V dc
Single supply operation	+10.0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Unless otherwise specified all voltages are referenced to ground.
2/ Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.
3/ For temperatures above +75°C derate linearly at 2.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics (dual supply).

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current from V_{DD}	I_{DD}	Outputs unloaded, $V_{IN} = V_{INL}$ or V_{INH}	1, 2, 3	All		13.0	mA
Supply current from V_{SS}	I_{SS}	Outputs unloaded, $V_{IN} = V_{INL}$ or V_{INH}	1, 2, 3	All		11.0	mA
Reference voltage	V_{REF}		1, 2, 3	All	2.0	V_{DD} - 4	V
Reference input resistance	R_I		1, 2, 3	All	2		kΩ
Reference input capacitance	C_{IN}	Each DAC loaded with all 1's see 4.3.1c	4	All		300	pF
Total unadjusted error		V_{DD} = +15 V ±5%, V_{REF} = +10 V	1, 2, 3	All		±2	LSB
Relative accuracy			1, 2, 3	All		±1	LSB
Differential nonlinearity		Guaranteed monotonic	1, 2, 3	All		±1	LSB
Full scale error			1, 2, 3	All		±1.5	LSB
Zero code error			1, 2, 3	All		±30	mV
Input high voltage	V_{INH}		1, 2, 3	All	2.4		V
Input low voltage	V_{INL}		1, 2, 3	All		0.8	V
Input leakage current	I_{lkg}	V_{IN} = 0 V or V_{DD}	1, 2, 3	All		±1	µA
Functional tests		See 4.3.1d	7	All			
Voltage output slew rate 2/	SR		4, 5, 6	All	2.5		V/µs
Voltage output settling time (pos. full scale change) 2/	t_{tot}	Settling time to ±1/2 LSB V_{REF} = +10 V	4, 5, 6	All		5.0	µs
Voltage output settling time (neg. full scale change) 2/	t_{tot}	Settling time to ±1/2 LSB V_{REF} = +10 V	4, 5, 6	All		7.0	µs
Load resistance	R_O	V_{OUT} = +10 V	4	All	2.0		kΩ
Address to write setup time	t_{AS}		9, 10,11	All	0.0		ns
Address to write hold time	t_{AH}		9, 10,11	All	10.0		ns
Data valid to write setup time	t_{DS}		9	All	90		ns
			10,11		100		
Data valid to write hold time	t_{DH}		9, 10, 11	All	10.0		ns
Write pulse width	t_{WR}		9	All	150		ns
			10, 11		250		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (single supply) - continued.

Test	Symbol	Conditions 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current from V_{DD}	I_{DD}	Outputs unloaded, $V_{IN} = V_{INL}$ or V_{INH}	1, 2, 3	All		13.0	mA
Reference input resistance	R_I		1, 2, 3	All	2		kΩ
Reference input capacitance	C_{IN}	Each DAC loaded with all 1's see 4.3.1c	4	All		300	pF
Total unadjusted error			1, 2, 3	All		±2	LSB
Differential nonlinearity		Guaranteed monotonic	1, 2, 3	All		±1	LSB
Input high voltage	V_{INH}		1, 2, 3	All	2.4		V
Input low voltage	V_{INL}		1, 2, 3	All		0.8	V
Input leakage current	I_{Ikg}	V_{IN} = 0 V or V_{DD}	1, 2, 3	All		±1	µA
Functional tests		See 4.3.1d	7	All			
Voltage output slew rate 2/	SR		4, 5, 6	All	2.0		V/µs
Voltage output settling time (pos. full scale change) 2/	t_{tot}	Settling time to ±1/2 LSB V_{REF} = +10 V	4, 5, 6	All		5.0	µs
Voltage output settling time (neg. full scale change) 2/	t_{tot}	Settling time to ±1/2 LSB V_{REF} = +10 V	4, 5, 6	All		20.0	µs
Load resistance	R_O	V_{OUT} = +10 V	4	All	2.0		kΩ
Address to write setup time	t_{AS}		9, 10,11	All	0.0		ns
Address to write hold time	t_{AH}		9, 10,11	All	10.0		ns
Data valid to write setup time	t_{DS}		9	All	90		ns
			10,11		100		
Data valid to write hold time	t_{DH}		9, 10, 11	All	10.0		ns
Write pulse width	t_{WR}		9	All	150		ns
			10, 11		250		

1/ V_{DD} = 11.4 V to 16.5 V; V_{SS} = -5 V ±10%; AGND = DGND = 0.0 V; V_{REF} = 2 V to (V_{DD} – 4 V) (unless otherwise specified).
2/ Guaranteed if not tested to the limits specified.
3/ V_{DD} = +15 V ±5%; V_{SS} = AGND = DGND = 0.0 V; V_{REF} = +10 V (unless otherwise specified).

Device type	01
Case outline	R and 2
Terminal number	Terminal symbol
1	V_{OUT} B
2	V_{OUT} A
3	V_{SS}
4	V_{REF}
5	AGND
6	DGND
7	DB7 (MSB)
8	DB6
9	DB5
10	DB4
11	DB3
12	DB2
13	DB1
14	DB0 (LSB)
15	$\overline{WR}$
16	A1
17	A0
18	V_{DD}
19	V_{OUT} D
20	V_{OUT} C

FIGURE 1. Terminal connections.

Control inputs			Operation
$\overline{WR}$	A1	A0	
H	X	X	No operation device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = Low state, H = High state, X = Don't care

FIGURE 2. Truth table.

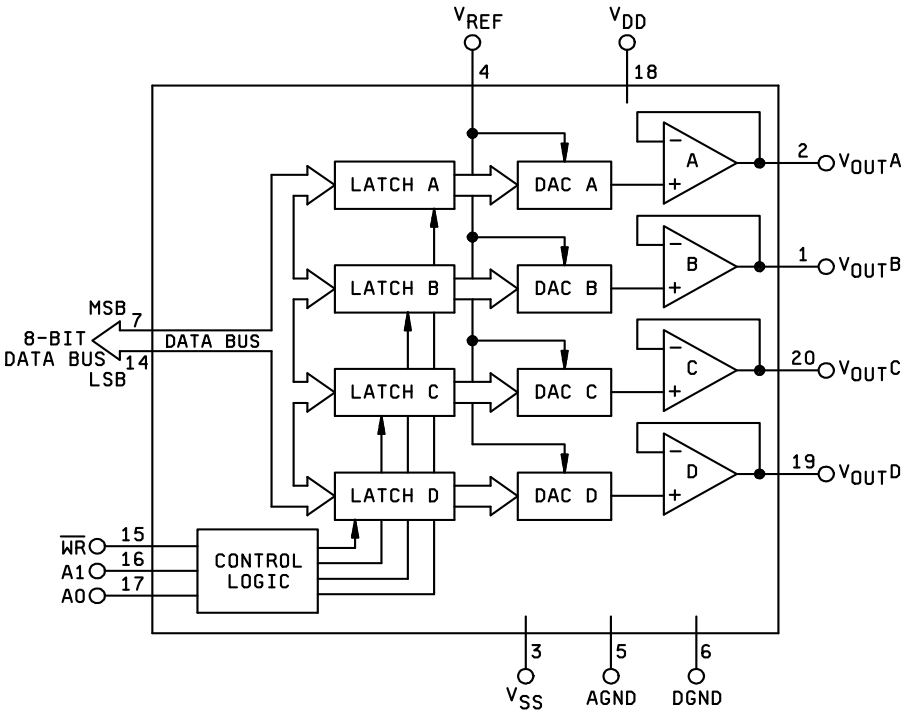


FIGURE 3. Functional block diagram.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 9, (10, 11)**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 tests shall verify the truth table on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-11-07

Approved sources of supply for SMD 5962-87802 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-87802012A	24355	AD7226TE/883B
	01295	TLC7226MFKB
5962-87802012C	01295	TLC7226MFKB
	1ES66	MX7226TE/883B
	3/	PM7226ARC/883
5962-8780201RA	24355	AD7226TQ/883B
	1ES66	MX7226TQ/883B
	3/	PM7226AR/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland
1ES66	Maxim Integrated Products 120 San Gabriel Dr Sunnyvale, CA 94086-5125
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

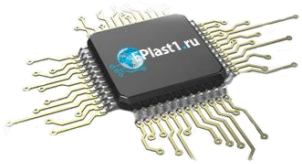
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.