NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
ISL9106

ISL6273

1.2A Low Quiescent Current 1.5MHz High Efficiency Synchronous Buck Regulator

FN9256
Rev 0.00
March 7, 2006

ISL6273 is a 1.2A, 1.5MHz step-down regulator, which is ideal for powering low-voltage microprocessors in compact devices such as PDAs and cellular phones. It is optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.7V to 5.5V allowing the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has guaranteed minimum output current of 1.2A. 1.5MHz pulse-width modulation (PWM) switching frequency allows using small external components. It has flexible operation mode selection of forced PWM mode and low IQ mode with as low as 25µA quiescent current for highest light load efficiency to maximize battery life.

The ISL6273 includes a pair of low on-resistance P-channel and N-channel internal MOSFETs to maximize efficiency and minimize external component count. 100% duty-cycle operation allows less than 200mV dropout voltage at 1.2A.

The ISL6273 offers a 200ms Power-On-Reset (POR) timer at power up. The timer output can be reset by RSI. When shutdown, ISL6273 discharges the output capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown.

The ISL6273 is offered in a 10 Ld 3x3mm DFN package with 1mm maximum height. The complete converter occupies less than 1 cm^2 area.

Ordering Information

PART NUMBER (NOTE)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6273IRZ	273Z	-40 to 85	10 Ld 3x3 DFN	L10.3x3C
ISL6273IRZ-T	273Z	-40 to 85	10 Ld 3x3 DFN	L10.3x3C

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

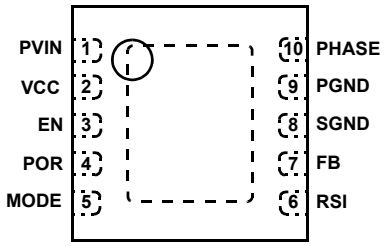
- High efficiency Synchronous Buck Regulator with up to 95% Efficiency
- 200ms Reset Timer
- Discharge Output Cap when Shutdown
- 2.7V to 5.5V Supply Voltage
- 3% Output Accuracy Over Temperature/Load/Line
- 1.2A Guaranteed Output Current
- 25µA Quiescent Supply Current in IQ Mode
- Selectable Forced PWM Mode and IQ Mode
- Less than 1µA Logic Controlled Shutdown Current
- 100% Maximum Duty Cycle for Lowest Dropout
- Internal Loop Compensation
- Internal Digital Soft-Start
- Peak Current Limiting, Short Circuit Protection
- Over-Temperature Protection
- Enable
- Small 10 Ld 3x3mm DFN
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Single Li-Ion Battery-Powered Equipment
- DSP Core Power
- PDAs and Palmtops

Pinout

ISL6273 (10 LD 3X3 DFN)
TOP VIEW



Absolute Maximum Ratings (Reference to SGND)

Supply Voltage (PVIN, VCC) . . . . . -0.3V to 6.5V
EN, RSI, MODE, PHASE, POR . . . . . -0.3V to VCC+0.3V
FB . . . . . -0.3V to 2.7V
PGND. . . . . -0.3V to 0.3V

Recommended Operating Conditions

PVIN Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 1.2A
Ambient Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package	44	5.5

Junction Temperature Range. . . . . -40°C to 125°C
Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specification are measured at the following conditions: T_A = 25°C, V_{PVIN} = V_{VCC} = 3.6V, EN = VCC, RSI = 0V, MODE = VCC, L = 1.8µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A (see the Typical Application Circuit).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
VCC Undervoltage Lockout Threshold	V_{UVLO}	Rising	-	2.5	2.7	V
		Falling	2.2	2.4	-	V
Quiescent Supply Current	I_{PVIN}	MODE = VCC, no load at the output	-	25	50	µA
		MODE = SGND, no load at the output	-	5	8	mA
Shut Down Supply Current	I_{SD}	VCC = PVIN = 5.5V, EN = low	-	0.1	2	µA
OUTPUT REGULATION						
FB Regulation Voltage	V_{FB}	T_A = 0°C to 85°C	0.784	0.8	0.816	V
		T_A = -40°C to 85°C	0.78	0.8	0.82	V
FB Bias Current	I_{FB}	FB = 0.75V	-	0.1	-	µA
Output Voltage Accuracy		PVIN = V_O + 0.5V to 5.5V, Io = 0 to 1.2A , T_A = -40°C to 85°C	-3	-	3	%
Line Regulation		PVIN = V_O + 0.5V to 5.5V (minimal 2.7V)	-	0.2	-	%/V
Maximum Output Current			1.2	-	-	A
COMPENSATION						
Error Amplifier Trans-conductance		Adjustable version, design info only	-	20	-	µA/V
PHASE						
P-Channel MOSFET On Resistance		PVIN = 3.6V, Io = 200mA	-	0.12	0.22	Ω
		PVIN = 2.7V, Io = 200mA	-	0.16	0.27	Ω
N-Channel MOSFET On Resistance		PVIN = 3.6V, Io = 200mA	-	0.11	0.22	Ω
		PVIN = 2.7V, Io = 200mA	-	0.15	0.27	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		1.5	2.1	2.6	A
PHASE Maximum Duty Cycle			-	100	-	%
PWM Switching Frequency	f_S	T_A = -40°C to 85°C	1.35	1.5	1.75	MHz
PHASE Minimum On Time		MODE = low (forced PWM mode)	-	-	140	ns
Soft Start-Up Time			-	1.1	-	ms

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specification are measured at the following conditions: T_A = 25°C, V_{PVIN} = V_{VCC} = 3.6V, EN = VCC, RSI = 0V, MODE = VCC, L = 1.8µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A (see the Typical Application Circuit).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POR						
Output Low Voltage		Sinking 1mA, FB = 0.7V	-	-	0.3	V
Delay Time			150	200	275	ms
POR Pin Leakage Current		POR = VCC = 3.6V	-	0.01	0.1	µA
Minimum Supply Voltage for Valid POR Signal			1.2	-	-	V
Internal PGOOD Low Rising Threshold		Percentage of Nominal Regulation Voltage	89.5	92	94.5	%
Internal PGOOD Low Falling Threshold		Percentage of Nominal Regulation Voltage	85	88	91	%
Internal PGOOD High Rising Threshold		Percentage of Nominal Regulation Voltage	105.5	108	110.5	%
Internal PGOOD High Falling Threshold		Percentage of Nominal Regulation Voltage	102	105	108	%
Internal PGOOD Delay Time			-	50	-	µs
EN, MODE, RSI						
Logic Input Low			-	-	0.4	V
Logic Input High			1.4	-	-	V
Logic Input Leakage Current		Pulled up to 5.5V	-	0.1	1	µA
Thermal Shutdown			-	150	-	°C
Thermal Shutdown Hysteresis			-	25	-	°C

Typical Operating Performance

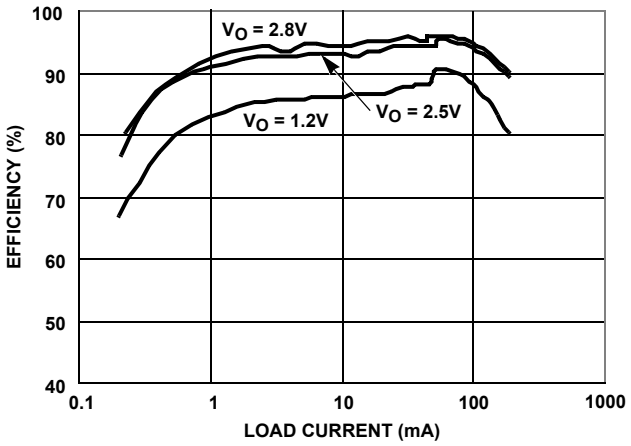


FIGURE 1. EFFICIENY vs LOAD CURRENT (V_{IN} = 3.6V)

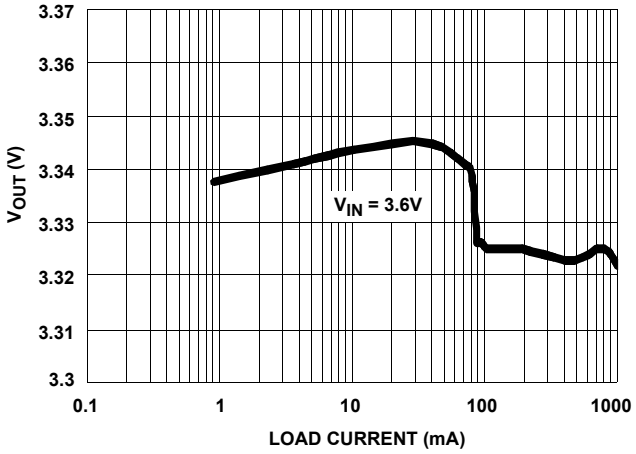


FIGURE 2. V_{OUT} vs LOAD CURRENT (V_{IN} = 3.6V)

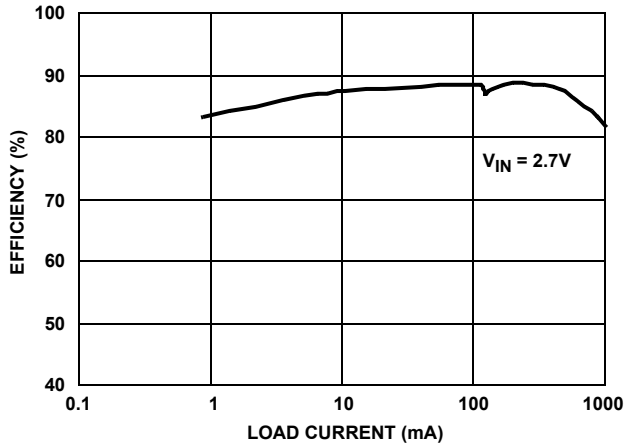


FIGURE 3. EFFICIENCY vs LOAD CURRENT (V_O = 1.8V)

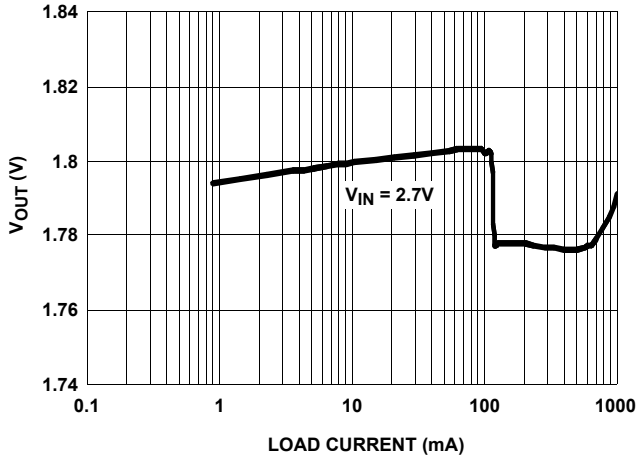


FIGURE 4. V_{OUT} vs LOAD CURRENT (V_{IN} = 2.7V)

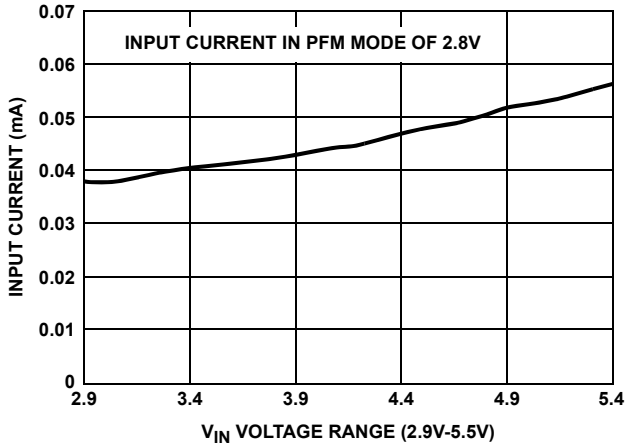


FIGURE 5. I_Q vs V_{IN} (PFM)

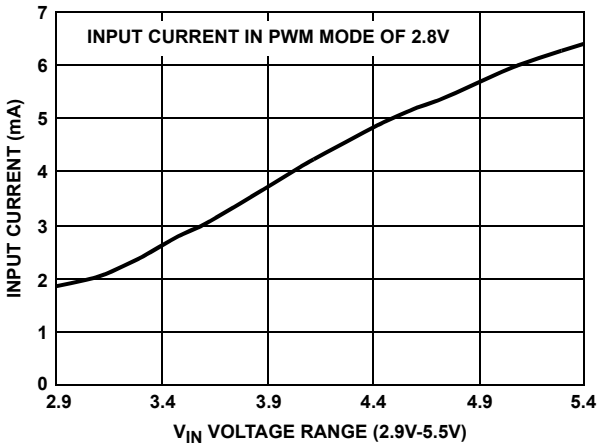


FIGURE 6. I_Q vs V_{IN} (PWM)

Typical Operating Performance (Continued)

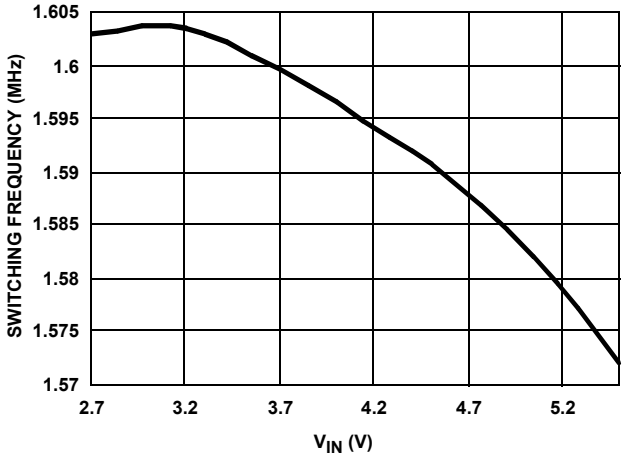


FIGURE 7. SWITCHING FREQUENCY vs V_{IN}

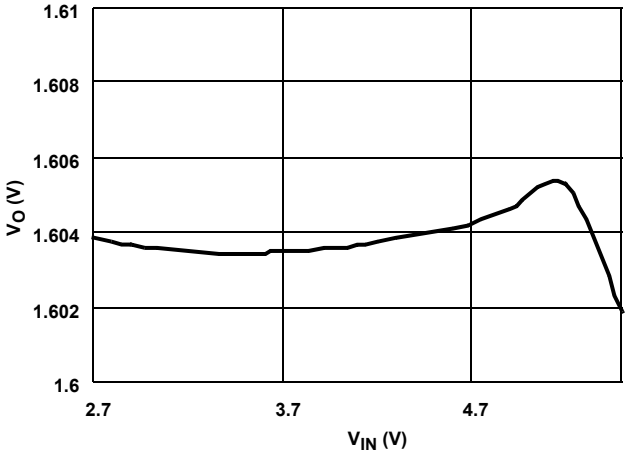


FIGURE 8. LINE REGULATION (I_O = 1A)

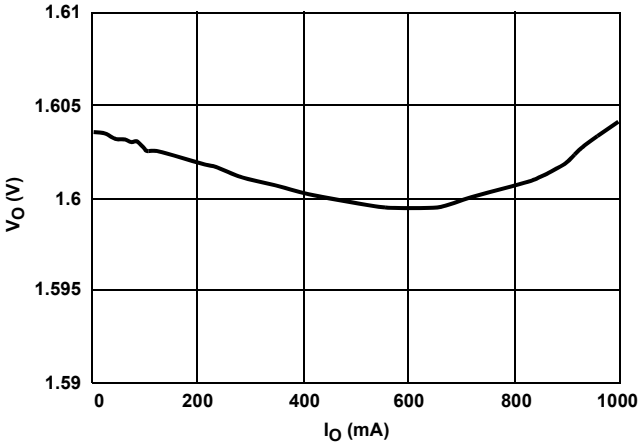


FIGURE 9. LOAD REGULATION (V_{IN} = 3.6V IN PWM MODE)

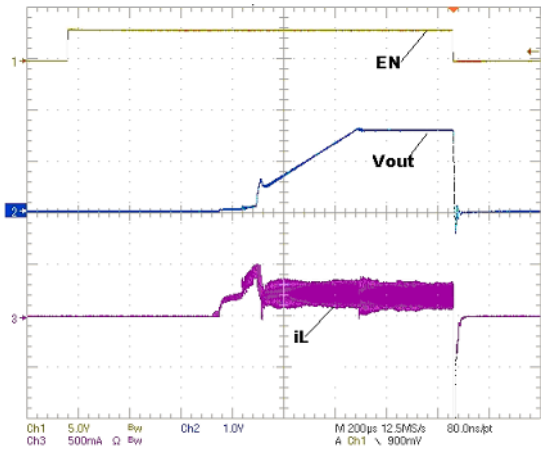


FIGURE 10. SOFT-START

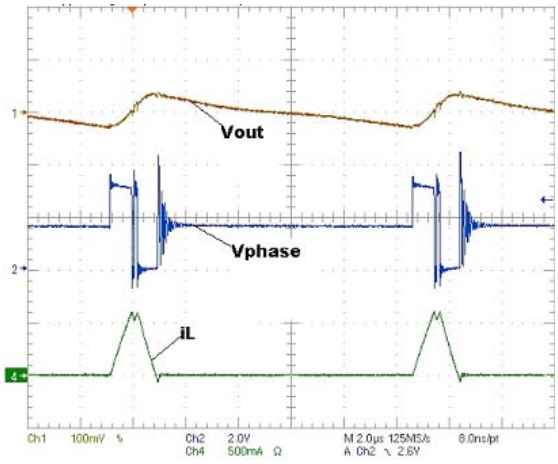


FIGURE 11. PFM MODE (V_{IN} = 3V; V_O = 1.6V; I_O = 50mA)

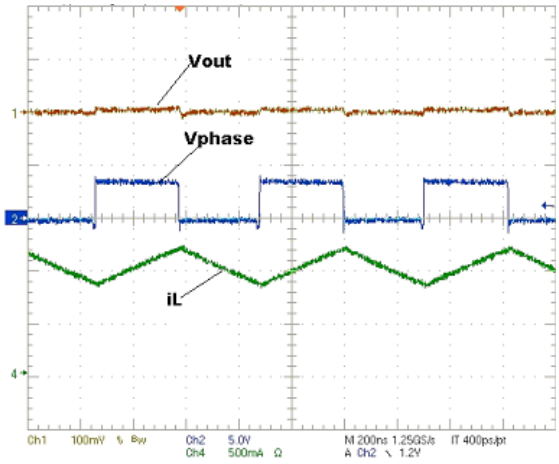


FIGURE 12. STEADY-STATE IN PWM MODE (V_{IN} = 3.6V; V_O = 1.6V; I_O = 1A)

Typical Operating Performance (Continued)

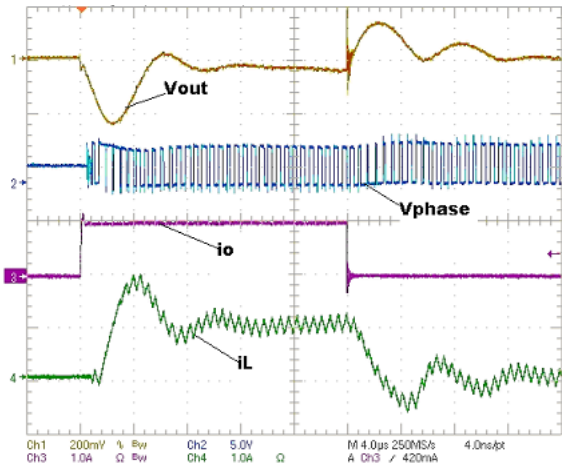


FIGURE 13. TRANSIENT LOAD TEST (PFM & PWM V_{IN} = 3.6V; V_O = 1.6V; I_O = 0A~1A)

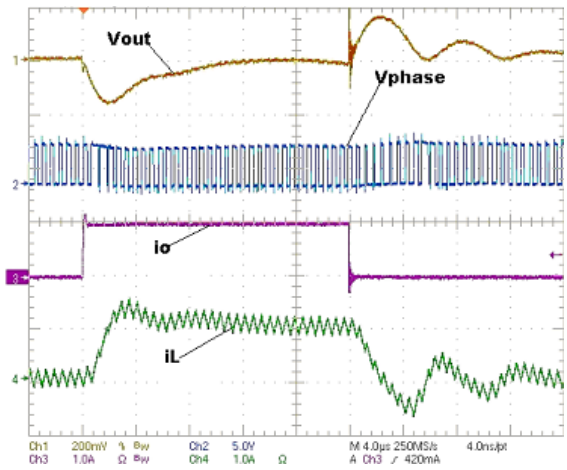


FIGURE 14. LOAD TRANSIENT IN PWM MODE (V_{IN} = 3.6V; V_O = 1.6V; I_O = 0A~1A)

Pin Descriptions

PVIN

Input supply voltage. Connect a 10µF ceramic capacitor to power ground.

VCC

Supply voltage for internal analog and digital control circuits, delivered from PVIN. Bypass with 0.1µF ceramic capacitor to signal ground.

EN

Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low. Do not leave this pin floating.

POR

200ms timer output. At power up or EN HI, this output is a 200ms delayed Power-Good signal for the output voltage. This output can be reset by a low RSI signal. 200ms starts when RSI goes to high.

MODE

Mode Selection pin. Connect to logic high or input voltage VCC for low IQ mode; connect to logic low or ground for forced PWM mode. Do not leave this pin floating.

PHASE

Switching node connection. Connect to one terminal of inductor.

PGND

Power ground. Connect all power grounds to this pin

SGND

Analog ground. SGND and PGND should only have one point connection.

FB

Buck regulator output feedback. Connect to the output through a resistor divider for adjustable output voltage (ISL6273-ADJ). For preset output voltage, connect this pin to the output.

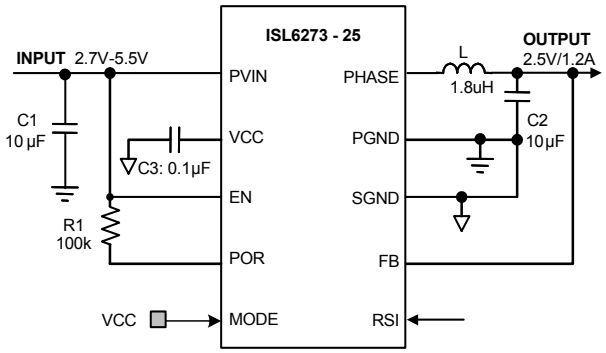
RSI

This input resets the 200ms timer. When the output voltage is within the PGOOD window, an internal timer is started and generates a POR signal 200ms later when RSI is low. A low RSI resets POR and RSI high to low transition restarts the internal counter if the output voltage is within the window, otherwise the counter is reset by the output voltage condition.

Exposed Pad

The exposed pad must be connected to the PGND pin for proper electrical performance. The exposed pad must also be connected to as much as possible for optimal thermal performance.

Typical Applications



PARTS	DESCRIPTION	MANUFACTURERS	PART NUMBER	SPECIFICATIONS	SIZE
L	Output inductor	Sumida	CDRH4D18 2R2	2.2µH/1.32A/58mΩ	5.0×5.0×2.0mm
		Coilcraft	1008PS-182M	1.8µH/1.9A/90mΩ	3.8x3.8x2.8mm
C1	Input capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V/3mΩ	2.0x1.25x1.25mm (0805)
C3	Bypass capacitor	Taiyo Yuden	EMK107BJ104MA	0.1µF/16V	1.6x0.8x0.8mm (0603)
C2	Output capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V/3mΩ	2.0x1.25x1.25mm (0805)
R1	Pull-up resistor	Various		100kΩ	1.6x0.8x0.45mm (0603)

FIGURE 15. TYPICAL APPLICATION FOR FIXED OUTPUT VERSION

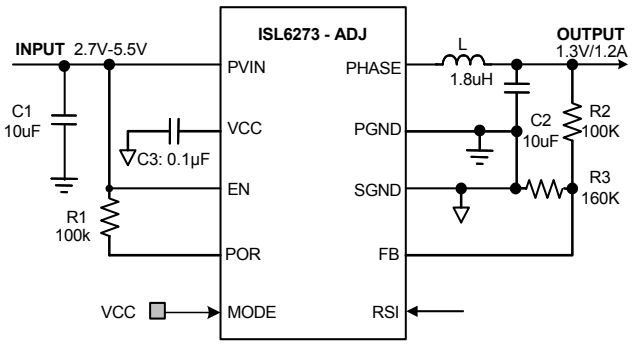
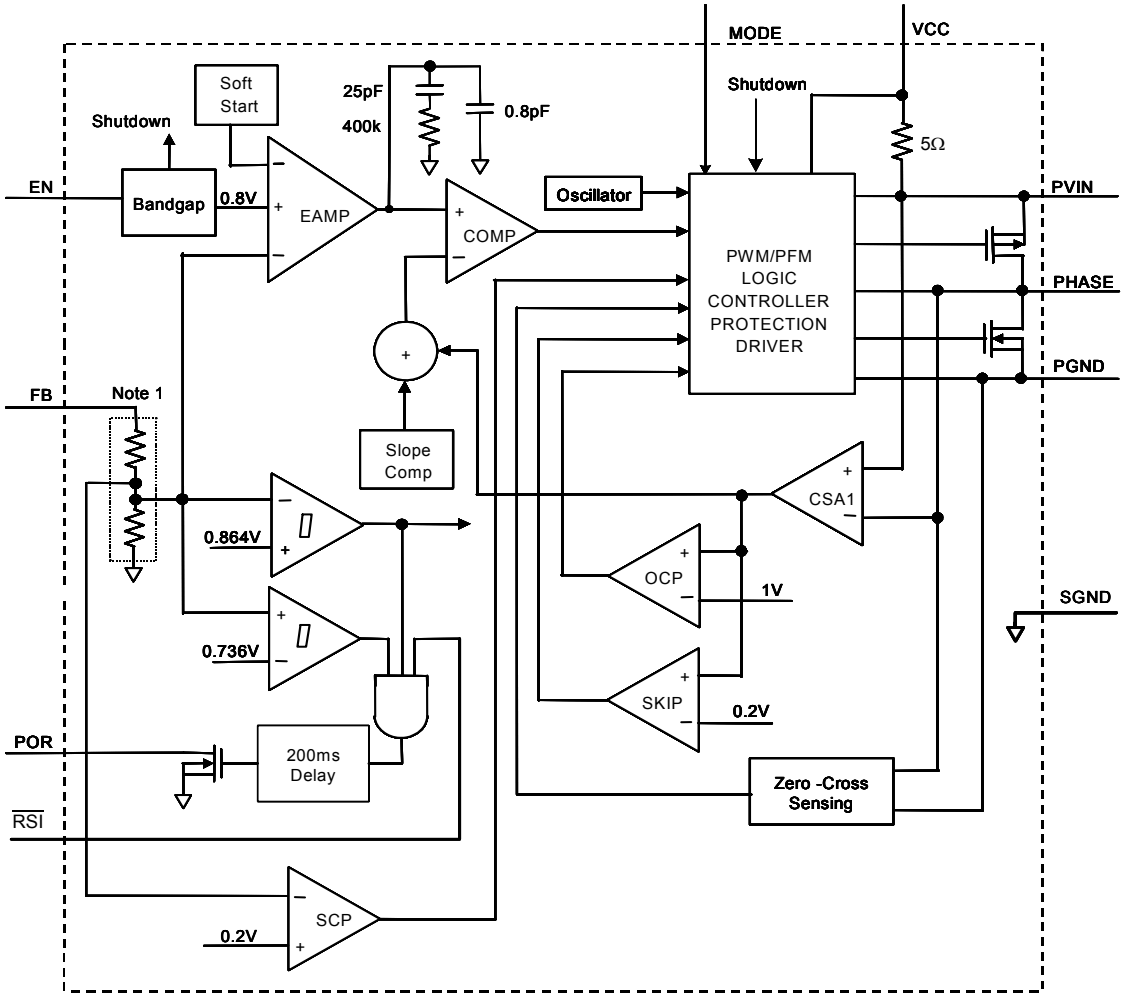


FIGURE 16. TYPICAL APPLICATION FOR ADJUSTABLE VERSION

Block Diagram



Note 1:
For adjustable output version, the internal feedback resistor divider is disabled and the FB pin is directly connected to the error amplifier.

FIGURE 17. FUNCTIONAL BLOCK DIAGRAM

Theory of Operation

The ISL6273 is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1.5MHz fixed switching frequency under heavy load condition to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 25µA. The supply current is typically only 0.1µA when the regulator is shut down. The ISL6273 has four fixed output voltage versions and one adjustable version.

PWM Control Scheme

The ISL6273 employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 17 shows the block diagram. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-channel MOSFET when it is turned on and the current sense amplifier CSA. The gain for the current sensing circuit is typically 0.4V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the compensation slope (0.675V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 18 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA output.

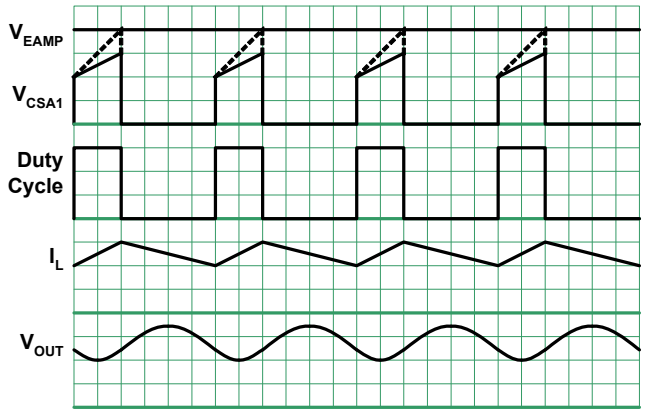


FIGURE 18. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the FB pin. The soft-start block only affects the operation during the start-up and will be discussed separately shortly. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 30pF and 300kΩ RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

SKIP Mode

The ISL6273 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the effective switching frequency. Figure 19 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 17 monitors the N-MOSFET current for zero crossing. When 8 consecutive cycles of the N-MOSFET crossing zero are detected, the regulator enters the skip mode. During the 8 detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

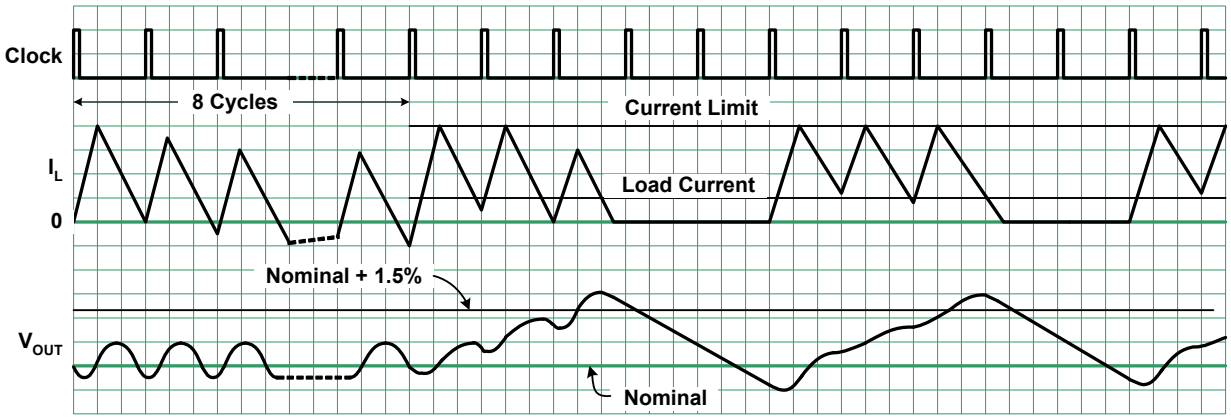


FIGURE 19. SKIP MODE OPERATION WAVEFORMS

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 17. Each pulse cycle is still synchronized by the PWM clock. The N-MOSFET is turned on at the clock and turned off when its current reaches 20% of the current limit value (0.2V at the CSA output). As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage reaches 1.5% above the nominal voltage, the P-MOSFET is turned off immediately. Then the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-MOSFET will be turned on again at the clock, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Mode Control

The ISL6273 has a MODE pin that controls the operation mode. When the MODE pin is driven to low or shorted to ground, the regulator operates in a forced PWM mode. The forced PWM mode remains the fixed PWM frequency at light load instead of entering the skip mode.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 17. The current sensing circuit has a gain of 0.4V/A, from the N-MOSFET current to the CSA output. When the CSA output reaches 1V, which is equivalent to 2.5A for the switch current, the OCP comparator is tripped to turn off the P-MOSFET immediately.

Short-Circuit Protection

A short-circuit protection SCP comparator monitors the FB pin voltage for output short-circuit protection. When the FB is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

POR Signal

The ISL6273 offers a power-on reset (POR) signal for resetting the microprocessor at the power up. When the output voltage is not within a power-good window, the POR pin outputs an open-drain low signal to reset the microprocessor. The output voltage is monitored through the FB pin. For the fixed output voltage versions, the monitoring node is the center of the resistive voltage divider. For the adjustable version, the FB pin voltage is monitored directly. When the voltage of the monitored node is within the window of 0.736V and 0.864V, a power-good signal is issued to turn off the open-drain POR pin. The rising edge of the POR output is delayed by 200ms.

RSI Signal

The RSI signal is a reset input control for the POR signal. The power-good signal is gated by the RSI signal, as shown in Figure 17. When the RSI is high, the POR signal will remain low, independent on the power good signal.

UVLO

When the input voltage is below the undervoltage lock out (UVLO) threshold, the regulator is disabled.

Soft Start-Up

The soft start-up eliminates the inrush current during the start-up. The soft start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency.

Figure 10 shows the start-up waveforms.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The on resistance for the P-MOSFET is typically150mΩ and the on resistance for the N-MOSFET is typically 150mΩ.

100% Duty Cycle

The ISL6273 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL6273 can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum drop out voltage under the 100% duty-cycle operation is the product of the load current and the on resistance of the P-MOSFET.

Enable

The enable (EN) input allows user to control the turning on or off the regulator for purposes such as power-up sequencing. The the regulator is enabled, there is typically a 300µs delay for waking up the bandgap reference. Then the soft start-up begins. When the regulator is disabled, the P-MOSFET is turned off immediately and the N-MOSFET is turned on.

Thermal Shut Down

The ISL6273 has built-in thermal protection. When the internal temperature reaches 150°C, the regulator is completely shut down. As the temperature drops to 130°C, the ISL6273 resumes operation by stepping through a soft start-up.

VCC By-Passing

The VCC is voltage is the supply to the internal control circuit and is derived from the PVIN pin. An internal 10Ω resistor connects the two pins and also serves as an filtering resistor. An external 0.1µF ceramic capacitor is recommended to by-pass the VCC supply.

Applications Information

Output Inductor and Capacitor Selection

To consider state steady and transient operation, ISL6273 typically uses a 1.8µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased as shown in Table 1. The inductor ripple current can be expressed as follows:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S}$$

The inductor's saturation current rating needs be at least larger than the peak current. The ISL6273 protects the peak current 2.1A. The saturation current needs be over 2.1A for maximum output current application.

ISL6273 uses internal compensation network and the output capacitor value is dependant on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values are shown in Table 1.

TABLE 1. OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT}	C_{OUT}	L
0.8V	10µF	1.0µH~2.2µH
1.2V	10µF	1.2µH~2.2µH
1.6V	10µF	1.8µH~2.2µH
1.8V	10µF	1.8µH~3.3µH
2.5V	10µF	1.8µH~3.3µH
3.3V	6.8µF	1.8µH~4.7µH
3.6V	4.7µF	1.8µH~4.7µH

In Table 1, the minimum output capacitor value is given for different output voltage to make sure the whole converter system stable. Due to the limitation on power dissipation when the regulator disable and discharge output capacitor, there is the maximum output capacitor value. The maximum output capacitor value is variable with the output voltage. The plot curve is shown in Figure 20.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. A 10µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection.

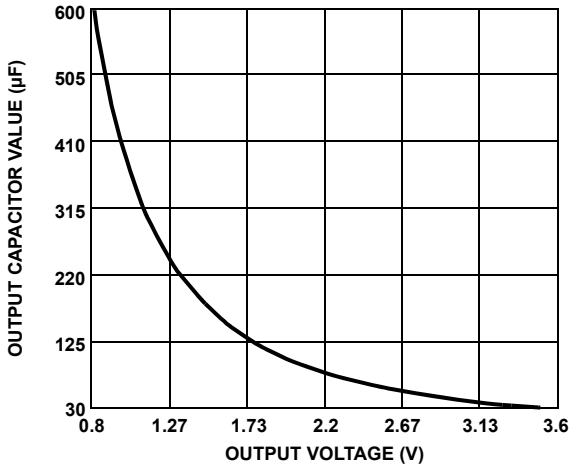


FIGURE 20. THE MAXIMUM CAP vs THE OUTPUT VOLTAGE

Output Voltage Setting Resistor Selection

The resistors R2 and R3 shown in Figure 16 set the output voltage for the adjustable version. The output voltage can be calculated by:

$$V_O = 0.8 \bullet \left(1 + \frac{R_2}{R_3}\right)$$

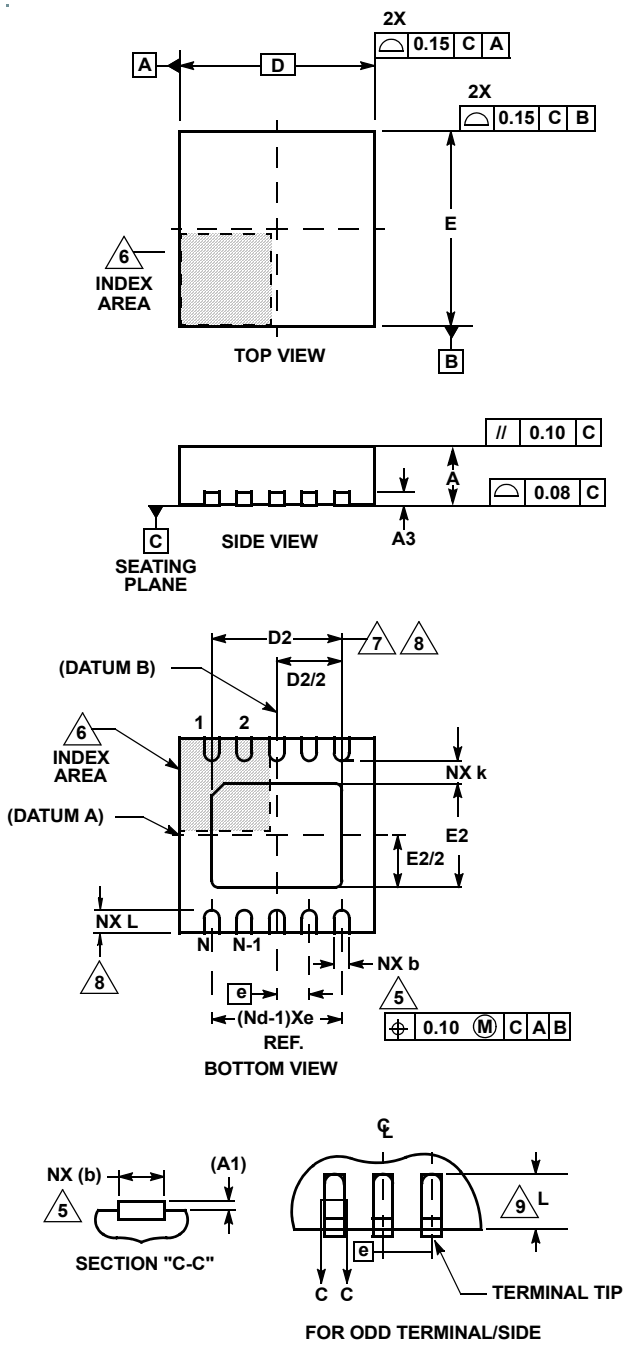
where the 0.8V is the reference voltage. The voltage divider consists of R2 and R3 increases the quiescent current by Vo/(R2+R3) so larger resistance is desirable. On the other hand, the FB pin has leakage current that will cause error in the output voltage setting. The leakage current has a typical value of 0.1µA. To minimize the accuracy impact on the output voltage, select the R3 no larger than 200kΩ.

Layout Recommendation

The layout is a very important converter design step to make sure the designed converter works well. For ISL6273 buck converter, the power loop is composed of the output inductor L, the output capacitor C_{OUT}, Phase pin and PGND pin. It is necessary to make the power loop as small as possible. In order to make the output voltage regulate well and avoid the noise couple from the power loop specially for PFM mode operation, SGND pin should be connected with PGND pin at the terminals of the load.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for EMI performance.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.23	2.38	2.48	7, 8
E		3.00 BSC		-
E2	1.49	1.64	1.74	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		10		2
Nd		5		3

Rev. 0 3/05

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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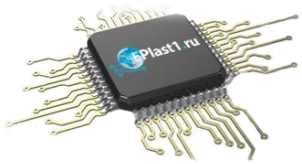
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.