

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7W74FU, TC7W74FK

D-Type Flip Flop with Preset and Clear

The TC7W74 is a high speed C²MOS D Flip Flop fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

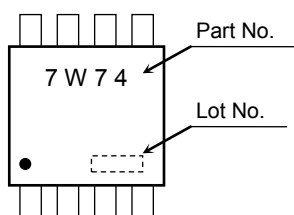
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse. CLEAR and PRESET are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level. Input is equipped with protection circuits against static discharge or transient excess voltage.

Features

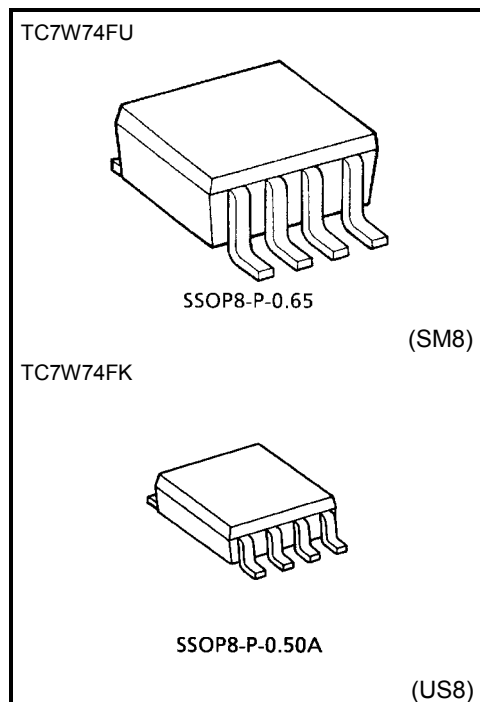
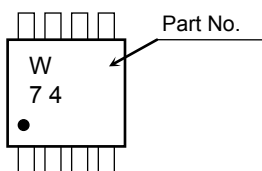
- High speed: $f_{MAX} = 77 \text{ MHz (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \text{ } \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 4 \text{ mA (min)}$
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$

Marking

TC7W74FU



TC7W74FK



Weight

SSOP8-P-0.65: 0.02 g (typ.)

SSOP8-P-0.50A: 0.01 g (typ.)

Start of commercial production
1992-02

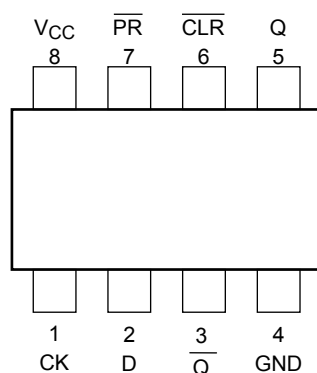
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 25	mA
Power dissipation	P_D	300 (SM8)	mW
		200 (US8)	
Storage temperature range	T_{stg}	-65 to 150	°C
Lead temperature (10 s)	T_L	260	°C

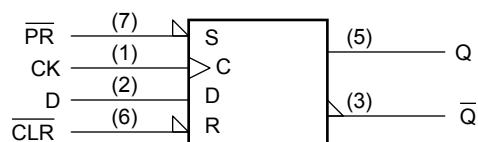
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Pin Configuration (top view)



Logic Diagram



Truth Table

Inputs				Outputs		Function
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	$\uparrow$	L	H	—
H	H	H	$\uparrow$	H	L	—
H	H	X	$\downarrow$	Qn	$\overline{\text{Qn}}$	No Change

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature range	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{\text{CC}} = 2.0 \text{ V}$)	ns
		0 to 500 ($V_{\text{CC}} = 4.5 \text{ V}$)	
		0 to 400 ($V_{\text{CC}} = 6.0 \text{ V}$)	

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit				
					V _{CC} (V)	Min	Typ.	Max	Min		Max			
Input voltage	High level	V _{IH}	—		2.0	1.5	—	—	1.5	—	V			
					4.5	3.15	—	—	3.15	—				
					6.0	4.2	—	—	4.2	—				
	Low level	V _{IL}	—		2.0	—	—	0.5	—	0.5				
					4.5	—	—	1.35	—	1.35				
					6.0	—	—	1.8	—	1.8				
Output voltage	High level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V			
					4.5	4.4	4.5	—	4.4	—				
					6.0	5.9	6.0	—	5.9	—				
				I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—				
					I _{OH} = -5.2 mA	6.0	5.68	5.80	—	5.63		—		
						Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0		—	0	0.1
	4.5	—	0	0.1						—		0.1		
	6.0	—	0	0.1	—					0.1				
	I _{OL} = 4 mA	4.5	—	0.17	0.26				—	0.33				
		I _{OL} = 5.2 mA	6.0	—	0.18				0.26	—		0.33		
			Input leakage current		I _{IN}				V _{IN} = V _{CC} or GND			6.0	—	—
	Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	2.0	—		20.0	μA	

Timing Requirements (input $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CLOCK)	t_W (L) t_W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t_W (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t_{rem}	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	4	5	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation delay time (CLOCK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	13	26	ns
Propagation delay time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$ -Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	14	26	ns
Maximum clock frequency	f_{MAX}	—	36	77	—	MHz

AC Electrical Characteristics ($C_L = 50 \text{ pF}$, input $t_r = t_f = 6 \text{ ns}$)

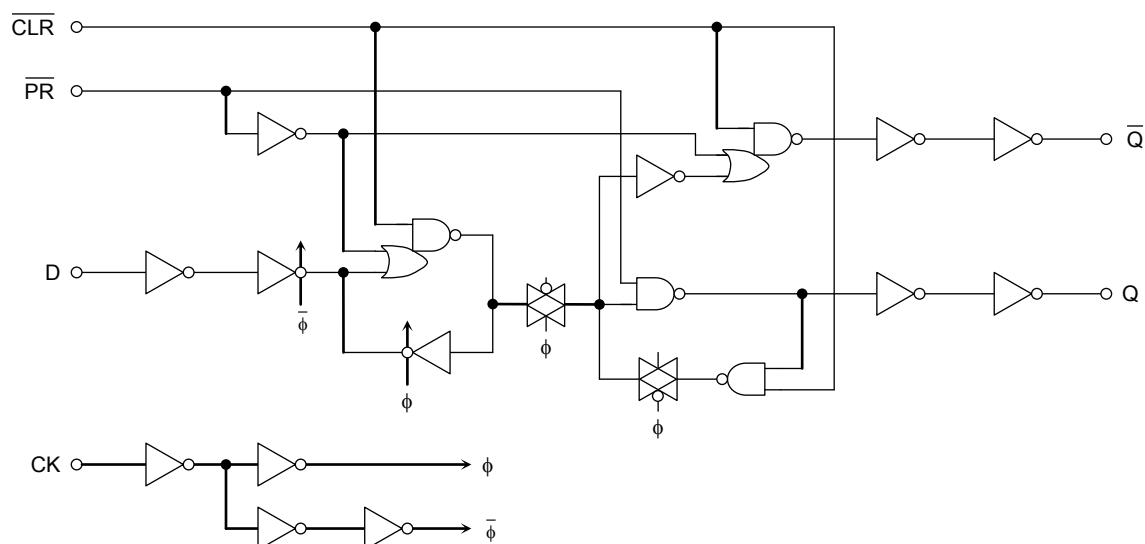
Characteristics	Symbol	Test Condition	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CLOCK-Q, $\bar{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	48	150	—	190	ns
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Propagation delay time ($\bar{\text{CLR}}$, $\bar{\text{PR}}$ -Q, $\bar{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	51	150	—	190	ns
			4.5	—	17	30	—	38	
			6.0	—	15	26	—	32	
Maximum clock frequency	f_{MAX}	—	2.0	6	21	—	5	—	MHz
			4.5	31	63	—	25	—	
			6.0	36	67	—	29	—	
Input capacitance	C_{IN}	—	—	5	10	—	10	—	pF
Power dissipation capacitance	C_{PD}	(Note)	—	34	—	—	—	—	pF

Note: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

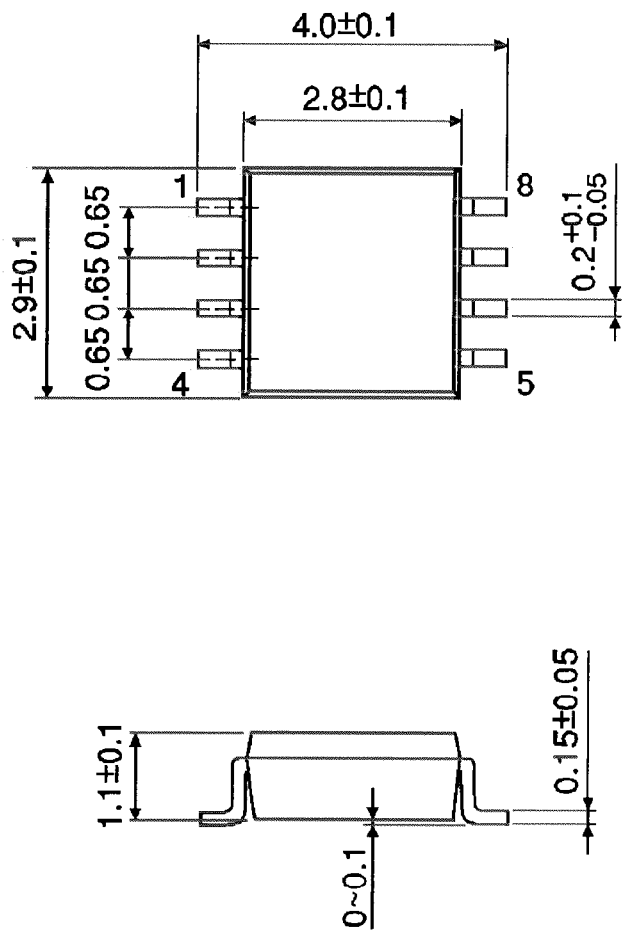
System Diagram



Package Dimensions

SSOP8-P-0.65

Unit : mm

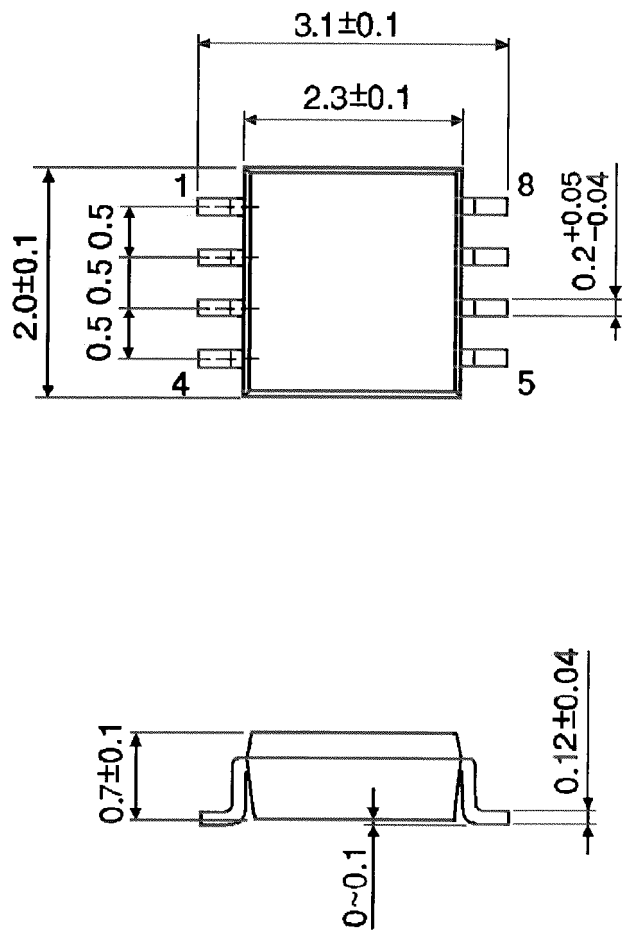


Weight: 0.02 g (typ.)

Package Dimensions

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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