Single-Channel, 128-/64-/32-Position, Up/Down, ±8% Resistor Tolerance, Nonvolatile Digital Potentiometer

Data Sheet

AD5111/AD5113/AD5115

FEATURES

Nominal resistor tolerance error: ±8% maximum
Wiper current: ±6 mA
Rheostat mode temperature coefficient: 35 ppm/°C
Low power consumption: 2.5mA max @ 2.7 V and 125°C
Wide bandwidth: 4 MHz (5 kΩ option)
Power-on EEPROM refresh time < 50 µs
50-year typical data retention at 125°C
1 million write cycles
2.3 V to 5.5 V supply operation
Chip select enable multiple device operation
Wide operating temperature: −40°C to +125°C
Thin, 2 mm × 2 mm × 0.55 mm 8-lead LFCSP package

APPLICATIONS

Mechanical potentiometer replacement
Portable electronics level adjustment
Audio volume control
Low resolution DAC
LCD panel brightness and contrast control
Programmable voltage to current conversion
Programmable filters, delays, time constants
Feedback resistor programmable power supply
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

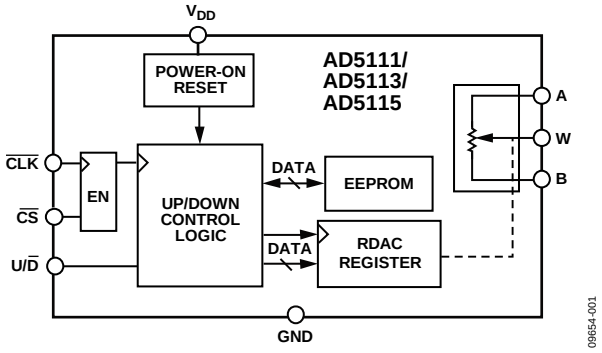

Figure 1.

Table 1. ±8% Resistance Tolerance Family

Model	Resistance (kΩ)	Position	Interface
AD5110	10, 80	128	I²C
AD5111	10, 80	128	Up/down
AD5112	5, 10, 80	64	I²C
AD5113	5, 10, 80	64	Up/down
AD5116	5, 10, 80	64	Push-button
AD5114	10, 80	32	I²C
AD5115	10, 80	32	Up/down

GENERAL DESCRIPTION

The AD5111/AD5113/AD5115 provide a nonvolatile solution for 128-/64-/32-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the A, B, and W pins. The low resistor tolerance, low nominal temperature coefficient, and high bandwidth simplify open-loop applications, as well as tolerance matching applications.

The new low wiper resistance feature minimizes the wiper resistance in the extremes of the resistor array to only 45 Ω, typical.

A simple 3-wire up/down interface allows manual switching or high speed digital control with clock rates up to 50 MHz.

The AD5111/AD5113/AD5115 are available in a 2 mm × 2 mm LFCSP package. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Rev. A
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4/12—Rev. 0 to Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5111

10 kΩ and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		7			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ, V_{DD} = 2.3 V to 2.7 V	−2.5	±0.5	+2.5	LSB
		R_{AB} = 10 kΩ, V_{DD} = 2.7 V to 5.5 V	−1	±0.25	+1	LSB
		R_{AB} = 80 kΩ	−0.5	±0.1	+0.5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1	±0.25	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.15	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	−2.5			LSB
		R_{AB} = 80 kΩ	−1.5			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 10 kΩ			1.5	LSB
		R_{AB} = 80 kΩ			0.5	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3, 6]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		20		pF
Capacitance W[3, 6]	C_W	f = 1 MHz, measured to GND, code = half scale		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}		2			V
Low	V_{INL}				0.8	V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 5 V		0.75	3.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.7 V			2.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.3 V			2.4	mA
EEMEM Store Current[3, 7]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 8]	$I_{DD_NVM_READ}$			320		µA
Power Dissipation[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		5		µW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[3, 10]						
Bandwidth	BW	Code = half scale, −3 dB				
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2 + 1$ V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		3		µs
		R_{AB} = 80 kΩ		12		µs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[11]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $0.8 \times V_{DD}/R_{AB}$.
[3] Guaranteed by design and characterization; not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on current direction with respect to each other.
[6] C_A is measured with $V_W = V_A$ = 2.5 V, C_B is measured with $V_W = V_B$ = 2.5 V, and C_W is measured with $V_A = V_B$ = 2.5 V.
[7] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[8] Different from operating current; supply current for NVM read lasts approximately 20 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).
[10] All dynamic characteristics use V_{DD} = 5.5 V and V_{LOGIC} = 5 V.
[11] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[12] Retention lifetime equivalent at junction temperature (T_J) is 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5113

5 kΩ, 10 kΩ, and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		6			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 5 kΩ, V_{DD} = 2.3 V to 2.7 V	−2.5	±0.5	+2.5	LSB
		R_{AB} = 5 kΩ, V_{DD} = 2.7 V to 5.5 V	−1	±0.25	+1	LSB
		R_{AB} = 10 kΩ	−1	±0.25	+1	LSB
		R_{AB} = 80 kΩ	−0.25	±0.1	+0.25	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1	±0.25	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.15	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 5 kΩ	−2.5			LSB
		R_{AB} =10 kΩ	−1.5			LSB
		R_{AB} = 80 kΩ	−1			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 5 kΩ			1.5	LSB
		R_{AB} =10 kΩ			1	LSB
		R_{AB} = 80 kΩ			0.25	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 5 kΩ, 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3, 6]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		20		pF
Capacitance W[3, 6]	C_W	f = 1 MHz, measured to GND, code = half scale		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}		2			V
Low	V_{INL}				0.8	V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 5 V		0.75	3.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.7 V			2.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.3 V			2.4	mA
EEMEM Store Current[3, 7]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 8]	$I_{DD_NVM_READ}$			320		µA
Power Dissipation[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		5		µW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 5 kΩ		−43		dB
		R_{AB} =10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[3, 10]						
Bandwidth	BW	Code = half scale, −3 dB				
		R_{AB} = 5 kΩ		4		MHz
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2 + 1$ V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 5 kΩ		−75		dB
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 5 kΩ		2.5		µs
		R_{AB} = 10 kΩ		3		µs
		R_{AB} = 80 kΩ		10		µs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 5 kΩ		7		nV/√Hz
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[11]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $0.8 \times V_{DD}/R_{AB}$.
[3] Guaranteed by design and characterization; not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on current direction with respect to each other.
[6] C_A is measured with $V_W = V_A$ = 2.5 V, C_B is measured with $V_W = V_B$ = 2.5 V, and C_W is measured with $V_A = V_B$ = 2.5 V.
[7] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[8] Different from operating current; supply current for NVM read lasts approximately 20 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).
[10] All dynamic characteristics use V_{DD} = 5.5 V and V_{LOGIC} = 5 V.
[11] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[12] Retention lifetime equivalent at junction temperature (T_J) is 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5115

10 kΩ and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		5			Bits
Resistor Integral Nonlinearity[2]	R-INL		−0.5		+0.5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.25		+0.25	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.25		+0.25	LSB
Differential Nonlinearity[4]	DNL		−0.25		+0.25	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	−1			LSB
		R_{AB} = 80 kΩ	−0.5			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 10 kΩ			1	LSB
		R_{AB} = 80 kΩ			0.25	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3, 6]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		20		pF
Capacitance W[3, 6]	C_W	f = 1 MHz, measured to GND, code = half scale		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}		2			V
Low	V_{INL}				0.8	V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 5 V		0.75	3.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.7 V			2.5	mA
		$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.3 V			2.4	mA
EEMEM Store Current[3, 7]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 8]	$I_{DD_NVM_READ}$			320		µA
Power Dissipation[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		5		µW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[3, 10]						
Bandwidth	BW	Code = half scale, −3 dB				
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2 + 1$ V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2.7		µs
		R_{AB} = 80 kΩ		9.5		µs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		V
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[11]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to $0.8 \times V_{DD}/R_{AB}$.
[3] Guaranteed by design and characterization; not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on current direction with respect to each other.
[6] C_A is measured with $V_W = V_A$ = 2.5 V, C_B is measured with $V_W = V_B$ = 2.5 V, and C_W is measured with $V_A = V_B$ = 2.5 V.
[7] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[8] Different from operating current; supply current for NVM read lasts approximately 20 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).
[10] All dynamic characteristics use V_{DD} = 5.5 V and V_{LOGIC} = 5 V.
[11] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[12] Retention lifetime equivalent at junction temperature (T_J) is 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.3 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Description
f_{CLK}	$V_{DD} \geq 2.7$ V			50	MHz	Clock frequency
	$V_{DD} < 2.7$ V			25	MHz	
t_1		25			ns	$\overline{CS}$ setup time
t_2	$V_{DD} \geq 2.7$ V	10			ns	$\overline{CLK}$ low time
	$V_{DD} < 2.7$ V	20			ns	
t_3	$V_{DD} \geq 2.7$ V	10			ns	$\overline{CLK}$ high time
	$V_{DD} < 2.7$ V	20			ns	
t_4		15			ns	U/$\overline{D}$ setup time
t_5		6			ns	U/$\overline{D}$ hold time
t_6	$V_{DD} \geq 2.7$ V	20			ns	$\overline{CS}$ rise to $\overline{CLK}$ hold time
	$V_{DD} < 2.7$ V	40			ns	
t_7		15			ns	$\overline{CS}$ rising edge to next $\overline{CLK}$ ignored
t_8	$V_{DD} \geq 2.7$ V	12			ns	U/$\overline{D}$ minimum pulse time
	$V_{DD} < 2.7$ V	24			ns	
t_9		12			ns	U/$\overline{D}$ rise to $\overline{CLK}$ falling edge
t_{10}		1			µs	Minimum $\overline{CS}$ time
$t_{EEPROM_PROGRAM}$[1]			15	50	ms	Memory program time
t_{POWER_UP}[2]				50	µs	Power-on EEPROM restore time

[1] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at a lower temperature and higher write cycles.
[2] Maximum time after V_{DD} is equal to 2.3 V.

TIMING DIAGRAMS

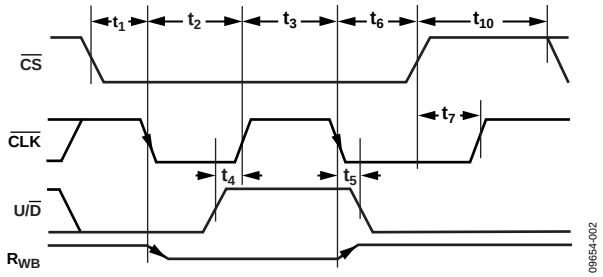

Figure 2. Increment/Decrement Mode Timing

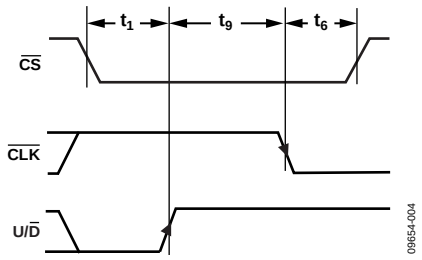

Figure 4. Shutdown Mode Timing

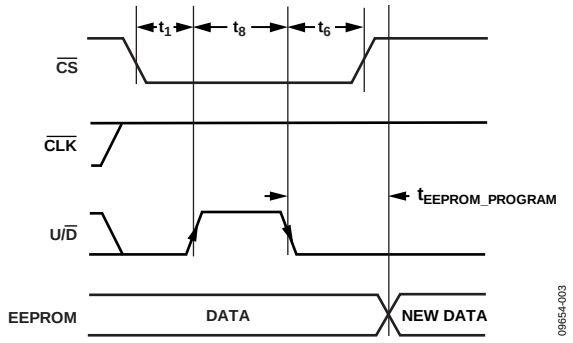

Figure 3. Storage Mode Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{LOGIC} to GND	−0.3 V to +7.0 V
V_A, V_W, V_B to GND	GND − 0.3 V to V_{DD} + 0.3 V
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/d[2]
R_{AW} = 80 kΩ	±1.5 mA/d[2]
Frequency ≤ 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/√d[2]
R_{AW} = 80 kΩ	±1.5 mA/√d[2]
Continuous	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA
R_{AW} = 80 kΩ	±1.5 mA
Digital Inputs U/$\overline{D}$, $\overline{CLK}$, and $\overline{CS}$	−0.3 V to +7 V or V_{DD} + 0.3 V (whichever is less)
Operating Temperature Range[3]	−40°C to +125°C
Maximum Junction Temperature (T_J Max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of EEPROM memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51, and the value is dependent on the test board and test environment.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	90[1]	25	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

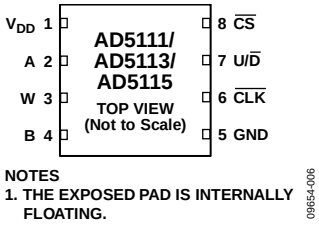

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. GND ≤ V_A ≤ V_{DD}.
3	W	Wiper Terminal of RDAC. GND ≤ V_W ≤ V_{DD}.
4	B	Terminal B of RDAC. GND ≤ V_B ≤ V_{DD}.
5	GND	Ground Pin, Logic Ground Reference.
6	$\overline{CLK}$	Clock Input. Each clock pulse executes the step-up or step-down of the resistance. The direction is determined by the state of the U/$\overline{D}$ pin. $\overline{CLK}$ is a negative edge trigger. Data can be transferred at rates up to 50 MHz.
7	U/$\overline{D}$	Up/Down Selection Counter Control.
8	$\overline{CS}$	Chip Select. Active Low.
	EPAD	Exposed Pad. The exposed pad is internally floating.

TYPICAL PERFORMANCE CHARACTERISTICS

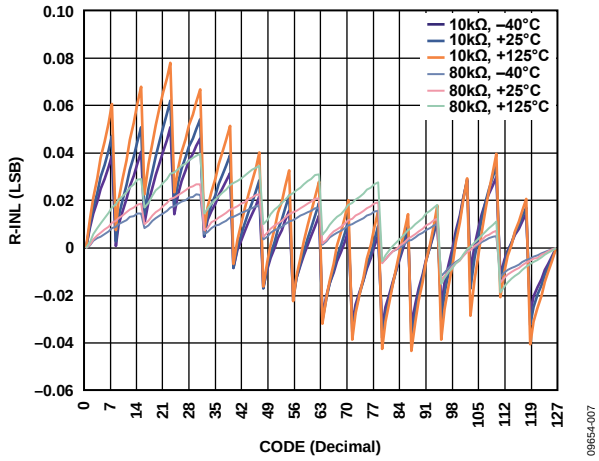

Figure 6. R-INL vs. Code (AD5111)

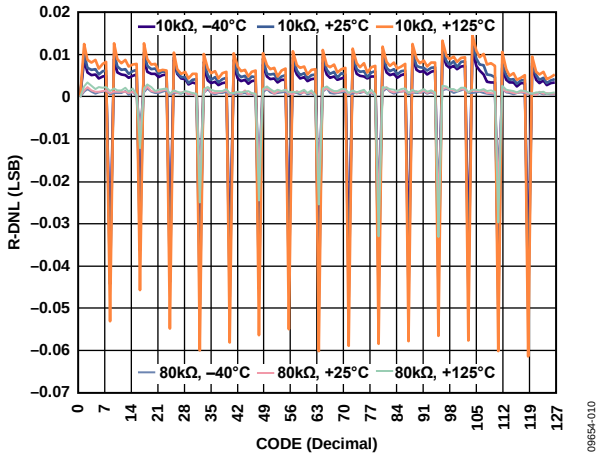

Figure 9. R-DNL vs. Code (AD5111)

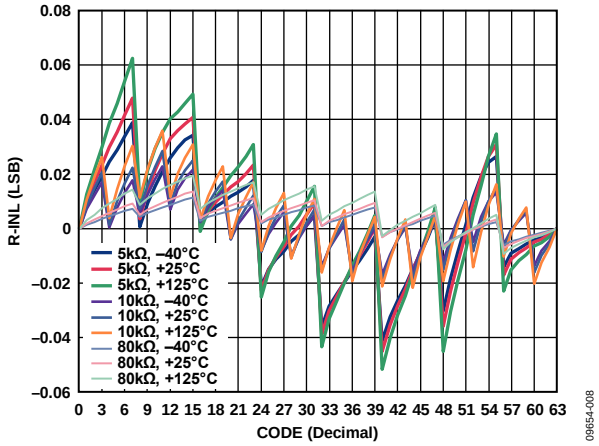

Figure 7. R-INL vs. Code (AD5113)

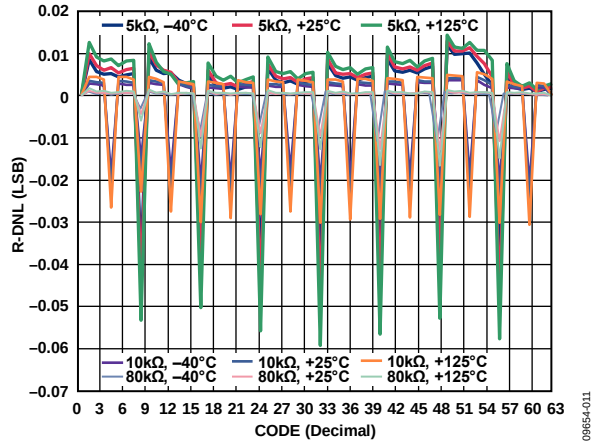

Figure 10. R-DNL vs. Code (AD5113)

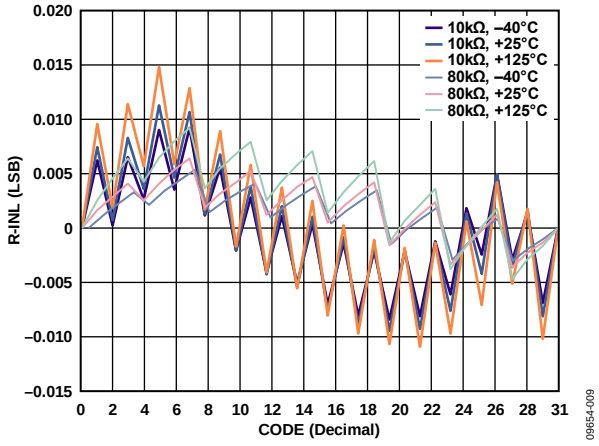

Figure 8. R-INL vs. Code (AD5115)

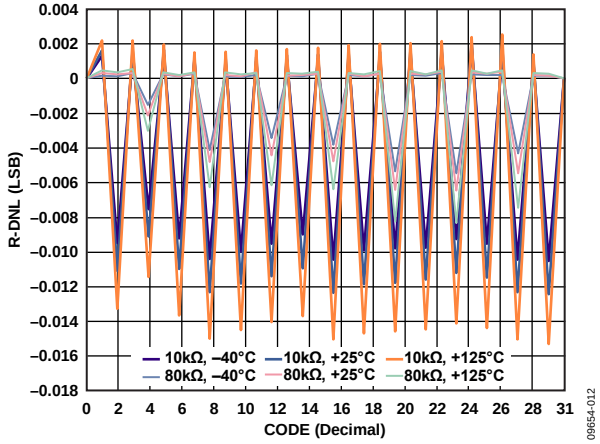

Figure 11. R-DNL vs. Code (AD5115)

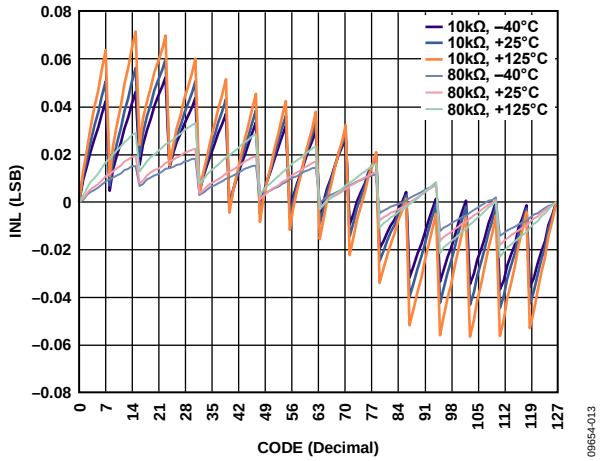

Figure 12. INL vs. Code (AD5111)

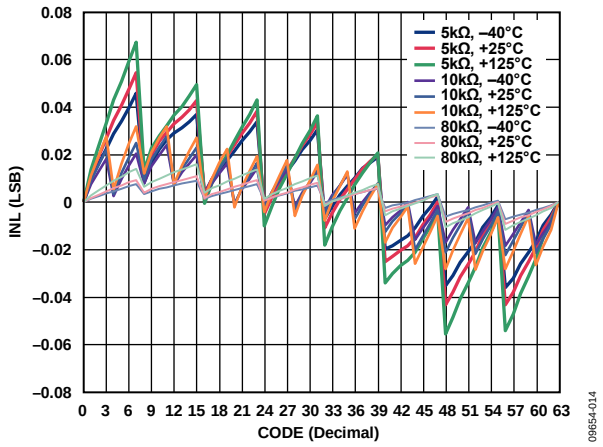

Figure 13. INL vs. Code (AD5113)

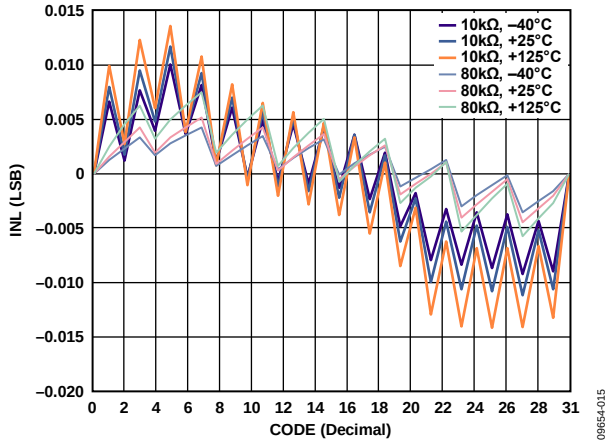

Figure 14. INL vs. Code (AD5115)

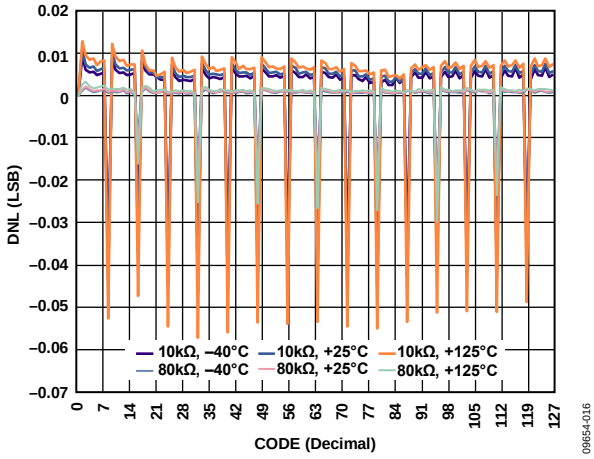

Figure 15. DNL vs. Code (AD5111)

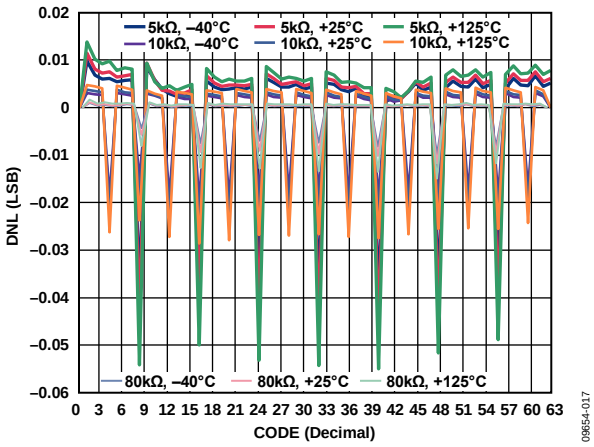

Figure 16. DNL vs. Code (AD5113)

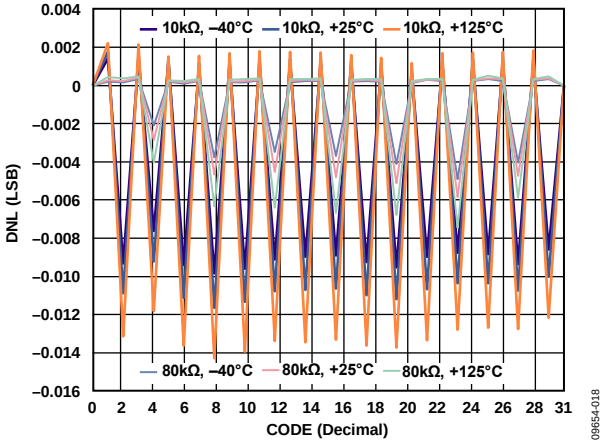

Figure 17. DNL vs. Code (AD5115)

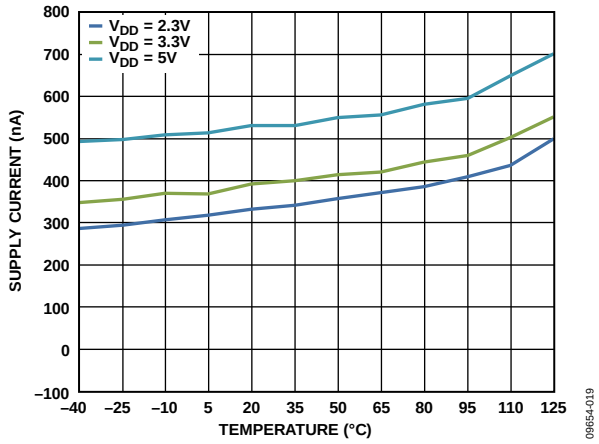

Figure 18. Supply Current vs. Temperature

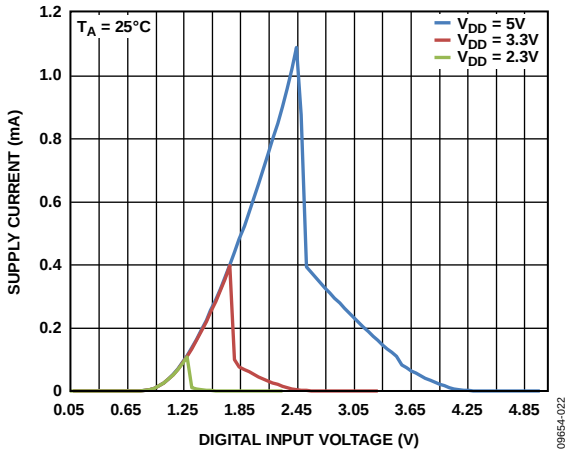

Figure 21. Supply Current (I_{DD}) vs. Digital Input Voltage

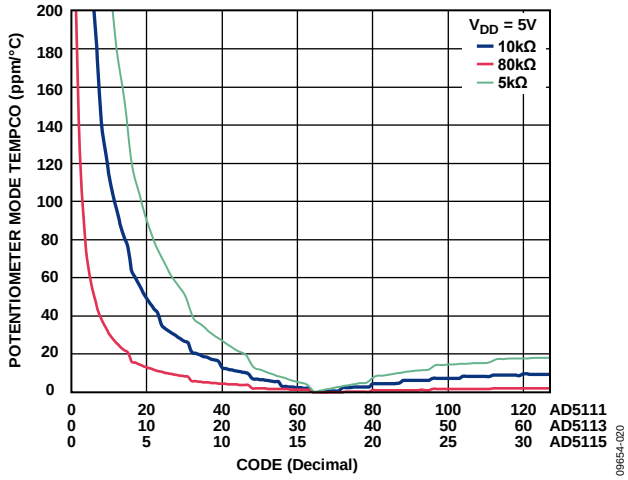

Figure 19. Potentiometer Mode Tempco ($(\Delta V_W/V_W)/\Delta T \times 10^6$) vs. Code

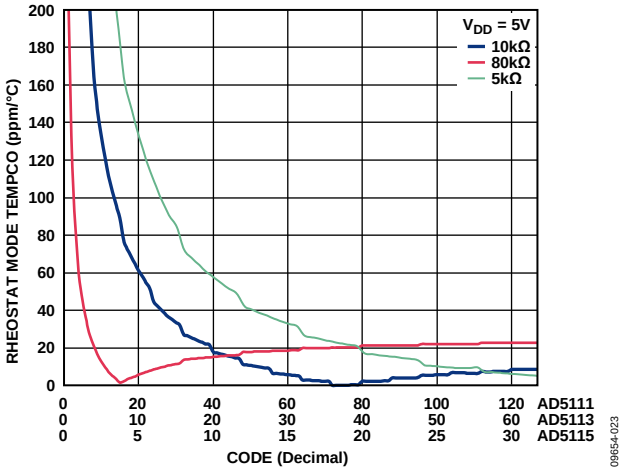

Figure 22. Rheostat Mode Tempco ($(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$) vs. Code

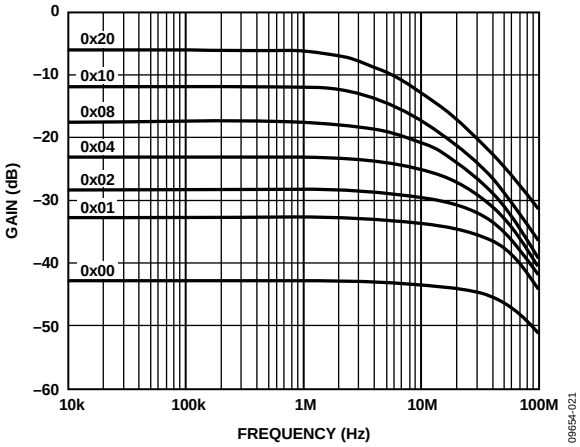

Figure 20. 5 kΩ Gain vs. Frequency vs. Code

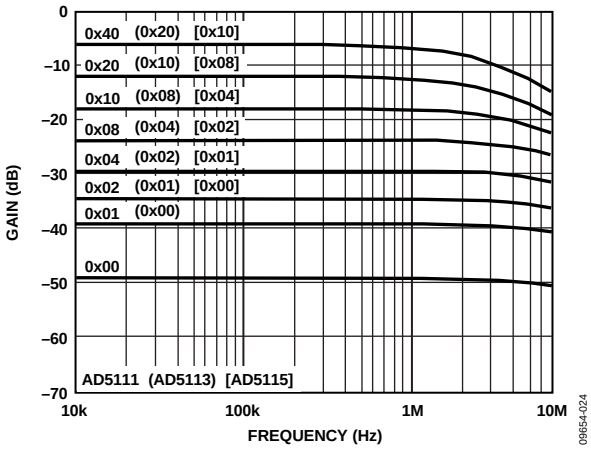

Figure 23. 10 kΩ Gain vs. Frequency vs. Code

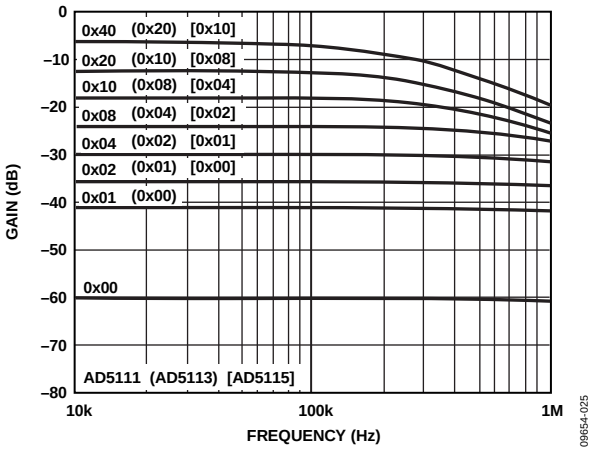

Figure 24. 80 kΩ Gain vs. Frequency vs. Code

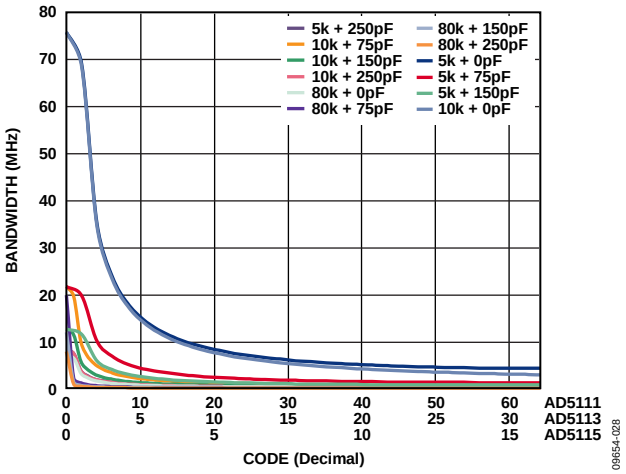

Figure 27. Maximum Bandwidth vs. Code vs. Net Capacitance

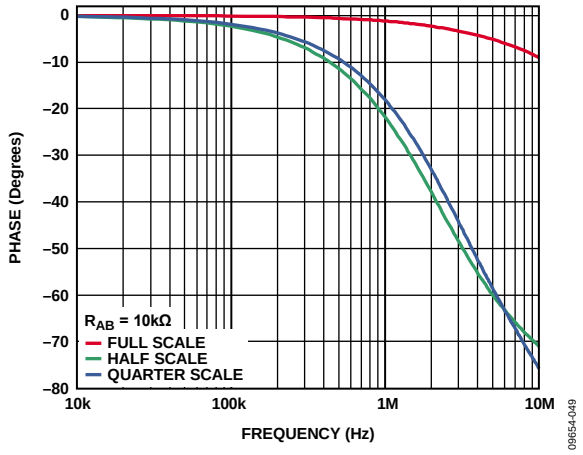

Figure 25. Normalized Phase Flatness vs. Frequency

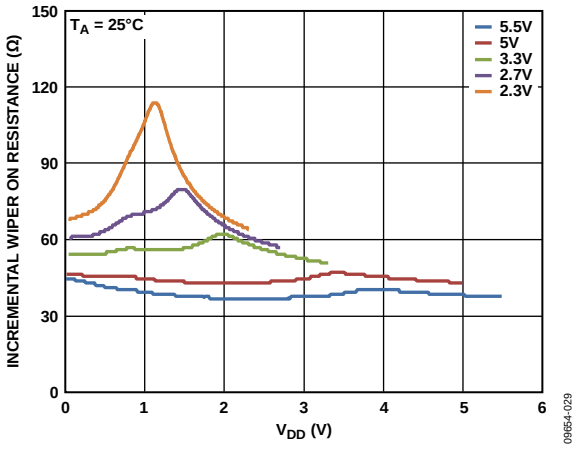

Figure 28. Incremental Wiper On Resistance vs. V_{DD}

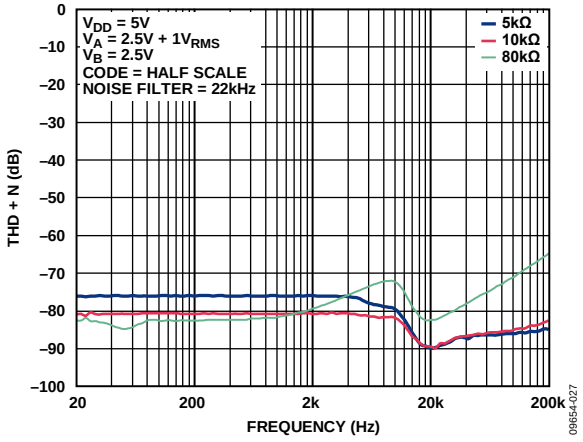

Figure 26. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

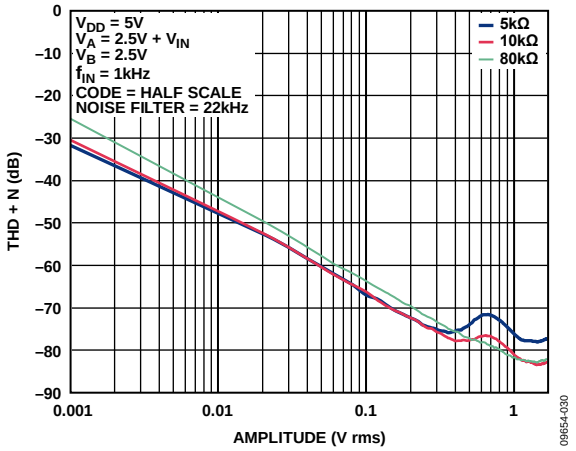

Figure 29. Total Harmonic Distortion + Noise (THD + N) vs. Amplitude

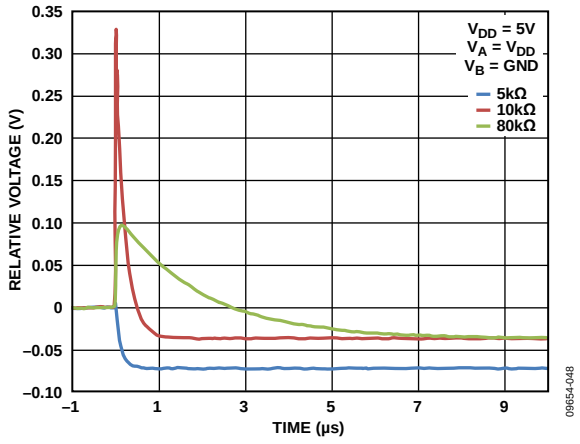

Figure 30. Maximum Transition Glitch

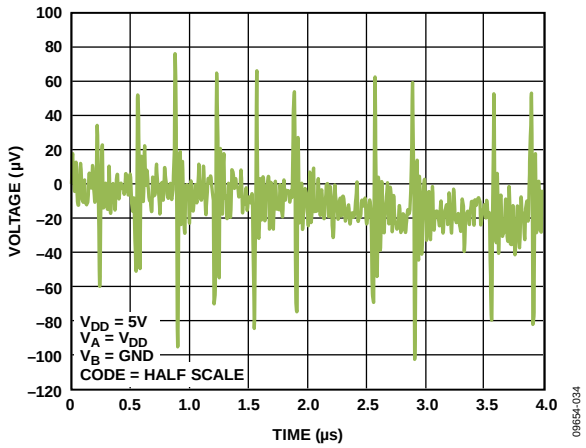

Figure 33. Digital Feedthrough

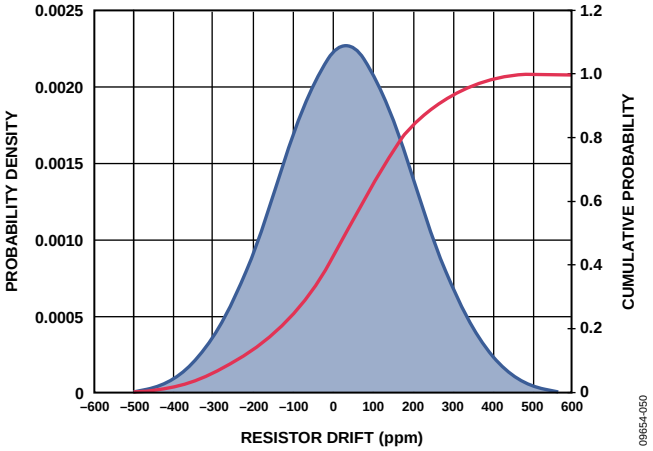

Figure 31. Resistor Lifetime Drift

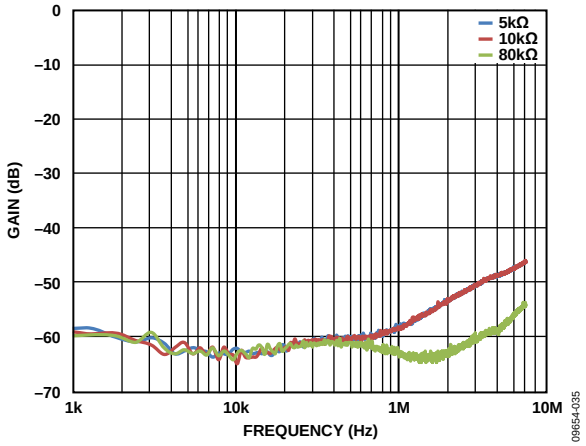

Figure 34. Shutdown Isolation vs. Frequency

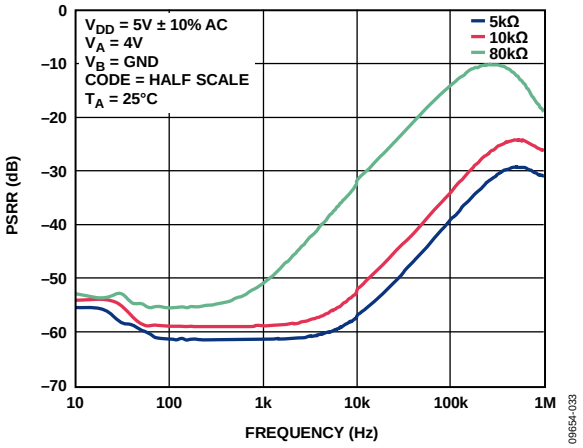

Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency

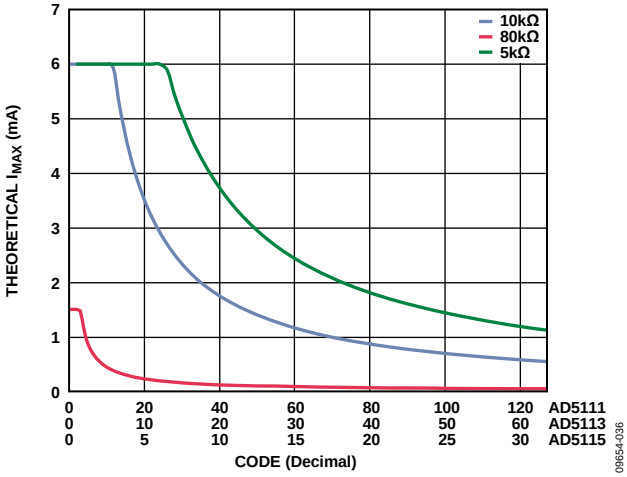

Figure 35. Theoretical Maximum Current vs. Code

TEST CIRCUITS

Figure 36 to Figure 41 define the test conditions used in the Specifications section.

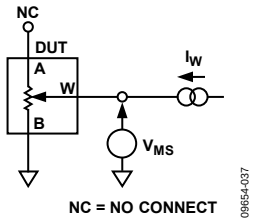

Figure 36. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

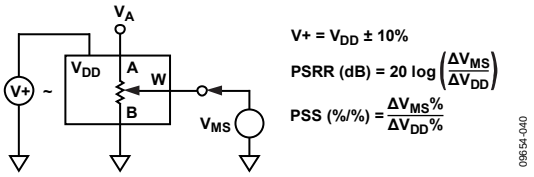

Figure 39. Power Supply Sensitivity (PSS, PSRR)

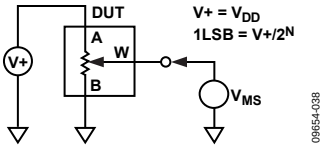

Figure 37. Potentiometer Divider Nonlinearity Error (INL, DNL)

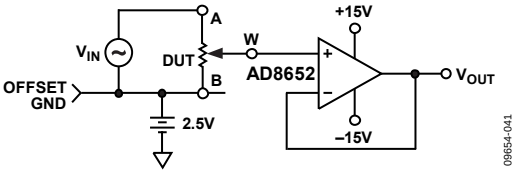

Figure 40. Gain and Phase vs. Frequency

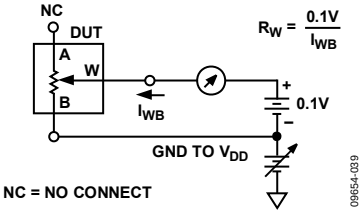

Figure 38. Wiper Resistance

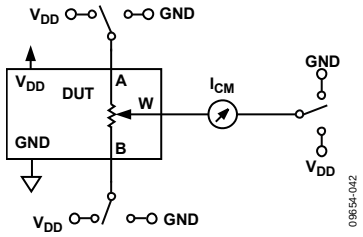

Figure 41. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5111/AD5113/AD5115 digital programmable resistors are designed to operate as true variable resistors for analog signals within the terminal voltage range of GND < V_{TERM} < V_{DD}. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings.

The RDAC register can be programmed with any position setting using the up/down interface. Once a desirable wiper position is found, this value can be stored in the EEPROM. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of EEPROM data takes approximately 30 ms; during this time, the device is locked and does not accept any new operation, thus preventing any changes from taking place.

The AD5111/AD5113/AD5115 are designed to allow high speed digital control with clock rates up to 50 MHz.

RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is 0x40 (AD5111), the wiper is connected to midscale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

Once a desirable wiper position is found, this value can be saved into the EEPROM. Thereafter, the wiper position is always set at that position for any future on-off-on power supply sequence or recall operation.

BASIC OPERATION

When $\overline{CS}$ is pulled low, changing the resistance settings is achieved by clocking the $\overline{CLK}$ pin. It is negative edge triggered, and the direction of stepping into the RDAC register is determined by the state of the U/$\overline{D}$ input. When a specific state of the U/$\overline{D}$ remains, the device continues to change in the same direction under consecutive clocks until it comes to the end of the resistance setting. When the wiper reaches the maximum or minimum setting, additional $\overline{CLK}$ pulses do not change the wiper setting. Figure 2 shows a typical increment/decrement operation.

The U/$\overline{D}$ pin value can be changed only when the $\overline{CLK}$ pin is low.

LOW WIPER RESISTANCE FEATURE

The AD5111/AD5113/AD5115 include a new feature to reduce the resistance between terminals. These extra steps are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 70 Ω to 45 Ω. At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB and the total resistance is reduced to 70 Ω. The new extra steps are loaded automatically in the RDAC register after zero-scale or full-scale position has been reached.

The extra steps are not equal to 1 LSB and are not included in the INL, DNL, R-INL, and R-DNL specifications.

SHUTDOWN MODE

This feature places Terminal A in open circuit, disconnected from the internal resistor, and connects Terminal W and Terminal B. A finite wiper resistance of 45 Ω is present between these two terminals. The command is sent by a low-to-high transition on the U/$\overline{D}$ pin, when $\overline{CLK}$ is high and $\overline{CS}$ is enabled. The command is executed on the $\overline{CLK}$ negative edge, as shown in Figure 4.

The AD5111/AD5113/AD5115 return the wiper to prior shutdown position if any other operation is performed.

EEPROM WRITE OPERATION

The AD5111/AD5113/AD5115 contain an EEPROM that allows the wiper position storage. Once a desirable wiper position is found, this value can be saved into the EEPROM. Thereafter, the wiper position is always set at that position for any future power-up sequence or a memory recall operation.

During the storage cycle, the device is locked and does not accept any new operation, thus preventing any changes from taking place.

The write cycle is started by applying a pulse in the U/$\overline{D}$ pin when $\overline{CS}$ is enabled and $\overline{CLK}$ remains high, as shown in Figure 3. The write cycle takes approximately 20 ms.

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5111/AD5113/AD5115 employ a two-stage segmentation approach as shown in Figure 42. The AD5111/AD5113/AD5115 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD}.

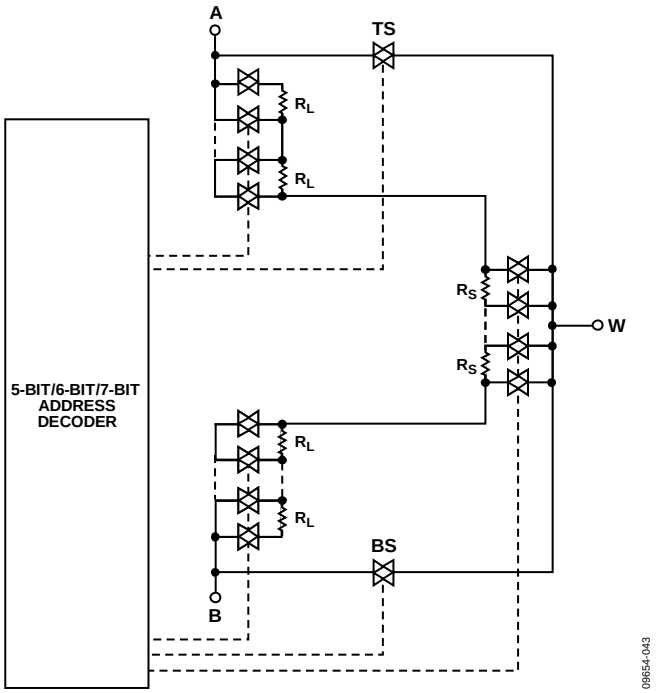

Figure 42. AD5111/AD5113/AD5115 Simplified RDAC Circuit

Low Wiper Resistance Feature

In addition, the AD5111/AD5113/AD5115 include a new feature to reduce the resistance between terminals. These extra steps are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 70 Ω to 45 Ω. At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB and the total resistance is reduced to 70 Ω. The extra steps are not equal to 1 LSB and are not included in the INL, DNL, R-INL, and R-DNL specifications.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—±8% Resistor Tolerance

The AD5111/AD5113/AD5115 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating or tied to the W terminal as shown in Figure 43.

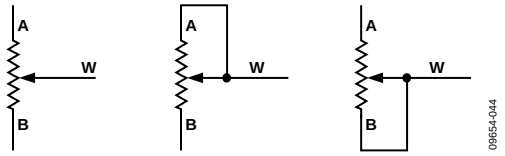

Figure 43. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 5 kΩ, 10 kΩ, and 80 kΩ and has 128/64/32 tap points accessed by the wiper terminal. The 5-/6-/7-bit data in the RDAC latch is decoded to select one of the 128/64/32 possible wiper settings. The general equations for determining the digitally programmed output resistance between the W terminal and B terminal are

AD5111:

$$R_{WB} = R_{BS} \quad \text{Bottom scale} \quad (1)$$

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \quad \text{From 0 to 128} \quad (2)$$

AD5113:

$$R_{WB} = R_{BS} \quad \text{Bottom scale} \quad (3)$$

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + R_W \quad \text{From 0 to 64} \quad (4)$$

AD5115:

$$R_{WB} = R_{BS} \quad \text{Bottom scale} \quad (5)$$

$$R_{WB}(D) = \frac{D}{32} \times R_{AB} + R_W \quad \text{From 0 to 32} \quad (6)$$

where:
D is the decimal equivalent of the binary code in the 5-/6-/7-bit RDAC register; 128, 64, and 32 refer to the top scale step.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.
R_{BS} is the wiper resistance at bottom scale.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5111:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale} \quad (7)$$

$$R_{AW}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \quad \text{From 0 to 127} \quad (8)$$

$$R_{AW} = R_{TS} \quad \text{Top scale} \quad (9)$$

AD5113:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale} \quad (10)$$

$$R_{AW}(D) = \frac{64 - D}{64} \times R_{AB} + R_W \quad \text{From 0 to 63} \quad (11)$$

$$R_{AW} = R_{TS} \quad \text{Top scale} \quad (12)$$

AD5115:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale} \quad (13)$$

$$R_{AW}(D) = \frac{32 - D}{32} \times R_{AB} + R_W \quad \text{From 0 to 31} \quad (14)$$

$$R_{AW} = R_{TS} \quad \text{Top scale} \quad (15)$$

where:
D is the decimal equivalent of the binary code in the 5-/6-/7-bit RDAC register; 128, 64, and 32 refer to top scale step.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.
R_{TS} is the wiper resistance at top scale.

Regardless of which setting the part is operating in, take care to limit the current between A to B, W to A, and W to B, to the maximum continuous current of ±6 mA (5 kΩ and 10 kΩ) or ±1.5 mA (80 kΩ), or pulse current specified in Table 6. Otherwise, degradation or possible destruction of the internal switch contact can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at W-to-B and W-to-A that is proportional to the input voltage at A-to-B, as shown in Figure 44. Unlike the polarity of V_{DD} to GND, which must be positive, current across A-to-B, W-to-A, and W-to-B can be in either direction.

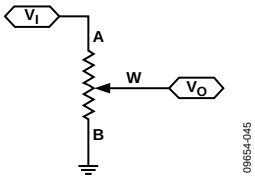

Figure 44. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at W to B ranging from 0 V to 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (16)$$

where:
$R_{WB}(D)$ can be obtained from Equation 1 to Equation 6.
$R_{AW}(D)$ can be obtained from Equation 7 to Equation 14.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

TERMINAL VOLTAGE OPERATING RANGE

The AD5111/AD5113/AD5115 are designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on the A, B, or W terminals that exceed V_{DD} are clamped by the forward-biased diode. There is no polarity constraint between V_A, V_W, and V_B, but they cannot be higher than V_{DD} or lower than GND.

POWER-UP SEQUENCE

Because of the ESD protection diodes that limit the voltage compliance at the A, B, and W terminals (see Figure 45), it is important to power on V_{DD} before applying any voltage to the A, B, and W terminals. Otherwise, the diodes are forward-biased such that V_{DD} is powered on unintentionally and can affect other parts of the circuit. Similarly, V_{DD} should be powered down last. The ideal power-on sequence is in the following order: GND, V_{DD}, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W and the digital inputs is not important as long as they are powered on after V_{DD}.

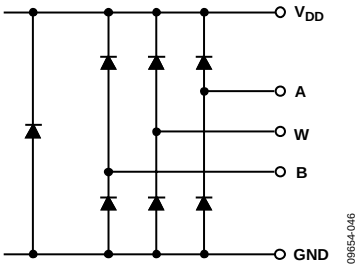

Figure 45. Maximum Terminal Voltages Set by V_{DD} and GND

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Apply low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 46 illustrates the basic supply bypassing configuration for the AD5111/AD5113/AD5115.

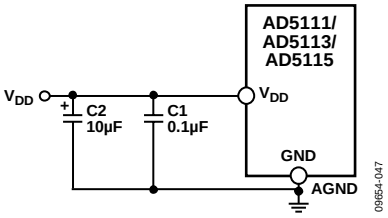

Figure 46. Power Supply Bypassing

OUTLINE DIMENSIONS

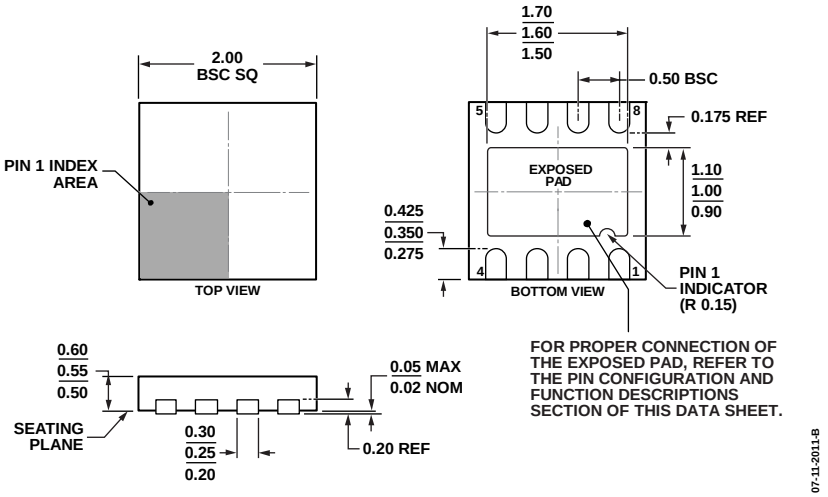

Figure 47. 8-Lead Frame Chip Scale Package [LFCSP_UD]
2 mm × 2 mm Body, Very Thin, Dual Lead (CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option	Branding Code
AD5111BCPZ10-RL7	10	128	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7S
AD5111BCPZ10-500R7	10	128	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7S
AD5111BCPZ80-RL7	80	128	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7T
AD5111BCPZ80-500R7	80	128	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7T
AD5113BCPZ5-RL7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	85
AD5113BCPZ5-500R7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	85
AD5113BCPZ10-RL7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	84
AD5113BCPZ10-500R7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	84
AD5113BCPZ80-RL7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	86
AD5113BCPZ80-500R7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	86
AD5115BCPZ10-RL7	10	32	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7Y
AD5115BCPZ10-500R7	10	32	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7Y
AD5115BCPZ80-RL7	80	32	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7Z
AD5115BCPZ80-500R7	80	32	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7Z
EVAL-AD5111SDZ				Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5111SDZ has an R_{AB} of 10 kΩ.

NOTES

NOTES

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