

Features

- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62147DV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 7 μA (Industrial)
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} [1] and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine ball grid array (VFBGA) (single/dual CE option) and 44-pin thin small outline package (TSOP) II packages
- Byte power-down feature

Functional Description

The CY62147EV30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH or both BLE and BHE are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

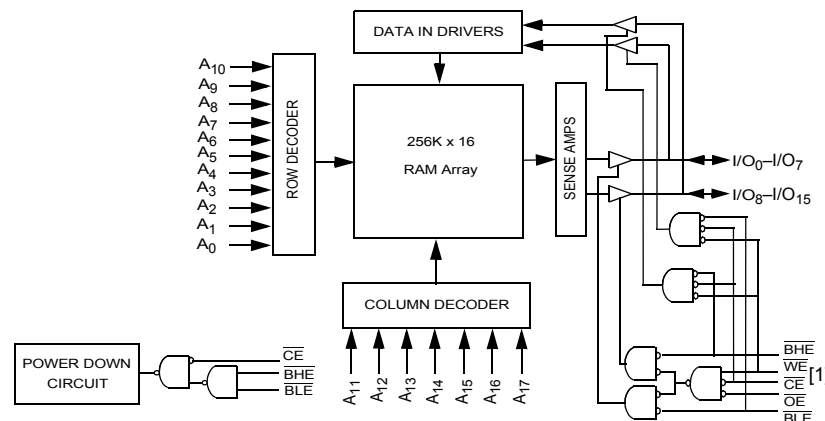
- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (\overline{CE} LOW and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Note

1. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, CE is LOW. For all other cases CE is HIGH.

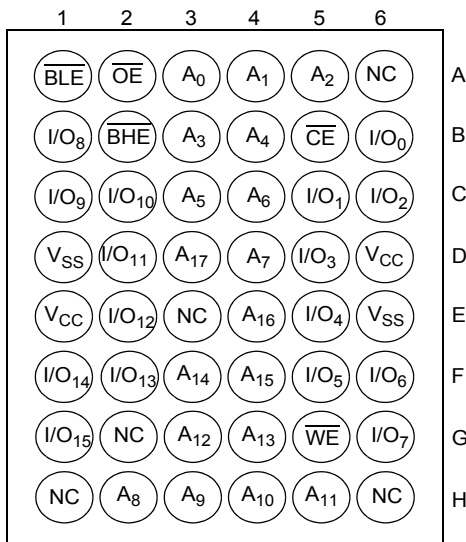
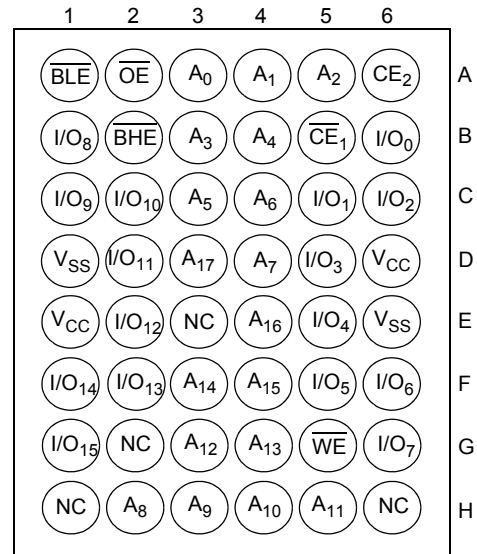
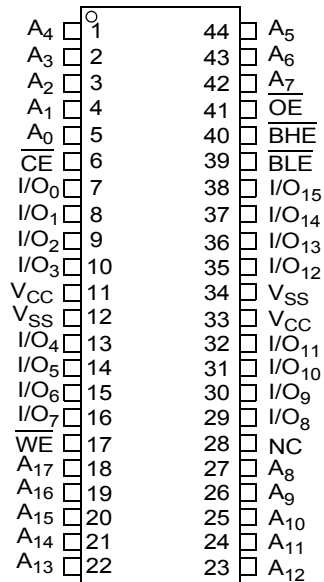
Contents

Product Portfolio	3	Ordering Information	12
Pin Configurations	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagrams	13
Operating Range	4	Acronyms	15
Electrical Characteristics	4	Document Conventions	15
Capacitance	5	Units of Measure	15
Thermal Resistance	5	Document History Page	16
AC Test Load and Waveforms	5	Sales, Solutions, and Legal Information	18
Data Retention Characteristics	6	Worldwide Sales and Design Support	18
Data Retention Waveform	6	Products	18
Switching Characteristics	7	PSoC@Solutions	18
Switching Waveforms	8	Cypress Developer Community	18
Truth Table	11	Technical Support	18

Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62147EV30LL	Industrial	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Single Chip Enable)^[3, 4]

Figure 2. 48-ball VFBGA pinout (Dual Chip Enable)^[3, 4]

Figure 3. 44-pin TSOP II pinout^[3]


Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- NC pins are not connected on the die.
- Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage to ground potential -0.3 V to + 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs in High Z state ^[5, 6] -0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage ^[5, 6] -0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) 20 mA

Static discharge voltage (MIL-STD-883, method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[7]
CY62147EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial)			Unit
			Min	Typ ^[8]	Max	
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	2.0	-	-	V
		I _{OH} = -1.0 mA, V _{CC} ≥ 2.70 V	2.4	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	-	-	0.4	V
		I _{OL} = 2.1 mA, V _{CC} = 2.70 V	-	-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7 V	1.8	-	V _{CC} + 0.3	V
		V _{CC} = 2.7 V to 3.6 V	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V	-0.3	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-0.3	-	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC}	-	15	20	mA
		f = 1 MHz	-	2	2.5	
I _{SB1} ^[9]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE, BHE, BLE and WE), V _{CC} = 3.60 V	-	1	7	μA
I _{SB2} ^[9]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = 3.60 V	-	1	7	μA

Notes

5. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.

6. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.

7. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

9. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

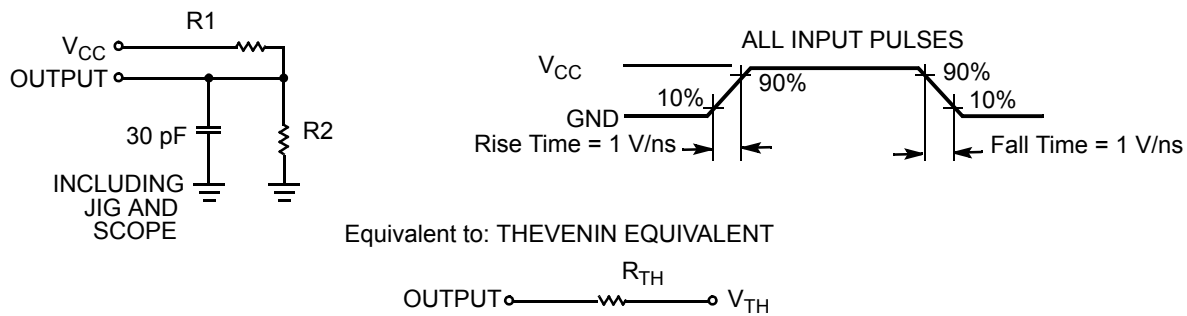
Parameter ^[10]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	48-ball VFBGA Package	44-pin TSOP II Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	42.10	55.52	°C/W
Θ _{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Load and Waveforms

Figure 4. AC Test Load and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

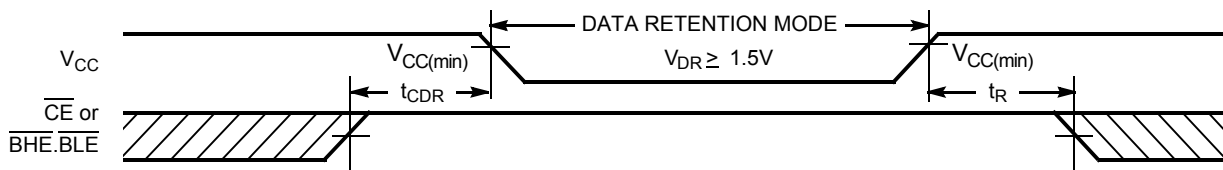
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} ^[12]	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	0.8	7	μA
t_{CDR} ^[13]	Chip deselect to data retention time		0	–	–	ns
t_R ^[14]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform^[15, 16]



Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
- Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
- BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, CE is LOW. For all other cases CE is HIGH.
- $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to low Z [19]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z [19, 20]	–	18	ns
t_{LZCE}	\overline{CE} LOW to low Z [19]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z [19, 20]	–	18	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z [19, 21]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z [19, 20]	–	18	ns
Write Cycle [22, 23]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z [19, 20]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to low Z [19]	10	–	ns

Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 4 on page 5](#).
18. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. If both byte enables are toggled together, this value is 10 ns.
22. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
23. The minimum write cycle pulse width for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [24, 25]

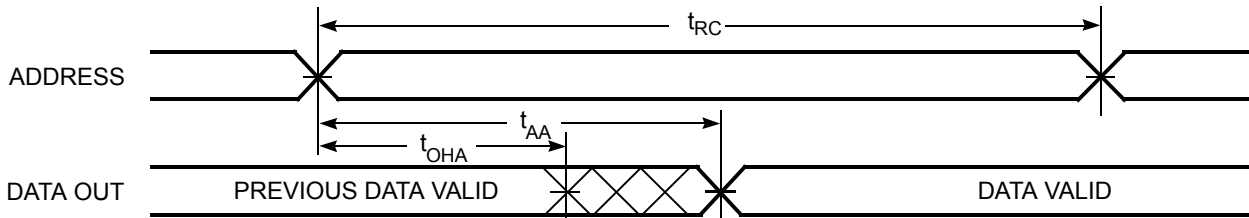
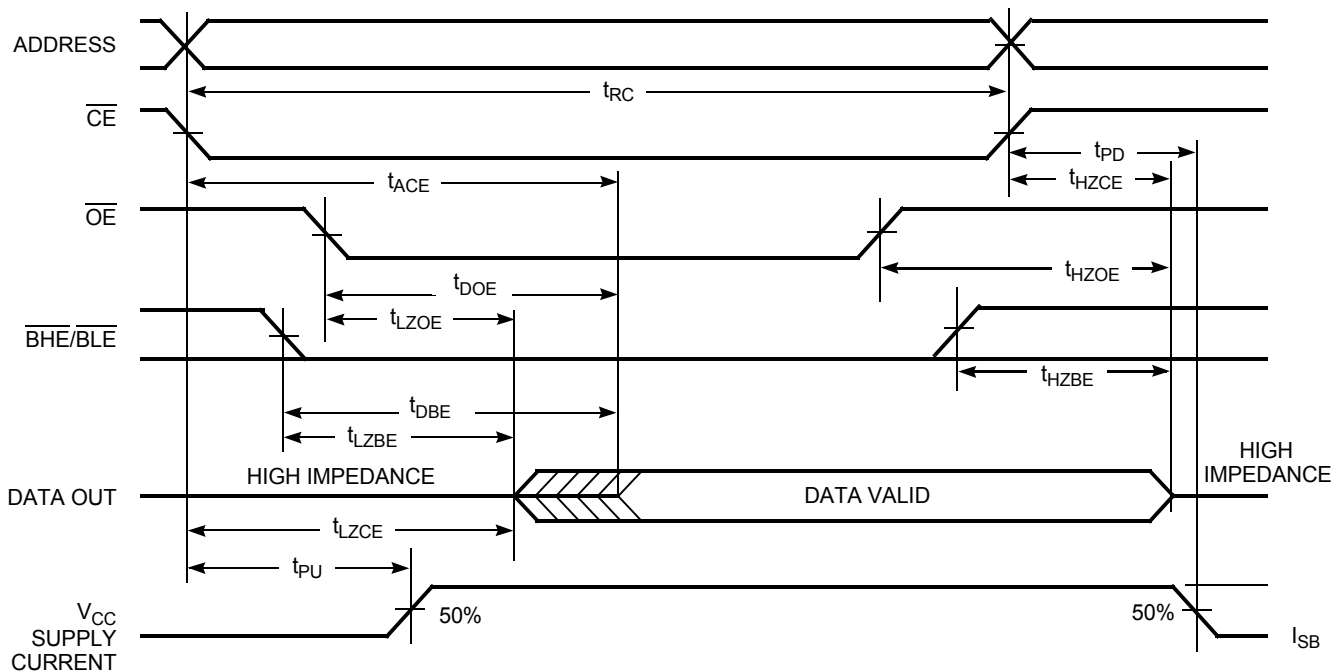


Figure 7. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [25, 26, 27]



Notes

24. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} .

25. $\overline{\text{WE}}$ is HIGH for read cycle.

26. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{\text{CE}}$ refers to the internal logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ such that when $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW. For all other cases $\overline{\text{CE}}$ is HIGH.

27. Address valid before or similar to CE and BHE, BLE transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (WE Controlled) [28, 29, 30, 31]

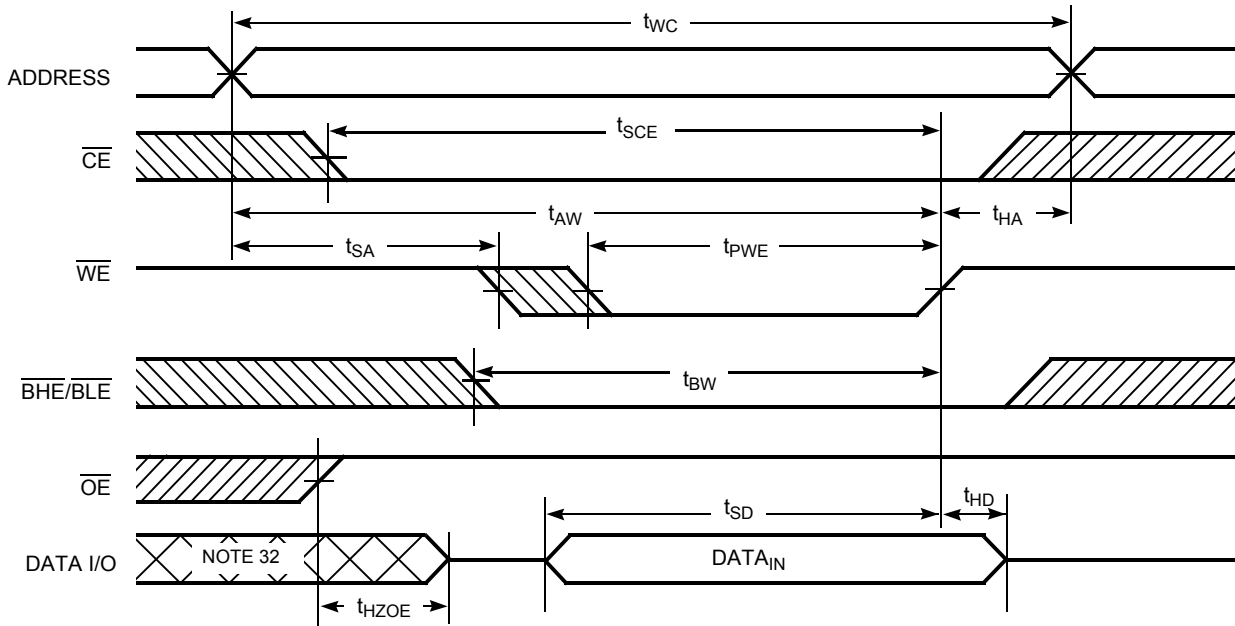
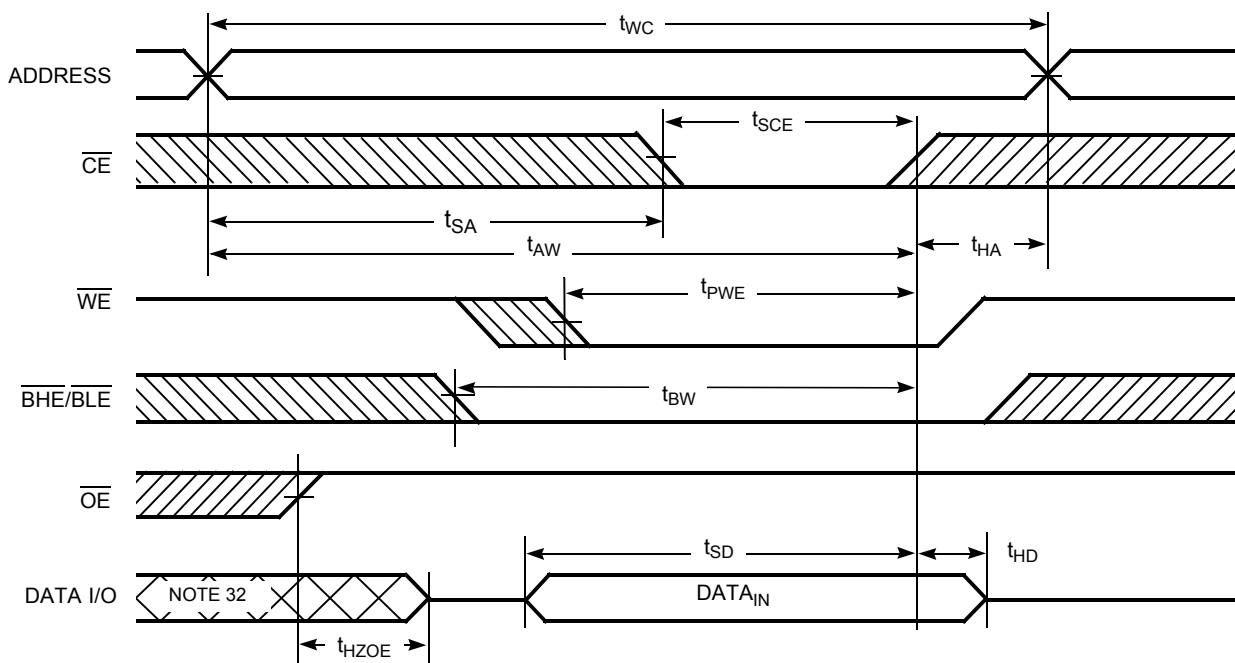


Figure 9. Write Cycle No. 2 (CE Controlled) [28, 29, 30, 31]



Notes

- 28. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- 29. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL} , BHE, BLE, or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 30. Data I/O is high impedance if OE = V_{IH} .
- 31. If CE goes HIGH simultaneously with WE = V_{IH} , the output remains in a high impedance state.
- 32. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [33, 34, 35]

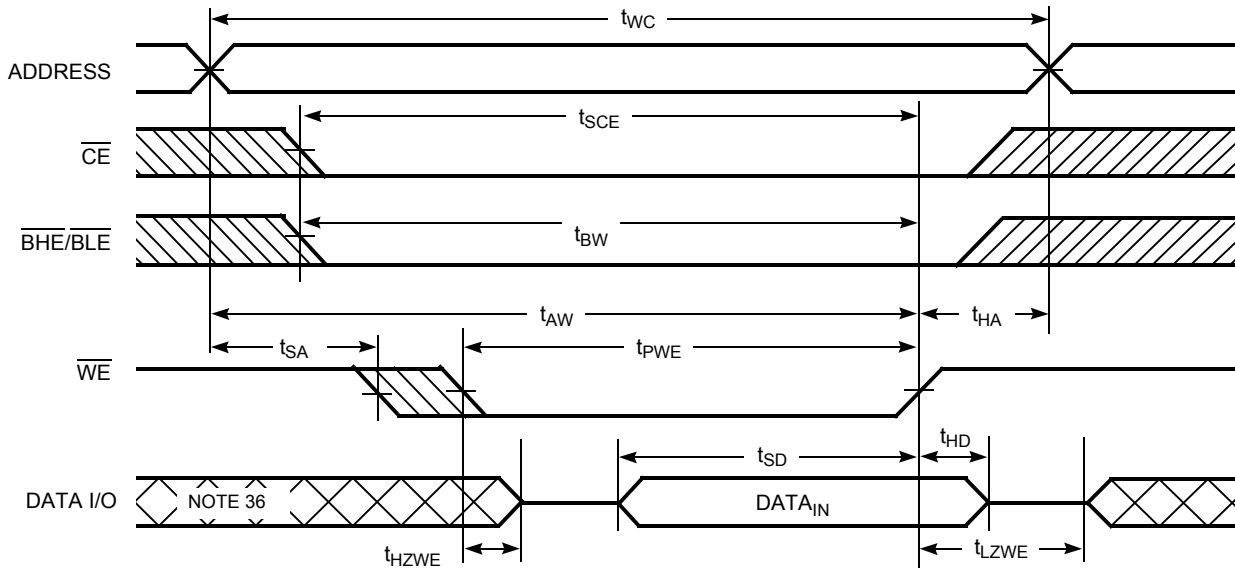
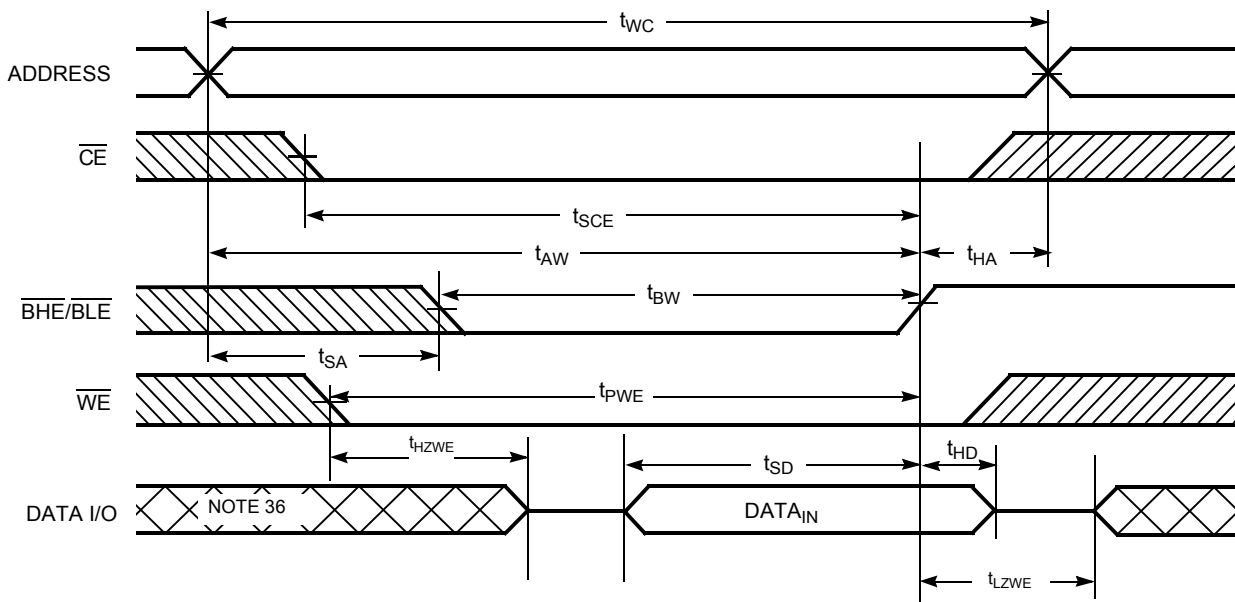


Figure 11. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled) [33, 34]



Notes

33. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.

34. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

35. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

36. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}$ [37, 38]	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	I/Os	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I_{CC})

Notes

37. BGA packaged device is offered in single CE and dual CE options. In this data sheet for a dual CE device, $\overline{\text{CE}}$ refers to the internal logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ such that when $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW. For all other cases $\overline{\text{CE}}$ is HIGH.

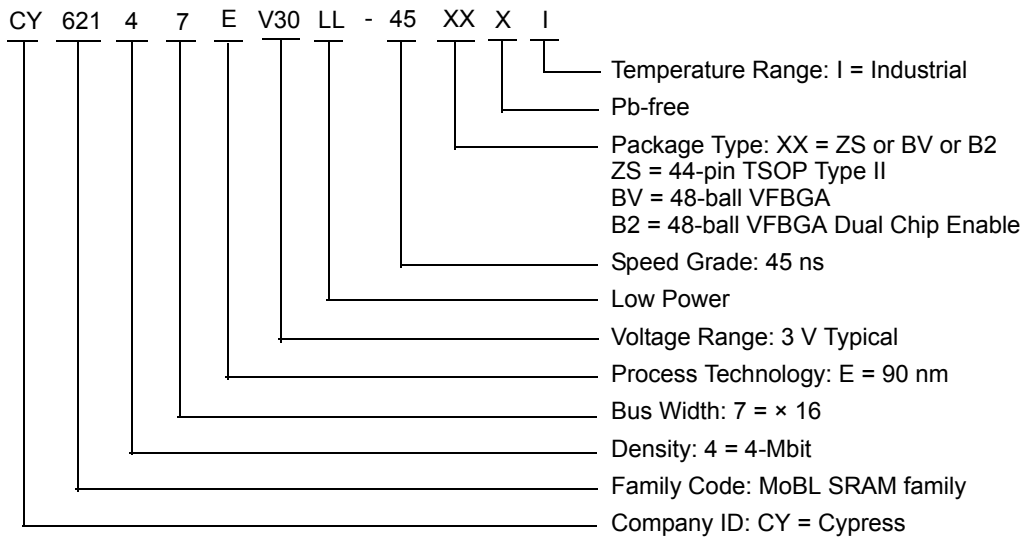
38. For the Dual Chip Enable device, $\overline{\text{CE}}$ refers to the internal logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ such that when $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW. For all other cases $\overline{\text{CE}}$ is HIGH. Intermediate voltage levels are not permitted on any of the Chip Enable pins (CE for the Single Chip Enable device; $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ for the Dual Chip Enable device).

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV30LL-45BVI	51-85150	48-ball VFBGA [39]	Industrial
	CY62147EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free) [39]	
	CY62147EV30LL-45B2XI	51-85150	48-ball VFBGA (Pb-free) [40]	
	CY62147EV30LL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

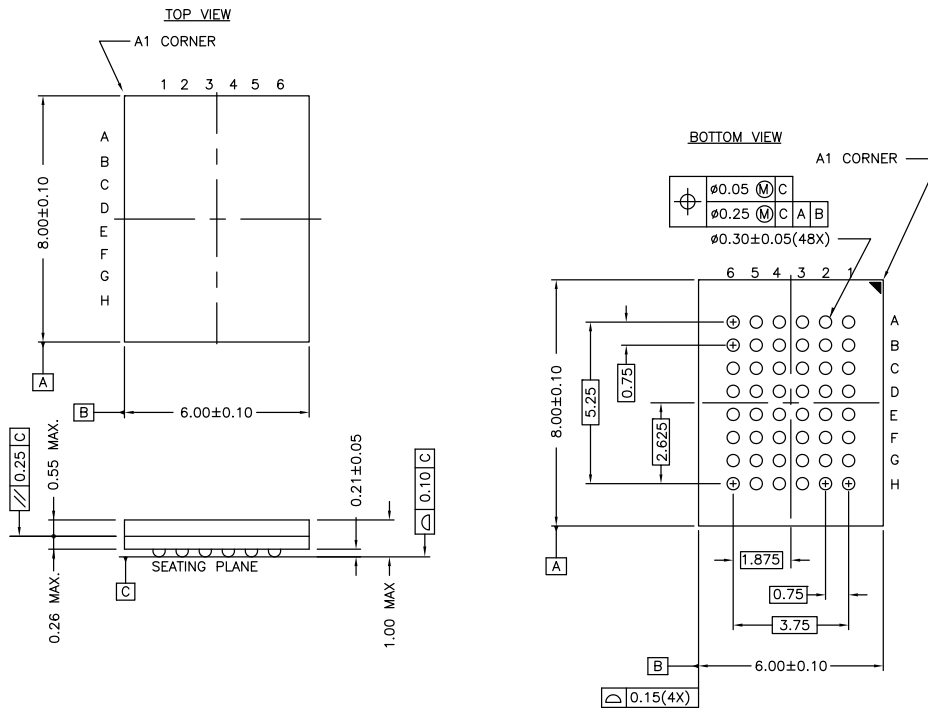


Notes

- 39. This BGA package is offered with single chip enable.
- 40. This BGA package is offered with dual chip enable.

Package Diagrams

Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

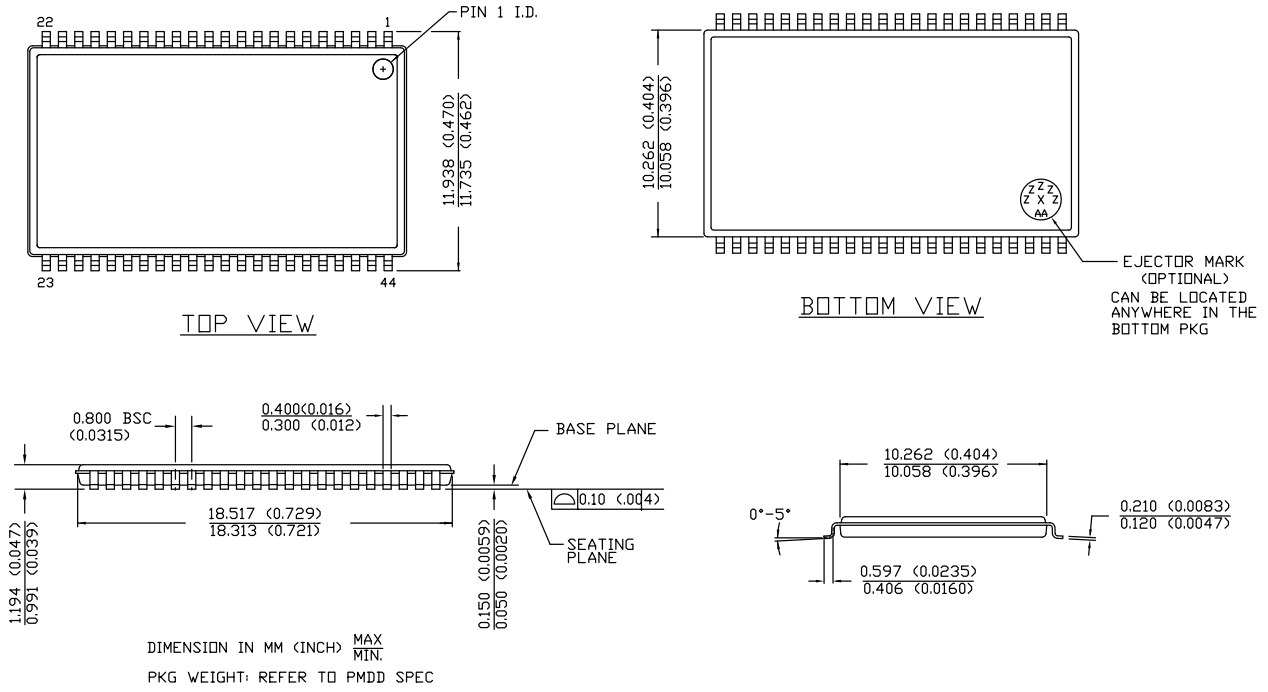


NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 13. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62147EV30 MoBL [®] , 4-Mbit (256K × 16) Static RAM Document Number: 38-05440				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201861	AJU	01/13/04	New data sheet.
*A	247009	SYT	See ECN	<p>Changed status from Advanced Information to Preliminary Moved Product Portfolio to Page 2 Changed Vcc stabilization time in footnote #8 from 100 μs to 200 μs Removed Footnote #15(t_{LZBE}) from Previous Revision Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics(t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages</p>
*B	414807	ZSD	See ECN	<p>Changed status from Preliminary to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Removed 35ns Speed Bin, "L" version of CY62147EV30 Changed ball E3 from DNU to NC. Removed redundant foot note on DNU. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA. Changed I_{CCDR} from 2.5 μA to 7 μA. Added I_{CCDR} typical value. Changed AC test load capacitance from 50 pF to 30 pF on Page #4, changed t_{LZOE} from 3 ns to 5 ns, changed t_{LZCE}, t_{LZBE} and t_{LZWE} from 6 ns to 10 ns, changed t_{HZCE} from 22 ns to 18 ns, changed t_{PWE} from 30 ns to 35 ns and changed t_{SD} from 22 ns to 25 ns. Updated the package diagram 48-pin VFBGA from *B to *D Updated the ordering information table and replaced the Package Name column with Package Diagram.</p>
*C	464503	NXR	See ECN	<p>Included Automotive Range in product offering Updated Ordering Information.</p>
*D	925501	VKN	See ECN	<p>Added Preliminary Automotive-A information Added footnote #9 related to I_{SB2} and I_{CCDR} Added footnote #14 related AC timing parameters</p>
*E	1045701	VKN	See ECN	<p>Converted Automotive-A and Automotive -E specs from preliminary to final</p>
*F	2577505	VKN / PYRS	10/03/08	<p>Added -45B2XI part (Dual CE option)</p>
*G	2681901	VKN / PYRS	04/01/09	<p>Added CY62147EV30LL-45ZSXA in the ordering information table</p>
*H	2886488	AJU	03/02/2010	<p>Added Contents. Added Note 38. Updated Package Diagrams. Updated links in Sales, Solutions, and Legal Information.</p>

Document History Page (continued)

Document Title: CY62147EV30 MoBL [®] , 4-Mbit (256K × 16) Static RAM				
Document Number: 38-05440				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*I	3109050	PRAS	12/13/2010	Changed Table Footnotes to Notes. Added Ordering Code Definitions .
*J	3123973	RAME	01/31/2011	Separated Industrial and Auto parts from this datasheet Removed Automotive info Added Acronyms and Units of Measure .
*K	3296744	RAME	08/09/2011	Updated Functional Description (Removed reference to AN1064 SRAM system guidelines). Added I _{SB1} to footnote 9 and 12. Notes 17 and 18 moved to parameter section of Switching Characteristics . Added Note 21 and referred the same note in the description of t _{LZBE} parameter.
*L	3456837	TAVA	12/06/2011	Updated Package Diagrams . Updated to new template.
*M	3724736	JISH	08/23/2012	Fixed typo errors and minor clean-up.
*N	4102445	VINI	08/22/2013	Updated Switching Characteristics : Updated Note 18. Updated Package Diagrams : spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*O	4576526	VINI	11/21/2014	Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. Updated Switching Characteristics : Added Note 23 and referred the same note in “Write Cycle”. Updated Switching Waveforms : Added Note 35 and referred the same note in Figure 10 .
*P	4918858	VINI	09/14/2015	Updated Switching Waveforms : Updated caption of Figure 11 (Removed “ $\overline{\text{OE}}$ LOW”). Updated to new template. Completing Sunset Review.
*Q	5445135	VINI	09/22/2016	Updated Thermal Resistance : Updated all values of Θ_{JA} and Θ_{JC} parameters. Updated to new template. Completing Sunset Review.
*R	5984537	AESATMP9	12/05/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2004-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.