## Features

- Very high speed: 45 ns
- Temperature ranges
  - ❏ Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62147DV30
- Ultra low standby power
  - ❏ Typical standby current: 1 μA
  - ❏ Maximum standby current: 7 μA (Industrial)
- Ultra low active power
  - ❏ Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ [1] and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine ball grid array (VFBGA) (single/dual CE option) and 44-pin thin small outline package (TSOP) II packages
- Byte power-down feature

## Functional Description

The CY62147EV30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins (I/O$_0$ through I/O$_{15}$) are placed in a high impedance state when:
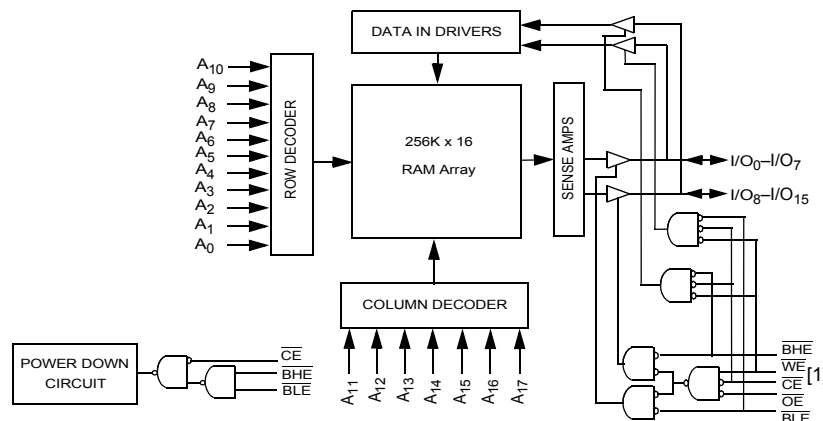
- Deselected ($\overline{CE}$ HIGH)

- Outputs are disabled ($\overline{OE}$ HIGH)

- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)

- Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$) is written into the location specified on the address pins (A$_0$ through A$_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{17}$).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O$_0$ to I/O$_7$. If Byte High enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O$_8$ to I/O$_{15}$. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

## Logic Block Diagram

# Contents

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | Standby $I_{SB2}$ (μA) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$ (mA) | | | | | |
| | | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | | Min | Typ [2] | Max | | Typ [2] | Max | Typ [2] | Max | Typ [2] | Max |
| CY62147EV30LL | Industrial | 2.2 | 3.0 | 3.6 | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |

## Pin Configurations

**Figure 1.  48-ball VFBGA pinout (Single Chip Enable)** [3, 4]
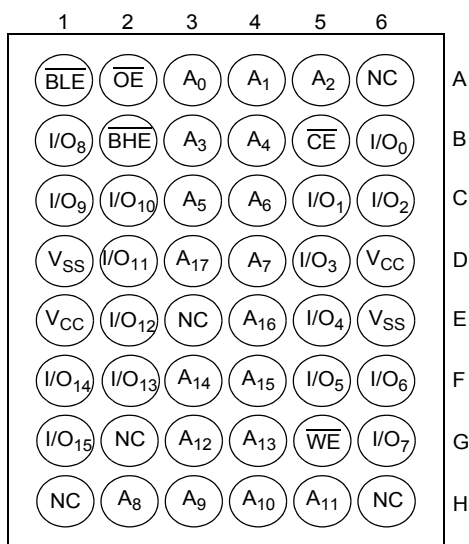


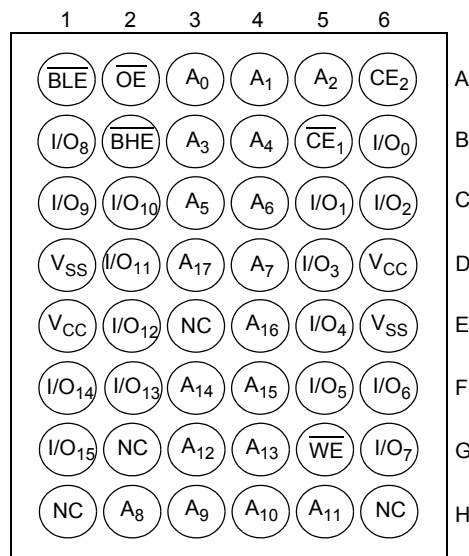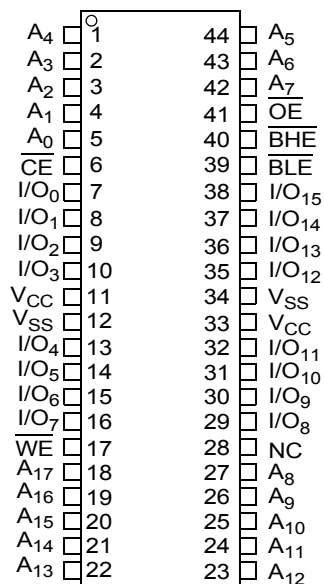**Figure 2.  48-ball VFBGA pinout (Dual Chip Enable)** [3, 4]



**Figure 3.  44-pin TSOP II pinout** [3]



### Notes
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
3. NC pins are not connected on the die.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ............................... –65 °C to + 150 °C

Ambient temperature
with power applied ................................... –55 °C to +125 °C

Supply voltage
to ground potential ........ –0.3 V to + 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs
in High Z state [5, 6] .......... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage [5, 6] ....... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) ............................. 20 mA

Static discharge voltage
(MIL-STD-883, method 3015) ................................ > 2001 V

Latch-up current ................................................... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [7] |
|---|---|---|---|
| CY62147EV30LL | Industrial | –40 °C to +85 °C | 2.2 V to 3.6 V |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns (Industrial) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [8] | Max | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA | | 2.0 | – | – | V |
| | | $I_{OH}$ = –1.0 mA, $V_{CC} \geq$ 2.70 V | | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA | | – | – | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA, $V_{CC}$ = 2.70 V | | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ = 2.2 V to 2.7 V | | 1.8 | – | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | 2.2 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | $V_{CC}$ = 2.2 V to 2.7 V | | –0.3 | – | 0.6 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | –0.3 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND $\leq V_I \leq V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | GND $\leq V_O \leq V_{CC}$, output disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | f = $f_{max}$ = 1/$t_{RC}$ | $V_{CC} = V_{CC(max)}$ $I_{OUT}$ = 0 mA CMOS levels | – | 15 | 20 | mA |
| | | f = 1 MHz | | – | 2 | 2.5 | |
| $I_{SB1}$[9] | Automatic $\overline{CE}$ power-down current – CMOS inputs | $\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |
| $I_{SB2}$[9] | Automatic $\overline{CE}$ power-down current – CMOS inputs | $\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |

**Notes**
5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after $V_{CC}$ stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
9. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

## Capacitance

| Parameter [10] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [10] | Description | Test Conditions | 48-ball VFBGA Package | 44-pin TSOP II Package | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 42.10 | 55.52 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 23.45 | 16.03 | °C/W |

## AC Test Load and Waveforms

Figure 4.  AC Test Load and Waveforms
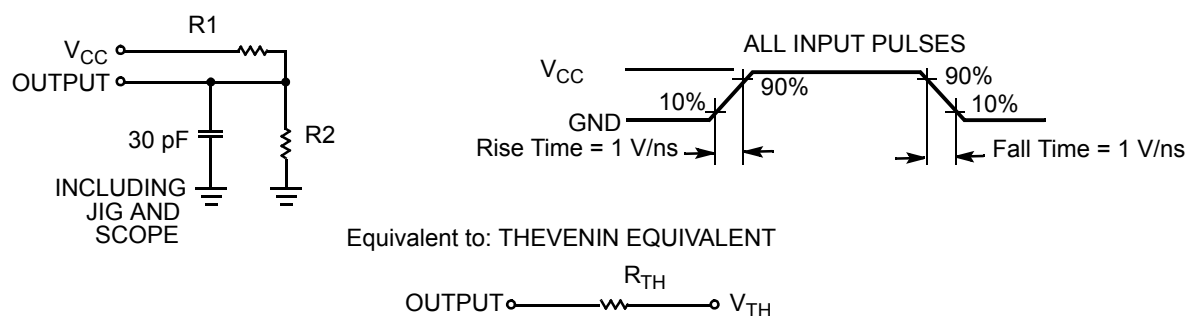


| Parameters | 2.50 V | 3.0 V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

**Note**
10. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ [11] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1.5 | – | – | V |
| $I_{CCDR}$ [12] | Data retention current | $V_{CC} = 1.5$ V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 0.8 | 7 | µA |
| $t_{CDR}$ [13] | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$ [14] | Operation recovery time | | 45 | – | – | ns |

## Data Retention Waveform

### Figure 5. Data Retention Waveform [15, 16]
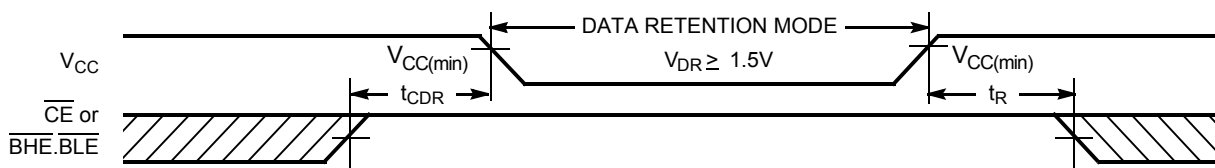


**Notes**

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
12. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
15. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, CE is LOW. For all other cases CE is HIGH.
16. BHE.BLE is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [17, 18] | Description | 45 ns (Industrial) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z [19] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z [19, 20] | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z [19] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z [19, 20] | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to low Z [19, 21] | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to high Z [19, 20] | – | 18 | ns |
| **Write Cycle** [22, 23] | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z [19, 20] | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z [19] | 10 | – | ns |

**Notes**
17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}$/2, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the Figure 4 on page 5.
18. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
19. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
20. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
21. If both byte enables are toggled together, this value is 10 ns.
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
23. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

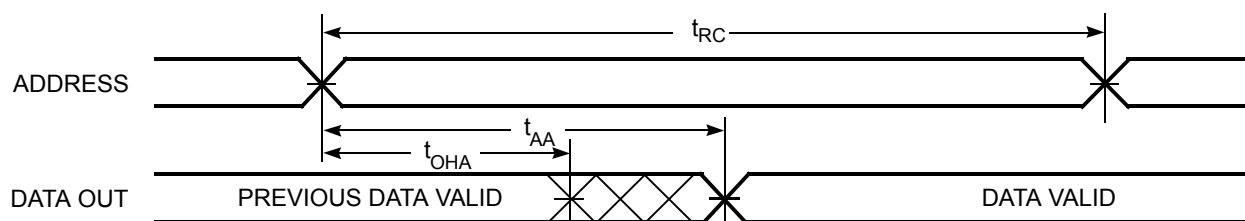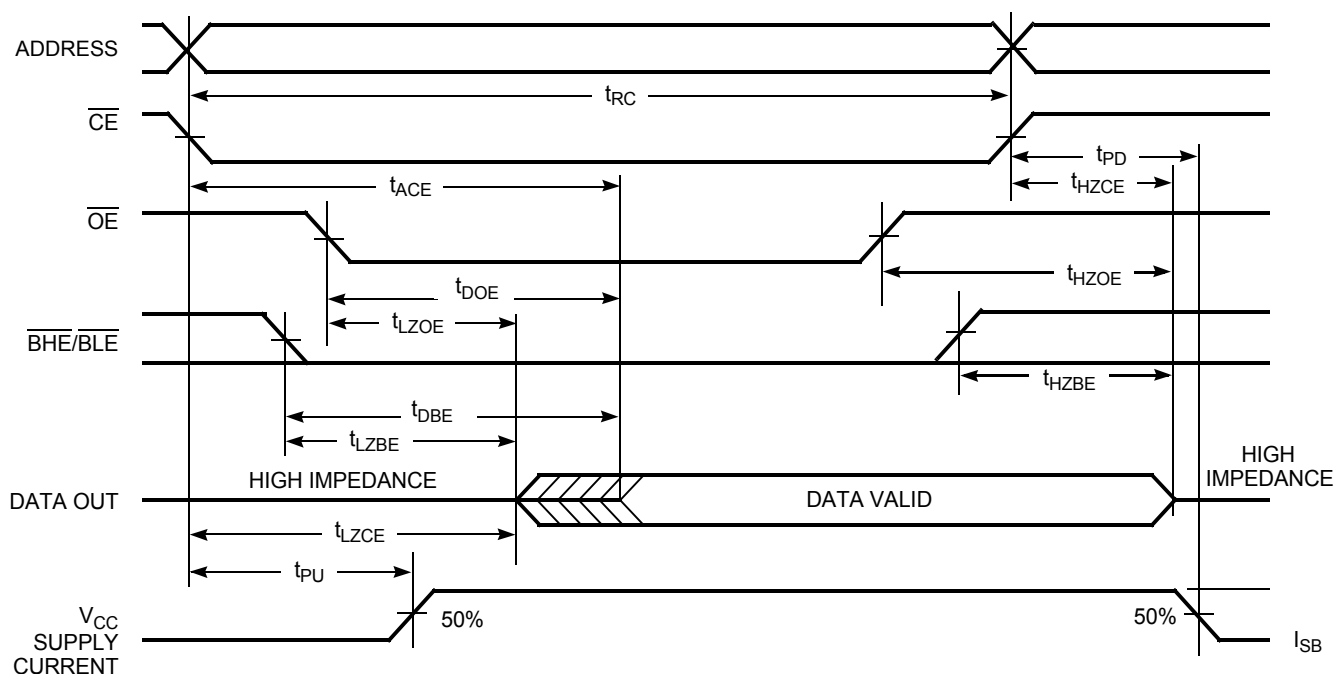**Figure 6. Read Cycle No. 1 (Address Transition Controlled)** [24, 25]



**Figure 7. Read Cycle No. 2 (OE Controlled)** [25, 26, 27]



**Notes**
24. The device is continuously selected. OE, CE = $V_{IL}$, BHE, BLE, or both = $V_{IL}$.
25. WE is HIGH for read cycle.
26. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, CE refers to the internal logical combination of CE$_1$ and CE$_2$ such that when CE$_1$ is LOW and CE$_2$ is HIGH, CE is LOW. For all other cases CE is HIGH.
27. Address valid before or similar to CE and BHE, BLE transition LOW.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled)** [28, 29, 30, 31]
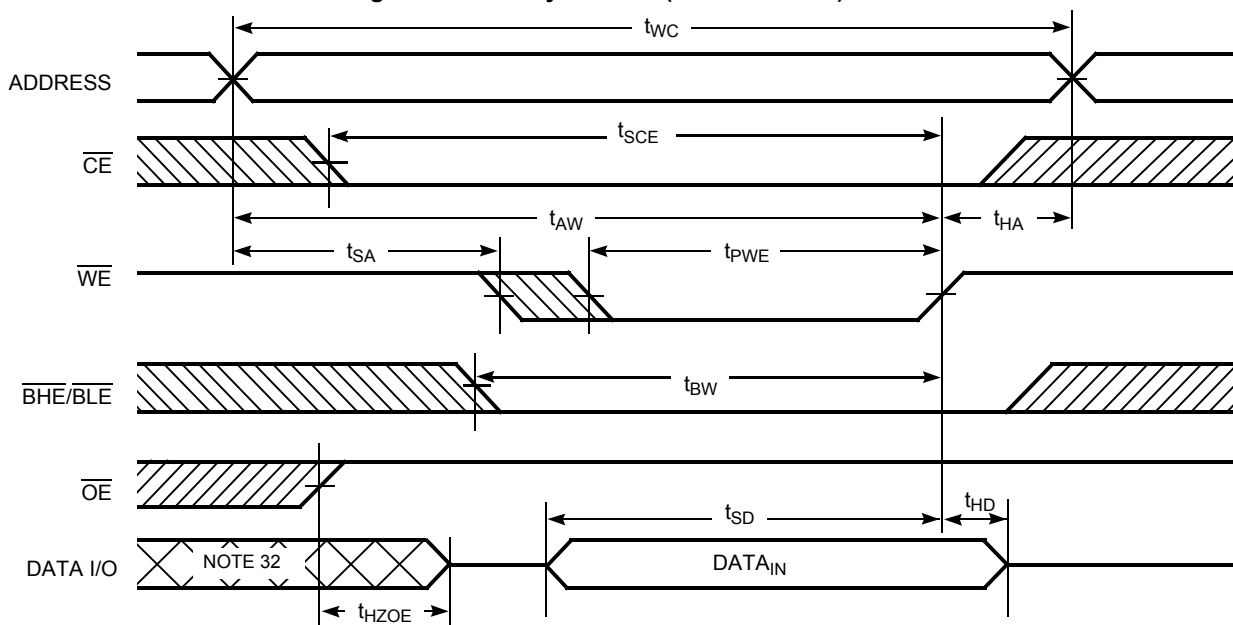


**Figure 9. Write Cycle No. 2 ($\overline{CE}$ Controlled)** [28, 29, 30, 31]
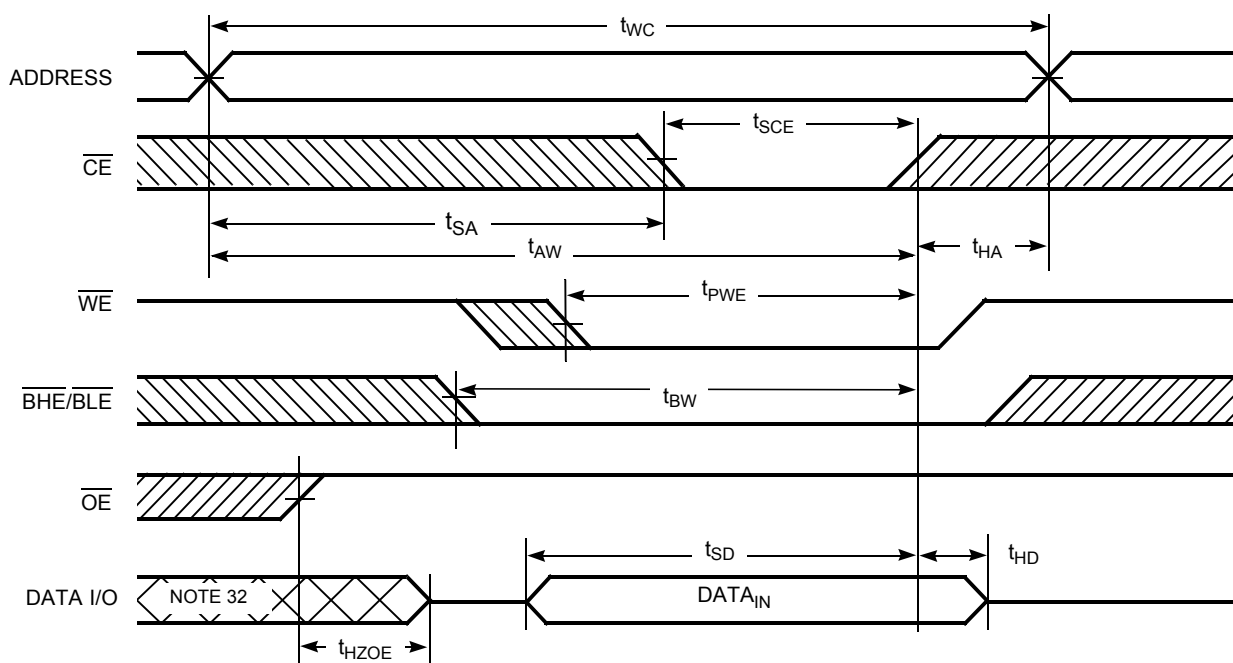


**Notes**
28. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
31. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

### Figure 10. Write Cycle No. 3 (WE Controlled, OE LOW) [33, 34, 35]



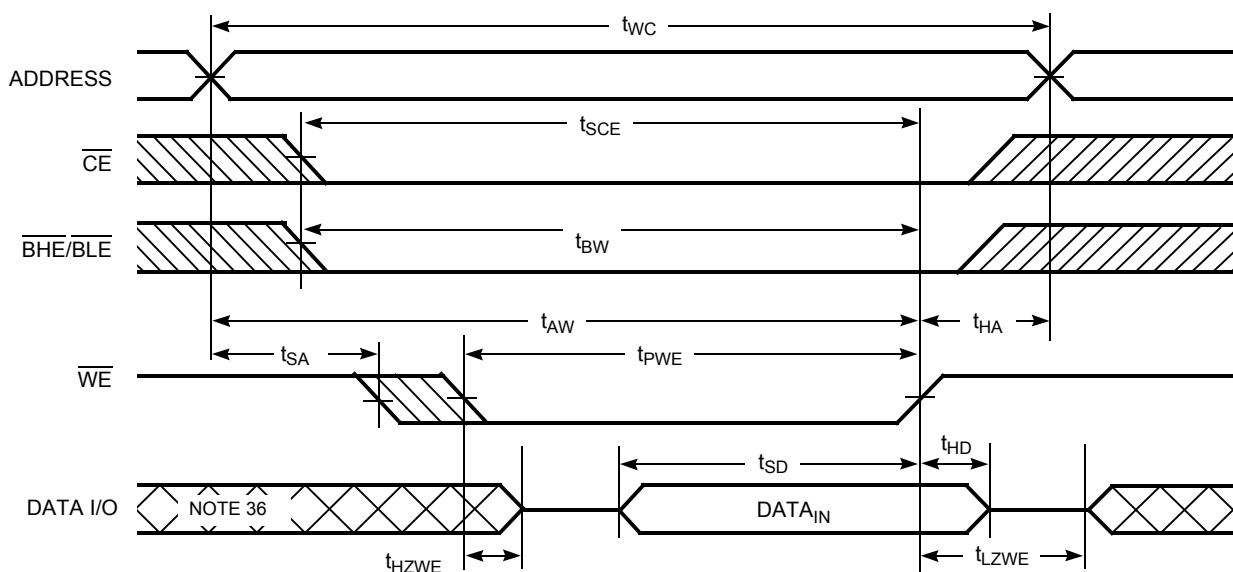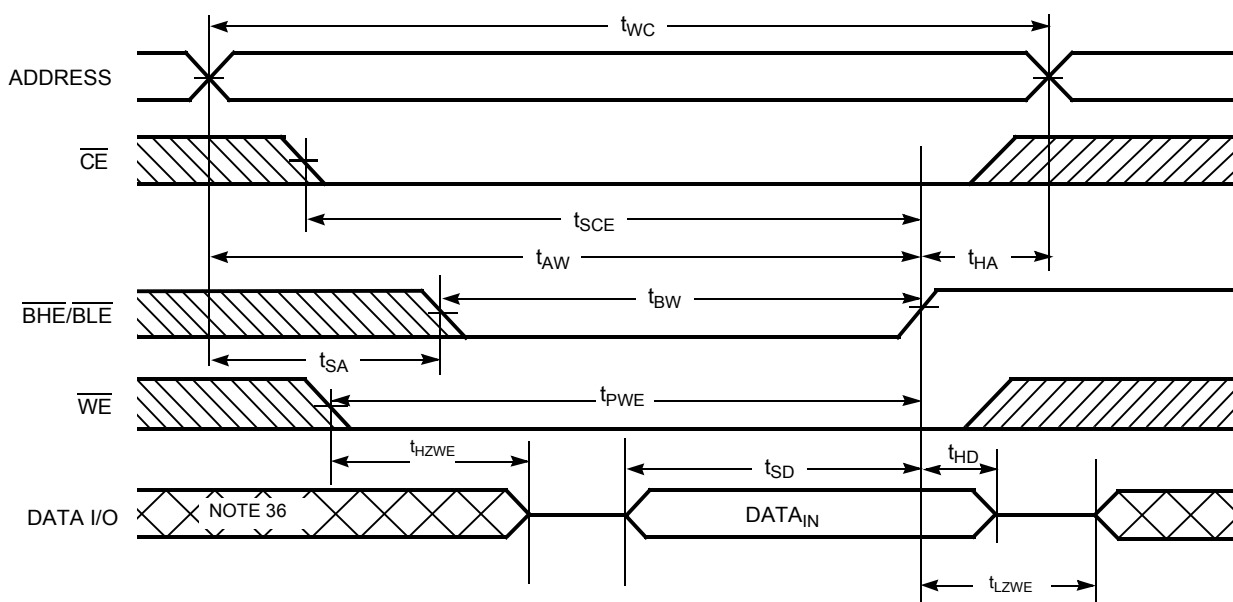### Figure 11. Write Cycle No. 4 (BHE/BLE Controlled) [33, 34]



**Notes**
33. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, CE refers to the internal logical combination of CE₁ and CE₂ such that when CE₁ is LOW and CE₂ is HIGH, CE is LOW. For all other cases CE is HIGH.
34. If CE goes HIGH simultaneously with WE = $V_{IH}$, the output remains in a high impedance state.
35. The minimum write cycle pulse width should be equal to the sum of tSD and tHZWE.
36. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}$ [37, 38] | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | I/Os | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | X | X | H | H | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data out (I/O$_0$–I/O$_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data out (I/O$_0$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data out (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data in (I/O$_0$–I/O$_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data in (I/O$_0$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data in (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High Z | Write | Active ($I_{CC}$) |

**Notes**
37. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE$_2$ such that when $\overline{CE}_1$ is LOW and CE$_2$ is HIGH, CE is LOW. For all other cases CE is HIGH.
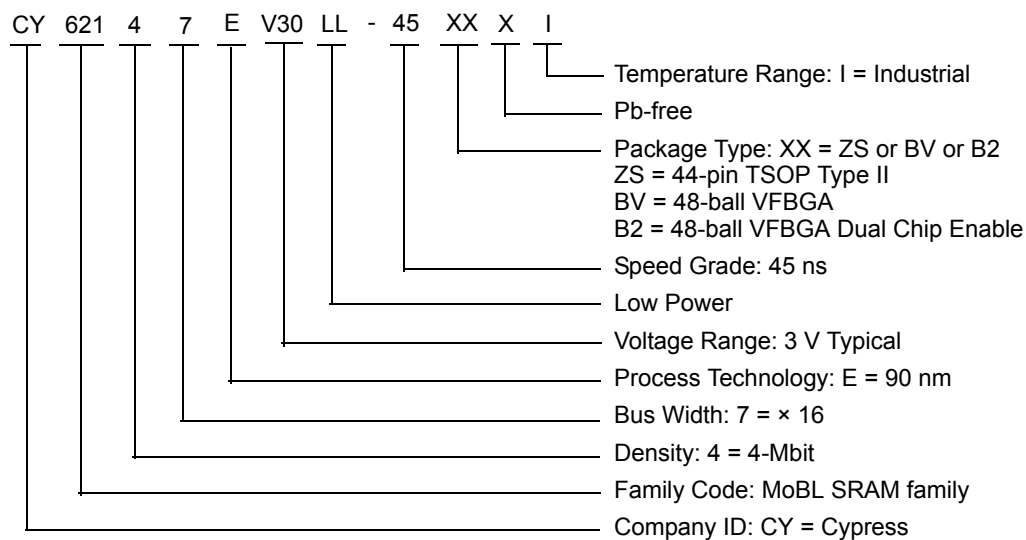38. For the Dual Chip Enable device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE$_2$ such that when $\overline{CE}_1$ is LOW and CE$_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases CE is HIGH. Intermediate voltage levels are not permitted on any of the Chip Enable pins (CE for the Single Chip Enable device; $\overline{CE}_1$ and CE$_2$ for the Dual Chip Enable device).

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62147EV30LL-45BVI | 51-85150 | 48-ball VFBGA [39] | Industrial |
| | CY62147EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) [39] | |
| | CY62147EV30LL-45B2XI | 51-85150 | 48-ball VFBGA (Pb-free) [40] | |
| | CY62147EV30LL-45ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |

Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions

CY 621 4 7 E V30 LL - 45 XX X I

Temperature Range: I = Industrial

Pb-free

Package Type: XX = ZS or BV or B2
ZS = 44-pin TSOP Type II
BV = 48-ball VFBGA
B2 = 48-ball VFBGA Dual Chip Enable

Speed Grade: 45 ns

Low Power

Voltage Range: 3 V Typical

Process Technology: E = 90 nm

Bus Width: 7 = × 16

Density: 4 = 4-Mbit

Family Code: MoBL SRAM family

Company ID: CY = Cypress

**Notes**
39. This BGA package is offered with single chip enable.
40. This BGA package is offered with dual chip enable.

## Package Diagrams

### Figure 12.  48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150
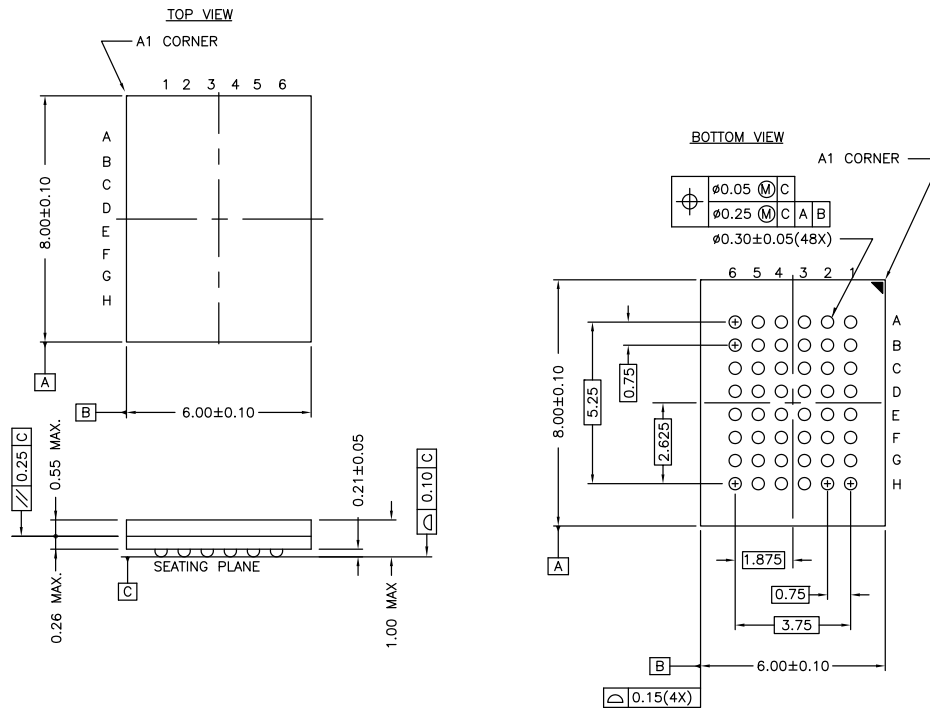


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

## Package Diagrams (continued)

**Figure 13.  44-pin TSOP Z44-II Package Outline, 51-85087**
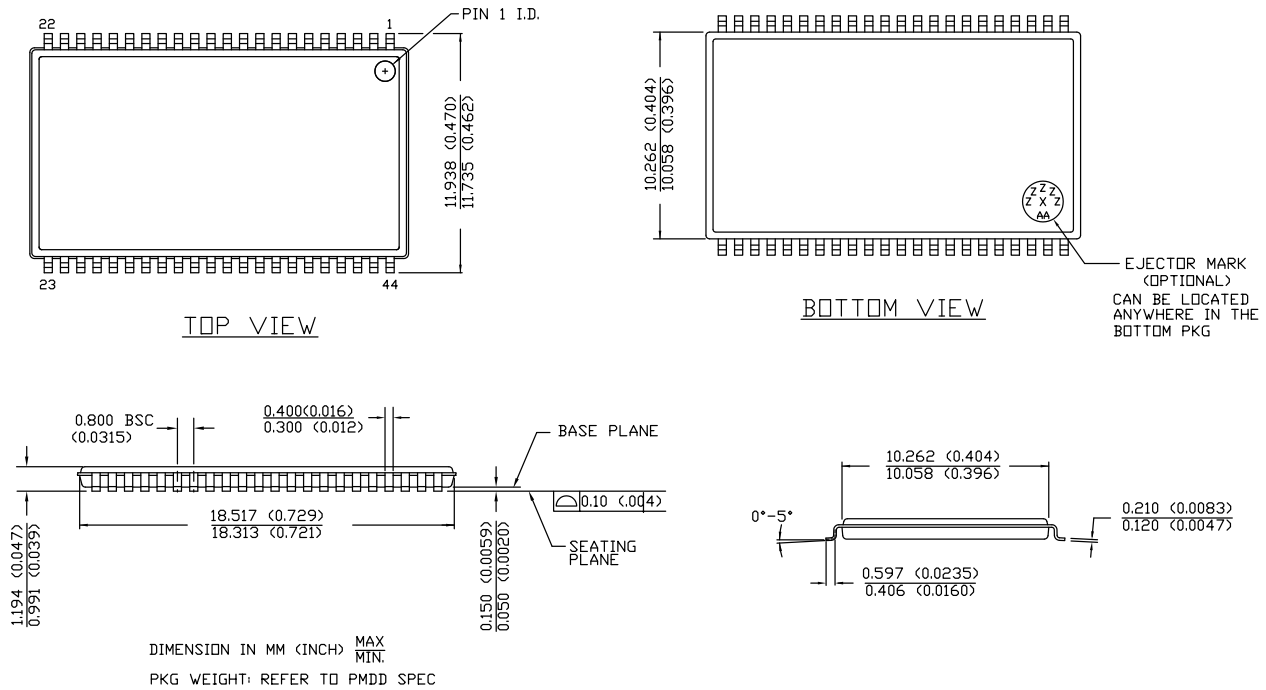


51-85087 *E

## Acronyms

| Acronym | Description |
|---------|-------------|
| $\overline{\text{BHE}}$ | Byte High Enable |
| $\overline{\text{BLE}}$ | Byte Low Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{\text{WE}}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

**Document Title: CY62147EV30 MoBL®, 4-Mbit (256K × 16) Static RAM**
**Document Number: 38-05440**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 201861 | AJU | 01/13/04 | New data sheet. |
| *A | 247009 | SYT | See ECN | Changed status from Advanced Information to Preliminary<br>Moved Product Portfolio to Page 2<br>Changed Vcc stabilization time in footnote #8 from 100 $\mu$s to 200 $\mu$s<br>Removed Footnote #15($t_{LZBE}$) from Previous Revision<br>Changed $I_{CCDR}$ from 2.0 $\mu$A to 2.5 $\mu$A<br>Changed typo in Data Retention Characteristics($t_R$) from 100 $\mu$s to $t_{RC}$ ns<br>Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin<br>Changed $t_{HZOE}$, $t_{HZBE}$, $t_{HZWE}$ from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin<br>Changed $t_{SCE}$ and $t_{BW}$ from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin<br>Changed $t_{HZCE}$ from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin<br>Changed $t_{SD}$ from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin<br>Changed $t_{DOE}$ from 15 to 18 ns for 35 ns Speed Bin<br>Changed Ordering Information to include Pb-Free Packages |
| *B | 414807 | ZSD | See ECN | Changed status from Preliminary to Final<br>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"<br>Removed 35ns Speed Bin, "L" version of CY62147EV30<br>Changed ball E3 from DNU to NC.<br>Removed redundant foot note on DNU.<br>Changed $I_{CC}$ (Max) value from 2 mA to 2.5 mA and $I_{CC}$ (Typ) value from 1.5 mA to 2 mA at f = 1 MHz<br>Changed $I_{CC}$ (Typ) value from 12 mA to 15 mA at f = $f_{max}$<br>Changed $I_{SB1}$ and $I_{SB2}$ Typ values from 0.7 $\mu$A to 1 $\mu$A and Max values from 2.5 $\mu$A to 7 $\mu$A.<br>Changed $I_{CCDR}$ from 2.5 $\mu$A to 7 $\mu$A.<br>Added $I_{CCDR}$ typical value.<br>Changed AC test load capacitance from 50 pF to 30 pF on Page #4, changed $t_{LZOE}$ from 3 ns to 5 ns, changed $t_{LZCE}$, $t_{LZBE}$ and $t_{LZWE}$ from 6 ns to 10 ns, changed $t_{HZCE}$ from 22 ns to 18 ns, changed $t_{PWE}$ from 30 ns to 35 ns and changed $t_{SD}$ from 22 ns to 25 ns.<br>Updated the package diagram 48-pin VFBGA from *B to *D<br>Updated the ordering information table and replaced the Package Name column with Package Diagram. |
| *C | 464503 | NXR | See ECN | Included Automotive Range in product offering<br>Updated Ordering Information. |
| *D | 925501 | VKN | See ECN | Added Preliminary Automotive-A information<br>Added footnote #9 related to $I_{SB2}$ and $I_{CCDR}$<br>Added footnote #14 related AC timing parameters |
| *E | 1045701 | VKN | See ECN | Converted Automotive-A and Automotive -E specs from preliminary to final |
| *F | 2577505 | VKN / PYRS | 10/03/08 | Added -45B2XI part (Dual CE option) |
| *G | 2681901 | VKN / PYRS | 04/01/09 | Added CY62147EV30LL-45ZSXA in the ordering information table |
| *H | 2886488 | AJU | 03/02/2010 | Added Contents.<br>Added Note 38.<br>Updated Package Diagrams.<br>Updated links in Sales, Solutions, and Legal Information. |

## Document History Page (continued)

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| *I | 3109050 | PRAS | 12/13/2010 | Changed Table Footnotes to Notes.<br>Added Ordering Code Definitions. |
| *J | 3123973 | RAME | 01/31/2011 | Separated Industrial and Auto parts from this datasheet<br>Removed Automotive info<br>Added Acronyms and Units of Measure. |
| *K | 3296744 | RAME | 08/09/2011 | Updated Functional Description (Removed reference to AN1064 SRAM system guidelines).<br>Added $I_{SB1}$ to footnote 9 and 12.<br>Notes 17 and 18 moved to parameter section of Switching Characteristics.<br>Added Note 21 and referred the same note in the description of $t_{LZBE}$ parameter. |
| *L | 3456837 | TAVA | 12/06/2011 | Updated Package Diagrams.<br>Updated to new template. |
| *M | 3724736 | JISH | 08/23/2012 | Fixed typo errors and minor clean-up. |
| *N | 4102445 | VINI | 08/22/2013 | Updated Switching Characteristics:<br>Updated Note 18.<br>Updated Package Diagrams:<br>spec 51-85150 – Changed revision from *G to *H.<br>spec 51-85087 – Changed revision from *D to *E.<br>Updated to new template.<br>Completing Sunset Review. |
| *O | 4576526 | VINI | 11/21/2014 | Updated Functional Description:<br>Added "For a complete list of related documentation, click here." at the end.<br>Updated Switching Characteristics:<br>Added Note 23 and referred the same note in "Write Cycle".<br>Updated Switching Waveforms:<br>Added Note 35 and referred the same note in Figure 10. |
| *P | 4918858 | VINI | 09/14/2015 | Updated Switching Waveforms:<br>Updated caption of Figure 11 (Removed "$\overline{OE}$ LOW").<br>Updated to new template.<br>Completing Sunset Review. |
| *Q | 5445135 | VINI | 09/22/2016 | Updated Thermal Resistance:<br>Updated all values of $\Theta_{JA}$ and $\Theta_{JC}$ parameters.<br>Updated to new template.<br>Completing Sunset Review. |
| *R | 5984537 | AESATMP9 | 12/05/2017 | Updated logo and copyright. |

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