**MOTOROLA**
SEMICONDUCTOR TECHNICAL DATA

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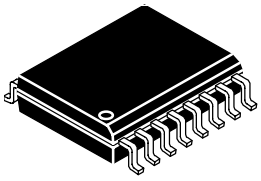
**33099**

# Adaptive Alternator Voltage Regulator

**ALTERNATOR VOLTAGE REGULATOR**

The 33099 is designed to regulate the output voltage in diode-rectified alternator charging systems common to automotive applications. The 33099 provides either an analog or digital fixed frequency duty cycle (ON/OFF ratio) control of an alternator's field current. Load Response Control (LRC) of the alternator field current is accomplished by selecting the duty cycle for prevailing engine conditions to eliminate engine speed hunting and vibrations caused by abrupt torque loading of the engine owing to sudden electrical loads being applied to the system at low engine RPM. Four LRC rates are selectable.

The 33099 uses a feedback voltage to establish an alternator field current that is in harmony with system load currents. The output voltage is monitored by an internal voltage divider scheme and compared to an internal voltage ramp referenced to a bandgap voltage. This approach provides precision output voltage control over a wide range of temperature, electrical loads, and engine RPM.



**DW SUFFIX**
**CASE 751G-04**
**16-TERMINAL SOICW**

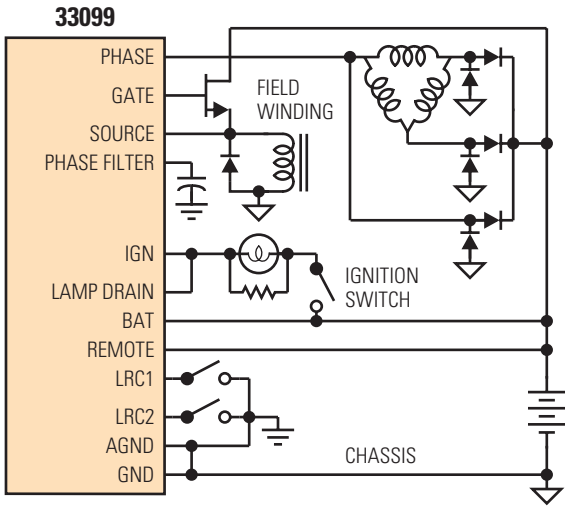
**Features**

- External High-Side MOSFET Control of a Ground-Referenced Field Winding
- LRC Active During Initial Start
- $V_{set}$ at ±0.1 V @ 25°C
- <0.1 V Variation Over Engine Speeds of 2,000 to 10,000 RPM
- <0.2 V Variation Over 10% to 95% of Maximum Field Current
- Controlled MOSFET and Field Flyback Diode Recovery Characteristics for Minimum RFI
- Trimmed Devices Available at 14.6 V and 14.8 V (typical) $V_{set}$

**ORDERING INFORMATION**

| Device | Temperature Range ($T_A$) | Package |
|---|---|---|
| MC33099DW/R2 | -40°C to 125°C | 16 SOICW |
| MC33099CDW/R2 | | |

**33099 Simplified Application Diagram**




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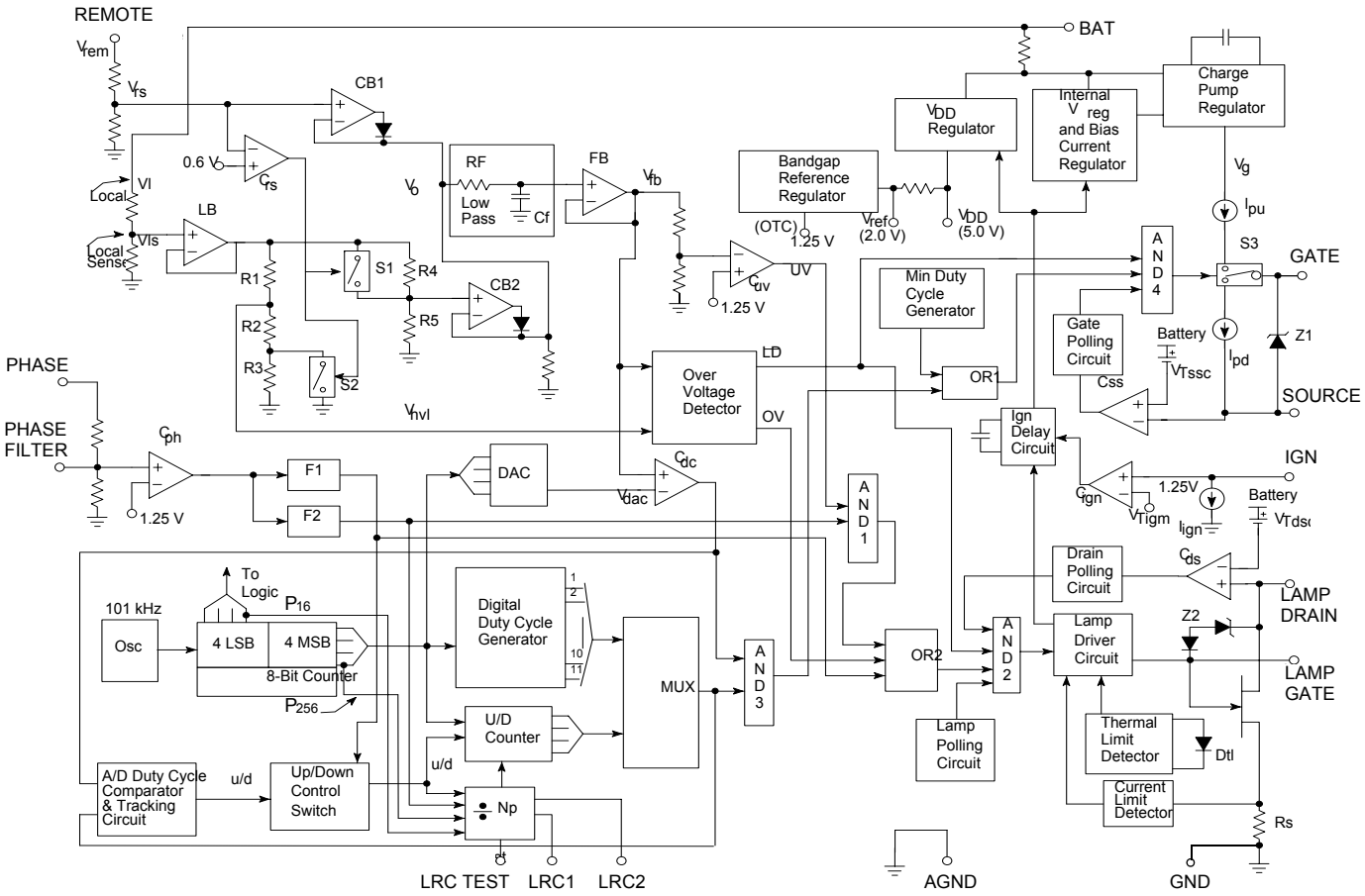
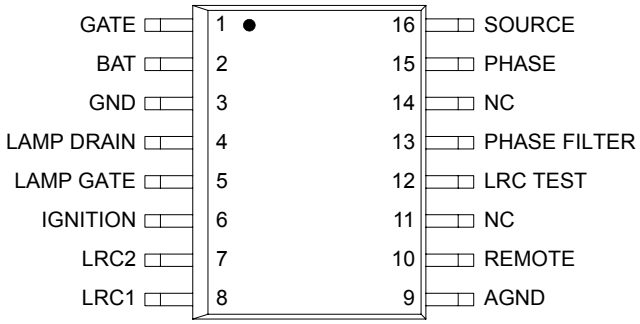



**Figure 1. 33099 Simplified Internal Block Diagram**

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**TERMINAL FUNCTION DESCRIPTION**

| Terminal | Terminal Name | Formal Name | Definition |
|---|---|---|---|
| 1 | GATE | Gate Drive | Controls the GATE of the MOSFET to control the alternator field current. |
| 2 | BAT | Battery | Primary power connection to the system battery. |
| 3 | GND | Ground | Source lamp current and digital ground. |
| 4 | LAMP DRAIN | Lamp Drain | Controls the Fault Lamp current. |
| 5 | LAMP GATE | Lamp Gate | Controls the Fault Lamp internal driver as an override function. |
| 6 | IGN | Ignition | Controls the ON or OFF function of the regulator. |
| 7<br>8 | LRC2<br>LRC1 | Load Response Control 2<br>Load Response Control 1 | Inputs for selecting the LRC rate. |
| 9 | AGND | Analog Ground | Ground connection for analog circuitry. |
| 10 | REMOTE | Remote | Provides for external Kelvin connection to system battery. |
| 11, 14 | NC | No Connect | No internal connection to this terminal. |
| 12 | LRC TEST | Load Response Control Test | Provides acceleration of LRC rate for testing. |
| 13 | PHASE FILTER | Phase Filter | Provides access to Phase Resistive Divider for External Phase Filter capacitance. |
| 15 | PHASE | Phase Sense Input | Input for phase voltage. |
| 16 | SOURCE | Source | Coupled to source of MOSFET to provide a GATE voltage reference and to monitor for source shorts to ground. |

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## MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| Power Supply Voltage | $V_{bat}$ | 24 | V |
| Load Dump Transient Voltage (Note 1) | $+V_{max}$ | 40 | |
| Negative Voltage (Note 2) | $-V_{min}$ | -2.5 | |
| ESD Voltage | | | V |
| Human Body Model (Note 3) | $V_{ESD1}$ | ±2000 | |
| Machine Model (Note 4) (Note 5) | $V_{ESD2}$ | ±200 | |
| **THERMAL RATINGS** | | | |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 to 125 | °C |
| Storage Temperature Range | $T_{STG}$ | -45 to 150 | °C |
| Power Dissipation and Thermal Characteristics | | | |
| Maximum Power Dissipation @ $T_A$ = 125°C | $P_D$ | 640 | mW |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 85 | °C/W |
| Terminal Soldering Temperature (Note 6) | $T_{SOLDER}$ | 220 | °C |

Notes

1. 125ns wide square wave pulse.
2. Maximum time = 2 minutes.
3. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$=100 pF, $R_{ZAP}$=1500 Ω).
4. ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}$=200 pF, $R_{ZAP}$=0 Ω).
5. ESD2 voltage capability of PHASE FILTER terminal is greater than 150 V. All other device terminals are as indicated.
6. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

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**STATIC ELECTRICAL CHARACTERISTICS** $T_A$ = 25°C unless otherwise noted.

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Regulation Voltage @ 50% Duty Cycle | | $V_{set}$ | | | | V |
| $V_{rem} = V_{set}$ or $V_{rem} < V_{Trem}$ | MC33099 | | 14.55 | 14.8 | 15.05 | |
| $V_{rem} = V_{set}$ or $V_{rem} < V_{Trem}$ | MC33099C | | 14.3 | 14.6 | 14.85 | |
| Regulation Voltage Range | | dVset | | | | mV |
| 10% < DC < 95% | | | – | 210 | 300 | |
| Regulation Voltage Temperature Coefficient (TC) | | $TC(V_{set})$ | | | | mV/°C |
| $V_{rem} = V_{bat}$ or $V_{rem} < V_{Trem}$ | | | -13 | -11 | -9 | |
| Power Up/Down IGN Threshold Voltage | | $V_{Tign}$ | 0.9 | 1.25 | 1.6 | V |
| Operating Drain Current (Ignition ON) | | | | | | mA |
| $V_{ign} > V_{Tign}$, $V_{rem} = V_{ph} = V_{set}$, $T_A$ = 25°C | | $I_{Q1(on)}$ | – | 6.5 | 8.0 | |
| $V_{ign} > V_{Tign}$, $V_{rem} = V_{ph} = V_{set}$, -40°C ≤ $T_A$ ≤ 125°C | | $I_{Q2(on)}$ | – | 6.5 | 8.4 | |
| Standby Drain Current (Ignition OFF) | | | | | | mA |
| $V_{ign} < V_{Tign}$, $V_{ph}$ = 0 V, $V_{rem} = V_{bat}$ = 12.6 V, $T_A$ = 25°C | | $I_{Q1(off)}$ | – | 0.6 | 1.5 | |
| $V_{ign} < V_{Tign}$, $V_{ph}$ = 0 V, $V_{rem} = V_{bat}$ = 12.6 V, -40°C ≤ $T_A$ ≤ 125°C | | $I_{Q2(off)}$ | – | 1.0 | 3.4 | |
| Remote Loss Voltage Threshold | | $V_{Trem}$ | 4.2 | 4.5 | 4.8 | V |
| Phase Detection Threshold Voltage | | $V_{Tph}$ | 3.75 | 4.0 | 4.25 | V |
| Undervoltage Threshold Voltage | | $V_{Tuv}$ | | | | V |
| $V_{set}$ = 14.8 typical | MC33099 | | 10.9 | 11.35 | 11.6 | |
| $V_{set}$ = 14.6 typical | MC33099C | | 10.35 | 10.95 | 11.55 | |
| Overvoltage Threshold Voltage | | $V_{Tov}$ | | | | V |
| $V_{set}$ = 14.8 typical | MC33099 | | 16.15 | 16.65 | 17.15 | |
| $V_{set}$ = 14.6 typical | MC33099C | | 15.8 | 16.4 | 17.0 | |
| Overvoltage Threshold Voltage TC | | $TC(V_{Tov})$ | – | -12.4 | – | mV/°C |
| Load Dump Threshold Voltage | | $V_{Tld}$ | | | | V |
| $V_{set}$ = 14.8 typical | MC33099 | | 18.9 | 19.25 | 19.8 | |
| $V_{set}$ = 14.6 typical | MC33099C | | 18.45 | 19.15 | 19.85 | |
| Load Dump Threshold Voltage TC | | $TC(V_{Tld})$ | – | -14.3 | – | mV/°C |
| Secondary Regulation | | $V_{set2}$ | | | | V |
| $V_{set}$ = 14.8 typical | MC33099 | | 18.0 | 18.5 | 18.8 | |
| $V_{set}$ = 14.6 typical | MC33099C | | 17.65 | 18.15 | 18.75 | |
| Secondary Regulation TC | | $TC(V_{set2})$ | – | -13.4 | – | mV/°C |
| Secondary Load Dump Threshold Voltage | | $V_{Tld2}$ | | | | V |
| $V_{set}$ = 14.8 typical | MC33099 | | 23.5 | 24 | 25 | |
| $V_{set}$ = 14.6 typical | MC33099C | | 23.5 | 23.85 | 24.65 | |
| Secondary Load Dump Threshold Voltage TC | | $TC(V_{Tld2})$ | – | -17.9 | – | mV/°C |

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**STATIC ELECTRICAL CHARACTERISTICS (continued)** $T_A$ = 25°C unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Lamp Drain Short Circuit Threshold Voltage (Note 7) | $V_{Tdsc}$ | 1.8 | 2.25 | 2.85 | V |
| Lamp Drain Short Circuit Current | $I_{dsc}$ | 2.0 | 2.5 | 3.0 | Amps |
| Lamp Drain ON Voltage<br>$I_{lamp}$ = 0.4 A | $V_{d(sat)}$ | – | 0.3 | 2.5 | V |
| Lamp Drain-to-GATE Clamping Voltage | $V_{dg}$ | – | 48.48 | 55 | V |
| Lamp GATE Override Resistance | $R_{lg}$ | – | 4.6 | – | kΩ |
| Lamp Driver Thermal Shutdown Temperature Limit (Note 7) | $T_{Lim}$ | – | 185 | – | °C |
| GATE Drive Source Current | $I_{pu}$ | 240 | 300 | 340 | μA |
| GATE Drive Sink Current | $I_{pd}$ | 400 | 480 | 560 | μA |
| GATE Drive GATE-to-Source Clamping Voltage | $V_{gs}$ | 10 | 12 | 15 | V |
| Minimum Charge Pump GATE Drive Voltage<br>$V_{bat} = V_{source} = V_{set}$ | $V_{g(min)}$ | 21.5 | 23.4 | – | V |
| Source Short Circuit Threshold Voltage | $V_{Tssc}$ | 1.85 | 2.3 | 2.75 | V |
| Remote Input Resistance<br>$V_{rem} = V_{set}$ | $R_{rem}$ | – | 68 | – | kΩ |
| Phase Input Resistance<br>$V_{ph} = V_{set}$ | $R_{ph}$ | – | 60 | – | kΩ |
| IGN Input Pull-Down Current<br>$V_{ign}$ = 1.25 V | $I_{ign}$ | 40 | 73 | 90 | μA |
| LRC Input Current<br>$V_{lrc}$ = 0 V | $I_{lrc}$ | 35 | 45 | 55 | μA |

Notes
7. Not 100% tested.

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**DYNAMIC ELECTRICAL CHARACTERISTICS** $T_A$ = 25°C unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Duty Cycle Regulation Output Frequency<br>$f_{osc}/256$ | $f_{dc}$ | <br>300 | <br>375 | <br>440 | Hz |
| Phase Rotation Detection Frequency | $f_1$ | 44.28 | 49 | 53.8 | Hz |
| Low/High RPM Transition Phase Frequency | $f_2$ | 267.5 | 296 | 325 | Hz |
| GATE Duty Cycle at Startup and WOT<br>$f_{ph} > f2$ | $DC_{start}$ | <br>30 | <br>31.25 | <br>34.5 | % |
| Minimum GATE LRC Duty Cycle<br>$f_{ph} < f2$ | $DC_{(LRC)min}$ | <br>29 | <br>31.25 | <br>33.5 | % |
| Minimum GATE Duty Cycle<br>$V_{bat} > V_{reg(max)}$ | $DC_{min}$ | <br>2.1 | <br>3.1 | <br>3.3 | % |
| LRC Increasing GATE Duty Cycle Rate<br>Low RPM Mode ($f_{ph} < f2$)<br>LRC1 at GND, LRC2 at GND<br>LRC1 Open, LRC2 at GND<br>LRC1 at GND, LRC2 Open<br>LRC1 Open, LRC2 Open<br>High RPM Mode ($f_{ph} > f2$) | <br><br>$R_{lrc1}$<br>$R_{lrc2}$<br>$R_{lrc3}$<br>$R_{lrc4}$<br>$R_{lrc(max)}$ | <br><br>–<br>–<br>–<br>–<br>– | <br><br>9.31<br>12.45<br>18.71<br>37.42<br>616 | <br><br>–<br>–<br>–<br>–<br>– | %/s |
| Ignition Turn OFF Delay (Lamp ON) | $t_{id(off)}$ | – | 10.2 | – | ms |
| Lamp Short Circuit ON Polling Frequency | $f_{lsc}$ | – | 98.6 | – | Hz |
| Lamp Short Circuit ON Duty Cycle | $DC_l$ | – | 1.56 | – | % |
| Lamp OFF Polling Frequency | $f_{l(off)}$ | – | 98.6 | – | Hz |
| Lamp Polling OFF Duty Cycle | $DC_{l(off)}$ | – | 1.56 | – | % |
| Field Short Circuit ON Polling Frequency | $f_{fsc}$ | – | 98.6 | – | Hz |
| Field Short Circuit Polling ON Duty Cycle | $DC_f$ | – | 1.56 | – | % |

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## SYSTEM/APPLICATION INFORMATION

### INTRODUCTION

The 33099 is specifically designed for regulation of an automotive system voltage using diode-rectified alternator charging systems commonly found in automotive applications. The 33099 provides either an analog or digital duty cycle control of an ON/OFF ratio of an alternator field current at a fixed frequency. This provides for a Load Response Control (LRC) of the alternator field current at low engine RPM to eliminate engine speed hunting and vibration owing to abrupt torque loading of the engine when a sudden electrical load is applied to the system. Four LRC rates are selectable using a combination of terminals 7 and 8 being connected to ground.

The 33099 provides a regulated voltage feedback system to activate the alternator field current in response to system load current. The output voltage is monitored by an internal voltage divider scheme and compared to an internal voltage ramp referenced to a bandgap voltage. The 33099 regulates the system voltage to 14.8 V for the DW suffix and to 14.6 V for the CDW suffix by generating a pulse width modulation (PWM) voltage waveform at the GATE of an external MOSFET to provide an average alternator field coil current as a function of the internal voltage comparison.

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## APPLICATIONS

### Introduction

The 33099 is an alternator voltage regulator designed with internal level shifting resistors to control the voltage in a 12 V automotive system that uses a three-phase alternator with a rotating field winding. The system shown in Figure 2 includes an alternator with its associated field coil, stator coils and rectifiers, an automotive battery, a fault indicator lamp, an ignition switch, a field flyback diode, and the 33099.

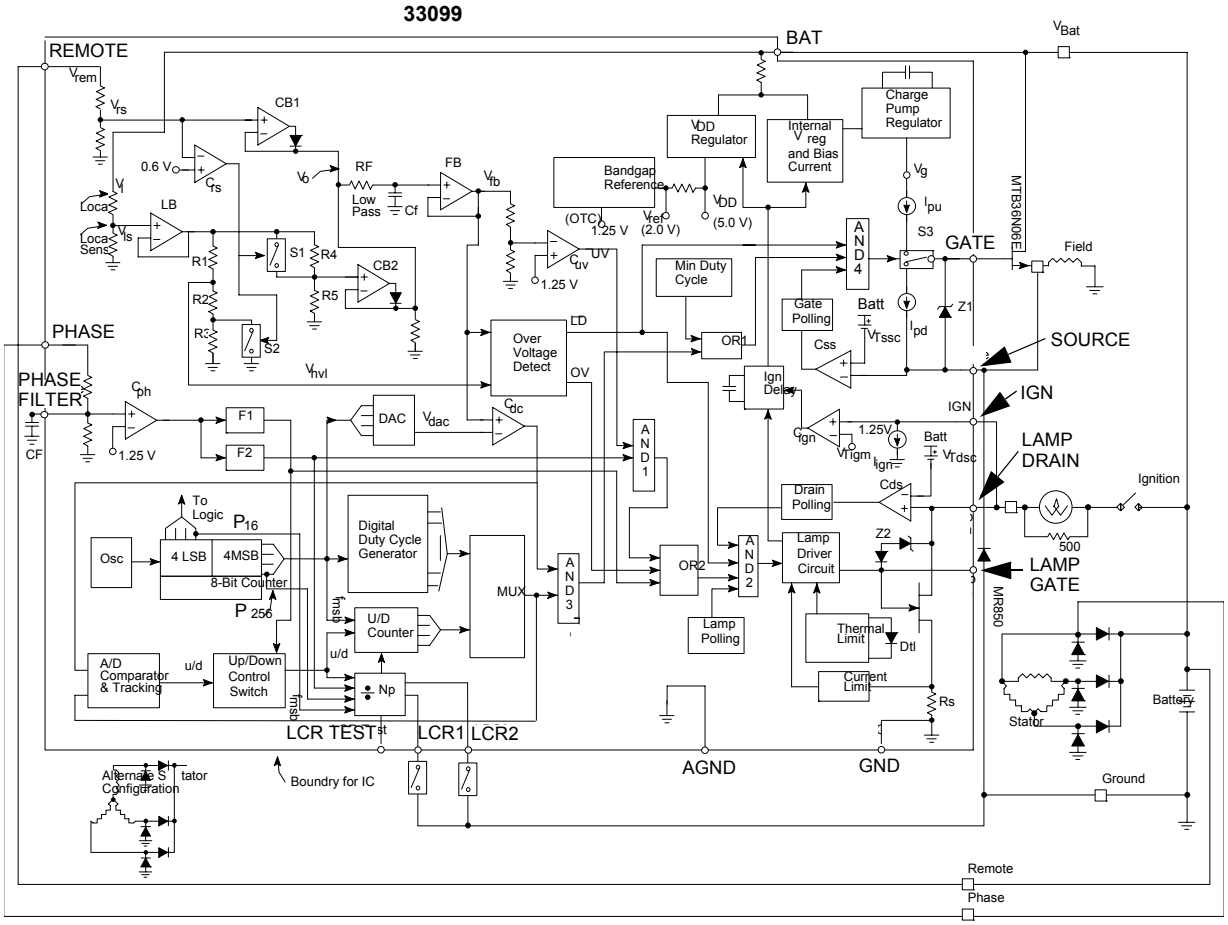



**Figure 2. 33099 Simplified Application**

The 12 V system voltage ($V_{bat}$) is connected to a REMOTE input by a remote wire, which provides the IC regulator with an external Kelvin connection directly to the battery to provide REMOTE voltage, $V_{rem}$. The system voltage at the BAT terminal is also sensed by an internal Local IC connection as Local voltage $V_l$. The Local connection is provided in the event the remote wire or remote connection becomes faulty such as being resistive, an open, or shorted to ground.

The PHASE input is normally connected to a tap on one corner of the alternator's stator winding, which provides an AC phase voltage ($V_{ph}$) for the IC to determine the rotational frequency ($f_{ph}$) of the alternator rotor. Two frequency comparators (F1 and F2) monitor voltage $V_{ph}$ to determine a phase rotation detection frequency ($f_1$) and a Low/High RPM transition phase frequency ($f_2$), respectively. A PHASE FILTER terminal is provided for externally providing a filter capacitance for filtering phase input noise.

The regulated DC system set voltage ($V_{set}$) is achieved by employing feedback to compare a ratioed value of $V_{set}$ to an internal IC bandgap voltage reference having a negative temperature coefficient (TC). The GATE drive of an external N-channel MOSFET is regulated by the IC to control the field current in the alternator field coil as an alternating ON or OFF state dependent on load current conditions affecting voltage $V_{set}$. The external MOSFET receives GATE-to-source voltage drive from between the GATE and SOURCE output terminals of the IC. The GATE-to-source voltage is a Pulse Width Modulated (PWM) waveform having a variable ON/OFF duty cycle ratio that is determined by an analog or a digital duty cycle control circuitry that responds to variations in the system voltage due to variations in system load current. The PWM

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waveform has a duty cycle regulation output frequency of about 395 Hz ($f_{dc}$) defined by an 8-bit division of an internal 101 kHz oscillator clock frequency ($f_{osc}$). The GATE voltage at the GATE terminal is due to a charge pump GATE voltage ($V_g$) generated by voltage multiplication using an internal charge pump voltage regulator. The high GATE-to-source voltage applied to the external MOSFET during the ON cycle of the PWM waveform minimizes a low drain-to-source ON resistance ($R_{DS(ON)}$) and associated drain-to-source voltage $V_{d(SAT)}$ to maximize the field current while minimizing the associated power dissipation in the MOSFET.

A unique feature of the 33099 is the combinational use of analog and digital duty cycle controllers to provide a Load Response Control (LRC) duty cycle function when rotor frequency $f_{ph}$ is less than frequency $f_2$. A classic analog duty cycle function is provided at the GATE output when frequency $f_{ph}$ is greater than frequency $f_2$. During the LRC mode when $f_1 < f_{ph} < f_2$, a sudden decrease in the system voltage due to a sudden increase in system load current will cause the analog duty cycle to rapidly increase to as great as 100%. However, the LRC circuitry causes the digital duty cycle to increase to 100% at a controlled predetermined LRC rate and overrides the analog duty cycle. Thus the alternator response time is decreased in the LRC mode and prevents the alternator from placing a sudden high torque load on the automobile engine during this slow RPM mode. This can occur when a high current accessory is switched on to the 12 V system, producing a sudden drop in system voltage. When frequency $f_{ph}$ is greater than frequency $f_2$, the slow LRC response is not in effect and the analog duty cycle controller controls the PWM voltage waveform applied to the external MOSFET to regulate the system voltage. By selectively coupling the LRC1 and LRC2 terminals to ground or leaving them open, the user can program four different LRC rates ($R_{lrc1}$-$R_{lrc4}$) from 9.37%/sec to 37.4%/sec. During an initial ignition ON and engine start-up, the LRC rate is also in effect to minimize alternator torque loading on the engine during start, even when a Wide Open Throttle (WOT) condition ($f_{ph} > f_2$) occurs.

An internal N-Channel MOSFET is provided on the IC to directly drive lamp current as a fault indicator. The fault lamp is connected between the low side of the ignition switch and the LAMP DRAIN terminal of the IC. A fault is indicated during an undervoltage battery condition when frequency $f_{ph}$ is greater than frequency $f_2$, during an overvoltage battery condition, and when frequency $f_{ph}$ is less than frequency $f_1$. Frequency $f_{ph} < f_1$ when an insufficient alternator output voltage results or a slow or non-rotating rotor occurs due to a slipping or broken belt. An external LAMP GATE terminal is also provided for the internal lamp driver to allow the user to override the internal IC fault logic and externally drive the internal lamp drive MOSFET.

When a loose wire or battery terminal corrosion causes the Remote voltage to decrease but is not a Remote Open condition, the system voltage will increase, causing an overvoltage Lamp fault indication, and is regulated at a secondary value of about 18.5 V.

During a system load dump condition, load dump protection circuitry prevents GATE-to-source drive to the external MOSFET and to the internal lamp drive MOSFET. This ensures that neither the field current nor the lamp current is activated during load dump conditions. A drain-to-GATE voltage clamp is also provided for the internal lamp driver for further protection of this driver during load dump.

An ignition terminal (IGN) is provided to activate the regulator from the standby mode into a normal operating mode when the ignition switch is ON and an ignition voltage ($V_{ign}$) is greater than a power up/down ignition threshold voltage ($V_{Tign}$). When the ignition switch is OFF, voltage $V_{ign}$ is less than voltage $V_{Tign}$, and the regulator is switched into a low current standby mode, when frequency $f_{ph} < f_1$. The IGN terminal can either be coupled to the low side of the ignition switch or to the low side of the lamp. When the IGN terminal is connected to the low side of the lamp, the lamp must be shunted by a resistor to ensure that ignition ON is sensed, even with an OPEN lamp fault condition. When the lamp in ON, lamp current is polled OFF periodically at an ignition polling frequency in order for the IGN terminal to periodically sense that the ignition voltage is high even though the lamp is ON. An ignition input pull-down current ($I_{ign}$) is provided to pull voltage $V_{ign}$ to ground when the IGN terminal is OPEN or terminated on a high resistance.

Two ground terminals are provided by the 33099 to separate sensitive analog circuit ground (AGND) from noisy digital and high-current ground (GND).

### Alternator Regulator Biasing and Power Up/Down

The biasing of the regulator is derived from the BAT terminal voltage $V_{bat}$. In the normal operating mode when the ignition switch is ON and voltage $V_{ign}$ is greater than $V_{Tign}$ (about 1.25 V), a 5.0 V $V_{DD}$ voltage regulator biases the IC logic and provides bias to a bandgap shunt voltage regulator. The bandgap regulator maintains a reference voltage ($V_{ref}$) of approximately 2.0 V with an internal negative temperature coefficient (-TC) as well as a 1.25 V Zero Temperature Coefficient (OTC) reference voltage. Additional bias currents and reference voltages, including a charge pump GATE voltage $V_g$, are also generated from voltage $V_{bat}$. The typically ignition ON drain current ($I_{Q1(on)}$) is about 6.5 mA at 25°C. When the ignition switch is OFF and voltage $V_{ign}$ is less than $V_{Tign}$, the regulator is in a low current standby mode, having a standby drain current of about 0.7 mA ($I_{Q1(off)}$) at 25°C. During the sleep mode, some internal voltage regulators and bias currents are either terminated or minimized. However, the $V_{DD}$ regulator and the bandgap voltage regulator continue to maintain voltages $V_{DD}$ for the logic, the 2.0 V $V_{ref}$, and the 1.25 V reference voltage. In addition, all logic is reset in the standby mode.

After switching the ignition switch to the ON position, voltage $V_{ign}$ will exceed voltage $V_{Tign,}$ causing comparator $C_{ign}$ to switch states, providing an ignition-ON signal to the Ignition Delay circuit. After an Ignition start Delay Time of 500 ms, the Ignition Delay circuit activates additional current for the $V_{DD}$

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regulator and activates all other voltage regulators and bias currents. After engine start, the LRC mode is activated, independent of the phase frequency or independent of a Wide Open Throttle condition. When the battery system voltage increases to $V_{set}$, the regulator resumes the normal operational mode. After switching the ignition switch to the OFF position, voltage $V_{ign}$ decreases below voltage $V_{Tign}$, causing the comparator $C_{ign}$ to provide an ignition-OFF signal to the Ignition Delay Circuit. After phase frequency $f_{ph} < f_1$ due to ignition turn OFF, supply currents and voltages are reduced in the regulator to provide the standby drain current drain. However, voltage $V_{DD}$ for logic and voltage $V_{ref}$ for reference voltages remain active to be able to sense an ignition input voltage.

In some applications, the ignition input is connected to the low side of the fault lamp as shown in Figure 2, page 9. When the lamp driver circuitry is generating a lamp ON signal, a lamp polling signal causes the Lamp Drain output to be periodically GATED OFF. As a result, voltage $V_{ign} > V_{Tign}$ during the lamp OFF polling period, causing comparator $C_{ign}$ to periodically provides an ignition-ON signal to the Ignition Delay Circuit. During the Lamp On condition, the Ignition Delay Circuit provides a minimum ignition turn-off delay ($t_{id(off)}$) such that all currents and regulator voltages remain ON between the Lamp Off polling pulses.

### Battery and Alternator Output Voltage Sensing

The system battery voltage is directly sensed by the REMOTE input using a remote wire as a Kelvin connection. The Remote input resistance ($R_{rem}$) at the REMOTE input is typically 68 kΩ. The voltage at the Remote Sense input ($V_{rs}$) is a ratioed value of the Remote voltage ($V_{rem}$). The intended ratio of $V_{rem}/V_{rs}$ is about 7.45. The BAT terminal voltage ($V_{bat}$) is also sensed as an internal Local voltage ($V_l$). A Local Sense voltage ($V_{ls}$) is a ratioed value of voltage $V_l$, where the intended ratio of $V_l/V_{ls}$ is also 7.45. The Local internal connection is provided for fault protection against the remote wire being grounded or exhibiting a high remote wire resistance due to being disconnected or due to a corrosive or loose connection. Thus the Local connection ensures that alternator regulation of the system voltage continues in well-defined states for all possible Remote input fault conditions.

### Local and Remote Voltage Processing and Switching

During Remote operation both the external Remote input connection and internal Local connection senses approximately the same regulated system voltage of $V_{set}$ = 14.8 V. For this case, voltages $V_{rs}$ and $V_{ls}$ are approximately 2.0 V. Because the remote switching comparator $C_{rs}$ is referenced to 0.6 V, both switches S1 and S2 are OPEN and remain open when voltage $V_{rs} > 0.6$ V or when voltage $V_{rem}$ is greater than the remote loss threshold voltage ($V_{Trem}$). Voltage $V_{rs}$ is coupled to the input of a unity-gain combiner/buffer CB1. Voltage $V_{ls}$ is buffered and coupled to the output of a unity-gain Local Buffer (LB) and ratioed by the R5/(R4+R5) resistor divider to provide an input voltage to a unity-gain combiner/buffer CB2. Thus the voltage at the input of the combiner CB2 is normally 0.8 $V_{ls}$ (or 1.6 V typically), while voltage $V_{rs}$ on the input of CB1 is typically 2.0 V. Because voltage $V_o$ reflects the highest voltage at the input of either combiner, voltage $V_o$ will be voltage $V_{rs}$ in Remote operation with Remote connected to $V_{bat}$. For this case, voltage $V_{rs}$ is filtered by a 300 Hz low-pass filter and translated to the FB buffer output. Voltage $V_{rs}$ at the FB buffer output is then compared to a digital-to-analog converter output voltage ramp ($V_{dac}$) for duty cycle regulation.

During a Remote fault condition when the remote sense line is OPEN or grounded, voltage $V_{rs}$ at the Remote Sense input will be zero, causing comparator $C_{rs}$ to activate switches S1 and S2 to a CLOSED position. As a result, voltage $V_{ls}$ is coupled through buffer LB directly to the input of combiner CB2. Because the voltage $V_{ls}$ on the input of combiner CB2 is greater than voltage $V_{rs}$ (= 0 V) on the input of combiner CB1, voltage $V_{ls}$ is coupled to the output of the combiners as voltage $V_o$. Thus in this fault case, voltage $V_{ls}$ is filtered and translated to the FB buffer output for being compared to voltage ramp $V_{dac}$ for regulation.

During a remote fault condition in which the resistance of the Remote sense wire increases due to the corrosion or a loose connection, a finite external remote fault resistance occurs causing voltage $V_{rem}$ to decrease, but voltage $V_{rem}$ remains greater than voltage $V_{Trem}$. As a result, switches S1 and S2 remain in an OPEN condition, while the system voltage will increase due to the effective increase in the Remote resistor divider ratio. As a result, voltage $V_l$ increases until the voltage at the input of combiner CB2 is approximately 2.0 V, or $V_{ls}$ is about 1.2 (2.0 V), or 2.25 V due to the R4/R5 divider ratio. Because the local divider ratio translates voltage $V_{ls}$ to $V_{bat}$ by about factor 7.4, the final regulated output voltage for this condition is 7.4 (2.25), or 18.5 V. This is the secondary regulation voltage ($V_{set2}$). When the system voltage increases to the Overvoltage Threshold ($V_{Tov}$), a fault indication occurs by the lamp. Thus this particular Remote fault condition produces a fault indication, but regulates to prevent an extreme system overvoltage condition. When the Remote fault resistance becomes great enough to cause voltage $V_{rem} < V_{Trem}$, the regulated system voltage returns to the local regulation as described for an OPEN or grounded Remote input.

### Internal Clock Oscillator and 8-Bit Counter

An internal clock oscillator is provided having a typical oscillation frequency ($f_{osc}$) of 101 kHz. The output of the oscillator is coupled to an 8-bit counter that provides 8 counting bits to the logic and the four most significant counting bits (MSB) to the LRC circuitry and to a digital-to-analog converter

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(DAC) waveform generator. The output MSB frequency ($f_{msb}$) of the 8-bit divider is about 395 Hz ($f_{msb} = f_{osc}/256$), which determines the PWM frequency at the GATE output. An external LRC TEST terminal is provided for accelerating internal testing of the LRC function and logic. Under normal operation, the LRC TEST terminal is grounded by an internal 10 kΩ resistance to ground. Under accelerated test conditions, the LRC TEST voltage is 5.0 V, and a fourth bit ($f_{osc}/16$) from the 8-bit divider is used to determine the PWM GATE frequency. Thus, the rates are accelerated by a factor of 16.

### Low-Pass Filter, DAC, and Analog Duty Cycle Regulator Comparator

The output voltage $V_o$ of combiners CB1 and CB2 is coupled to an input of a 300 Hz low-pass filter (Rf, Cf) to remove high-frequency components of system noise at $V_{bat}$ and thus associated with voltages $V_{ls}$, or $V_{rs}$. The output of the low-pass filter is coupled to a unity-gain buffer FB that provides a filter buffer FB output.

The 4 MSBs of the 8-bit counter causes the DAC to generate a 4-bit 395 Hz voltage waveform having 16 descending 1.75 mV steps, ramping from $V_{ref}$ to [$V_{ref}$ - 28 mV], where $V_{ref}$ is the 2.0 V reference voltage.

An analog duty cycle comparator ($C_{dc}$) compares the DAC output voltage waveform to the voltage at the FB output ($V_{fb}$). When voltage $V_{fb}$ is less then voltage [$V_{ref}$ - 28 mV], comparator $C_{dc}$ outputs a logic [1], for a 100% duty cycle. When voltage $V_{fb}$ is greater than $V_{ref}$, comparator $C_{dc}$ outputs a logic [0] for a 0% duty cycle. When ($V_{ref}$ - 28 mV) < $V_{fb}$ < $V_{ref}$, comparator $C_{dc}$ outputs a duty cycle defined by the High/Low output voltage ratio for each period (about 2.54 ms) of the DAC output voltage waveform.

### Basic System Voltage Regulation

From a system voltage regulation viewpoint, the voltages $V_{rem}$ and $V_l$ from the Remote or Local connections, respectively, are scaled to the Remote Sense and Local Sense inputs as voltages $V_{rs}$ and $V_{ls}$ respectively and transferred to the FB output as voltage $V_{fb}$. Voltage $V_{fb}$ is compared to the DAC output voltage waveform to generate the ON and OFF time of the analog duty cycle waveform. When voltage $V_{fb}$ is less than $V_{ref}$ - 28 mV, the output of comparator $C_{dc}$ is in a high state. This high state propagates through an AND3 GATE, an OR1 GATE, and an AND4 GATE to activate switch S3, generating a fully ON or High GATE drive voltage. When voltage $V_{fb}$ is greater than $V_{ref}$, the output of comparator $C_{dc}$ is in a low state. This low state propagates through the AND3 GATE, the OR1 GATE, and the AND4 GATE to activate switch S3 to generate a fully OFF or low GATE drive voltage. Assuming voltage $V_{ref}$ is 2.0 V and $V_{fb} = V_{rs}$, and the local or remote input resistive scale factor is 7.45, the external MOSFET provides a fully ON field current when the system voltage is less than 7.45 ($V_{ref}$ - 28 mV), or 14.6 V. The field current is also fully OFF when the system voltage is greater than 7.45 ($V_{ref}$), or 14.9 V. When voltage $V_{fb}$ is less than any portion of the DAC waveform voltage, comparator $C_{dc}$ output is high to produce an ON field current. When voltage $V_{fb}$ is greater than any portion of the DAC waveform voltage, comparator $C_{dc}$ output is low to produce an OFF field current. Thus the system feedback will regulate the PWM duty cycle of the field current from 0% to 100% over about a 210 mV system regulation voltage range (dVreg). The system voltage is centered at 14.8 V, where a 50% duty cycle field current results for an average system load current, and the duty cycle regulation frequency is ($f_{osc}/256$), or 395 Hz. Since voltage $V_{ref}$ has a negative TC, voltage $V_{set}$ will also have a regulation voltage temperature coefficient ($TC_{Vreg}$) of about -11 mV/°C.

### Input Phase and Frequency Switch Response

The phase voltage $V_{ph}$ results from the alternator's stator AC output voltage being applied to the PHASE input terminal. A phase detection threshold voltage ($V_{Tph}$) is approximately 4.0 V due to the 1.25 V phase reference voltage for the phase comparator ($C_{ph}$) and the 3.22 voltage ratio associated with the phase input resistor divider. The phase input resistance ($R_{ph}$) is typically 60 kΩ. A PHASE FILTER terminal is coupled to the input of Comparator $C_{ph}$, providing for an external phase filter capacitance when filtering of high frequency phase noise is desired. A typical value of .003 μF to AGND provides for an input phase 3.0 db roll-off frequency of about 10 kHz. Comparator $C_{ph}$ also provides about 480 mV of hysteresis at the PHASE input terminal. Comparator $C_{ph}$ further provides a phase signal binary output voltage having a phase frequency of $f_{ph}$ and is applied to digital frequency switches F1 and F2. Switch F1 outputs a logic [1] when frequency $f_{ph}$ is less then phase detection frequency $f_1$. Frequency $f_1$ is equal to frequency $f_{msb}/8$, or 49.3 Hz for a 101 kHz oscillator frequency. Switch F2 outputs a logic [1] when the frequency $f_{ph}$ is greater then the low/high transition frequency $f_2$. Frequency $f_2$ is equal to frequency $3f_{msb}/4$, or 296 Hz for a 101 kHz oscillator frequency. These frequency switches are used to define the Load Response Control region of operation, an undervoltage at a high RPM fault condition, and a low RPM fault condition due to a broken or loose belt.

### Load Response Control (LRC)

The LRC circuit consists of a digital duty cycle generator, an analog/digital (A/D) duty cycle comparator and tracking circuit, an up/down control switch, an up/down (U/D) counter, a programmable divider (Np), and a multiplexer (MUX). During normal operation, the LRC circuit becomes active and generates digital duty cycle control of the GATE drive when frequency $f_{ph}$ is less than frequency $f_2$ ($f_1 < f_{ph} < f_2$). The slow LRC response becomes inactive and the analog duty cycle controls the GATE drive when frequency $f_{ph}$ is greater than frequency $f_2$ ($f_1 < f_{ph} < f_2$). During initial ignition and initial

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engine start, the LRC response is in effect, independent of frequency $f_{ph}$, until system voltage is regulating at voltage $V_{set}$.

The digital duty cycle generator receives the 4 MSBs from the 8-bit counter as input and generates 11 discrete digital duty cycles on 11 output lines. The frequency of each duty cycle waveform is about 395 Hz ($f_{msb}$), which results from the MSB of the 8-bit division of the 101 kHz OSC clock frequency. The minimum duty cycle on the first output line is 31.25% and the maximum duty cycle on the eleventh output line is 93.75%. The duty cycle difference between each incremental duty cycle is 6.25%. All 11 duty cycle generator output lines are coupled as data inputs to the MUX.

Normally the programmable divider Np divides frequency $f_{msb}$ by a counter divide ratio N and applies the $f_{msb}/N$ frequency as input to the U/D counter. Divide ratio N can be pre-selected by the user for four different divide ratios by switching a combination of the LRC1 and LRC2 normally open terminals to ground. An LRC input current ($I_{lrc}$) from each LRC terminal to ground is about 45 μA. The phase frequency $f_{ph}$ and an up/down (u/d) state on a u/d line from the up/down control switch determines ratio N. In the LRC mode when $f_{ph} < f_2$, a high, or up, state on the u/d line causes divider Np to output a frequency of $f_{msb}/N$, or 395 Hz/N. The LRC1 and LRC2 terminal combinations produce N divide ratios of 66, 132, 198, and 264. When the u/d line is in the down, or low, state, divider Np provides a divide ratio of $f_{msb}/4$, or 395 Hz/4. When $f_{ph} > f_2$, the output frequency of divider Np is always $f_{msb}/4$ = 395 Hz/4, independent of the state of the u/d input line.

The u/d line from the up/down control switch determines the direction of the count as well as the divide ratio N. For an up state on the u/d line, the output of the 4-bit U/D counter increments up at a rate of 5.98 Hz (count change every 167 ms) for N=66, 2.99 Hz (count change every 334 ms) for N=132, 1.99 Hz (count change every 502 ms) for N=198, or 1.496 Hz (count change every 671 ms) for N=264. For a down state on the u/d line, the output of the 4-bit U/D counter decrements at a rate of about 99 Hz (count decrement about every 10 ms). The 4-bit output lines of the up/down counter are coupled as control inputs of the MUX.

The MUX couples one of the 11 digital duty cycle input lines to the MUX output dependent upon the 4-bit control inputs from the U/D counter. When the MUX control input count is 0, the first 31.25% digital duty cycle is selected and provided at the MUX output. When the control input count is 10, the eleventh 93.75% digital duty cycle is selected at output of the MUX. A MUX control input of 11 produces a 100% duty cycle at the MUX output. Thus each of the MUX input lines is selected and provided at the MUX output and incremented to the next line at a rate dependent on the rate the MUX control inputs increment. For an up state on the u/d line, the digital duty cycle at the output of the MUX will increment from 31.24% to 100% in 11 steps at a rate from 167 ms/step (or a fourth LRC rate ($R_{lrc4}$) of 37.42%/sec) to 671 ms/step (or a first LRC rate ($R_{lrc1}$) of 9.31%/sec) dependent on the LRC1 and LRC2 terminal terminations. For a down state on the u/d line, the digital duty cycle will count down at a rate of about 10 ms/step change.

The A/D duty cycle comparator and tracking circuit receives the analog duty cycle from comparator $C_{dc}$ and the digital duty cycle from the MUX output. The A/D duty cycle comparator provides a high, or up (u), output when the analog duty cycle is greater than the digital duty cycle, and a low, or down (d), output when the analog duty cycle is less than the digital duty cycle.

In the LRC mode when frequency $f_1 < f_{ph} < f_2$, the up/down control switch enables the u/d output of the A/D duty cycle comparator to be coupled to the u/d line. In the steady state, the A/D duty cycle comparator will provide an u/d input to the U/D counter and Np divider to increase or decrease the digital duty cycle to track the analog duty cycle. If the analog duty cycle increases to a value greater than the digital duty cycle at a rate that is greater than the selected LRC digital duty cycle rate, the A/D duty cycle comparator will output an up signal on the u/d line to cause the digital duty cycle to increase to the analog duty cycle at the selected LRC digital duty cycle rate. If the analog duty cycle decreases to a value less than the digital duty cycle, the A/D duty cycle comparator will output a down signal on the u/d line to cause the digital duty cycle to decrease to the analog duty cycle at a fixed rate of about 10 ms/step. For an analog duty cycle less than 31.25%, the down count at the output of the U/D counter will remain at 0 and the digital duty cycle will remain at 31.25%.

If frequency $f_{ph}$ is less than frequency $f_1$ ($f_{ph} < f_1$), then the up/down control switch will provide a down signal on the u/d line independent of the duty cycle comparator u/d output. The resulting down count of 0 to the MUX control input for $f_{ph} < f_1$ will cause the digital duty cycle to be constant at 31.25% and provides a divide ratio of $f_{msb}/4$ as the input frequency to the U/D counter.

When approximately 5.0 V is applied to the LRC TEST terminal, divider Np utilizes the $f_{osc}/16$ frequency as input to the divider instead of the normal $f_{osc}/256$ frequency. As a result, the LRC function is accelerated by a factor of 16, which allows the testing of all LRC associated rates to be accelerated by a factor of 16. During normal LRC operation, the LRC terminal is in a low ground state, having an internal 10 kΩ pull-down resistor.

The duty cycle output of the AND3 GATE reflects the minimum duty cycle at the AND3 GATE inputs. Thus when the analog duty cycle exceeds the digital duty cycle, the digital duty cycle becomes the controlling duty cycle at the AND3 GATE output. When the analog duty cycle is less than the digital duty cycle, the analog duty cycle becomes the controlling duty cycle at the AND3 GATE output. Thus in the LRC mode when $f_1 < f_{ph} < f_2$, an increasing step response in the analog duty cycle from 0% to 100% will cause the duty cycle at the output of the AND3 GATE to increase rapidly from 0% to 31.25% and then increase slowly at the LRC rate from 31.25% to 100%. If the analog duty cycle provides a step increase from a duty cycle greater than 31.25%, then the resulting LRC duty cycle increase from the initial analog duty cycle at the output of the

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AND3 GATE. For a decreasing step response in the analog duty cycle, the output of the AND3 GATE will rapidly follow the decreasing analog duty cycle. The output of the AND3 GATE drives the GATE output (and the field current) through an OR1 GATE, an AND4 GATE, and switch S3. Thus the minimum GATE LRC duty cycle ($DC_{(LRC)min}$) is 31.25%.

A 0% analog duty cycle will produce a 0% duty cycle at the output of the AND3 GATE. However, the output of the AND3 GATE is ORed with a 3.1% minimum duty cycle signal from the minimum duty cycle generation at the OR1 GATE input to provide a minimum 3.1% duty cycle to the AND4 GATE input. This provides the resulting minimum GATE duty cycle ($DC_{min}$) of 3.1% at the GATE output, even though the analog duty cycle is 0%.

When the phase frequency is greater than frequency $f_2$ ($f_{ph} > f_2$), the N divide factor is reduced to 4. As a result, the LRC circuitry still functions as previously described, but the rate of digital duty cycle increase or decrease is a maximum LRC rate ($R_{lrc(max)}$) of about 10 ms/step. Thus a step increase in the analog duty cycle from 31.25% to 100% will cause about a 110 ms delay before the digital duty cycle provides a 100% duty cycle at the output of the AND3 GATE (and GATE drive).

The conditions for LRC response also occur during an initial engine start up period after engine cranking even when a WOT condition occurs ($f_{ph} > f_2$). When the ignition switch is turned ON, comparator $C_{ign}$ is activated, activating all biasing into the normal state and activating the start-up LRC mode. After engine cranking and immediately after initial engine start up, the system BATTERY voltage is generally low while a WOT condition occurs. For this case, the slow LRC response is in effect to prevent excessive torque loading on the engine by the alternator during engine start up. The GATE duty cycle at start-up with WOT ($DC_{start}$) is the minimum LRC duty cycle and will increase at the LRC rate. Once the system voltage returns to voltage $V_{set}$, the normal LRC response will occur as previously described.

### Field Coil Drive and Device Protection

The external MOSFET provides PWM drive current from the system BATTERY to the field coil for system voltage regulation. The GATE-to-Source voltage for this MOSFET is provided by the IC's GATE-to-SOURCE terminal drive voltage. During the ON state, the AND4 GATE activates switch S3 to couple the GATE drive pull-up source current ($I_{pu}$) to the GATE output. Current $I_{pu}$ drives the GATE of the MOSFET to the charge pump GATE voltage $V_g$ (typically 23 V), causing the MOSFET to drive the field coil terminal to near the system BATTERY voltage. Voltage $V_g$ has a minimum charge pump GATE voltage ($V_{g(min)}$) of 21.5 V. This high GATE-to-Source voltage minimizes power dissipation in the external MOSFET by minimizing a Drain-to-Source ON resistance ($R_{DS(ON)}$) of the MOSFET during the ON state. This results in a typical Lamp Drain ON voltage ($V_{d(sat)}$) of about 0.3 V at a Lamp Drain current of 400 mA as measured from the LAMP DRAIN terminal to ground. During the OFF state, the AND4 GATE activates switch S3 to couple a GATE drive pull-down sink current ($I_{pd}$) to the GATE output. Current $I_{pd}$ pulls the GATE voltage to the Source voltage, turning OFF the MOSFET and its associated field coil current. The limited GATE current drive of the MOSFET GATE capacitance reduces the magnitude and frequency of the high-frequency components associated with the GATE duty cycle waveform, minimizing RFI. Zener diode Z1 is employed to provide a GATE-to-Source clamping voltage ($V_{gs}$), which limits and protects the GATE-to-Source voltage of the external MOSFET.

When the external MOSFET fails to increase the source (or field coil terminal) voltage to within a source short circuit threshold voltage ($V_{Tssc}$) of the BATTERY terminal voltage ($V_{Tssc} < [V_{bat} - V_{source}]$), a shorted-source comparator $C_{ss}$ outputs a short circuit signal to a GATE polling circuit. A shorted field coil to ground is an example of this fault condition. This GATE polling circuit provides short GATE polling pulses to the AND4 GATE to allow the IC to test for an unshorted condition without damaging the external MOSFET. The polling duty cycle is 1.56%, or about a 158 μs ON pulse at a frequency of $f_{msb}/4$, or 98.6 Hz. When the source shorting condition is removed, comparator $C_{ss}$ provides a no-short signal to the GATE polling circuitry, which provides a logic [1] to the AND4 GATE, which then operates normally.

The AND4 GATE is also driven by the no load dump ($\overline{LD}$) line from the Overvoltage Detector circuitry. Thus during a load dump system overvoltage condition, a logic [0] is provided to the AND4 GATE from the Overvoltage Detector circuit and all GATE drive is terminated.

A flyback diode MR850 is externally provided to limit the negative source voltage on the field terminal (and the SOURCE terminal) caused by a turn-OFF transition of the field current. The forward current through this diode is approximately the peak field current prior to field current turn OFF.

### Fault Lamp Indicator—Drive and Protection

The fault indicator lamp is driven by an internal N-channel MOSFET lamp driver, which controls the lamp current. The lamp is coupled between the ignition switch and the LAMP DRAIN terminal of the lamp driver. The Lamp GATE of the lamp driver is driven by the lamp driver circuitry or from an external LAMP GATE terminal. Inputs to the lamp driver circuitry are from an output of an AND2 GATE, an output of a thermal limit circuit, and an output of a current limit circuit. By applying an external Lamp GATE override voltage ($V_{go}$) to the LAMP GATE terminal (5), the Lamp Drain current will increase, providing lamp current independent of the lamp driver logic state. When the lamp driver circuity is forcing the lamp driver OFF, the LAMP GATE terminal resistance to ground will be about 4.6 kΩ. The source of the lamp driver is coupled to ground through an internal current sense resistor $R_S$. When the lamp is ON, the Lamp Drain ON voltage ($V_{d(sat)}$) is the Lamp Drain-to-ground voltage measured at 400 mA of Lamp Drain current.

Normally, current flows through the lamp driver (and lamp), indicating a fault when the output of the AND2 GATE is a logic [1]. Assuming the lamp is not shorted, is not being current

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limited, is not in the thermal shut down mode, and the system is not in a load dump mode, the lamp ON current is controlled by the output of the OR2 GATE. The output of the OR2 GATE is a logic [1] and the lamp will normally be ON when the UV (undervoltage) line and the F2 output line are both a logic [1] state, indicating an undervoltage condition when frequency $f_{ph} > f_2$. The output of the OR2 GATE is also a logic [1] when the output of the OV (overvoltage) line is a logic [1], indicating an overvoltage condition, or the output of the F1 line is also a logic [1], indicating a loss of phase signal ($f_{ph} < f_1$) due to a broken phase wire, broken or slipping belt, or otherwise failed alternator or open field circuit.

When the lamp current exceeds a lamp drain short circuit current ($I_{dsc}$), the voltage across resistor Rs will exceed a current limit threshold voltage associated with the current limit circuitry. As a result, a signal is sent to the lamp driver circuitry to limit the lamp drive and regulates the lamp current to current $I_{dsc}$. When the power dissipation of the lamp driver causes the temperature of the lamp driver to exceed a thermal shut-down temperature limit ($T_{Lim}$), a temperature sensing diode ($D_{tl}$) causes the thermal limit circuitry to send a signal to the lamp driver circuitry to limit the lamp drive current and reduce the power dissipation and resulting device temperature. When the lamp driver is ON, but the Lamp Drain terminal voltage is not below the BAT terminal voltage $V_{bat}$ by at least a lamp drain short circuit threshold voltage ($V_{Tdsc}$) or ($[V_{bat} - V_{drain}] < V_{Tdsc}$), comparator $C_{ds}$ will output a lamp short circuit signal to the Drain Polling circuit to indicate a lamp shorted condition. The Drain Polling circuit provides a low duty cycle polling output to the input of the AND2 GATE to poll the lamp driver ON, continuously testing for a lamp short without damaging the lamp driver. The polling duty cycle is 1.56%, (or about a 158 μs ON pulse) at a frequency of $f_{msb}/4$, or 98.6 Hz. After the lamp short has been removed, the comparator $C_{ds}$ outputs a lamp not-shorted signal to the Drain Polling circuitry, which provides a logic [1] to the AND2 GATE, which then operates normally.

Lamp polling is also present when the lamp is ON. In this case, lamp polling turns OFF the lamp for a short period of time with the lamp being ON for the remainder of the time. In this case the lamp ON duty cycle is 98.44% (or OFF for 158 μs) at a frequency of $f_{msb}/4$, or 98.6 Hz. This causes the lamp voltage on the lamp drain terminal to be greater than ignition threshold voltage $V_{Tign}$ for at least 158 μs of a 10.1 ms period. During the lamp ON mode, the Ignition Turn Off Delay of the Ignition Delay circuit is greater then the 10.1 ms period. As a result, the regulator biasing remains ON even when the IGN terminal is coupled to the LAMP DRAIN terminal and the lamp drain voltage is less than voltage $V_{Tign}$ most of the time when the lamp is ON.

The lamp driver is also protected from load dump, since during load dump, the $\overline{LD}$ signal is a logic [0], preventing the AND2 GATE from activating the lamp driver. In addition, a drain-to-GATE clamp device Z2 limits the drain-to-GATE clamping voltage ($V_{dg}$) to about 40 V typically.

### Undervoltage, Overvoltage, and Load Dump Protection

An undervoltage, overvoltage and load dump condition is sensed by the regulator to generate fault indications and to protect the regulator and associated external devices. As previously discussed, a load dump signal during load dump will prevent GATE drive to the external MOSFET and prevent GATE drive to the lamp driver. Thus the external and internal MOSFETs will turn OFF during a system load dump. As previously discussed, the undervoltage and overvoltage signals are also provided for fault indications.

The undervoltage signal is provided on the UV line by an undervoltage comparator $C_{uv}$ having a voltage reference of 1.25 V and a resistor divider voltage transfer of 1.26 from the FB output to comparator $C_{uv}$ input. When voltage $V_{fb}$ on the FB output becomes less than 1.52 V, the voltage at input to comparator $C_{uv}$ becomes less than 1.25 V, causing comparator $C_{uv}$ to output an undervoltage UV signal. Because voltage $V_{fb}$ is ideally voltage $V_{rs}$ (or voltage $V_{ls}$), and the ratio of $V_r/V_{rs}$ (or $V_l/V_{ls}$) is 7.45, the UV signal will occur when the system voltage at the Remote input (or Local input) is less than an undervoltage threshold voltage ($V_{Tuv}$), or 11.35 V. However, GATE AND1 ensures that frequency $f_{ph}$ must be greater than $f_2$ before an undervoltage Fault is indicated by the lamp.

The load dump and overvoltage detection also utilizes similar resistor dividers and voltage comparators in an Overvoltage Detect circuitry where all comparators are referenced to voltage $V_{ref}$, or about 2.0 V. When voltage $V_{fb}$ on the FB output is greater than 2.58 V, or 1.29 $V_{ref}$ ($V_{fb}/V_{ref}$ = 1.29), an output load dump signal of a logic [0] is generated on the $\overline{LD}$ line. Thus during load dump, voltage $V_{rs}$ (or $V_{local}$) will be about 2.58 V, and the actual load dump threshold voltage ($V_{Tld}$) will be about 19.25 V, or 1.3 $V_{set}$. When voltage $V_{fb}$ on the FB output is greater than 1.117 $V_{ref}$ ($V_{fb}/V_{ref}$ = 1.117), an output overvoltage signal is generated on the OV line. Thus voltage $V_{rs}$ (or $V_l$) will be about 2.235 V, and the actual overvoltage threshold voltage ($V_{Tov}$) will be about 16.65 V, or 1.125 $V_{set}$.

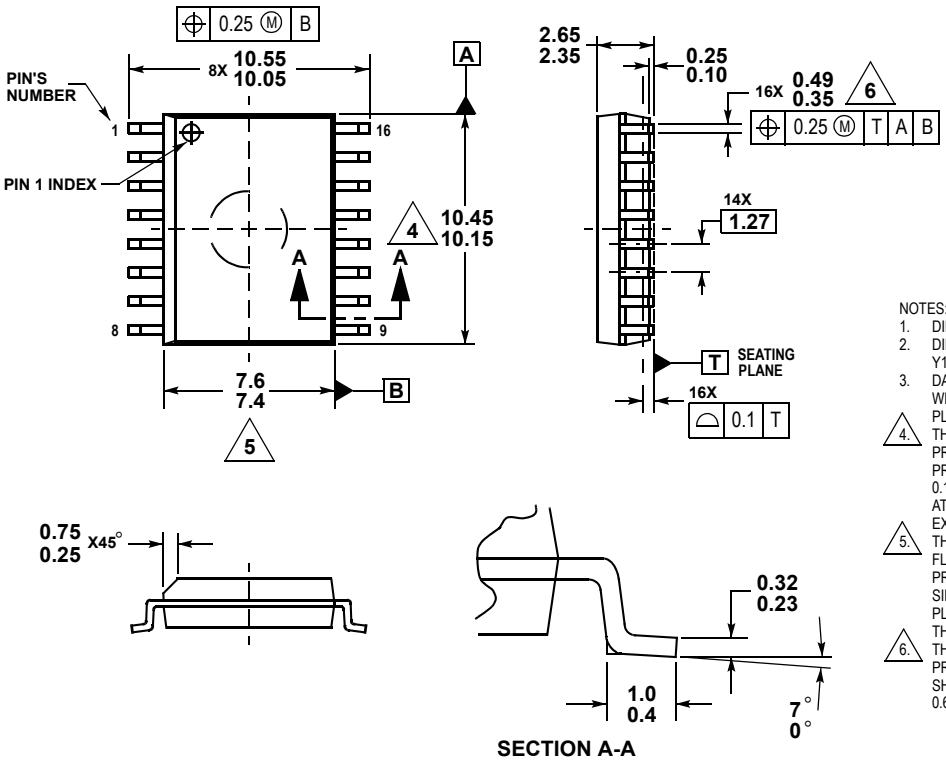
The regulator also indicates an overvoltage condition on the system during the Remote fault condition when the remote wire resistance increases to a finite value and the system voltage is being regulated by secondary regulation at $V_{set2}$. When a load dump occurs during secondary regulation, the load dump threshold increases to 1.3 $V_{set2}$, or about 24 V.

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## PACKAGE DIMENSIONS

**DW SUFFIX**
16-TERMINAL SOICW
PLASTIC PACKAGE
CASE 751G-04
ISSUE D




SECTION A-A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

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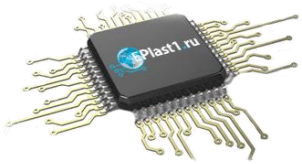
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