

LM611 Operational Amplifier and Adjustable Reference

Check for Samples: [LM611](#)

FEATURES

OP AMP

- **Low Operating Current:** 300 μ A (op amp)
- **Wide Supply Voltage Range:** 4V to 36V
- **Wide Common-Mode Range:** V^- to ($V^+ - 1.8$ V)
- **Wide Differential Input Voltage:** ± 36 V
- **Available in Low Cost 8-pin DIP**
- **Available in Plastic Package Rated for Military Temperature Range Operation**

REFERENCE

- **Adjustable Output Voltage:** 1.2V to 6.3V
- **Tight Initial Tolerance Available:** $\pm 0.6\%$
- **Wide Operating Current Range:** 17 μ A to 20 mA
- **Reference Floats Above Ground**
- **Tolerant of Load Capacitance**

APPLICATIONS

- **Transducer Bridge Driver**
- **Process and Mass Flow Control Systems**
- **Power Supply Voltage Monitor**
- **Buffered Voltage References for A/D's**

Connection Diagrams

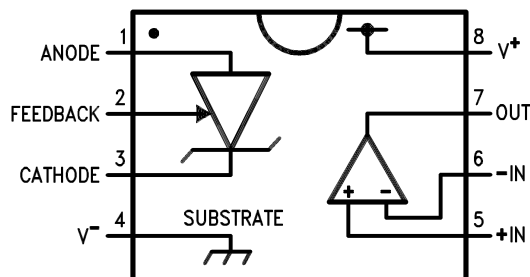


Figure 1. Hermetic Dual-In-Line Package

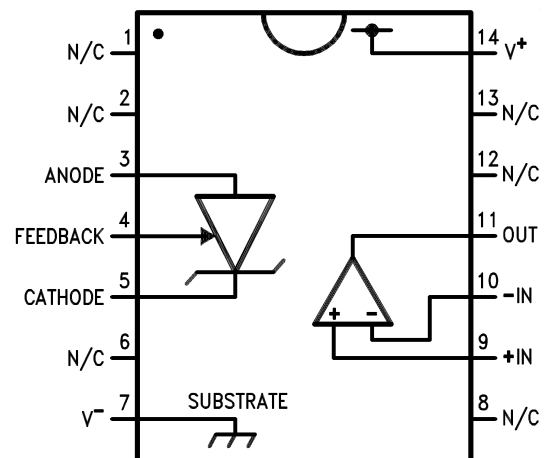


Figure 2. Plastic Surface Mount Narrow Package



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Voltage on Any Pins Except V_R (referred to V^- pin)	36V (Max)
See ⁽³⁾	-0.3V (Min)
Current through Any Input Pin and V_R Pin	± 20 mA
Differential Input Voltage	
Military and Industrial	± 36 V
Commercial	± 32 V
Storage Temperature Range	$-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	
N Package	100°C/W
D Package	150°C/W
Soldering Information Soldering (10 seconds)	
N Package	260°C
D Package	220°C
ESD Tolerance ⁽⁵⁾	± 1 kV

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
- (4) Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package and 135°C/W for the D package.
- (5) Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Operating Temperature Range

LM611AI, LM611I, LM611BI	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LM611AM, LM611M	$-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
LM611C	$0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$

Electrical Characteristics⁽¹⁾

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical ⁽²⁾	LM611AM LM611AI Limits ⁽³⁾	LM611M LM611BI LM611I LM611C Limits ⁽³⁾	Units
I _S	Total Supply Current	R _{LOAD} = ∞, 4V ≤ V ⁺ ≤ 36V (32V for LM611C)	210 221	300 320	350 370	μA max μA max
V _S	Supply Voltage Range		2.2 2.9	2.8 3	2.8 3	V min V min
			46 43	36 36	32 32	V max V max
OPERATIONAL AMPLIFIER						
V _{OS1}	V _{OS} Over Supply	4V ≤ V ⁺ ≤ 36V (4V ≤ V ⁺ ≤ 32V for LM611C)	1.5 2.0	3.5 6.0	5.0 7.0	mV max mV max
V _{OS2}	V _{OS} Over V _{CM}	V _{CM} = 0V through V _{CM} = (V ⁺ − 1.8V), V ⁺ = 30V, V [−] = 0V	1.0 1.5	3.5 6.0	5.0 7.0	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V _{OS} Drift	See ⁽³⁾	15			μV/°C max
I _B	Input Bias Current		10 11	25 30	35 40	nA max nA max
I _{OS}	Input Offset Current		0.2 0.3	4 5	4 5	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		4			pA/°C
R _{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C _{IN}	Input Capacitance	Common-Mode	5.7			pF
e _n	Voltage Noise	f = 100 Hz, Input Referred	74			nV/ √Hz
I _n	Current Noise	f = 100 Hz, Input Referred	58			fA/√Hz
CMRR	Common-Mode Rejection-Ratio	V ⁺ = 30V, 0V ≤ V _{CM} ≤ (V ⁺ − 1.8V) CMRR = 20 log (ΔV _{CM} /ΔV _{OS})	95 90	80 75	75 70	dB min dB min
PSRR	Power Supply Rejection-Ratio	4V ≤ V ⁺ ≤ 30V, V _{CM} = V ⁺ /2, PSRR = 20 log (ΔV ⁺ /ΔV _{OS})	110 100	80 75	75 70	dB min dB min
A _V	Open Loop Voltage Gain	R _L = 10 kΩ to GND, V ⁺ = 30V, 5V ≤ V _{OUT} ≤ 25V	500 50	100 40	94 40	V/mV min
SR	Slew Rate	V ⁺ = 30V ⁽⁴⁾	0.70 0.65	0.55 0.45	0.50 0.45	V/μs
GBW	Gain Bandwidth	C _L = 50 pF	0.80 0.50			MHz
V _{O1}	Output Voltage Swing High	R _L = 10 kΩ to GND V ⁺ = 36V (32V for LM611C)	V ⁺ − 1.4 V ⁺ − 1.6	V ⁺ − 1.7 V ⁺ − 1.9	V ⁺ − 1.8 V ⁺ − 1.9	V min V min
V _{O2}	Output Voltage Swing Low	R _L = 10 kΩ to V ⁺ V ⁺ = 36V (32V for LM611C)	V [−] + 0.8 V [−] + 0.9	V [−] + 0.9 V [−] + 1.0	V [−] + 0.95 V [−] + 1.0	V max V max
I _{OUT}	Output Source Current	V _{OUT} = 2.5V, V _{+IN} = 0V, V _{−IN} = −0.3V	25 15	20 13	16 13	mA min mA min

- (1) Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.
- (2) Typical values in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.
- (3) All limits are specified at room temperature (standard type face) or at operating temperature extremes (**bold face type**).
- (4) Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Electrical Characteristics⁽¹⁾ (continued)

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical ⁽²⁾	LM611AM LM611AI Limits ⁽³⁾	LM611M LM611BI LM611I LM611C Limits ⁽³⁾	Units
I _{SINK}	Output Sink Current	V _{OUT} = 1.6V, V _{+IN} = 0V, V _{-IN} = 0.3V	17 9	14 8	13 8	mA min mA min
I _{SHORT}	Short Circuit Current	V _{OUT} = 0V, V _{+IN} = 3V, V _{-IN} = 2V, Source	30 40	50 60	50 60	mA max mA max
		V _{OUT} = 5V, V _{+IN} = 2V, V _{-IN} = 3V, Sink	30 32	60 80	70 90	mA max mA max
VOLTAGE REFERENCE						
V _R	Reference Voltage	See ⁽⁵⁾	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T_J}$	Average Temperature Drift	See ⁽⁶⁾	10	80	150	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	Hyst = (V _{ro'} – V _{ro})/ΔT _J ⁽⁷⁾	3.2			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V _R Change with Current	V _R (100 μA) – V _R (17 μA)	0.05 0.1	1 1.1	1 1.1	mV max mV max
		V _R (10 mA) – V _R (100 μA) ⁽⁸⁾	1.5 2.0	5 5.5	5 5.5	mV max mV max
R	Resistance	ΔV _R (10→0.1 mA)/9.9 mA ΔV _R (100→17 μA)/83 μA	0.2 0.6	0.56 13	0.56 13	Ω max Ω max
$\frac{\Delta V_R}{V_{RO}}$	V _R Change with High V _{RO}	V _R (V _{ro} = V _r) – V _R (V _{ro} = 6.3V) (5.06V between Anode and FEEDBACK)	2.5 2.8	7 10	7 10	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V _R Change with V ⁺ Change	V _R (V ⁺ = 5V) – V _R (V ⁺ = 36V) (V ⁺ = 32V for LM611C)	0.1 0.1	1.2 1.3	1.2 1.3	mV max mV max
		V _R (V ⁺ = 5V) – V _R (V ⁺ = 3V)	0.01 0.01	1 1.5	1 1.5	mV max mV max
$\frac{\Delta V_R}{\Delta V_{ANODE}}$	V _R Change with V _{ANODE} Change	V ⁺ = V ⁺ max, ΔV _R = V _R (@ V _{ANODE} = V ⁻ = GND) – V _R (@ V _{ANODE} = V ⁺ – 1.0V)	0.7 3.3	1.5 3.0	1.6 3.0	mV max mV max
I _{FB}	FEEDBACK Bias Current	I _{FB} ; V _{ANODE} ≤ V _{FB} ≤ 5.06V	22 29	35 40	50 55	nA max nA max
e _n	V _R Noise	10 Hz to 10,000 Hz, V _{RO} = V _R	30			μV _{RMS}

(5) V_{R} is the cathode-feedback voltage, nominally 1.244V.

(6) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \cdot \Delta V_{\text{R}} / (V_{\text{R}[25^\circ\text{C}]} \cdot \Delta T_{\text{J}})$, where ΔV_{R} is the lowest value subtracted from the highest, $V_{\text{R}[25^\circ\text{C}]}$ is the value at 25°C , and ΔT_{J} is the temperature range. This parameter is ensured by design and sample testing.

(7) Hysteresis is the change in V_{R} caused by a change in T_{J} , after the reference has been “dehysteresized”. To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

(8) Low contact resistance is required for accurate measurement.

Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

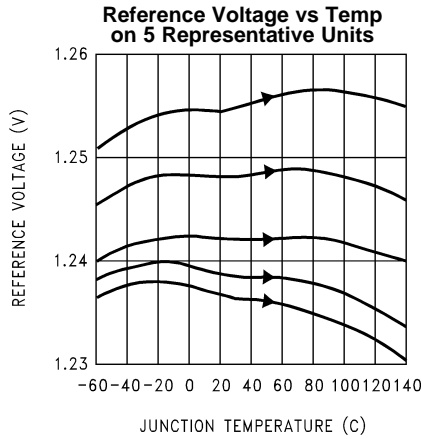


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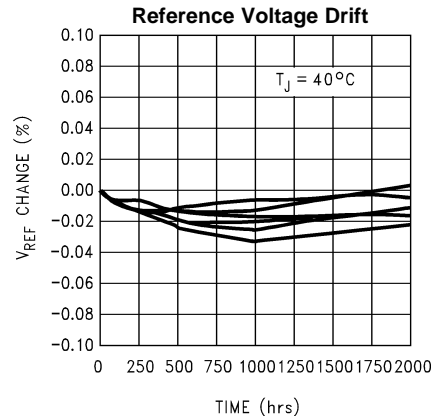


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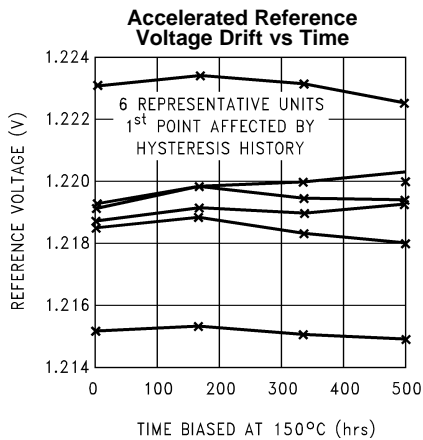


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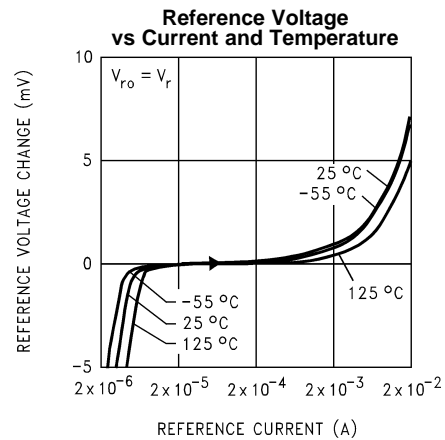


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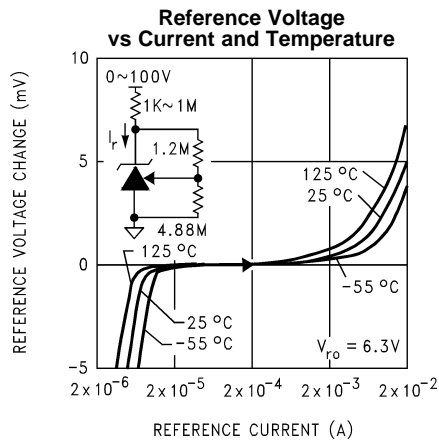


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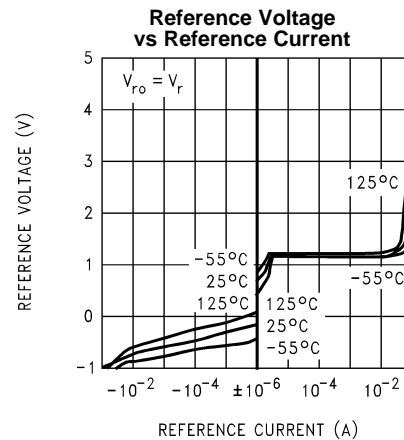


Figure 8.

Typical Performance Characteristics (Reference) (continued)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

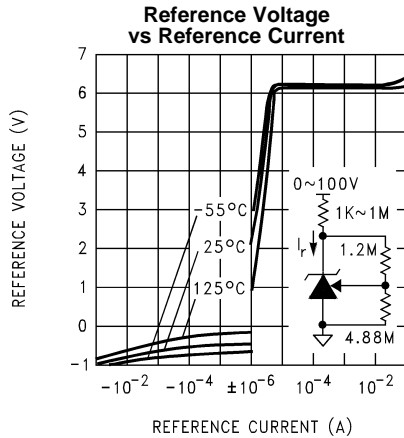


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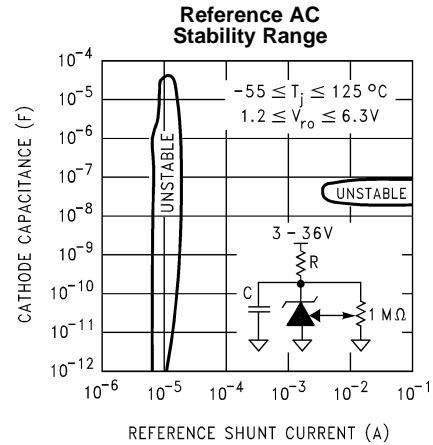


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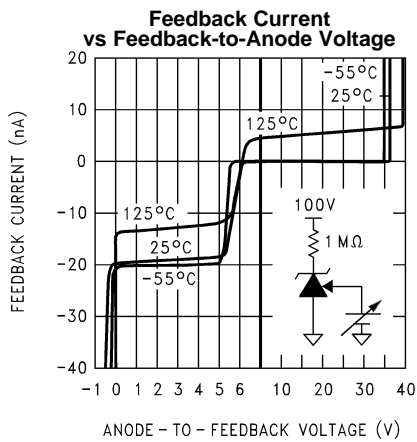


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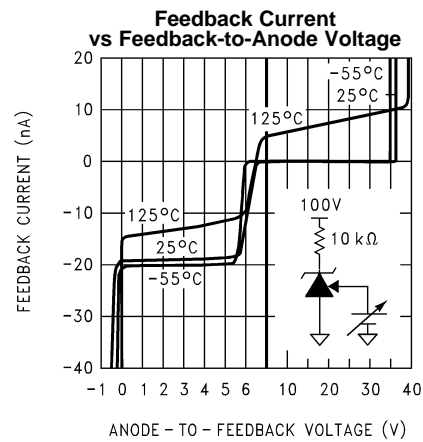


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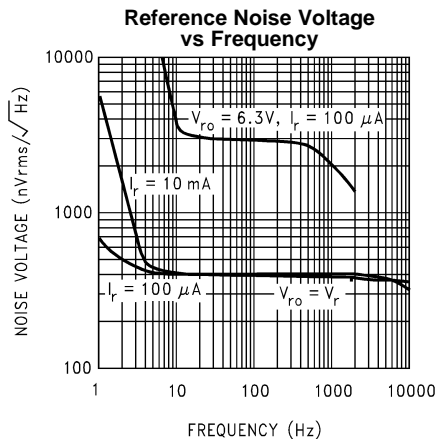


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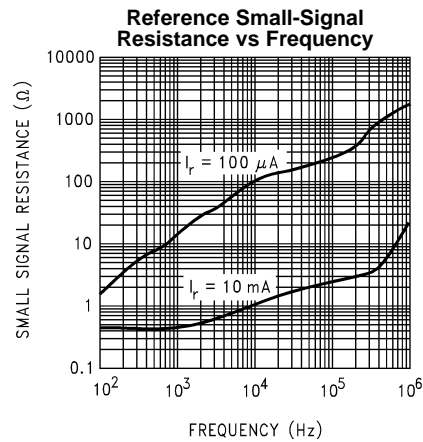


Figure 14.

Typical Performance Characteristics (Reference) (continued)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

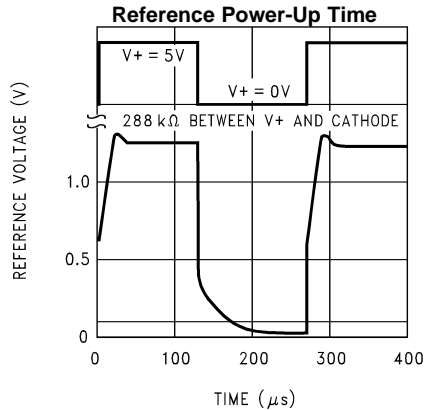


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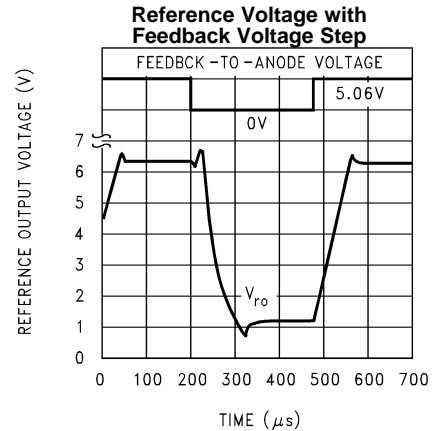


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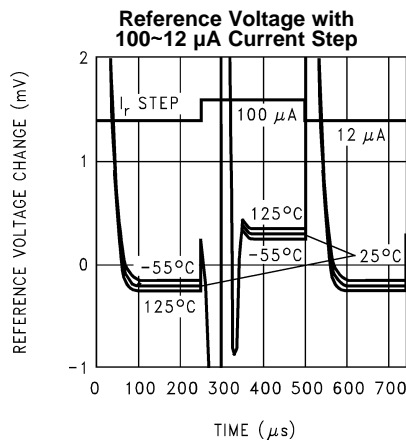


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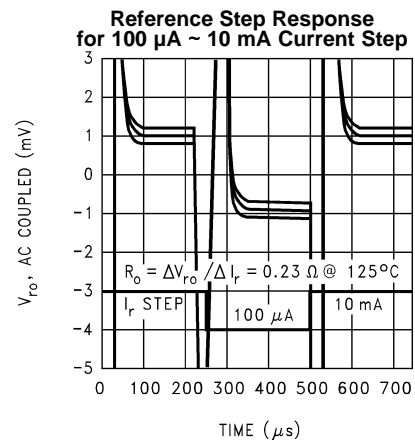


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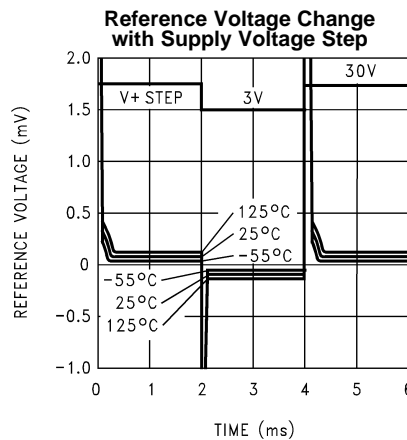
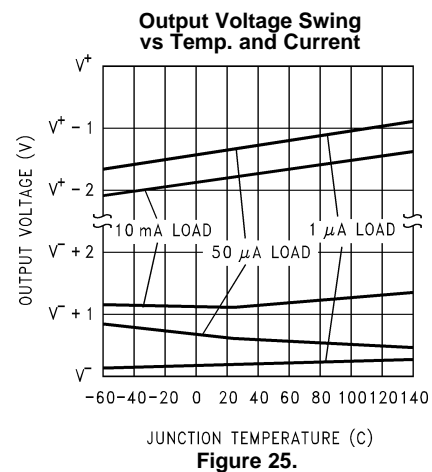
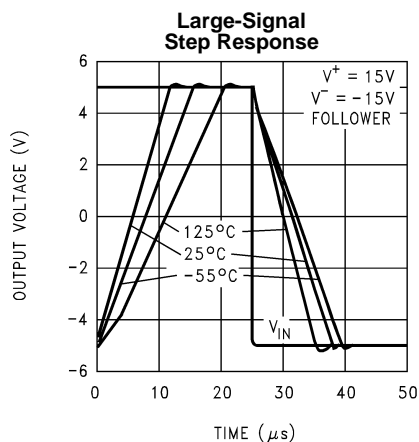
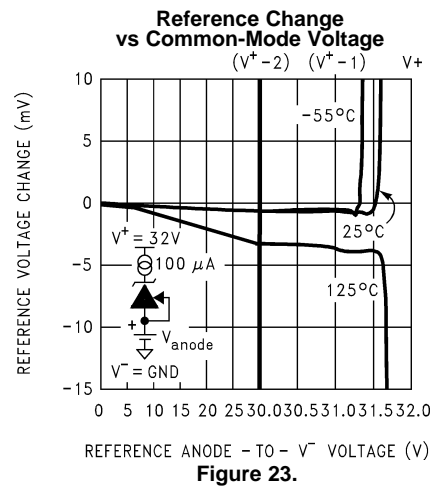
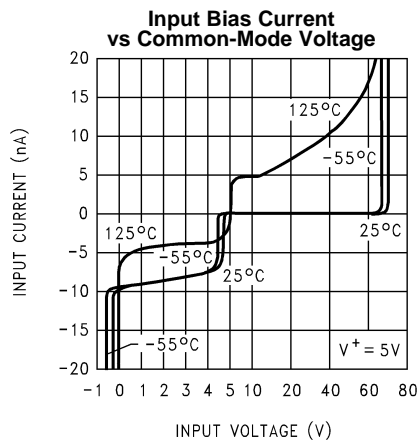
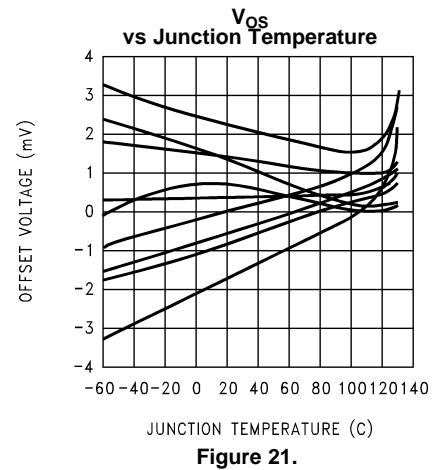
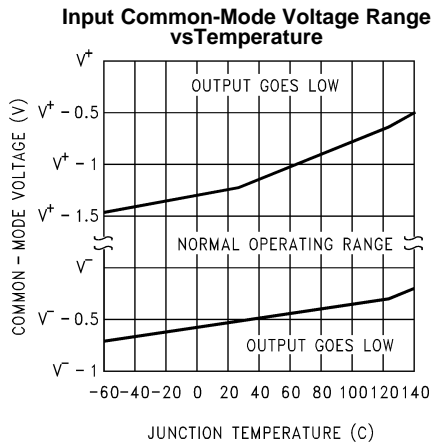


Figure 19.

Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted



Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

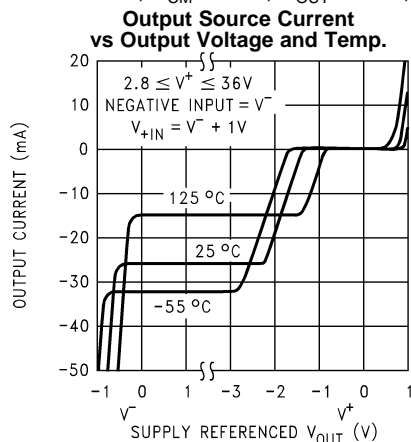


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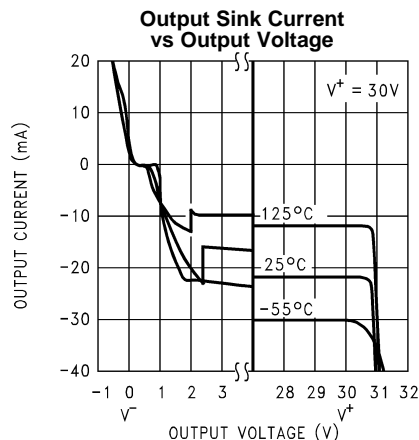


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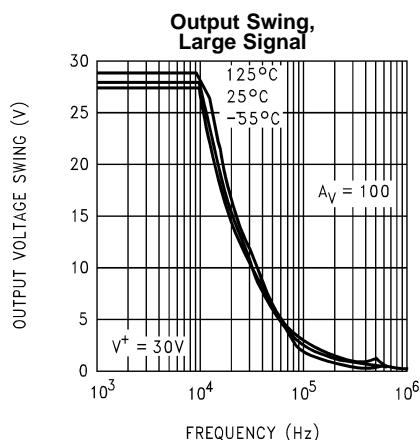


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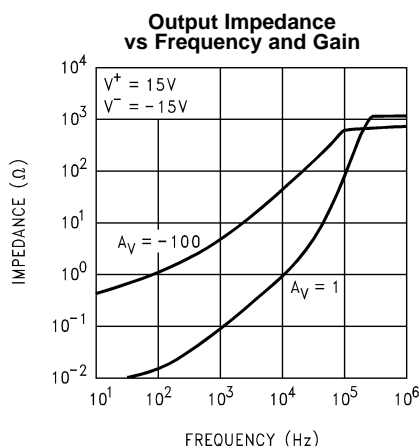


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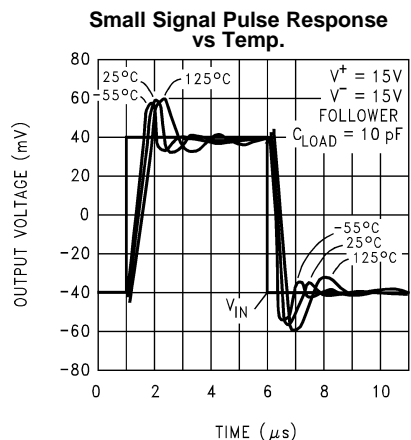


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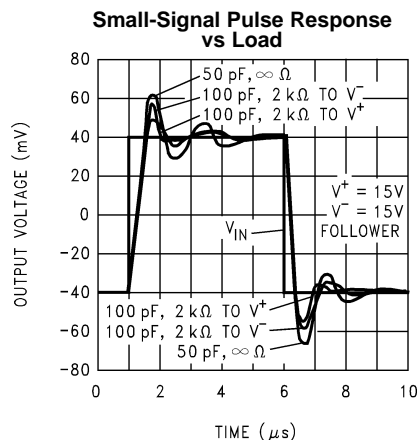


Figure 31.

Typical Performance Characteristics (Op Amps) (continued)

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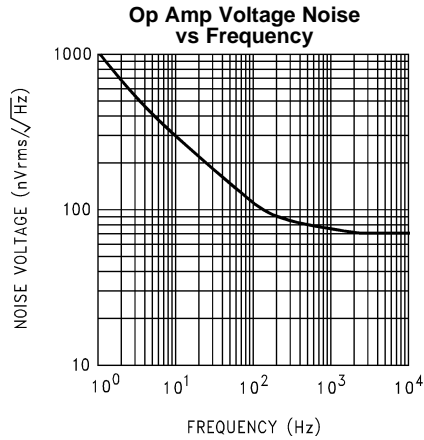


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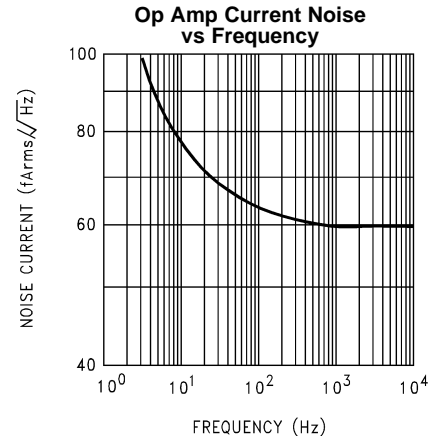


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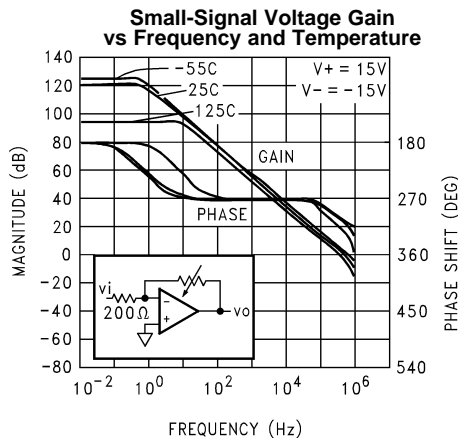


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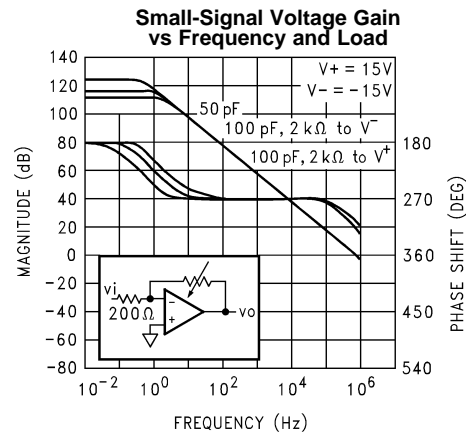


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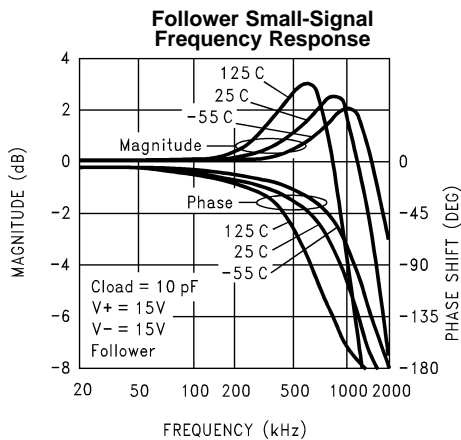


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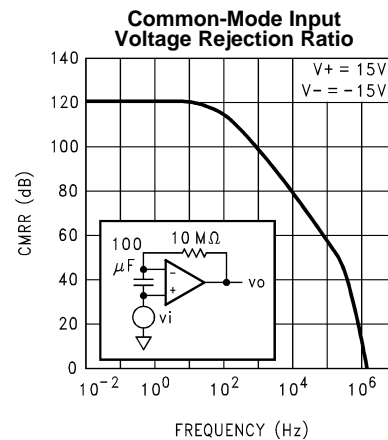
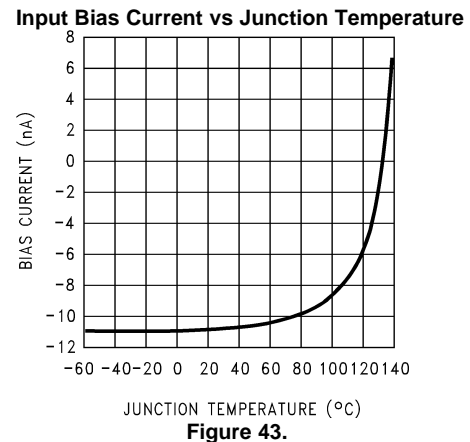
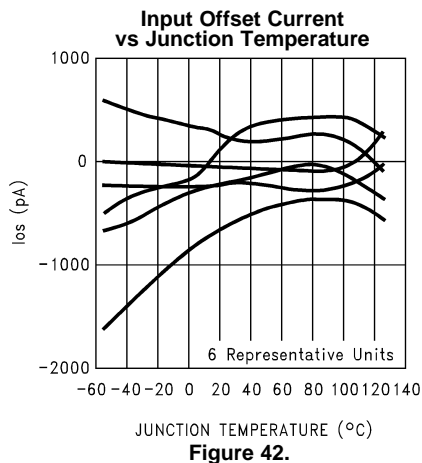
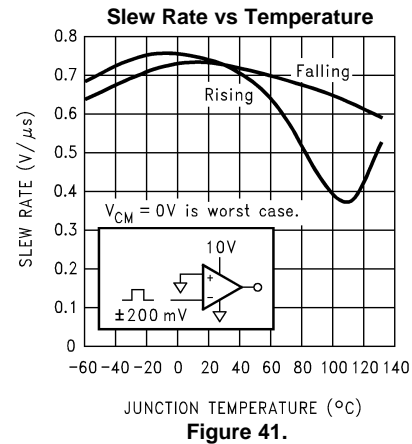
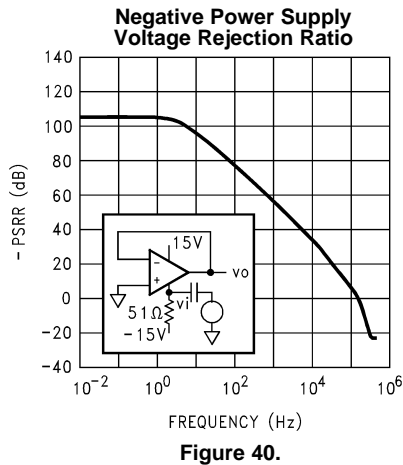
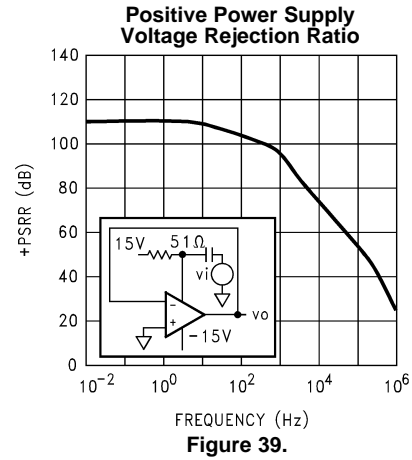
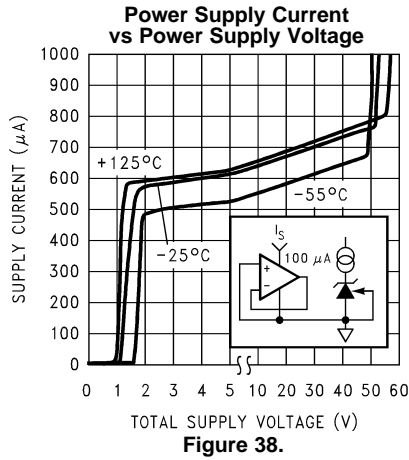


Figure 37.

Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted



Typical Performance Distributions

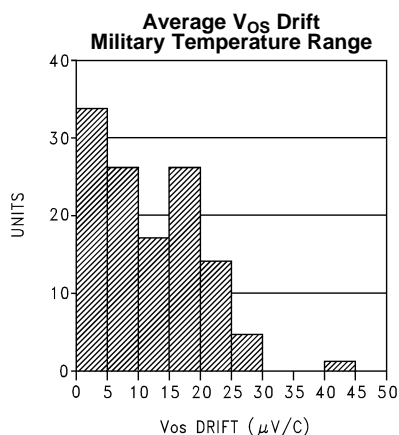


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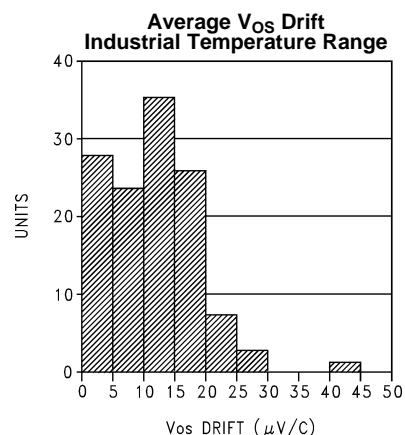


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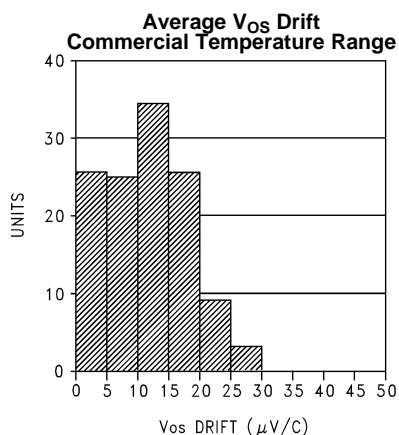


Figure 46.

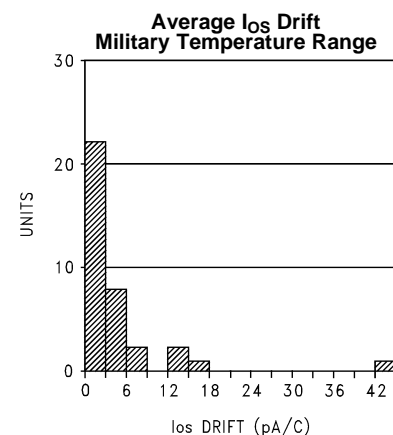


Figure 47.

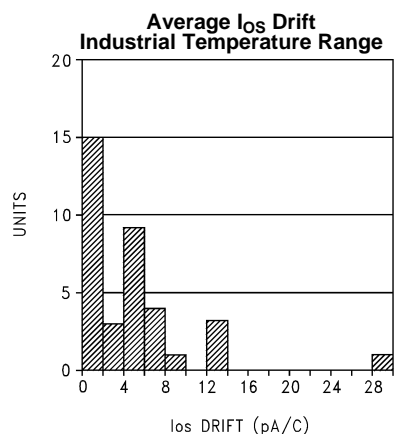


Figure 48.

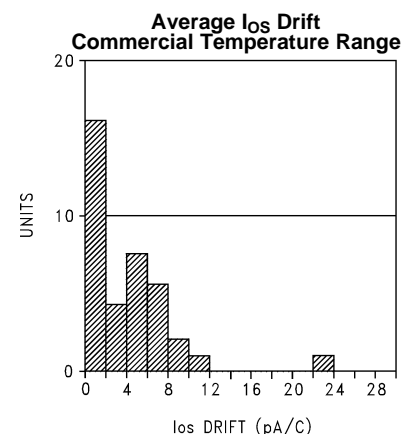


Figure 49.

Typical Performance Distributions (continued)

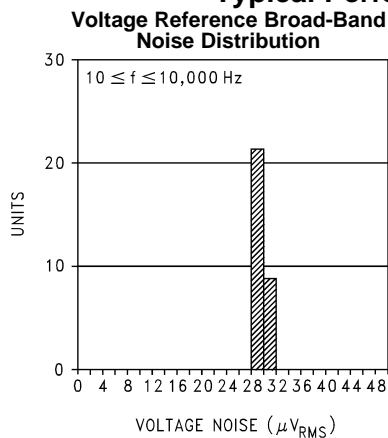


Figure 50.

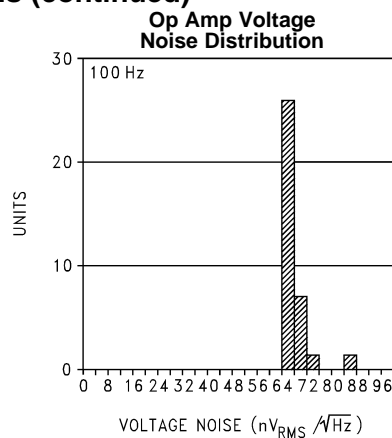


Figure 51.

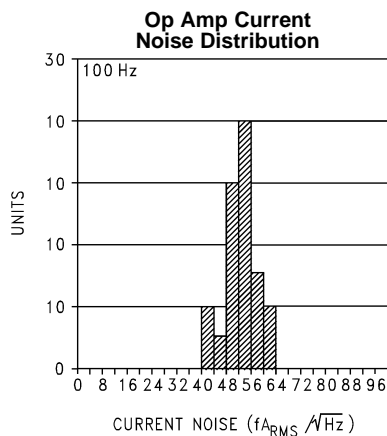


Figure 52.

APPLICATION INFORMATION

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

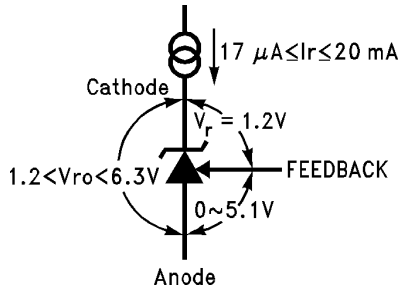


Figure 53. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .

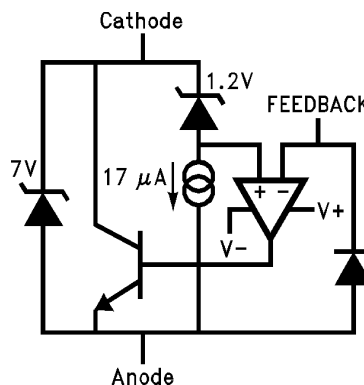


Figure 54. Reference Equivalent Circuit

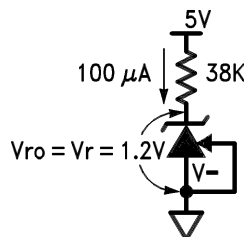


Figure 55. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the [Reference AC Stability Range curve](#) for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24\text{V}$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5\text{V}$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for $<0.1\%$ error— $I \geq 32\text{ }\mu\text{A}$ for the military grade over the military temperature range ($I \geq 5.5\text{ }\mu\text{A}$ for a 1% untrimmed error for a commercial part.)

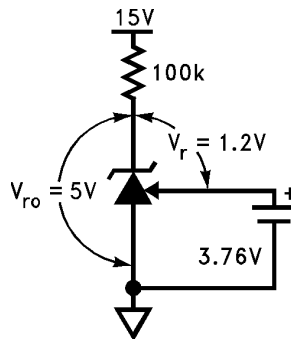
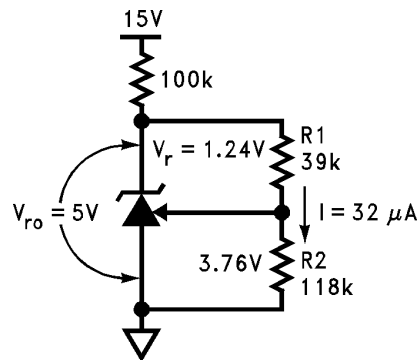


Figure 56. Thevenin Equivalent of Reference with 5V Output



$$R1 = V_r / I = 1.24 / 32\mu = 39k$$

$$R2 = R1 \{ (V_{ro}/V_r) - 1 \} = 39k \{ (5/1.24) - 1 \} = 118k$$

Figure 57. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

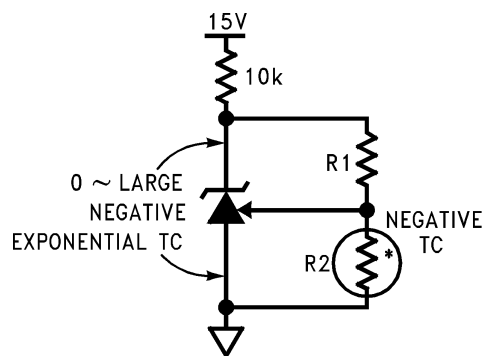


Figure 58. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

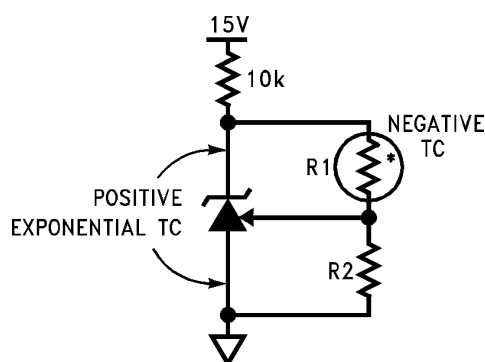


Figure 59. Output Voltage has Positive TC if R1 has Negative TC

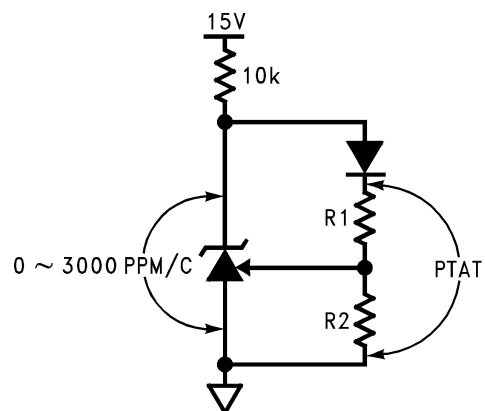
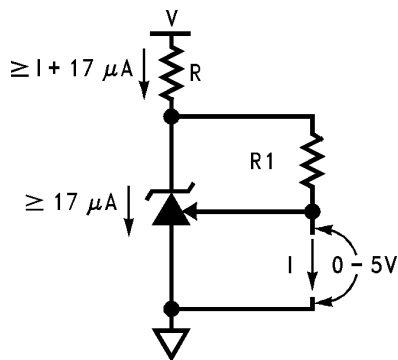


Figure 60. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



$$I = V_r/R1 = 1.24/R1$$

Figure 61. Current Source is Programmed by R1

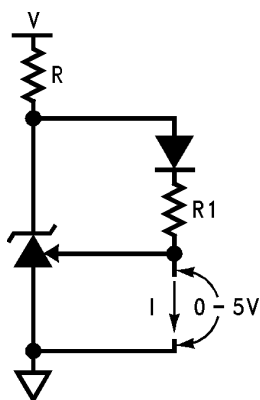


Figure 62. Proportional-to-Absolute-Temperature Current Source

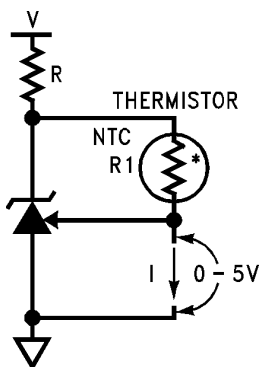


Figure 63. Negative -TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see ⁽¹⁾ under [Electrical Characteristics](#)). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. **Output Swing:** Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.
2. **Cross-over Distortion:** The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the [Typical Performance Characteristics curves](#). A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3. **Capacitive Drive:** Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25 Ω . 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

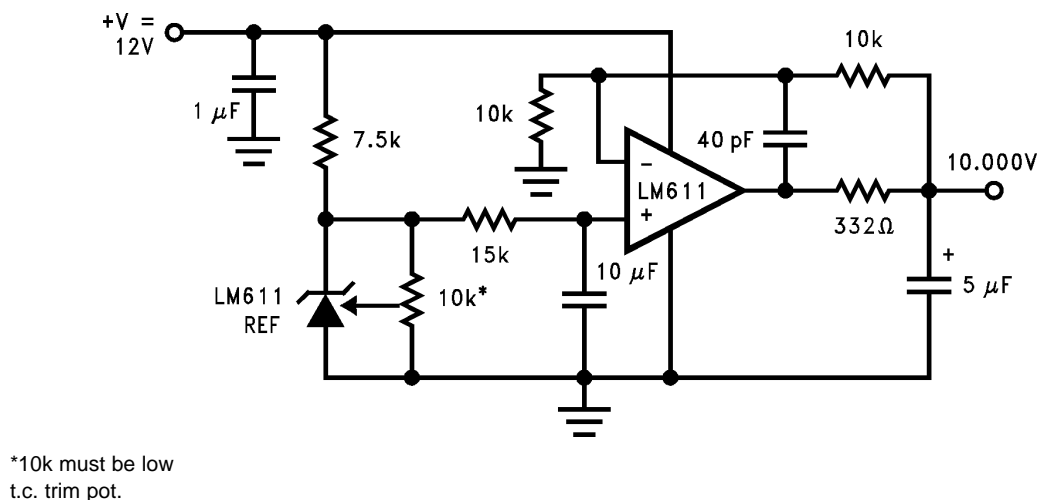


Figure 64. Ultra Low Noise 10.000V Reference.
Total Output Noise is Typically 14 μV_{RMS} .
Adjust the 10k pot for 10.000V.

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

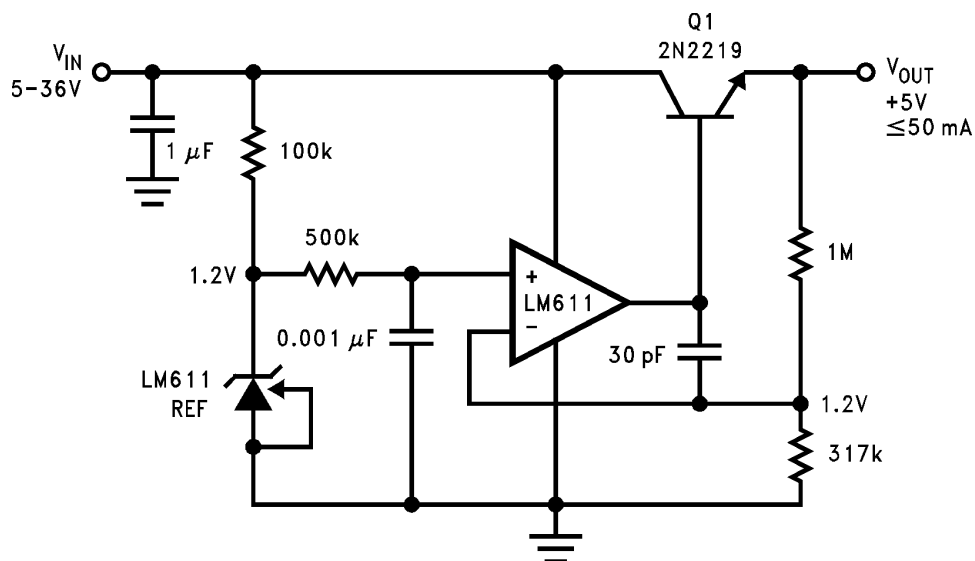
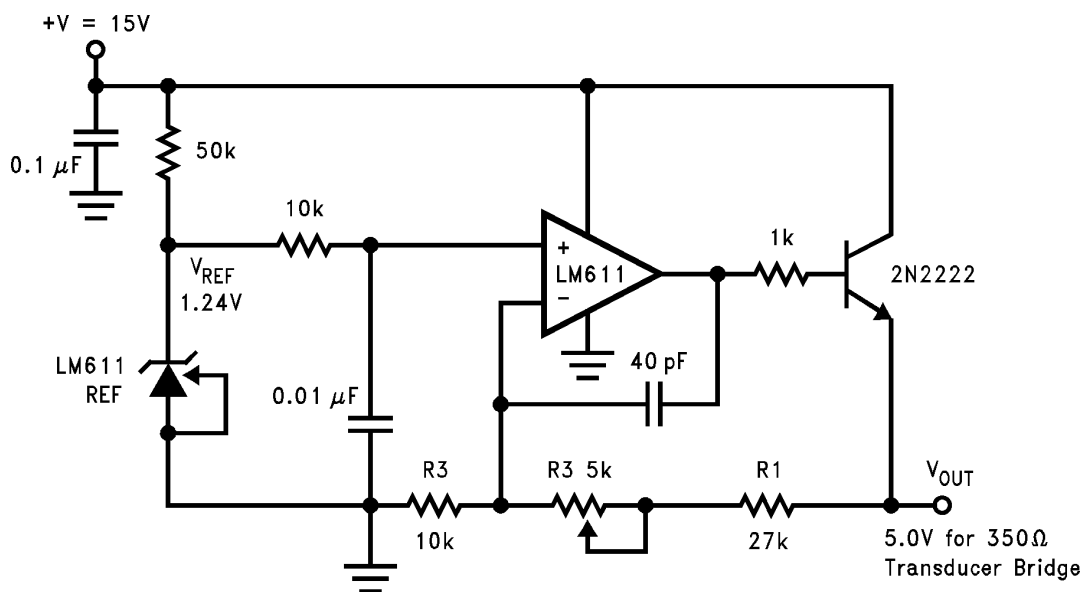


Figure 65. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately 320 μ A when $V_{IN} = 5V$, and output has no load.



$V_{OUT} = (R1/R2 + 1) V_{REF}$.
R1, R2 should be 1% metal film.
R3 should be low t.c. trim pot.

Figure 66. Slow Rise-Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise-time is approximately 0.5 ms.

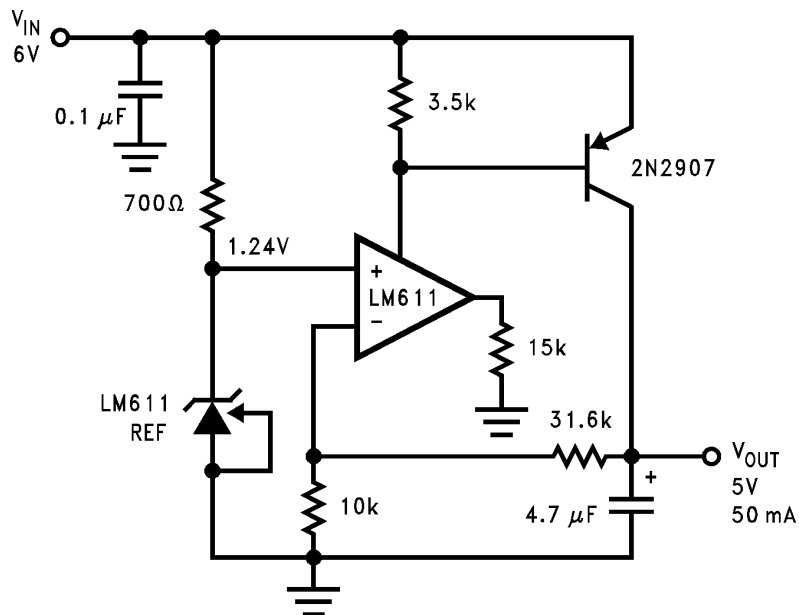


Figure 67. Low Drop-Out Voltage Regulator Circuit. Drop out voltage is typically 0.2V.

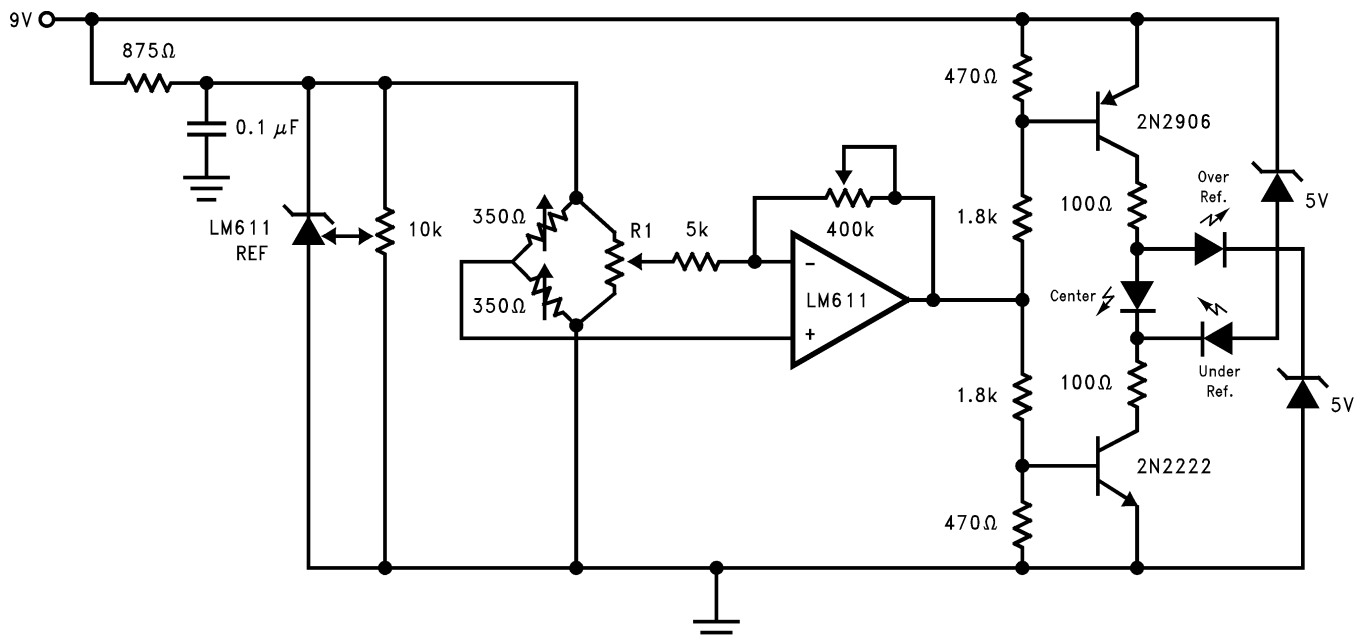


Figure 68. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot. Null offset with R1, and bridge drive with the 10k pot.

Simplified Schematic Diagrams

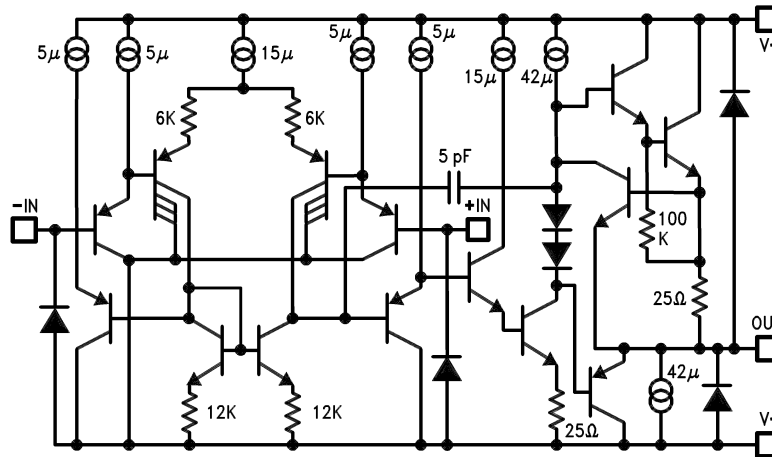


Figure 69. Op Amp

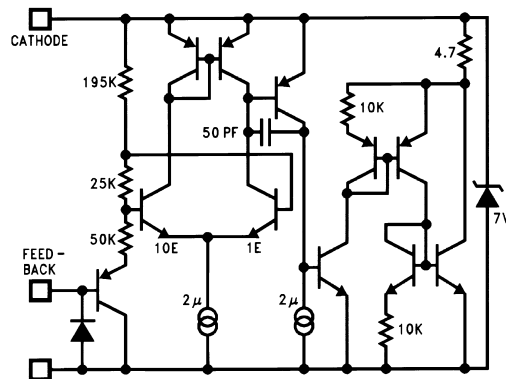


Figure 70. Reference

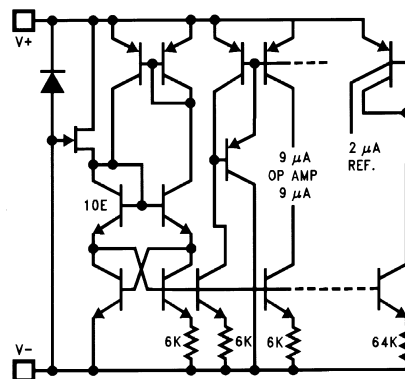


Figure 71. Bias

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM611CM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM611CM	Samples
LM611CM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611CMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LM611CM	Samples
LM611CMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611IM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM611IM	Samples
LM611IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples
LM611IMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LM611IM	Samples
LM611IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM611CMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM611CMX	SOIC	D	14	2500	349.0	337.0	45.0
LM611CMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LM611IMX	SOIC	D	14	2500	349.0	337.0	45.0
LM611IMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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