November 1999

# FDR8305N

## Dual N-Channel 2.5V Specified PowerTrench® MOSFET

### General Description

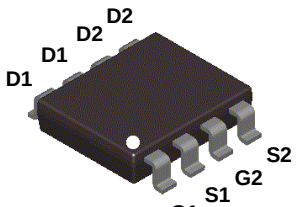
These N-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

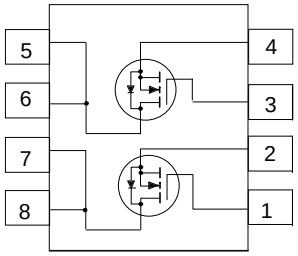
- Load switch
- Motor driving
- Power Management

### Features

- 4.5 A, 20 V. $R_{DS(ON)}$ = 0.022 Ω @ $V_{GS}$ = 4.5 V
  $R_{DS(ON)}$ = 0.028 Ω @ $V_{GS}$ = 2.5 V.
- Low gate charge (16.2nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- Small footprint (38% smaller than a standard SO-8);low profile package (1 mm thick); power handling capability similar to SO-8.




SuperSOT™-8




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 4.5 | A |
| | - Pulsed | | 20 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 0.8 | W |
| $T_J$, $T_{stg}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 156 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| .8305 | FDR8305N | 13'' | 12mm | 3000 units |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 14 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | | | 1 | µA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -8 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.4 | 0.85 | 1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | -3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 4.5 A<br>$V_{GS}$=4.5 V, $I_D$=4.5 A, $T_J$=125°C<br>$V_{GS}$ = 2.5 V, $I_D$ = 4 A | | 0.015<br>0.026<br>0.020 | 0.022<br>0.040<br>0.028 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 4.5 V, $I_D$ = 4.5 A | | 24 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1600 | | pF |
| $C_{oss}$ | Output Capacitance | | | 380 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 200 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 12 | 22 | ns |
| $t_r$ | Turn-On Rise Time | | | 15 | 27 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 35 | 55 | ns |
| $t_f$ | Turn-Off Fall Time | | | 18 | 30 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 4.5 A, $V_{GS}$ = 4.5 V | | 16.2 | 23 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 2.5 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 5.5 | | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 0.67 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.67 A (Note 2) | | 0.65 | 1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.





156°C/W on a minimum mounting pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Characteristics

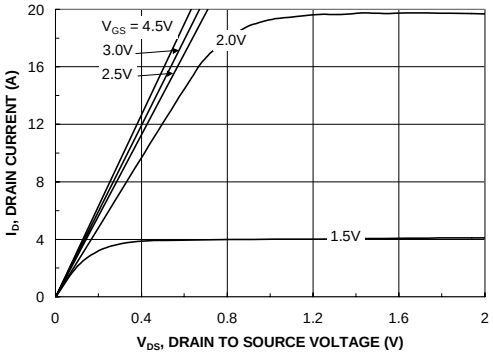



**Figure 1. On-Region Characteristics.**

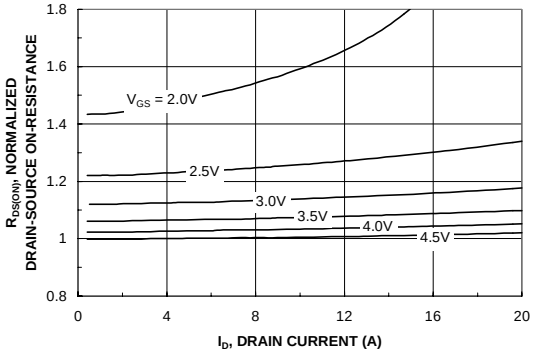



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

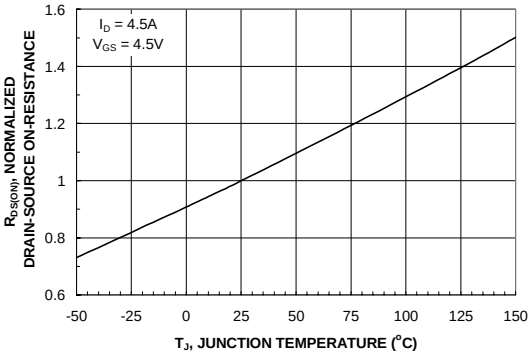



**Figure 3. On-Resistance Variation with Temperature.**

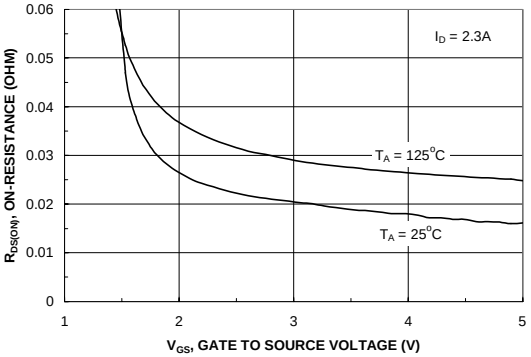



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

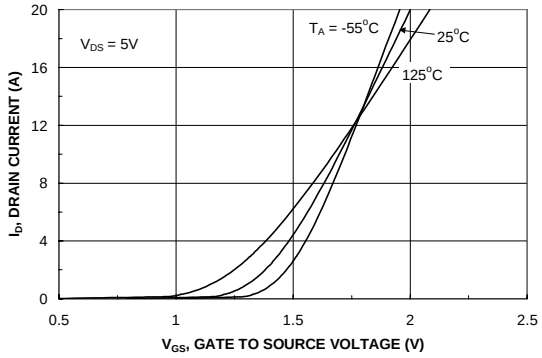



**Figure 5. Transfer Characteristics.**

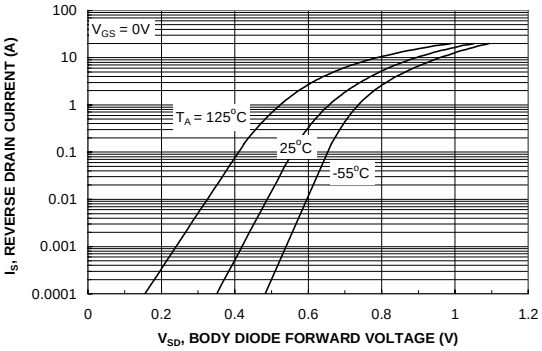



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics (continued)

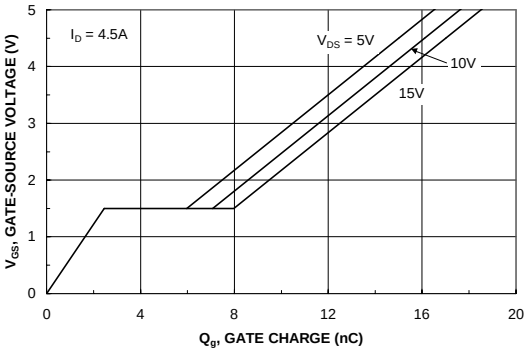



**Figure 7. Gate Charge Characteristics.**

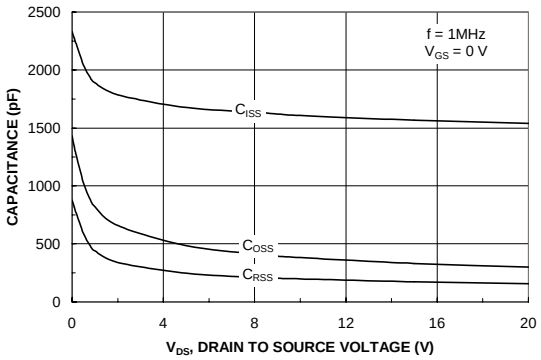



**Figure 8. Capacitance Characteristics.**

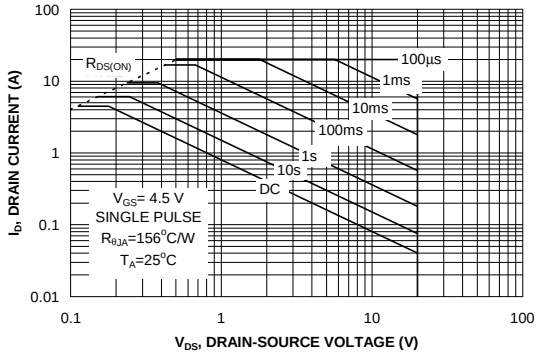



**Figure 9. Maximum Safe Operating Area.**

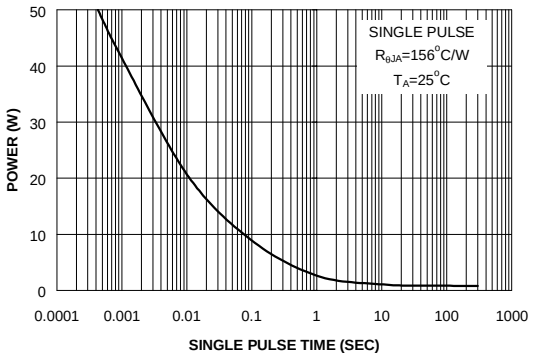
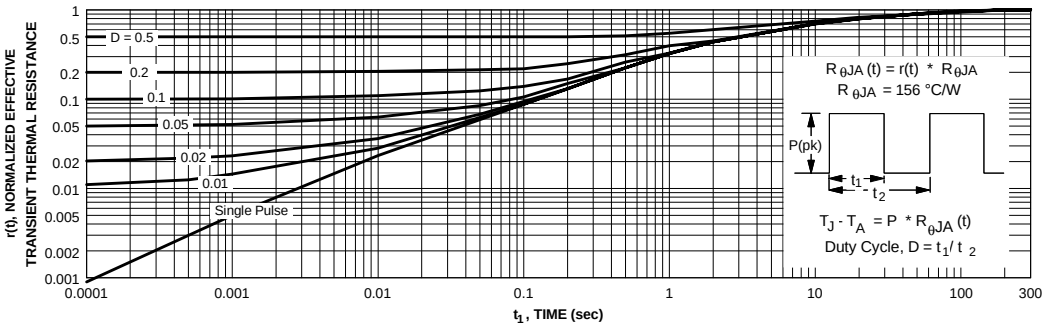



**Figure 10. Single Pulse Maximum Power Dissipation.**



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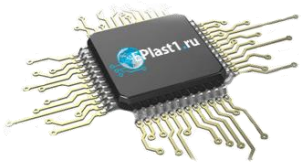
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