Rev. 3 — 17 April 2019

**Product data sheet** 

## 1. General description

The 74HC3G16 is a triple buffer. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{\rm CC}$ .

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- · CMOS input levels
- · Complies with JEDEC standard no. 7 A
- · Symmetrical output impedance
- High noise immunity
- Low-power dissipation
- Balanced propagation delays
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

#### **Table 1. Ordering information**

Type number	Package				
	Temperature range	Name	Description	Version	
74HC3G16DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2	

## 4. Marking

#### Table 2. Marking

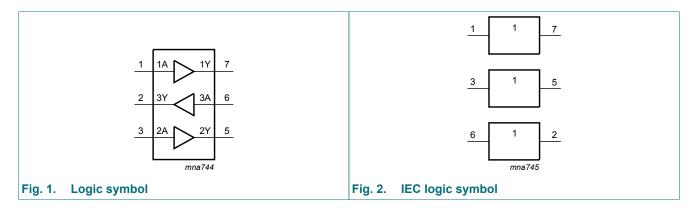
Type number	Marking code [1]
74HC3G16DP	P6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.



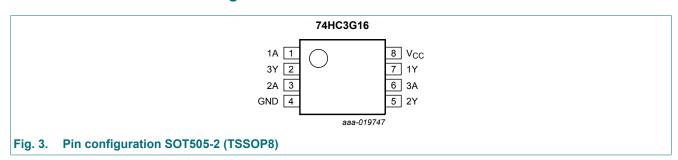
Triple buffer gate

# 5. Functional diagram



# 6. Pinning information

## 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description		
1A, 2A, 3A	1, 3, 6	data input		
1Y, 2Y, 3Y	7, 5, 2	data output		
GND	4	ground (0 V)		
V <sub>CC</sub>	8	supply voltage		

# 7. Functional description

#### **Table 4. Function table**

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$ 

Input	Output
nA	nY
L	L
Н	Н

**Triple buffer gate** 

## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	$V_{\rm O} = -0.5 \text{ V to } (V_{\rm CC} + 0.5 \text{ V})$	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$ [2]	-	300	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 9. Recommended operating conditions

#### **Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V

### 10. Static characteristics

#### **Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +85	S°C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V

<sup>[2]</sup> For TSSOP8 package: above 55 °C the value of Ptot derates linearly with 2.5 mW/K.

### **Triple buffer gate**

Symbol	Parameter	Conditions	-40	°C to +85	5 °C	-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
	voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	V
	$I_O = -20 \mu A; V_{CC} = 4.5 V$ 4.4 4.5 $I_O = -20 \mu A; V_{CC} = 6.0 V$ 5.9 6.0	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	V
		-	5.9	-	V			
		$I_{O}$ = -4.0 mA; $V_{CC}$ = 4.5 V	4.13	4.32	-	3.7	-	V
		$I_{O}$ = -5.2 mA; $V_{CC}$ = 6.0 V	5.63	5.81	-	5.2	-	V
V <sub>OL</sub> LOW-level output	· ·	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.33	-	0.4	V
Iį	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	per input pin; $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	10	-	20	μΑ
C <sub>I</sub>	input capacitance		-	1.5	-	-	-	pF

<sup>[1]</sup> All typical values are measured at  $T_{amb}$  = 25 °C.

# 11. Dynamic characteristics

#### **Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Symbol Parameter Conditions		-4	0 °C to +85	°C	-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 4 [2]						
		V <sub>CC</sub> = 2.0 V	-	29	95	-	125	ns
		V <sub>CC</sub> = 4.5 V	-	9	19	-	25	ns
		V <sub>CC</sub> = 6.0 V	-	8	16	-	20	ns
t <sub>t</sub>	transition time	nY; see <u>Fig. 4</u> [3]						
		V <sub>CC</sub> = 2.0 V	-	18	95	-	125	ns
		V <sub>CC</sub> = 4.5 V	-	6	19	-	25	ns
		V <sub>CC</sub> = 6.0 V	-	5	16	-	20	ns
$C_{PD}$	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$ [4]	-	10	-	-	-	pF

- All typical values are measured at T<sub>amb</sub> = 25 °C.
- $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] t<sub>t</sub> is the same as t<sub>TLH</sub> and t<sub>THL</sub>.
   [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

 $f_o$  = output frequency in MHz;

 $C_L$  = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

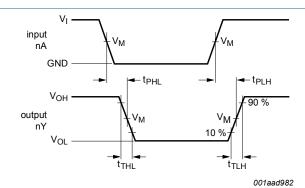
N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of outputs.

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Triple buffer gate

#### 11.1. Waveforms and test circuit



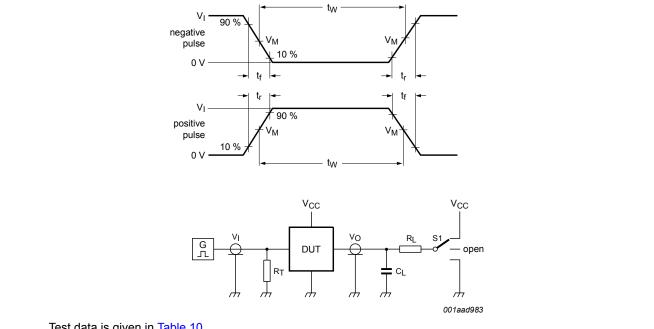
Measurement points are given in Table 9.

 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Propagation delay data input (nA) to data output (nY) and transition time output (nY)

**Table 9. Measurement points** 

Input	Output
V <sub>M</sub>	$V_{M}$
0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>



Test data is given in Table 10.

Definitions for test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

 $R_L$  = Load resistance; S1 = Test selection switch.

Test circuit for measuring switching times

Table 10. Test data

Input		Load	S1 position	
V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub> R <sub>L</sub>		t <sub>PHL</sub> , t <sub>PLH</sub>
GND to V <sub>CC</sub>	≤ 6 ns	50 pF	1 kΩ	open

Triple buffer gate

# 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

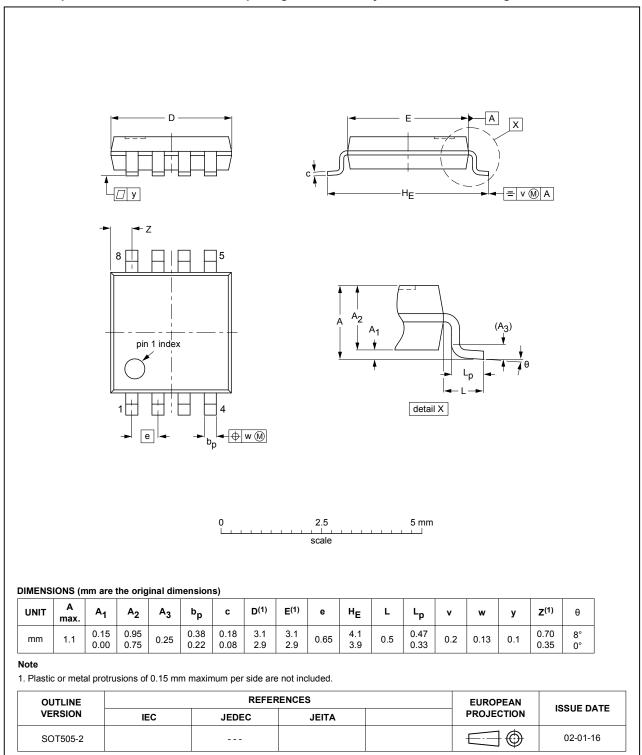


Fig. 6. Package outline SOT505-2 (TSSOP8)

Triple buffer gate

## 13. Abbreviations

#### **Table 11. Abbreviations**

Acronym	Description	
CMOS	Complementary Metal-Oxide Semiconductor	
DUT	evice Under Test	
ESD	ElectroStatic Discharge	
НВМ	Human Body Model	
MM	Machine Model	

# 14. Revision history

#### **Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC3G16 v.3	20190417	Product data sheet	-	74HC_HCT3G16 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74HCT3G16DP (SOT505-2) removed.</li> <li>Type numbers 74HC3G16GD and 74HCT3G16GD (SOT996-2) removed.</li> </ul>				
74HC_HCT3G16 v.2	20161007	Product data sheet	-	74HC_HCT3G16 v.1	
Modifications:	Type numbers 74HCT3G16DC and 74HCT3G16DC removed.				
74HC_HCT3G16 v.1	20151015	Product data sheet	-	-	

#### **Triple buffer gate**

## 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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### Triple buffer gate

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