Low Power HDMI Display Interface

AD9393

FEATURES

- HDMI interface
- Supports high bandwidth digital content protection
- RGB to YCrCb 2-way color conversion
- 1.8 V/3.3 V power supply
- 76-ball BGA package
- RGB and YCrCb output formats
- Digital video interface
  - HDMI 1.2a, DVI 1.0
  - 80 MHz HDMI receiver
  - Supports high bandwidth digital content protection (HDCP 1.1)
- Digital audio interface
  - HDMI 1.2a-compatible audio interface
  - S/PDIF (IEC60958-compatible) digital audio output
  - Multichannel I²S audio output (up to 8 channels)

APPLICATIONS

- Portable low power TV
- HDTV
- Projectors
- LCD monitor

FUNCTIONAL BLOCK DIAGRAM

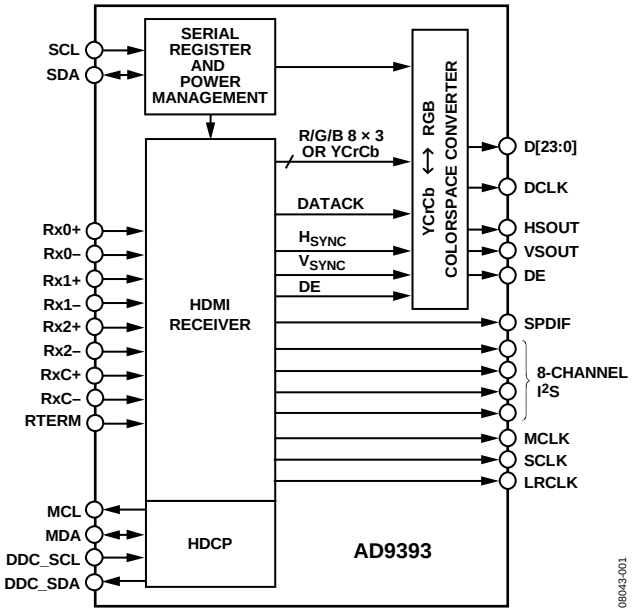

Figure 1.

GENERAL DESCRIPTION

The AD9393 offers a High-Definition Multimedia Interface (HDMI™) receiver integrated on a single chip. Support is also included for high bandwidth digital content protection (HDCP).

The AD9393 contains a HDMI 1.2a-compatible receiver and supports HDTV formats (up to 720p or 1080i) and displays resolutions up to XGA (1024 × 768 @ 75 Hz). The receiver features an intrapair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays may now receive encrypted video content. The AD9393 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.1 protocol.

Fabricated in an advanced CMOS process, the AD9393 is provided in a space-saving 76-ball, surface-mount, Pb-free, ball grid array (BGA) and is specified over the −10°C to +80°C temperature range.

Rev. 0

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REVISION HISTORY

10/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD}, V_D = 3.3 V, DV_{DD} = PV_{DD} = 1.8 V, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS (5 V Tolerant)						
Input Voltage, High (V_{IH})	Full	VI	2.6			V
Input Voltage, Low (V_{IL})	Full	VI			0.8	V
Input Current, High (I_{IH})	Full	V		–82		µA
Input Current, Low (I_{IL})	Full	V		82		µA
Input Capacitance	25°C	V		3		pF
DIGITAL OUTPUTS						
Output Voltage, High (V_{OH})	Full	VI	V_{DD} – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.4	V
Duty Cycle, DCLK	Full	V	45	50	55	%
Output Coding				Binary		
THERMAL CHARACTERISTICS						
θ_{JA} Junction-to-Ambient		V		59		°C/W
θ_{JC} Junction-to-Case		V		15.2		°C/W

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

V_{DD} = V_D =3.3 V, DV_{DD} = PV_{DD} = 1.8 V, unless otherwise noted.

Table 2.

Parameter	Test Level	Conditions	Min	Typ	Max	Unit
DC DIGITAL I/O Specifications						
High-Level Input Voltage (V_{IH})	VI		2.5			V
Low-Level Input Voltage (V_{IL})	VI				0.8	V
High-Level Output Voltage (V_{OH})	VI		V_{DD} − 0.1			V
Low-Level Output Voltage (V_{OL})	VI		V_{DD} − 0.1		0.1	V
DC SPECIFICATIONS						
Output High Level	IV	Output drive = high strength		36		mA
I_{OHD} (V_{OUT} = V_{OH})	IV	Output drive = low strength		24		mA
Output Low Level	IV	Output drive = high strength		12		mA
I_{OLD} (V_{OUT} = V_{OL})	IV	Output drive = low strength		8		mA
DCLK High Level	IV	Output drive = high strength		40		mA
V_{OHC} (V_{OUT} = V_{OH})	IV	Output drive = low strength		20		mA
DCLK Low Level	IV	Output drive = high strength		30		mA
V_{OLC} (V_{OUT} = V_{OL})	IV	Output drive = low		15		mA
Differential Input Voltage, Single-Ended Amplitude	IV		75		700	mV
POWER SUPPLY						
V_D	IV		3.15	3.3	3.47	V
V_{DD}	IV		1.7	3.3	347	V
DV_{DD}	IV		1.7	1.8	1.9	V
PV_{DD}	IV		1.7	1.8	1.9	V
Power—54 MHz, YCrCb 422, CSC Disabled				485		mW
Supply Current (Worst Pattern)[1]						
I_{VD}	V			95		mA
I_{VDD}	V			18		mA
I_{DVDD}[2]	V			51		mA
I_{PVDD}	V			26		mA
Power—74.25 MHz, RGB, CSC Disabled				593		mW
Supply Current (Worst Pattern)[1]						
I_{VD}	V			109		mA
I_{VDD}	V			38		mA
I_{DVDD}	V			66		mA
I_{PVDD}	V			26		mA
Power-Down Power	VI			130		mW
AC SPECIFICATIONS						
Intrapair (+ to −) Differential Input Skew (t_{DPS})	IV		0.4			t_{BIT}
Channel-to-Channel Differential Input Skew (t_{CCS})	IV		0.6			t_{PIXEL}
Low-to-High Transition Time for Data and Controls (D_{LHT})	IV	Output drive = high; C_L = 10 pF		1000		ps
	IV	Output drive = low; C_L = 5 pF				ps
Low-to-High Transition Time for DCLK (D_{LHT})	IV	Output drive = high; C_L = 10 pF		1000		ps
	IV	Output drive = low; C_L = 5 pF				ps
High-to-Low Transition Time for Data and Controls (D_{HLT})	IV	Output drive = high; C_L = 10 pF		1000		ps
	IV	Output drive = low; C_L = 5 pF				ps
High-to-Low Transition Time for DCLK (D_{HLT})	IV	Output drive = high; C_L = 10 pF		1000		ps
	IV	Output drive = low; C_L = 5 pF				ps
Clock-to-Data Skew[3] (t_{SKEW})	IV		−0.5		+2.0	ns
Duty Cycle, DCLK[3]	IV		45	50		%
DCLK Frequency (f_{CIP})	VI		20		80	MHz

[1] Worst-case pattern is alternating black and white pixels.
[2] DCLK load = 10 pF, data load = 5 pF.
[3] Drive strength = high.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_D	3.6 V
V_{DD}	3.6 V
DV_{DD}	1.98 V
PV_{DD}	1.98 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

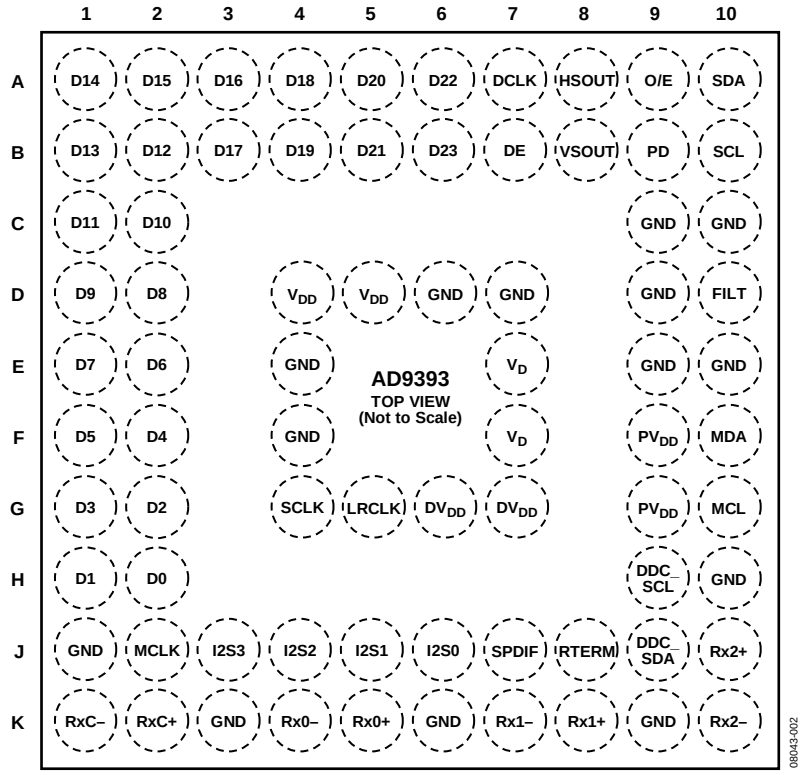

Figure 2. Pin Configuration

Table 4. Complete Pin List

Pin No.	Mnemonic	Description	Value
Inputs			
B9	PD	Power-Down Control. Power-Down Control/Three-State Control. The function of this pin is programmable via Register 0x26[2:1].	3.3 V CMOS
Digital Video Data Inputs			
K5, K4, K8, K7, J10, K10	Rx0+, Rx0−, Rx1+, Rx1−, Rx2+, Rx2−	Digital Input Channel x True/Complement. These six pins receive three pairs of transition minimized differential signaling (TMDS) pixel data (at 10× the pixel rate) from a digital graphics transmitter.	TMDS
Digital Video Clock Inputs			
K2, K1	RxC+, RxC−	Digital Data Clock True/Complement. This clock pair receives a TMDS clock at 1× pixel data rate.	TMDS
Outputs			
B6, A6, B5, A5, B4, A4, B3, A3, A2, A1, B1, B2, C1, C2, D1, D2, E1, E2, F1, F2, G1, G2, H1, H2	D[23:0]	Data Outputs. In RGB, D[23:16] = Red[7:0] D[15:8] = Green[7:0] D[7:0] = Blue[7:0] See Table 6	V_{DD}
A7	DCLK	Data Output Clock. This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x25[7:6]. These are related to the pixel clock (½× pixel clock, 1× pixel clock, 2× frequency pixel clock, and a 90° phase shifted pixel clock). They are produced by the internal PLL clock generator and are synchronous with the pixel clock. The polarity of DCLK can also be inverted via Register 0x24[0].	V_{DD}
A8	HSOUT	HSYNC Output Clock (Phase-Aligned with DCLK). Horizontal sync output. A reconstructed and phase-aligned version of the HSYNC input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DCLK and data, data timing with respect to horizontal sync can always be determined.	V_{DD}

Pin No.	Mnemonic	Description	Value
B8	VSOUT	VSYNC Output Clock (Phase-Aligned with DCLK). Vertical Sync Output. The separated VSYNC from a composite signal or a direct passthrough of the VSYNC signal. The polarity of this output can be controlled via the serial bus bit (Register 0x24[6]).	V_{DD}
A9	O/E	Odd/Even Field Output for Interlaced Video. This output identifies whether the current field (in an interlaced signal) is odd or even. The polarity of this signal is programmable via Register 0x24[4].	V_{DD}
References			
D10	FILT	Connection for External Filter Components for Audio PLL. For proper operation, the audio clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node. For more information, see the PCB Layout Recommendations section.	PV_{DD}
Power Supply[1]			
E7, F7	V_D	HDMI Terminator Power Supply (3.3 V). These pins supply power to the HDMI terminators. They should be as quiet and filtered as possible.	3.3 V
D4, D5	V_{DD}	Digital Output Power Supply (1.8 V to 3.3 V). A large number of output pins (up to 27) switching at high speed (up to 80 MHz) generates many power supply transients (noise). These supply pins are identified separately from the V_D pins, so output noise transferred into the sensitive circuitry can be minimized. If the AD9393 is interfacing with lower voltage logic, V_{DD} can be connected to a lower supply voltage (as low as 1.8 V) for compatibility.	1.8 V to 3.3 V
F9, G9	PV_{DD}	PLL Power Supply (1.8 V). The most sensitive portion of the AD9393 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The user should provide quiet, noise-free power to these pins.	1.8 V
G6, G7	DV_{DD}	Digital Logic Power Supply (1.8 V). These pins supply power to the digital logic.	1.8 V
C9, C10, D6, D7, D9, E4, E9, E10, F4, H10, J1, K3, K6, K9	GND	Ground. The ground return for all circuitry on chip. It is recommended that the AD9393 be assembled on a single solid ground plane, with careful attention to ground current paths.	0 V
Control			
A10	SDA	Serial Port Data I/O for Programming the AD9393 Registers. The I^2C address is Address 0x98.	3.3 V CMOS
B10	SCL	Serial Port Data Clock for Programming the AD9393 Registers.	3.3 V CMOS
HDCP			
H9	DDC_SCL	HDCP Slave Serial Port Data Clock for HDCP Communications to Transmitter.	3.3 V CMOS
J9	DDC_SDA	HDCP Slave Serial Port Data I/O for HDCP Communications to Transmitter. The I^2C address is Address 0x74 or Address 0x76.	3.3 V CMOS
F10	MDA	Master Serial Port I/O to EEPROM with HDCP Keys—I^2C Address is 0xA0.	3.3 V CMOS
G10	MCL	Master Serial Port Data Clock to EEPROM with HDCP Keys.	3.3 V CMOS
Audio Data Outputs			
J7	S/PDIF	S/PDIF Digital Audio Output.	V_{DD}
J6	I2S0	I^2S Audio (Channel 1, Channel 2). Channel 0 and Channel 1 Audio Output.	V_{DD}
J5	I2S1	I^2S Audio (Channel 3, Channel 4). Channel 2 and Channel 3 Audio Output.	V_{DD}
J4	I2S2	I^2S Audio (Channel 5, Channel 6). Channel 4 and Channel 5 Audio Output.	V_{DD}
J3	I2S3	I^2S Audio (Channel 7, Channel 8). Channel 6 and Channel 7 Audio Output.	V_{DD}
J2	MCLK	Audio Master Clock Output for S/PDIF Data.	V_{DD}
G4	SCLK	Audio Serial Clock Output for I^2S Data.	V_{DD}
G5	LRCLK	Data Output Clock for Left and Right Audio Channels.	V_{DD}
Data Enable			
B7	DE	Data Enable for Active Data Pixels.	3.3 V CMOS
RTERM			
J8	RTERM	Sets Internal Termination Resistance. Place a 500 Ω (1% tolerance) resistor from this pin to ground. This sets the internal termination of TMDS lines to 50 Ω.	500 Ω

[1] The supplies should be sequenced such that V_D and V_{DD} are never less than 300 mV below DV_{DD}. At no time should DV_{DD} be more than 300 mV greater than V_D or V_{DD}.

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9393 is a fully integrated solution for receiving DVI/HDMI signals and is capable of decoding HDCP-encrypted signals through connections to an external EEPROM. The circuit is ideal for providing an interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 80 MHz.

The AD9393 includes all necessary circuitry for decoding TMDS signaling including those encrypted with HDCP. Included in the output formatting is a color space converter (CSC), which accommodates any input color space and can output any color space. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive mixed signal functions makes system design straight forward and less sensitive to the physical and electrical environment.

DIGITAL INPUTS

The digital control inputs (I^2C) on the AD9393 operate to 3.3 V CMOS levels. In addition, all digital inputs except the TMDS inputs (HDMI/DVI) are 5 V tolerant. Applying 5 V to them does not cause any damage. The TMDS input pairs (Rx0±, Rx1±, Rx2±, and RxC±) must maintain a 100 Ω differential impedance (through proper PCB layout) from the connector to the input where they are internally terminated (50 Ω to 3.3 V). If additional ESD protection is desired, using a low capacitance ESD protection varistor offers 8 kV of protection to the HDMI TMDS lines.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic. However, it is tolerant of 5 V logic signals.

OUTPUT SIGNAL HANDLING

The digital outputs operate from 1.8 V to 3.3 V (V_{DD}).

POWER MANAGEMENT

To determine the correct power state, the AD9393 uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, the power-down bit, and the power-down ball. There are three power modes: full power, auto power-down, and power-down.

Table 5 summarizes how the AD9393 determines which power mode to use and which circuitry is powered on/off in each of these modes. The power-down command has first priority and the automatic circuitry second priority. The power-down ball (Ball B8—polarity set by Register 0x26[3]) can drive the chip into two power-down options. Bit 2 of Register 0x26 controls these two options. Bit 0 controls whether the chip is powered down or the outputs are placed in high impedance mode. Bit 7 to Bit 4 of Register 0x26 control whether the outputs, Sony/Philips digital interface (S/PDIF), or Inter-IC Sound bus (I^2S or IIS) outputs are in high impedance mode or not. See the 2-Wire Serial Control Register Detail section for the details.

Table 5. Power-Down Mode Descriptions

	Inputs		
Mode	**Power-Down[1]**	**Auto PD Enable[2]**	**Power-On/Comments**
Full Power	1	X	Everything
Auto Power-Down	1	1	Serial bus, sync activity detect, band gap reference
Power-Down	0	X	Serial bus, sync activity detect, band gap reference

[1] Power-down is controlled via Bit 0 in Register 0x26.
[2] Auto power-down is controlled via Bit 7 in Register 0x27.

TIMING

The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally.

Figure 3 shows the timing operation of the AD9393.

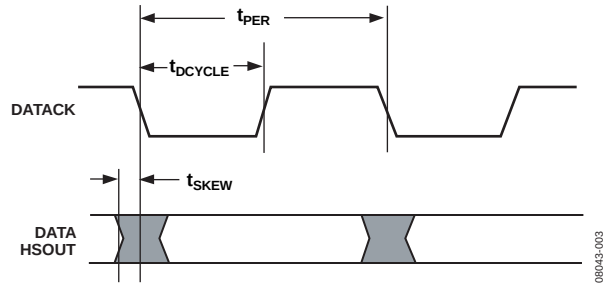

Figure 3. Output Timing

HDMI RECEIVER

The HDMI receiver section of the AD9393 allows the reception of a digital video stream (which is backward compatible with DVI and able to accommodate video of various formats (RGB, YCrCb 4:4:4, 4:2:2)). The receiver also allows up to eight channels of audio. Infoframes are transmitted carrying information about the video format, audio clocks, and many other items necessary for a monitor to utilize fully the information stream available.

The earlier digital visual interface (DVI) format was restricted to an RGB 24-bit color space only. Embedded in this data stream were HSYNCs, VSYNCs, and display enable (DE) signals; but no audio information. The HDMI specification allows transmission of all the DVI capabilities, but adds several YCrCb formats that make the inclusion of a programmable color space converter (CSC) a very desirable feature. With this feature, the scaler following the AD9393 can specify that it always wishes to receive a particular format, for instance, 4:2:2 YCrCb, regardless of the transmitted mode. If RGB is sent, the CSC can easily convert that to 4:2:2 YCrCb while relieving the scaler of this task.

In addition, the HDMI specification supports the transmission of up to eight channels of S/PDIF or I^2S audio. The audio information is separated into packets and transmitted during the video blanking periods along with specific information about the clock frequency. Part of this audio information (audio infoframe) tells the user how many channels of audio are being transmitted, where the channels should be placed, information regarding the source (make, model), and other data.

DE GENERATOR

The AD9393 has an on-board generator for DE, for the start of active video (SAV), and for the end of active video (EAV), all of which are necessary for describing the complete data stream for a BT656-compatible output. This signal alerts the following circuitry, which are displayable video pixels.

4:4:4 TO 4:2:2 FILTER

The AD9393 contains a filter that allows it to convert a signal from YCrCb 4:4:4 to YCrCb 4:2:2 while maintaining the maximum accuracy and fidelity of the original signal.

Input Color Space to Output Color Space

The AD9393 can accept a wide variety of input formats and either retain that format or convert to another. Input formats supported are

- 4:4:4 YCrCb 8-bit
- 4:2:2 YCrCb 8-, 10-, and 12-bit
- RGB 8-bit

Output modes supported are

- 4:4:4 YCrCb 8-bit
- 4:2:2 YCrCb 8-, 10-, and 12-bit
- Dual 4:2:2 YCrCb 8-bit

Color Space Conversion (CSC) Matrix

The CSC matrix in the AD9393 consists of three identical processing channels. In each channel, three input values are multiplied by three separate coefficients. An offset value for each row of the matrix and a scaling multiple for all values are also included. Each value has a 13-bit, twos complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 80 MHz supporting resolutions up to 720p at 60 Hz. With any-to-any color space support, formats such as RGB, YUV, YCrCb, and others are supported by the CSC.

The main inputs, R_{IN}, G_{IN}, and B_{IN}, come from the 8-bit or 12-bit inputs from each channel. These inputs are based on the input format detailed in Table 30 to Table 52. The mapping of these inputs to the CSC inputs is shown in Table 6.

Table 6. CSC Port Mapping

Input Channel	CSC Input Channel
R/Cr (D[23:16])	R_{IN}
Gr/Y (D[15:8])	G_{IN}
B/Cb (D[7:0])	B_{IN}

One of the three input channels is represented in Figure 4. In each processing channel, the three inputs are multiplied by three separate coefficients marked a1, a2, and a3. These coefficients are divided by 4096 to obtain nominal values ranging from −0.9998 to +0.9998. The variable labeled a4 is used as an offset control. The CSC_MODE setting is the same for all three processing channels. This multiplies all coefficients and offsets by a factor of 2^{CSC_MODE}.

The functional diagram for a single channel of the CSC (as shown in Figure 4) is repeated for the remaining G and B channels. The coefficients for these channels are b1, b2, b3, b4, c1, c2, c3, and c4.

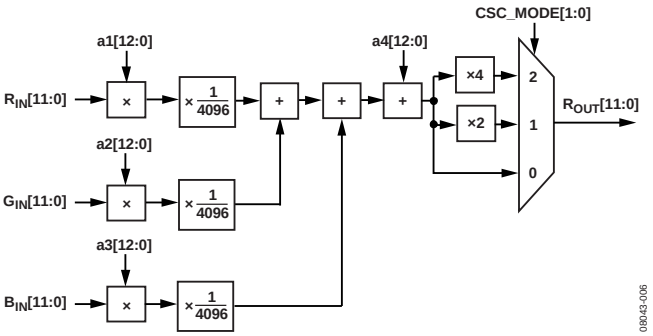

Figure 4. Single CSC Channel

A programming example and register settings for several common conversions are listed in the Color Space Converter (CSC) Common Settings section.

For a detailed functional description and more programming examples that are compatible with the AD9393, refer to the AN-795 Application Note, *AD9880 Color Space Converter User's Guide.*

AUDIO PLL SETUP

Data contained in the audio infoframes (among other registers) defines for the AD9393 HDMI receiver not only the type of audio, but also the sampling frequency (f_S). The audio infoframe also contains information about the N and CTS values used to recreate the clock. With this information, it is possible to regenerate the audio sampling frequency. The audio clock is regenerated by dividing the 20-bit CTS value into the TMDS clock, then multiplying by the 20-bit N value. This yields a multiple of the sampling frequency of either 128 × f_S or 256 × f_S. It is possible for this to be specified up to 1024 × f_S.

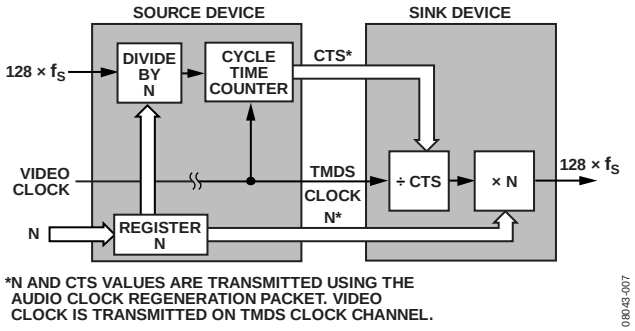

Figure 5. N and CTS for Audio Clock

To provide the most flexibility in configuring the audio sampling clock, an additional PLL is employed. The PLL characteristics are determined by the loop filter design (see Figure 6), the PLL charge pump current, and the VCO range setting.

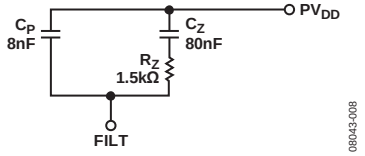

Figure 6. PLL Loop Filter Detail

To fully support all audio modes for all video resolutions up to 1080i, it is necessary to adjust certain audio-related registers from their power-on default values. Table 7 describes these registers and gives the recommended settings.

Table 7. Audio Register Settings

Register	Bits	Recommended Setting	Function	Comments
0x01	[7:0]	0x00	PLL divisor (MSBs)	The video PLL is used for the audio clock circuit when in HDMI mode. This is done automatically.
0x02	[7:4]	0x40	PLL divisor (LSBs)	
0x03	[7:6]	01	VCO range	
	[5:3]	010	Charge pump current	
	[2]	1	PLL enable	In HDMI mode, this bit enables a lower frequency to be used for audio MCLK generation.
0x34	[5:4]	11	Audio frequency mode override	Allows the chip to determine the low frequency mode of the audio PLL.
0x58	[7]	1	MCLK PLL enable	This enables the analog PLL to be used for audio MCLK generation.
	[6:4]	001	MCLK PLL divisor	When the analog PLL is enabled for MCLK generation, another frequency divider is provided; these bits set the divisor to 2.
	[3]	0	N/CTS disable	The N and CTS values should always be enabled.
	[2:0]	0**	MCLK sampling frequency	000 = 128 × f_S 001 = 256 × f_S 010 = 384 × f_S 011 = 512 × f_S

AUDIO BOARD LEVEL MUTING

The audio can be muted through the infoframes or locally via the serial bus registers. This can be controlled with Register 0x57, Bits[7:6].

AVI Infoframes

The HDMI TMDS transmission contains infoframes with specific information for the monitor such as:

- Audio information
  - Two channels to eight channels of audio identified
  - Audio coding
- Audio sampling frequency
- Speaker placement
- N and CTS values (for reconstruction of the audio)
- Muting
- Source information
  - CD
  - SACD
  - DVD
- Video information
  - Video ID code (per CEA861B)
  - Color space
  - Aspect ratio
  - Horizontal and vertical bar information
  - MPEG frame information (I, B, or P frame)
- Vendor (transmitter source) name and product model

This information is the fundamental difference between DVI and HDMI transmissions and is located in the read-only registers Register 0x5A to Register 0xEE. In addition to this information, registers are provided to indicate that new information has been received. Registers with addresses ending in 7 or F beginning with Register 0x87 contain the new data flags (NDF) information. All of these registers contain the same information and all are reset when any of them are read. Although there is no external interrupt signal, it is very easy for the user to read any of the NDF registers to see if there is new information to be processed.

OUTPUT DATA FORMATS

The AD9393 supports 4:4:4, 4:2:2, double data-rate (DDR), and BT656 output formats. Register 0x25[3:0] controls the output mode. These modes and the pin mapping are illustrated in Table 8.

Table 8. Output Formats[1]

	Bits D[23:0]																							
Port	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4:4:4	Red/Cr [7:0]								Green/Y [7:0]								Blue/Cb [7:0]							
4:2:2	CbCr [7:0]								Y [7:0]								DDR 4:2:2 ↑ CbCr ↓ Y, Y							
4:4:4 DDR	DDR ↑ G [3:0]				DDR ↑ B [7:4]				DDR ↑ B [3:0]				DDR 4:2:2 ↑ CbCr [11:0]											
	DDR ↓ R [7:0]								DDR ↓ G [7:4]				DDR 4:2:2 ↓ Y, Y [11:0]											
4:2:2 to 12-bit	CbCr [11:0]												Y [11:0]											

[1] Arrows indicate clock edge. The rising edge of clock = ↑, the falling edge = ↓.

2-WIRE SERIAL REGISTER MAP

The AD9393 is initialized and controlled by a set of registers that determines the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 9. Control Register Map

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x00	Read	[7:0]	00000000	Chip revision	Chip revision ID. Revision is read [7:4] = major revision. [3:0] = minor revision.
0x01	Read/write	[7:0]	01101001	PLL divider MSB	PLL feedback divider value MSB.
0x02	Read/write	[7:4]	1101xxxx	PLL divider LSB	PLL feedback divider value LSB.
0x03	Read/write	[7:6]	01xxxxxx	VCO range	VCO range.
		[5:3]	xx001xxx	Charge pump	Charge pump current control for PLL.
		[2]	xxxxx0xx	PLL enable	This bit enables a lower frequency to be used for audio MCLK generation.
0x11	Read/write	[7:0]	00000000	Reserved	Must be set to 0x00 (default).
0x12	Read/write	[7]	1xxxxxxx	Input HSYNC polarity	0 = active low. 1 = active high.
		[6]	x0xxxxxx	HSYNC polarity override	0 = auto HSYNC polarity. 1 = manual HSYNC polarity.
		[5]	xx1xxxxx	Input VSYNC polarity	0 = active low. 1 = active high.
		[4]	xxx0xxxx	VSYNC polarity override	0 = auto VSYNC polarity. 1 = manual VSYNC polarity.
0x17	Read	[3:0]	xxxx0000	HSYNCs per VSYNC MSB	MSB of HSYNCs per VSYNC.
0x18	Read	[7:0]	00000000	HSYNCs per VSYNC LSB	HSYNCs per VSYNC count.
0x22	Read/write	[7:0]	4	VSYNC duration	VSYNC duration.
0x23	Read/write	[7:0]	32	HSYNC duration	HSYNC duration. Sets the duration of the output HSYNC in pixel clocks.
0x24	Read/write	[7]	1xxxxxxx	HSYNC output polarity	Output HSYNC polarity. 0 = active low output. 1 = active high output.
		[6]	x1xxxxxx	VSYNC output polarity	Output VSYNC polarity. 0 = active low output. 1 = active high output.
		[5]	xx1xxxxx	DE output polarity	Output DE polarity. 0 = negative output. 1 = positive output.
		[4]	xxx1xxxx	Field output polarity	Output field polarity. 0 = active low output. 1 = active high output.
		[0]	xxxxxxx0	Output CLK invert	0 = noninverted clock output. 1 = inverted clock output.
0x25	Read/write	[7:6]	01xxxxxx	Output CLK select	Selects which clock to use on output ball. 1× CLK is divided down from TMDS clock input when pixel repetition is in use. 00 = ½× CLK. 01 = 1× CLK. 10 = 2× CLK. 11 = 90° phase 1× CLK.
		[5:4]	xx11xxxx	Output drive strength	Sets the drive strength of the outputs. 00 = lowest, 11 = highest.
		[3:2]	xxxx00xx	Output mode	Selects the data output mapping. 00 = 4:4:4 mode (normal). 01 = 4:2:2 + DDR 4:2:2 on D[7:0]. 10 = DDR 4:4:4 + DDR 4:2:2 on D[7:0]. 11 = 12-bit 4:2:2.
		[1]	xxxxxx1x	Primary output enable	Enables primary output.
		[0]	xxxxxxx0	Secondary output enable	Enables secondary output (DDR 4:2:2 in Output Mode 1 and Output Mode 2).

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x26	Read/write	[7]	0xxxxxxx	Output three-state	Three-state the outputs.
		[5]	xx0xxxxx	S/PDIF three-state	Three-state the S/PDIF output.
		[4]	xxx0xxxx	I^2S three-state	Three-state the I^2S output and the MCLK output.
		[3]	xxxx1xxx	Power-down ball polarity	Sets polarity of power-down ball. 0 = active low. 1 = active high.
		[2:1]	xxxxx00x	Power-down ball function	Selects the function of the power-down ball. 0x = power-down. 1x = three-state outputs.
		[0]	xxxxxxx0	Power-down	0 = normal. 1 = power-down.
0x27	Read/write	[7]	1xxxxxxx	Auto power-down enable	0 = disable auto low power state. 1 = enable auto low power state.
		[6]	x0xxxxxx	HDCP A0	Sets the LSB of the address of the HDCP I2C. Set to 1 only for a second receiver in a dual-link configuration.
		[5]	xx0xxxxx	Clock test	Must be written to 0.
		[4]	xxx0xxxx	BT656 EN	Enables EAV/SAV codes to be inserted into the video output data.
		[3]	xxxx0xxx	Force DE generation	Allows use of the internal DE generator—not the DE transmitted over TMDS.
		[2:0]	xxxxx000	Interlace offset	Sets the difference (in HSYNCs) in field length between Field 0 and Field 1.
0x28	Read/write	[7:2]	011000xx	VSYNC delay	Sets the delay (in lines) from the VSYNC leading edge to the start of active video.
		[1:0]	xxxxxx01	HSYNC delay MSB	HSYNC delay MSB of Register 0x29.
0x29	Read/write	[7:0]	00000100	HSYNC delay LSB	Sets the delay (in pixels) from the HSYNC leading edge to the start of active video.
0x2A	Read/write	[3:0]	xxxx0101	Line width MSB	Line width MSB of Register 0x2B.
0x2B	Read/write	[7:0]	00000000	Line width LSB	Sets the width of the active video line in pixels.
0x2C	Read/write	[3:0]	xxxx0010	Screen height MSB	Screen height MSB of Register 0x2D.
0x2D	Read/write	[7:0]	11010000	Screen height LSB	Sets the height of the active screen in lines.
0x2E	Read/write	[7]	0xxxxxxx	CTRL EN	Allows CTRL[3:0] to be output on the I^2S data pins.
		[6:5]	x00xxxxx	I^2S output mode	00 = I^2S mode. 01 = right-justified. 10 = left-justified. 11 = raw IEC60958 mode.
		[4:0]	xxx11000	I^2S bit width	Sets the desired bit width for right-justified mode.
0x2F	Read	[6]	x0xxxxxx	TMDS sync detect	Detects a TMDS DE.
		[5]	xx0xxxxx	TMDS active	Detects a TMDS clock.
		[4]	xxx0xxxx	AV mute	Gives the status of AV mute based on general control packets.
		[3]	xxxx0xxx	HDCP keys read	Returns 1 when read of EEPROM keys is successful.
		[2:0]	xxxxx000	HDMI quality	Returns quality number based on DE edges.
0x30	Read	[6]	x0xxxxxx	HDMI content encrypted	This bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Use this bit to allow copying of the content. The bit should be sampled at regular intervals because it can change on a frame-by-frame basis.
		[5]	xx0xxxxx	HDMI HSYNC polarity	Returns HDMI HSYNC polarity.
		[4]	xxx0xxxx	HDMI VSYNC polarity	Returns HDMI VSYNC polarity.
		[3:0]	xxxx0000	HDMI pixel repetition	Returns current HDMI pixel repetition amount. 0 = 1×, 1 = 2× … The clock and data outputs are automatically decimated by this value.

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x34	Read/write	[5:4]	xx00xxxx	Audio setup	Must be written to 0b11 for proper operation.
		[3]	xxxx0xxx	Upconversion mode	0 = repeat Cr and Cb values. 1 = interpolate Cr and Cb values.
		[2]	xxxxx0xx	CrCb filter enable	Enables the FIR filter for 4:2:2 CrCb output.
		[1]	xxxxxx0x	CSC_ENABLE	Enables the color space converter (CSC). The default settings for the CSC provide HDTV-to-RGB conversion. Sets the fixed point position of the CSC coefficients, including the A4, B4, and C4 offsets.
0x35	Read/write	[6:5]	x01xxxxx	CSC_MODE	00 = ±1.0, −4096 to +4095. 01 =±2.0, −8192 to +8190. 1x = ±4.0, −16,384 to +16,380.
		[4:0]	xxx01100	CSC_COEFF_A1 MSB	MSB of Register 0x36.
0x36	Read/write	[7:0]	01010010	CSC_COEFF_A1 LSB	Color space converter (CSC) coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x37	Read/write	[4:0]	xxx01000	CSC_COEFF_A2 MSB	MSB of Register 0x38.
0x38	Read/write	[7:0]	00000000	CSC_COEFF_A2 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x39	Read/write	[4:0]	xxx00000	CSC_COEFF_A3 MSB	MSB of Register 0x3A.
0x3A	Read/write	[7:0]	00000000	CSC_COEFF_A3 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x3B	Read/write	[4:0]	xxx11001	CSC_COEFF_A4 MSB	MSB of Register 0x3C.
0x3C	Read/write	[7:0]	11010111	CSC_COEFF_A4 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x3D	Read/write	[4:0]	xxx11100	CSC_COEFF_B1 MSB	MSB of Register 0x3E.
0x3E	Read/write	[7:0]	01010100	CSC_COEFF_B1 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x3F	Read/write	[4:0]	***01000	CSC_COEFF_B2 MSB	MSB of Register 0x40.
0x40	Read/write	[7:0]	00000000	CSC_COEFF_B2 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x41	Read/write	[4:0]	xxx11110	CSC_COEFF_B3 MSB	MSB of Register 0x42.
0x42	Read/write	[7:0]	10001001	CSC_COEFF_B3 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x43	Read/write	[4:0]	xxx00010	CSC_COEFF_B4 MSB	MSB of Register 0x44.
0x44	Read/write	[7:0]	10010010	CSC_COEFF_B4 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x45	Read/write	[4:0]	xxx00000	CSC_COEFF_C1 MSB	MSB of Register 0x46.
0x46	Read/write	[7:0]	00000000	CSC_COEFF_C1 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x47	Read/write	[4:0]	xxx01000	CSC_COEFF_C2 MSB	MSB of Register 0x48.
0x48	Read/write	[7:0]	00000000	CSC_COEFF_C2 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x49	Read/write	[4:0]	xxx01110	CSC_COEFF_C3 MSB	MSB of Register 0x4A.
0x4A	Read/write	[7:0]	10000111	CSC_COEFF_C3 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x4B	Read/write	[4:0]	xxx11000	CSC_COEFF_C4 MSB	MSB of Register 0x4C.
0x4C	Read/write	[7:0]	10111101	CSC_COEFF_C4 LSB	CSC coefficient for equation: $R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$ $G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$ $B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$
0x4D	Read/write	[7:0]	00110110	TMDS PLL Control1	Must be written to 0x3B.
0x4E	Read/write	[7:0]	00110110	TMDS PLL Control2	Must be written to 0x6D.
0x4F	Read/write	[7:0]	00110110	TMDS PLL Control3	Must be written to 0x54.
0x50	Read/write	[7:0]	00100000	Test	Must be written to 0x20 for proper operation.
0x56	Read/write	[7:0]	00001111	Test	Must be written to 0x0F (default) for proper operation.
0x57	Read/write	[7]	0xxxxxxx	AV mute override	A1 overrides the AV mute value with Bit 6.
		[6]	x0xxxxxx	AV mute value	Sets AV mute value if override is enabled.
		[3]	xxxx0xxx	Disable video mute	Disables mute of video during AV mute.
		[2]	xxxxx0xx	Disable audio mute	Disables mute of audio during AV mute.
0x58	Read/write	[7]	0	MCLK PLL enable	MCLK PLL enable—uses analog PLL.
		[6:4]	0	MCLK PLL_N	MCLK PLL_N [2:0]—this controls the division of the MCLK out of the PLL: 0 = /1, 1 = /2, 2 = /3, 3 = /4 …
		[3]	0	N_CTS_DISABLE	Prevents the N/CTS packet on the link from writing to the N and CTS registers.
		[2:0]	0	MCLK FS_N	Controls the multiple of 128 f_S used for MCLK out. 0 = 128 × f_S, 1 = 256 × f_S, 2 = 384 × f_S, 7 = 1024 × f_S.
0x59	Read/write	[6]	0	MDA/MCL PU	This disables the MDA/MCL pull-ups.
		[5]	0	CLK term O/R	Clock termination power-down override: 0 = auto, 1 = manual.
		[4]	0	Manual CLK term	Clock termination: 0 = normal, 1 = disconnected.
		[2]	0	FIFO reset UF	This bit resets the audio FIFO if underflow is detected.
		[1]	0	FIFO reset OF	This bit resets the audio FIFO if overflow is detected.
		[0]	0	MDA/MCL three-state	This bit three-states the MDA/MCL lines.
0x5A	Read	[6:0]	0	Packet detected	These seven bits are updated if any specific packet has been received since last reset or loss of clock detect. Normal is 0x00.
					Bit / **Data Packet Detected** 0 / AVI infoframe. 1 / Audio infoframe. 2 / SPD infoframe. 3 / MPEG source infoframe. 4 / ACP packets. 5 / ISRC1 packets. 6 / ISRC2 packets.
0x5B	Read	[3]	0	HDMI mode	0 = DVI, 1 = HDMI.

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x5E	Read	[7:6]	0	Channel status	Mode = 00. All others are reserved.
		[5:3]	0	PCM audio data	When Bit 1 = 0 (linear PCM): 000 = two audio channels without pre-emphasis. 001 = two audio channels with 50 µs/15 µs pre-emphasis. 010 = reserved. 011 = reserved.
		[2]	0	Copyright information	0 = software for which copyright is asserted. 1 = software for which no copyright is asserted.
		[1]	0	Linear PCM identification	0 = audio sample word represents linear PCM samples. 1 = audio sample word used for other purposes.
		[0]	0	Use of channel status block	0 = consumer use of channel status block.
Audio Channel Status					
0x5F	Read	[7:0]	0	Channel status category code	Per HDMI
0x60	Read	[7:4]	0	Channel number	Per HDMI
		[3:0]	0	Source number	Per HDMI
0x61	Read	[5:4]	0	Clock accuracy	Clock accuracy. 00 = Level II. 01 = Level III. 10 = Level I. 11 = reserved.
		[3:0]	0	Sampling frequency	0011 = 32 kHz. 0000 = 44.1 kHz. 1000 = 88.2 kHz. 1100 = 176.4 kHz. 0010 = 48 kHz. 1010 = 96 kHz. 1110 = 192 kHz.
0x62	Read	[3:0]	0	Word length	Word length. 0000 = not specified. 0100 = 16 bits. 0011 = 17 bits. 0010 = 18 bits. 0001 = 19 bits. 0101 = 20 bits. 1000 = not specified. 1100 = 20 bits. 1011 = 21 bits. 1010 = 22 bits. 1001 = 23 bits. 1101 = 24 bits.
0x7B	Read	[7:0]	0	CTS[19:12]	Cycle time stamp. This 20-bit value is used with the N value to regenerate an audio clock. For the remaining bits, see Register 0x7C and Register 0x7D.
0x7C	Read	[7:0]	0	CTS[11:4]	See Register 0x7B
0x7D	Read	[7:4]	0	CTS[3:0]	See Register 0x7B
	Read	[3:0]	0	N[19:16]	20-bit N used with CTS to regenerate the audio clock. For remaining bits, see Register 0x7E and Register 0x7F.
0x7E	Read	[7:0]	0	N[15:8]	See Register 0x7D
0x7F	Read	[7:0]	0	N[7:0]	See Register 0x7D
AVI Infoframe					
0x80	Read	[7:0]	0	AVI infoframe version	

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x81	Read	[6:5]	0	Y[1:0]	Y[1:0] indicates RGB, 4:2:2, or 4:4:4. 00 = RGB. 01 = YCrCb 4:2:2. 10 = YCrCb 4:4:4.
		[4]	0	Active format information status	Active format information present. 0 = no data. 1 = active format information valid.
		[3:2]	0	Bar information	B[1:0]. 00 = no bar information. 01 = horizontal bar information valid. 10 = vertical bar information valid. 11 = horizontal and vertical bar information valid.
		[1:0]	0	Scan information	S[1:0]. 00 = no information. 01 = overscanned (television). 10 = underscanned (computer).
0x82	Read	[7:6]	0	Colorimetry	C[1:0]. 00 = no data. 01 = SMPTE 170M, ITU601. 10 = ITU709.
		[5:4]	0	Picture aspect ratio	M[1:0]. 00 = no data. 01 = 4:3. 10 = 16:9.
		[3:0]	0	Active format aspect ratio	R[3:0]. 1000 = same as picture aspect ratio. 1001 = 4:3 (center). 1010 = 16:9 (center). 1011 = 14:9 (center).
0x83	Read	[1:0]	0	Nonuniform picture scaling	SC[1:0]. 00 = no known nonuniform scaling. 01 = picture has been scaled horizontally. 10 = picture has been scaled vertically. 11 = picture has been scaled horizontally and vertically.
0x84	Read	[6:0]	0	Video identification code	VIC[6:0] video identification code—refer to CEA EDID short video descriptors.
0x85	Read	[3:0]	0	Pixel repeat	PR[3:0] specifies how many times a pixel has been repeated. 0000 = no repetition (pixel sent once). 0001 = pixel sent twice (repeated once). 0010 = pixel sent three times. 1001 = pixel sent 10 times. 0xA to 0xF reserved.
0x86	Read	[7:0]	0	Active line start LSB	This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar. Combines with Register 0x88 for a 16-bit value.
0x87	Read	[6:0]	0	New data flags	New data flags. These eight bits are updated if any specific data changes. Normal (no NDFs) is 0x00. When any NDF register is read, all bits reset to 0x00. All NDF registers contain the same data.

Bit	Data Packet Changed
0	AVI infoframe.
1	Audio infoframe.
2	SPD infoframe.
3	MPEG source infoframe.
4	ACP packets.
5	ISRC1 packets.
6	ISRC2 packets.

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x88	Read	[7:0]	0	Active line start MSB	Active line start MSB (see Register 0x86).
0x89	Read	[7:0]	0	Active line end LSB	This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar. Combines with Register 0x8A for a 16-bit value.
0x8A	Read	[7:0]	0	Active line end MSB	Active line end MSB. See Register 0x89.
0x8B	Read	[7:0]	0	Active pixel start LSB	This represents the last pixel in a vertical pillar bar at the left side of the picture. If 0, there is no left bar. Combines with Register 0x8C for a 16-bit value.
0x8C	Read	[7:0]	0	Active pixel start MSB	Active pixel start MSB. See Register 0x8B.
0x8D	Read	[7:0]	0	Active pixel end LSB	This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar. Combines with Register 0x8E for a16-bit value.
0x8E	Read	[7:0]	0	Active pixel end MSB	Active pixel end MSB. See Register 0x8D.
0x8F	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0x90	Read	[7:0]	0	Audio infoframe version	Per HDMI
0x91	Read	[7:4]	0	Audio coding type	CT[3:0]. Audio coding type. 0x00 = refer to stream header. 0x01 = IEC60958 PCM. 0x02 = AC3. 0x03 = MPEG1 (Layer 1 and Layer 2). 0x04 = MP3 (MPEG1 Layer 3). 0x05 = MPEG2 (multichannel). 0x06 = AAC. 0x07 = DTS. 0x08 = ATRAC.
		[2:0]	0	Audio coding count	CC[2:0]. Audio channel count. 000 = refer to stream header. 001 = two channels. 010 = three channels. 111 = eight channels.
0x92	Read	[4:2]	0	Sampling frequency	SF[2:0]. Sampling frequency. 000 = refer to stream header. 001 = 32 kHz. 010 = 44.1 kHz (CD). 011 = 48 kHz. 100 = 88.2 kHz. 101 = 96 kHz. 110 = 176.4 kHz. 111 = 192 kHz.
		[1:0]	0	Sample size	SS [1:0]. Sample size. 00 = refer to stream header. 01 = 16 bits. 10 = 20 bits. 11 = 24 bits.
0x93	Read	[7:0]	0	Maximum bit rate	Maximum bit rate (compressed audio only). The value of this field multiplied by 8 kHz represents the maximum bit rate.
0x94	Read	[7:0]	0	Speaker mapping	CA[7:0]. Speaker mapping or placement for up to eight channels. See Table 24.
0x95	Read	[7]	0	Down-mix	DM_INH: down-mix inhibit. 0 = permitted or no information. 1 = prohibited.
		[6:3]	0	Level shift	LSV[3:0]: level shift values with attenuation information. 0000 = 0 dB attenuation. 0001 = 1 dB attenuation. . . . 1111 = 15 dB attenuation.

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0x96	Read	[7:0]	0		Reserved.
0x97	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
Source Product Description (SPD) Infoframe					
0x98	Read	[7:0]	0	Source product description (SPD) infoframe version	Per HDMI
0x99	Read	[7:0]	0	Vender Name Character 1	Vender name character 1 (VN1) 7-bit ASCII code. The first of eight characters naming the product company.
0x9A	Read	[7:0]	0	VN2	VN2.
0x9B	Read	[7:0]	0	VN3	VN3.
0x9C	Read	[7:0]	0	VN4	VN4.
0x9D	Read	[7:0]	0	VN5	VN5.
0x9E	Read	[7:0]	0	VN6	VN6.
0x9F	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xA0	Read	[7:0]	0	VN7	VN7.
0xA1	Read	[7:0]	0	VN8	VN8.
0xA2	Read	[7:0]	0	Product Description Character 1	Product Description Character 1 (PD1) 7-bit ASCII code. The first of 16 characters that contains the model number and a short description.
0xA3	Read	[7:0]	0	PD2	PD2.
0xA4	Read	[7:0]	0	PD3	PD3.
0xA5	Read	[7:0]	0	PD4	PD4.
0xA6	Read	[7:0]	0	PD5	PD5.
0xA7	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xA8	Read	[7:0]	0	PD6	PD6.
0xA9	Read	[7:0]	0	PD7	PD7.
0xAA	Read	[7:0]	0	PD8	PD8.
0xAB	Read	[7:0]	0	PD9	PD9.
0xAC	Read	[7:0]	0	PD10	PD10.
0xAD	Read	[7:0]	0	PD11	PD11.
0xAE	Read	[7:0]	0	PD12	PD12.
0xAF	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xB0	Read	[7:0]	0	PD13	PD13.
0xB1	Read	[7:0]	0	PD14	PD14.
0xB2	Read	[7:0]	0	PD15	PD15.
0xB3	Read	[7:0]	0	PD16	PD16.
0xB4	Read	[7:0]	0	Source device Information code	This is a code that classifies the source device. 0x00 = unknown. 0x01 = digital STB. 0x02 = DVD. 0x03 = D-VHS. 0x04 = HDD video. 0x05 = DVC. 0x06 = DSC. 0x07 = video CD. 0x08 = game. 0x09 = PC general.
0xB7	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
MPEG Source Infoframe					
0xB8	Read	[7:0]	0	MPEG source infoframe version	
0xB9	Read	[7:0]	0	MB[0]	MB[0] (lower byte of MPEG bit rate in hertz). This is the lower eight bits of 32 bits (4 bytes) that specify the MPEG bit rate in hertz.
0xBA	Read	[7:0]	0	MB[1]	MB[1].
0xBB	Read	[7:0]	0	MB[2]	MB[2].
0xBC	Read	[7:0]	0	MB[3]	MB[3] (upper byte).

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0xBD	Read	[4]	0	Field repeat	FR—new field or repeated field. 0 = new field or picture. 1 = repeated field.
		[1:0]	0	MPEG frame	MF[1:0]. This identifies whether frame is an I, B, or P picture. 00 = unknown. 01 = I picture. 10 = B picture. 11 = P picture.
0xBE	Read	[7:0]	0		Reserved.
0xBF	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xC0	Read	[7:0]	0	Audio content protection packet (ACP) type	Audio content protection packet (ACP) type. 0x00 = generic audio. 0x01 = IEC60958-identified audio. 0x02 = DVD audio. 0x03 = reserved for super audio CD (SACD). 0x04 to 0xFF = reserved.
0xC1	Read	[7:0]	0	ACP Packet Byte 0	ACP Packet Byte 0 (ACP_PB0).
0xC2	Read	[7:0]	0	ACP_PB1	ACP_PB1.
0xC3	Read	[7:0]	0	ACP_PB2	ACP_PB2.
0xC4	Read	[7:0]	0	ACP_PB3	ACP_PB3.
0xC5	Read	[7:0]	0	ACP_PB4	ACP_PB4.
0xC6	Read	[7:0]	0	ACP_PB5	ACP_PB5.
0xC7	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xC8	Read	[7]	0	ISRC1 continued	International standard recording code (ISRC1) continued. This indicates an ISRC2 packet is being transmitted.
		[6]	0	ISRC1 valid	0 = ISRC1 status bits and PBs not valid. 1 = ISRC1 status bits and PBs valid.
		[2:0]	0	ISRC1 status	001 = starting position. 010 = intermediate position. 100 = final position.
0xC9	Read	[7:0]	0	ISRC1 Packet Byte 0	ISRC1 Packet Byte 0 (ISRC1_PB0).
0xCA	Read	[7:0]	0	ISRC1_PB1	ISRC1_PB1.
0xCB	Read	[7:0]	0	ISRC1_PB2	ISRC1_PB2.
0xCC	Read	[7:0]	0	ISRC1_PB3	ISRC1_PB3.
0xCD	Read	[7:0]	0	ISRC1_PB4	ISRC1_PB4.
0xCE	Read	[7:0]	0	ISRC1_PB5	ISRC1_PB5.
0xCF	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xD0	Read	[7:0]	0	ISRC1_PB6	ISRC1_PB6.
0xD1	Read	[7:0]	0	ISRC1_PB7	ISRC1_PB7.
0xD2	Read	[7:0]	0	ISRC1_PB8	ISRC1_PB8.
0xD3	Read	[7:0]	0	ISRC1_PB9	ISRC1_PB9.
0xD4	Read	[7:0]	0	ISRC1_PB10	ISRC1_PB10.
0xD5	Read	[7:0]	0	ISRC1_PB11	ISRC1_PB11.
0xD6	Read	[7:0]	0	ISRC1_PB12	ISRC1_PB12.
0xD7	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xD8	Read	[7:0]	0	ISRC1_PB13	ISRC1_PB13.
0xD9	Read	[7:0]	0	ISRC1_PB14	ISRC1_PB14.
0xDA	Read	[7:0]	0	ISRC1_PB15	ISRC1_PB15.
0xDB	Read	[7:0]	0	ISRC1_PB16	ISRC1_PB16.
0xDC	Read	[7:0]	0	ISRC2 Packet Byte 0	ISRC2 Packet Byte 0 (ISRC2_PB0). This is transmitted only when the ISRC bit continues (Register 0xC8, Bit[7]) is set to 1.
0xDD	Read	[7:0]	0	ISRC2_PB1	ISRC2_PB1.
0xDE	Read	[7:0]	0	ISRC2_PB2	ISRC2_PB2.
0xDF	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xE0	Read	[7:0]	0	ISRC2_PB3	ISRC2_PB3.
0xE1	Read	[7:0]	0	ISRC2_PB4	ISRC2_PB4.
0xE2	Read	[7:0]	0	ISRC2_PB5	ISRC2_PB5.

Hex Address	Read/Write	Bits	Default Value	Register Name	Description
0xE3	Read	[7:0]	0	ISRC2_PB6	ISRC2_PB6.
0xE4	Read	[7:0]	0	ISRC2_PB7	ISRC2_PB7.
0xE5	Read	[7:0]	0	ISRC2_PB8	ISRC2_PB8.
0xE6	Read	[7:0]	0	ISRC2_PB9	ISRC2_PB9.
0xE7	Read	[6:0]	0	New data flags	New data flags (see Register 0x87).
0xE8	Read	[7:0]	0	ISRC2_PB10	ISRC2_PB10.
0xE9	Read	[7:0]	0	ISRC2_PB11	ISRC2_PB11.
0xEA	Read	[7:0]	0	ISRC2_PB12	ISRC2_PB12.
0xEB	Read	[7:0]	0	ISRC2_PB13	ISRC2_PB13.
0xEC	Read	[7:0]	0	ISRC2_PB14	ISRC2_PB14.
0xED	Read	[7:0]	0	ISRC2_PB15	ISRC2_PB15.
0xEE	Read	[7:0]	0	ISRC2_PB16	ISRC2_PB16.

2-WIRE SERIAL CONTROL REGISTER DETAILS

This section describes certain register details. Note that not all registers are discussed in this section.

CHIP IDENTIFICATION

0x00—Bits[7:0], Chip Revision

An 8-bit value that reflects the current chip revision.

0x17—Bits[3:0], HSYNCs per VSYNC MSB

These bits are four MSBs of the 12-bit counter that reports the number of HSYNCs per VSYNC on the active input. This is useful in determining the mode and aid in setting the PLL divide ratio.

0x18—Bit[7:0], HSYNCs per VSYNC LSB

These bits are eight LSBs of the 12-bit counter that reports the number of HSYNCs per VSYNCs on the active input.

0x23—Bits[7:0], HSYNC Duration

These bits are an 8-bit register that sets the duration of the HSYNC output pulse. The leading edge of the HSYNC output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9393 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the HSYNC output, which is also phase-adjusted. The power-up default is 32.

0x24—Bit[7], HSYNC Output Polarity

This bit sets the polarity of the HSYNC output. Setting this bit to 0 sets the HSYNC output to active low. Setting this bit to 1 sets the HSYNC output to active high. The power-up default setting is 1.

0x24—Bit[6], VSYNC Output Polarity

This bit sets the polarity of the VSYNC output. Setting this bit to 0 sets the VSYNC output to active low. Setting this bit to 1 sets the VSYNC output to active high. The power-up default is 1.

0x24—Bit[5] DE Output Polarity

This bit sets the polarity of the display enable (DE). 0 = DE output polarity is negative. 1 = DE output polarity is positive. The power-up default is 1.

0x24—Bit[4], Field Output Polarity

This bit sets the polarity of the odd/even field output signal on Ball A7. 0 = active low = even field; active high = odd field. 1 = active high = odd field; active high = even field. The power-up default setting is 1.

0x24—Bit[0], Output CLK Invert

This bit allows inversion of the output clock as specified by Register 0x25, Bits[7:6]. 0 = noninverted clock. 1 = inverted clock. The power-up default setting is 0.

0x25—Bits[7:6], Output CLK Select

These bits select the clock output on the DCLK ball. They include ½× clock, a 2× clock, a 90° phase shifted clock, or the normal pixel clock. The power-up default setting is 01. See Table 10.

Table 10. Output Clock Select

Select	Result
00	½× pixel clock
01	1× pixel clock
10	2× pixel clock
11	90° phase 1× pixel clock

0x25—Bits[5:4], Output Drive Strength

These two bits select the drive strength for all the high speed digital outputs (except the VSOUT, HSOUT, and O/E). Higher drive strength results in faster rise/fall times and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps to reduce EMI and digitally generated power supply noise. The power-up default setting is 11. See Table 11.

Table 11. Output Drive Strength

Output Drive	Result
00	Low output drive strength
01	Medium low output drive strength
10	Medium high output drive strength
11	High output drive strength

0x25—Bits[3:2], Output Mode

These bits choose between four options for the output mode. 4:4:4 mode is standard RGB; 4:2:2 mode is YCrCb, which reduces the number of active output pins from 24 to 16; 4:4:4 is double data rate (DDR) output mode; and the data is RGB mode that changes on every clock edge. The power-up default setting is 00. See Table 12.

Table 12. Output Mode

Output Mode	Result
00	4:4:4 RGB mode
01	4:2:2 YCrCb mode + DDR 4:2:2 on D[7:0] (secondary)
10	DDR 4:4:4 DDR mode + DDR 4:2:2 on D[7:0] (secondary)
11	12-bit 4:2:2

0x25—Bit[1], Primary Output Enable

This bit places the primary output in active or high impedance mode. The primary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes, the data on the red and green output channels (D[23:8]) is the primary output, whereas the output data on the blue channel (D[7:0], DDR YCrCb) is the secondary output. Double data rate 0 = primary output is in high impedance mode. 1 = primary output is enabled. The power-up default setting is 1.

0x25—Bit[0], Secondary Output Enable

This bit places the secondary output in active or high impedance mode. The secondary output is designated when using either 4:2:2 or DDR 4:4:4. In these modes, the data on the blue output channel (D[7:0]) is the secondary output and the output data on the red and green channels (D[23:8]) is the primary output. Secondary output is always a DDR YCrCb data mode. 0 = secondary output is in high impedance mode. 1 = secondary output is enabled. The power-up default setting is 0.

0x26—Bit[7], Output Three-State

When enabled, this bit puts all outputs in a high impedance state. 0 = normal outputs. 1 = all outputs in high impedance mode. The power-up default setting is 0.

0x26—Bit[5], S/PDIF Three-State

When enabled, this bit places the S/PDIF audio output pins in a high impedance state. 0 = normal S/PDIF output. 1 = S/PDIF pins in high impedance mode. The power-up default setting is 0.

0x26—Bit[4], I²S Three-State

When enabled, this bit places the I^2S output pins in a high impedance state. 0 = normal I^2S output. 1 = I^2S pins are in high impedance mode. The power-up default setting is 0.

0x26—Bit[3], Power-Down Ball Polarity

This bit defines the polarity of the input power-down ball. 0 = power-down ball is active low. 1 = power-down ball is active high. The power-up default setting is 1.

0x26—Bits[2:1], Power-Down Ball Function

These bits define the different operational modes of the power-down ball. These bits are functional only when the power-down ball is active; when it is inactive, the part is powered up and functioning. 0x = the chip is powered down and all outputs are in high impedance mode. 1x = the chip remains powered up, but all outputs are in three-state outputs mode. The power-up default setting is 00.

0x26—Bit[0], Power-Down

This bit is used to put the chip in power-down mode. In this mode, the power dissipation is reduced to a fraction of the typical power (see Table 2 for exact power dissipation). When in power-down, the HSOUT, VSOUT, DCLK, and all 24 of the data outputs are put into a high impedance state. Circuit blocks that continue to be active during power-down include the voltage references, sync detection, and the serial register. These blocks facilitate a fast start up from power-down. 0 = normal operation. 1 = power-down. The power-up default setting is 0.

0x27—Bit[7], Auto Power-Down Enable

This bit enables the chip to go into low power mode, or seek mode if no sync inputs are detected. 0 = auto power-down disabled. 1 = chip powers down if no sync inputs are present. The power-up default setting is 1.

0x27—Bit[6], HDCP A0

This bit sets the LSB of the address of the HDCP I^2C. Set this bit to 1 only for a second receiver in a dual-link configuration. The power-up default is 0.

0x27—Bit[5], Clock Test

The power-up default setting is 0.

BT656 GENERATION

0x27—Bit[4], BT656 EN

This bit enables the output to be BT656-compatible with the defined start of active video (SAV) and the end of active video (EAV) controls to be inserted. These require specification of the number of active lines, active pixels per line, and delays to place these markers. 0 = disable BT656 video mode. 1 = enable BT656 video mode. The power-up default setting is 0.

0x27—Bit[3], Force DE Generation

This bit allows the use of the internal DE generator in DVI mode. 0 = internal DE generation disabled. 1 = force DE generation via programmed registers. The power-up default setting is 0.

0x27—Bits[2:0], Interlace Offset

These bits define the offset in HSYNCs from Field 0 to Field 1. The power-up default setting is 000.

0x28—Bits[7:2], VSYNC Delay

These bits set the delay (in lines) from the leading edge of VSYNC to active video. The power-up default setting is 24d.

0x28—Bits[1:0], HSYNC Delay MSB and 0x29—Bits[7:0], HSYNC Delay LSB

These 10 bits set the delay (in pixels) from the HSYNC leading edge to the start of active video. The power-up default setting is 0x104.

0x2A—Bits[3:0], Line Width MSB and 0x2B—Bits[7:0] Line Width LSB

These 12 bits set the width of the active video line (in pixels). The power-up default setting is 0x500.

0x2C—Bits[3:0], Screen Height MSB and 0x2D—Bits[7:0] Screen Height LSB

These 12 bits set the height of the active screen (in lines). The power-up default setting is 0x2D0.

0x2E—Bit[7], CTRL EN

When set, this bit allows CTRL[3:0] signals decoded from the DVI to be output on the I^2S data pins. 0 = I^2S signals on I^2S lines. 1 = CTRL[3:0] output on I^2S lines. The power-up default setting is 0.

0x2E—Bits[6:5], I^2S Output Mode

These bits select between four options for the I^2S output: I^2S, right-justified, left-justified, or raw IEC60958 mode. The power-up default setting is 00. See Table 13.

Table 13. I^2S Output Select

I^2S Output Mode	Result
00	I^2S mode
01	Right-justified
10	Left-justified
11	Raw IEC60958 mode

0x2E—Bits[4:0], I^2S Bit Width

These bits set the I^2S bit width for right-justified mode. The power-up default setting is 24 bits.

0x2F—Bit[6], TMDS Sync Detect

This read-only bit indicates the presence of a TMDS DE. 0 = no TMDS DE present. 1 = TMDS DE detected.

0x2F—Bit[5], TMDS Active

This read-only bit indicates the presence of a TMDS clock. 0 = no TMDS clock present. 1 = TMDS clock detected.

0x2F—Bit[4], AV Mute

This read-only bit indicates the presence of AV mute based on general control packets. 0 = AV not muted. 1 = AV muted.

0x2F—Bit[3], HDCP Keys Read

This read-only bit reports if the HDCP keys were read successfully. 0 = failure to read HDCP keys. 1 = HDCP keys read.

0x2F—Bits[2:0], HDMI Quality

These read-only bits indicate a level of HDMI quality based on the DE (display enable) edges. A larger number indicates a higher quality.

0x30—Bit[6], HDMI Content Encrypted

This read-only bit is high when HDCP decryption is in use (content is protected). The signal goes low when HDCP is not being used. Use this bit to to allow copying of the content. Sample the bit at regular intervals because it can change on a frame-by-frame basis. 0 = HDCP not in use. 1 = HDCP decryption in use.

0x30—Bit[5], HDMI HSYNC Polarity

This read-only bit indicates the polarity of the HDMI HSYNC. 0 = HDMI HSYNC polarity is active low. 1 = HDMI HSYNC polarity is active high.

0x30—Bit[4], HDMI VSYNC Polarity

This read-only bit indicates the polarity of the HDMI VSYNC. 0 = HDMI VSYNC polarity is low active. 1 = HDMI VSYNC polarity is high active.

0x30—Bits[3:0], HDMI Pixel Repetition

These read-only bits indicate the pixel repetition on HDMI. 0 = 1×, 1 = 2×, 2 = 3×, with a maximum repetition of 10× (0x9). See Table 14.

Table 14.

Select	Repetition Multiplier
0000	1×
0001	2×
0010	3×
0011	4×
0100	5×
0101	6×
0110	7×
0111	8×
1000	9×
1001	10×

0x34—Bit[5:4], Audio Setup

This bit must be written to 0b11 for proper audio operation.

0x34—Bit[3], Up Conversion Mode

0 = repeat Cb and Cr values. 1 = interpolate Cb and Cr values.

0x34—Bit[2], CrCb Filter Enable

Enables the FIR filter for 4:2:2 CrCb output.

COLOR SPACE CONVERSION

The default power up values for the color space converter coefficients (Register 0x34 through Register 0x4C) are set for ATSC RGB-to-YCrCb conversion. They are completely programmable for other conversions.

0x34—Bit[1], CSC_ENABLE

This bit enables the color space converter. 0 = disable color space converter. 1 = enable color space converter. The power-up default setting is 0.

0x35—Bits[6:5], CSC_MODE

These two bits set the fixed-point position of the CSC coefficients, including the A4, B4, and C4 offsets.

Table 15. CSC Fixed Point Converter Mode

Select	Result
00	±1.0, −4096 to +4095
01	±2.0, −8192 to +8190
1x	±4.0, −16,384 to +16,380

0x35—Bits[4:0], CSC_COEFF_A1 MSB and 0x36—Bits[7:0], CSC_COEFF_A1 LSB

Register 0x35[4:0] form the five MSBs of the Color Space Conversion Coefficient A1. These bits, combined with the eight LSBs of Register 0x36 form a 13-bit, twos complement coefficient, which is user programmable. The equation takes the form of:

$$R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$$
$$G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$$
$$B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$$

The default value for the 13-bit A1 coefficient is 0x0C52.

0x37—Bits[4:0], CSC_COEFF_A2 MSB and 0x38—Bits[7:0], CSC _COEFF_A2 LSB

Register 0x37[4:0] form the five MSBs of the Color Space Conversion Coefficient A2. Combined with the eight LSBs of Register 0x38, these bits form a 13-bit, twos complement coefficient that is user programmable. The equation takes the form of:

$$R_{OUT} = (A1 \times R_{IN}) + (A2 \times G_{IN}) + (A3 \times B_{IN}) + A4$$
$$G_{OUT} = (B1 \times R_{IN}) + (B2 \times G_{IN}) + (B3 \times B_{IN}) + B4$$
$$B_{OUT} = (C1 \times R_{IN}) + (C2 \times G_{IN}) + (C3 \times B_{IN}) + C4$$

The default value for the 13-bit A2 coefficient is 0x0800.

0x39—Bits[4:0], CSC_COEFF_A3 MSB and 0x3A—Bits[7:0], CSC_COEFF_A3 LSB

The default value for the 13-bit A3 is 0x00000.

0x3B—Bits[4:0], CSC_COEFF_A4 MSB and 0x3C—Bits[7:0], CSC_COEFF_A4 LSB

The default value for the 13-bit A4 is 0x19D7.

0x3D—Bits[4:0], CSC_COEFF_B1 MSB and 0x3E—Bits[7:0], CSC_COEFF_B1 LSB

The default value for the 13-bit B1 is 0x1C54.

0x3F—Bits[4:0], CSC_COEFF_B2 MSB and 0x40—Bits[7:0], CSC_COEFF_B2 LSB

The default value for the 13-bit B2 is 0x0800.

0x41—Bits[4:0], CSC_COEFF_B3 MSB and 0x42—Bits[7:0], CSC_COEFF_B3 LSB

The default value for the 13-bit B3 is 0x1E89.

0x43—Bits[4:0], CSC_COEFF_B4 MSB and 0x44—Bits[7:0], CSC_COEFF_B4 LSB

The default value for the 13-bit B4 is 0x0291.

0x45—Bits[4:0], CSC_COEFF_C1 MSB and 0x46—Bits[7:0], CSC_COEFF_C1 LSB

The default value for the 13-bit C1 is 0x0000.

0x47—Bits[4:0], CSC_COEFF_C2 MSB and 0x48—Bits[7:0], CSC_COEFF_C2 LSB

The default value for the 13 bit C2 is 0x0800.

0x49—Bits[4:0], CSC_COEFF_C3 MSB and 0x4A—Bits[7:0], CSC_COEFF_C3 LSB

The default value for the 13-bit C3 is 0x0E87.

0x4B—Bits[4:0], CSC_COEFF_C4 MSB and 0x4C—Bits[7:0], CSC_COEFF_C4 LSB

The default value for the 13-bit C4 is 0x18BD.

0x58—Bit[7], MCLK PLL Enable

This bit enables the use of the analog PLL.

0x58—Bits[6:4], MCLK PLL_N

These bits control the division of the MCLK out of the PLL. See Table 16.

Table 16.

MCLK PLL_N [2:0]	MCLK Divide Value
0	/1
1	/2
2	/3
3	/4
4	/5
5	/6
6	/7
7	/8

0x58—Bit[3], N_CTS_Disable

This bit prevents the N/CTS packet on the link from writing to the N and CTS registers.

0x58—Bits[2:0], MCLK FS_N

These bits control the multiple of 128 f_S used for MCLK out. See Table 17.

Table 17.

MCLK FS_N [2:0]	f_S Multiple
0	128
1	256
2	384
3	512
4	640
5	768
6	896
7	1024

0x59—Bit[6], MDA/MCL PU

This bit disables the MDA/MCL pull-ups.

0x59—Bit[5], CLK Term O/R

This bit allows for overriding during power-down.
0 = auto, 1 = manual.

0x59—Bit[4], Manual CLK Term

This bit allows normal clock termination or disconnects this.
0 = normal, 1 = disconnected.

0x59—Bit[2], FIFO Reset UF

This bit resets the audio FIFO if underflow is detected.

0x59—Bit[1], FIFO Reset OF

This bit resets the audio FIFO if overflow is detected.

0x59—Bit[0], MDA/MCL Three-State

This bit three-states the MDA/MCL lines to allow in-circuit programming of the EEPROM.

0x5A—Bits[6:0], Packet Detected

This register indicates if a data packet in specific sections has been detected. These seven bits are updated if any specific packet has been received since the last reset or loss of clock detect. The default setting is 0x00. See Table 18.

Table 18.

Packet Detect Bit	Packet Detected
0	AVI infoframe
1	Audio infoframe
2	SPD infoframe
3	MPEG source infoframe
4	ACP packets
5	ISRC1 packets
6	ISRC2 packets

0x5B—Bit[3], HDMI Mode

0 = DVI, 1 = HDMI.

0x7B—Bits[7:0], CTS[19:12], 0x7C—Bits[7:0] CTS[11:4], and 0x7D—Bits[7:4], CTS[3:0]

These bits are the most significant eight bits of a 20-bit word used with the 20-bit N term in the regeneration of the audio clock.

0x7D—Bits[3:0], N[19:16], 0x7E—Bits[7:0], N[15:8], and 0x7F—Btis[7:0], N[7:0]

These are the most significant four bits of a 20-bit word used with the 20-bit CTS term to regenerate the audio clock.

0x81—Bits[6:5], Y[1:0]

This register indicates whether data is RGB, 4:4:4, or 4:2:2.

Table 19.

Y	Video Data
00	RGB
01	YCrCb 4:2:2
10	YCrCb 4:4:4

0x81—Bit[4], Active Format Information Status

0 = no data. 1 = active format information valid.

0x84—Bits[6:0], Video Identification Code

See the CEA EDID short video descriptors in EIA/CEA-861B.

0x85—Bits[3:0], Pixel Repeat

This value indicates how many times the pixel was repeated, for example, 0x0 = no repeats, sent once, 0x8 = eight repeats, sent nine times.

0x86—Bits[7:0], Active Line Start LSB and 0x88—Bits[7:0] Active Line Start MSB

These bits indicate the beginning line of active video. All lines before this comprise a top horizontal bar. This is used in letter box modes. If the 2-byte value is 0x00, there is no horizontal bar.

0x87—Bits[6:0], New Data Flags (NDF)

This register indicates whether data in specific sections has changed. In the address space from 0x80 to 0xFF, each register address ending in 0b111 (for example, 0x87, 0x8F, 0x97, 0xAF) is an NDF register. They all have the same data and all are reset when any one of them is read. See Table 20.

Table 20.

NDF Bit Number	Changes Occurred
0	AVI infoframe
1	Audio infoframe
2	SPD infoframe
3	MPEG source infoframe
4	ACP packets
5	ISRC1 packets
6	ISRC2 packets

0x89—Bits[7:0], Active Line End LSB and 0x8A—Bits[7:0], Active Line End MSB

These bits indicate the last line of active video. All lines past this comprise a lower horizontal bar. This is used in letter-box modes. If the 2-byte value is greater than the number of lines in the display, there is no lower horizontal bar.

0x8B—Bits[7:0], Active Pixel Start LSB and 0x8C—Bits[7:0], Active Pixel Start MSB

These bits indicate the first pixel in the display, which is active video. All pixels before this comprise a left vertical bar. If the 2-byte value is 0x00, there is no left bar.

0x8D—Bits[7:0], Active Pixel End LSB and 0x8E—Bits[7:0], Active Pixel End MSB

These bits indicate the last active video pixel in the display. All pixels past this comprise a right vertical bar. If the 2-byte value is greater than the number of pixels in the display, there is no vertical bar.

0x8F—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section.

0x91—Bits[7:4], Audio Coding Type

These bits identify the audio coding so that the receiver may process audio properly. See Table 21.

Table 21.

CT[3:0]	Audio Coding
0x0	Refer to stream header
0x1	IEC60958 PCM
0x2	AC3
0x3	MPEG1 (Layer 1 and Layer 2)
0x4	MP3 (MPEG1 Layer 3)
0x5	MPEG2 (multichannel)
0x6	AAC
0x7	DTS
0x8	ATRAC

0x91—Bits[2:0], Audio Channel Count

These bits specify how many audio channels (2 channels to 8 channels) are being sent.

Table 22.

CC[2:0]	Channel Count
000	Refer to stream header
001	2
010	3
011	4
100	5
101	6
110	7
111	8

0x93—Bits[7:0], Maximum Bit Rate

For compressed audio only, when this value is multiplied by 8 kHz, it represents the maximum bit rate. A value of 0x08 in this field yields a maximum bit rate of (8 kHz × 8 kHz = 64 kHz).

0x94—Bits[7:0], Speaker Mapping

Bits[4:0] define the suggested placement of speakers. Bits[7:5] are currently not available. See Table 23 and Table 24.

Table 23.

Abbreviation	Speaker Placement
FL	Front left
FC	Front center
FR	Front right
FCL	Front center left
FCR	Front center right
RL	Rear left
RC	Rear center
RR	Rear right
RCL	Rear center left
RCR	Rear center right
LFE	Low frequency effect

Table 24. Speaker Mapping

CA					Channel Number							
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	8	7	6	5	4	3	2	1
0	0	0	0	0							FR	FL
0	0	0	0	1						LFE	FR	FL
0	0	0	1	0					FC		FR	FL
0	0	0	1	1					FC	LFE	FR	FL
0	0	1	0	0				RC			FR	FL
0	0	1	0	1				RC		LFE	FR	FL
0	0	1	1	0				RC	FC		FR	FL
0	0	1	1	1				RC	FC	LFE	FR	FL
0	1	0	0	0			RR	RL			FR	FL
0	1	0	0	1			RR	RL		LFE	FR	FL
0	1	0	1	0			RR	RL	FC		FR	FL
0	1	0	1	1			RR	RL	FC	LFE	FR	FL
0	1	1	0	0		RC	RR	RL			FR	FL
0	1	1	0	1		RC	RR	RL		LFE	FR	FL
0	1	1	1	0		RC	RR	RL	FC		FR	FL
0	1	1	1	1		RC	RR	RL	FC	LFE	FR	FL
1	0	0	0	0	RRC	RLC	RR	RL			FR	FL
1	0	0	0	1	RRC	RLC	RR	RL		LFE	FR	FL
1	0	0	1	0	RRC	RLC	RR	RL	FC		FR	FL
1	0	0	1	1	RRC	RLC	RR	RL	FC	LFE	FR	FL
1	0	1	0	0	FRC	FLC				v	FR	FL
1	0	1	0	1	FRC	FLC			v	LFE	FR	FL
1	0	1	1	0	FRC	FLC			FC		FR	FL
1	0	1	1	1	FRC	FLC			FC	LFE	FR	FL
1	1	0	0	0	FRC	FLC		RC			FR	FL
1	1	0	0	1	FRC	FLC		RC		LFE	FR	FL
1	1	0	1	0	FRC	FLC		RC	FC		FR	FL
1	1	0	1	1	FRC	FLC		RC	FC	LFE	FR	FL
1	1	1	0	0	FRC	FLC	RR	RL		v	FR	FL
1	1	1	0	1	FRC	FLC	RR	RL		LFE	FR	FL
1	1	1	1	0	FRC	FLC	RR	RL	FC		FR	FL
1	1	1	1	1	FRC	FLC	RR	RL	FC	LFE	FR	FL

0x95—Bits[6:3], Level Shift

These bits define the amount of attenuation. The value directly corresponds to the amount of attenuation: for example, 0000 = 0 dB, 0001 = 1 dB, … ,1111 = 15 dB attenuation.

0x97—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0x99—Bits[7:0], Vender Name Character 1

This is the first character in eight that is the name of the vendor that appears on the product. The data characters are 7-bit ASCII code.

0x9F—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xA2—Bits[7:0], Product Description Character 1

This is the first character of 16, which contains the model number and a short description of the product. The data characters are 7-bit ASCII code.

0xA7—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xAF—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xB4—Bits[7:0], Source Device Information Code

These bytes classify the source device. See Table 25.

Table 25.

SDI Code	Source
0x00	Unknown
0x01	Digital STB
0x02	DVD
0x03	D-VHS
0x04	HDD video
0x05	DVC
0x06	DSC
0x07	Video CD
0x08	Game
0x09	PC general

0xB7—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xB9—Bits[7:0], MB0

These are the lower eight bits of 32 bits that specify the MPEG bit rate in hertz.

0xBD—Bit[4], Field Repeat

This defines whether the field is new or repeated. 0 = new field or picture. 1 = repeated field.

0xBD—Bits[1:0], MPEG Frame

This identifies the frame as I, B, or P. See Table 26.

Table 26.

MF[1:0]	Frame Type
00	Unknown
01	I (picture)
10	B (picture)
11	P (picture)

0xBF—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xC0—Bits[7:0], Audio Content Protection Packet (ACP Type)

These bits define which audio content protection is used.

Table 27.

Code	ACP Type
0x00	Generic audio
0x01	IEC 60958-identified audio
0x02	DVD-audio
0x03	Reserved for super audio CD (SACD)
0x04 to 0xFF	Reserved

0xC7—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xC8—Bit[7], ISRC1 Continued

This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted.

0xC8—Bit[6], ISRC1 Valid

This bit is an indication of whether the ISRC1 packet bytes are valid. 0 = ISRC1 status bits and PBs not valid. 1 = ISRC1 status bits and PBs valid.

0xC8—[2:0], ISRC Status

These bits define where in the ISRC track the samples are. At least two transmissions of 001 occur at the beginning of the track, while continuous transmission of 010 occurs in the middle of the track, followed by at least two transmissions of 100 near the end of the track.

0xCF—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xD7—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xDC—Bits[7:0], ISRC2 Packet Byte 0 (ISRC2_PB0)

This is transmitted only when the ISRC continued bit (Register 0xC8 Bit 7) is set to 1.

0xDF—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

0xE7—Bits[6:0], New Data Flags

See the 0x87—Bits[6:0], New Data Flags (NDF) section for a description.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided in the AD9393.

The 2-wire serial interface is comprised of a clock (SCL) and a bidirectional data (SDA) ball. The HDMI flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Change data on SDA only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal
- Acknowledge (ACK)

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slave devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise an 7-bit slave address (the first 7 bits) and a single R/$\overline{W}$ bit (the eight bit). The R/$\overline{W}$ bit indicates the direction of the data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device, the AD9393 acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9393 does not acknowledge.

Table 28. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A_6 (MSB)	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	1	1	0	0	R/$\overline{W}$

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9393 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9393 during a read sequence, the AD9393 interprets this as the end of data. The SDA remains high, so the master can generate a stop signal.

To write data to specific control registers of the AD9393, the 8-bit address of the control register of interest must be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by 1 for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value. Any base address higher than the maximum value does not produce an acknowledge signal.

Data are read from the control registers of the AD9393 in a similar manner. Reading requires two data transfer operations:

- The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation.
- Reading (the R/$\overline{W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9393, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

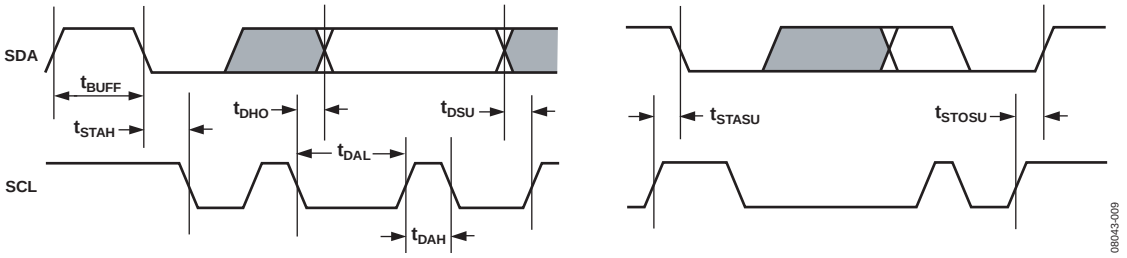

Figure 7. Serial Port Read/Write Timing

SERIAL INTERFACE READ/WRITE EXAMPLES

Write to one control register:

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Data byte to base address
5. Stop signal

Write to four consecutive control registers:

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

Read from one control register:

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/$\overline{W}$ bit = high)
6. Data byte from base address
7. Stop signal

Read from four consecutive control registers:

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/$\overline{W}$ bit = high)
6. Data byte from base address
7. Data byte from (base address + 1)
8. Data byte from (base address + 2)
9. Data byte from (base address + 3)
10. Stop signal

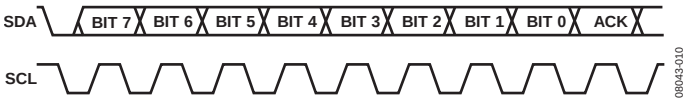

Figure 8. Serial Interface—Typical Byte Transfer

PCB LAYOUT RECOMMENDATIONS

The AD9393 is a high precision, high speed digital device. To achieve the maximum performance from the part, it is important to have a well laid-out board. The following sections are a guide for designing a board using the AD9393.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply ball with a 0.1 µF capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power ball. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9393, because that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power ball. Current should flow from the power plane to the capacitor to the power ball. Do not make the power connection between the capacitor and the power ball. Placing a via underneath the capacitor pads down to the power plane is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_{DD} (the clock generator supply). Abrupt changes in PV_{DD} can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by paying careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the circuitry groups (V_D and PV_{DD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during HSYNC and VSYNC periods). This can result in a measurable change in the voltage supplied to the regulator, which can in turn produce changes in the regulated supply voltage. This can be mitigated by regulating the PV_{DD} from a different, cleaner power source (for example, from a 12 V supply).

It is recommended to use a single ground plane for the entire board. Experience has shown repeatedly that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and long ground loops can result.

In some cases, using separate ground planes is unavoidable, so it is recommended to place a single ground plane under the AD9393. The location of the split should be at the receiver of the digital outputs. In this case, it is even more important to place components wisely because the current loops are much longer (current takes the path of least resistance).

OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which require more current that causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the AD9393. If series resistors are used, place them as close as possible to the AD9393 pins (although try not to add vias or extra length to the output trace to move the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside of the AD9393 and creates more digital noise on its power supplies.

DIGITAL INPUTS

The digital inputs on the AD9393 are designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. Therefore, no extra components need to be added if using 5.0 V logic.

Any noise that enters the HSYNC input trace can add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

COLOR SPACE CONVERTER (CSC) COMMON SETTINGS

HDTV YCRCB (0 TO 255) TO RGB (0 TO 255) (DEFAULT SETTING FOR AD9393)

Table 29.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x0C	0x52	0x08	0x00	0x00	0x00	0x19	0xD7

Table 30.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x1C	0x54	0x08	0x00	0x3E	0x89	0x02	0x91

Table 31.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x00	0x00	0x08	0x00	0x0E	0x87	0x18	0xBD

HDTV YCRCB (16 TO 235) TO RGB (0 TO 255)

Table 32.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x47	0x2C	0x04	0xA8	0x00	0x00	0x1C	0x1F

Table 33.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x1D	0xDD	0x04	0xA8	0x1F	0x26	0x01	0x34

Table 34.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x00	0x00	0x04	0xA8	0x08	0x 75	0x1B	0x7B

SDTV YCRCB (0 TO 255) TO RGB (0 TO 255)

Table 35.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x2A	0xF8	0x08	0x00	0x00	0x00	0x1A	0x84

Table 36.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x1A	0x6A	0x08	0x00	0x1D	0x50	0x04	0x23

Table 37.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x00	0x00	0x08	0x00	0x0D	0xDB	0x19	0x12

SDTV YCRCB (16 TO 235) TO RGB (0 TO 255)

Table 38.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x46	0x63	0x04	0xA8	0x00	0x00	0x1C	0x84

Table 39.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x1C	0xC0	0x04	0xA8	0x1E	0x6F	0x02	0x1E

Table 40.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x00	0x00	0x04	0xA8	0x08	0x11	0x1B	0xAD

RGB (0 TO 255) TO HDTV YCRCB (0 TO 255)

Table 41.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x08	0x2D	0x18	0x93	0x1F	0x3F	0x08	0x00

Table 42.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x03	0x68	0x0B	0x71	0x01	0x27	0x00	0x00

Table 43.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x1E	0x21	0x19	0xB2	0x08	0x2D	0x08	0x00

RGB (0 TO 255) TO HDTV YCRCB (16 TO 235)

Table 44.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x07	0x06	0x19	0xA0	0x1F	0x5B	0x08	0x00

Table 45.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x02	0xED	0x09	0xD3	0x00	0xFD	0x01	0x00

Table 46.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x1E	0x64	0x1A	0x96	0x07	0x06	0x08	0x00

RGB (0 TO 255) TO SDTV YCRCB (0 TO 255)

Table 47.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x08	0x2D	0x19	0x27	0x1E	0xAC	0x08	0x00

Table 48.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x04	0xC9	0x09	0x64	0x01	0xD3	0x00	0x00

Table 49.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x1D	0x3F	0x1A	0x93	0x08	0x2D	0x08	0x00

RGB (0 TO 255) TO SDTV YCRCB (16 TO 235)

Table 50.

Register	Red/Cr Coeff 1		Red/Cr Coeff 2		Red/Cr Coeff 3		Red/Cr Offset	
Address	0x35	0x36	0x37	0x38	0x39	0x3A	0x3B	0x3C
Value	0x07	0x06	0x1A	0x1E	0x1E	0xDC	0x08	0x00

Table 51.

Register	Green/Y Coeff 1		Green/Y Coeff 2		Green/Y Coeff 3		Green/Y Offset	
Address	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43	0x44
Value	0x04	0x1C	0x08	0x11	0x01	0x91	0x01	0x00

Table 52.

Register	Blue/Cb Coeff 1		Blue/Cb Coeff 2		Blue/Cb Coeff 3		Blue/Cb Offset	
Address	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C
Value	0x1D	0xA3	0x1B	0x57	0x07	0x06	0x08	0x00

OUTLINE DIMENSIONS

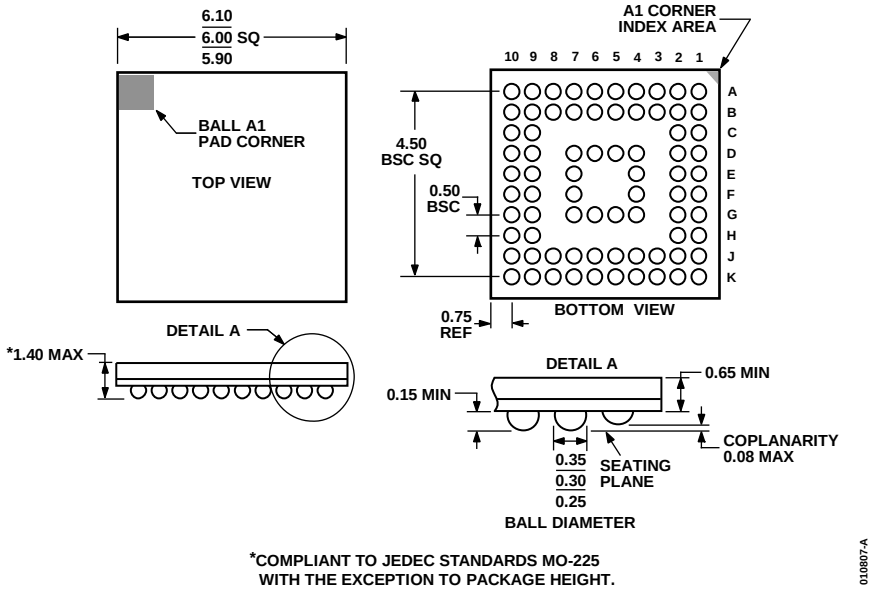

Figure 9. 76-Pin Chip Scale Package Pin Grid Array [CSP_BGA]
6 mm × 6 mm × 1.2 mm
(BC-76-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Max Speed (MHz) Digital	Temperature Range	Package Description	Package Option
AD9393BBCZ-80[1]	80	−10°C to +80°C	76-Pin Chip Scale Package Pin Grid Array (CSP_BGA)	BC-76-2
AD9393BBCZRL-80[1]	80	−10°C to +80°C	76-Pin Chip Scale Package Pin Grid Array (CSP_BGA)	BC-76-2
AD9393/PCBZ[1]			Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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D08043-0-10/09(0)

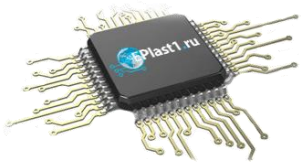
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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