CLC020 SMPTE 259M Digital Video Serializer with Integrated Cable Driver

Check for Samples: CLC020

FEATURES

- **SMPTE 259M Serial Digital Video Standard Compliant**
- **No External Serial Data Rate Setting or VCO Filtering Components Required(1)**
- **Built-In Self-Test (BIST) and Video Test Pattern Generator (TPG) with 16 Internal Patterns(1)**
- **Supports All NTSC and PAL Standard Component and Composite Serial Video Data Rates**
- **HCMOS/TTL-Compatible Data and Control Inputs and Outputs**
- **75Ω ECL-Compatible, Differential, Serial Cable-Driver Outputs**
- **Fast VCO Lock Time: <75 µs**
- **Single +5V TTL or −5V ECL Supply Operation**
- **Low Power: 235 mW Typical**
- **28-Lead PLCC Package**
- **Commercial Temperature Range 0°C to +70°C**

APPLICATIONS

- **SMPTE 259M Parallel-to-Serial Digital Video Interfaces for:**
  - **Video Cameras**
  - **VTRs**
  - **Telecines**
  - **Video Test Pattern Generators and Digital Video Test Equipment**
- **Non-SMPTE Video Applications**
- **Other High Data Rate Parallel/Serial Video and Data Systems**

DESCRIPTION

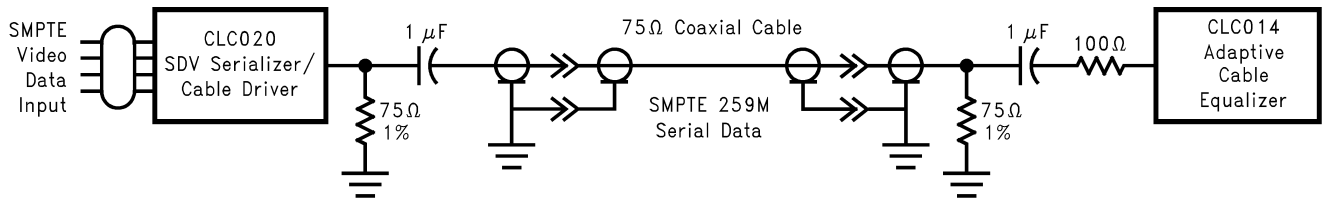
The CLC020 SMPTE 259M Digital Video Serializer with Integrated Cable Driver is a monolithic integrated circuit that encodes, serializes and transmits bit-parallel digital data conforming to SMPTE 125M and SMPTE 267M component video and SMPTE 244M composite video standards. The CLC020 can also serialize other 8 or 10-bit parallel data. The CLC020 operates at data rates from below 100 Mbps to over 400 Mbps. The serial data clock frequency is internally generated and requires no external frequency setting components, trimming or filtering*. Functions performed by the CLC020 include: parallel-to-serial data conversion, data encoding using the polynomial (X^9+X^4+1), data format conversion from NRZ to NRZI, parallel data clock frequency multiplication and encoding with the serial data, and coaxial cable driving. Input for sync (TRS) detection disabling and a PLL lock detect output are provided. The CLC020 has an exclusive built-in self-test (BIST) and video test pattern generator (TPG) with 4 component video test patterns, reference black, PLL and EQ pathologicals and modified colour bars, in 4:3 and 16:9 raster and both NTSC and PAL formats*. Separate power pins for the output driver, VCO and the digital logic improve power supply rejection, output jitter and noise performance.

The CLC020 is the ideal complement to the CLC011B SMPTE 259M Serial Digital Video Decoder, CLC014 Active Cable Equalizer, CLC016 Data Retiming PLL (clock-data separator), CLC018 8X8 Digital Crosspoint Switch and CLC006 or CLC007 Cable Drivers, for a complete parallel-serial-parallel, high-speed data processing and transmission system.

The CLC020 is powered from a single 5V supply. Power dissipation is typically 235 mW including two 75Ω back-matched output loads. The device is packaged in a JEDEC 28-lead PLCC.

(1) Patents Applications Made or Pending.

TYPICAL APPLICATION



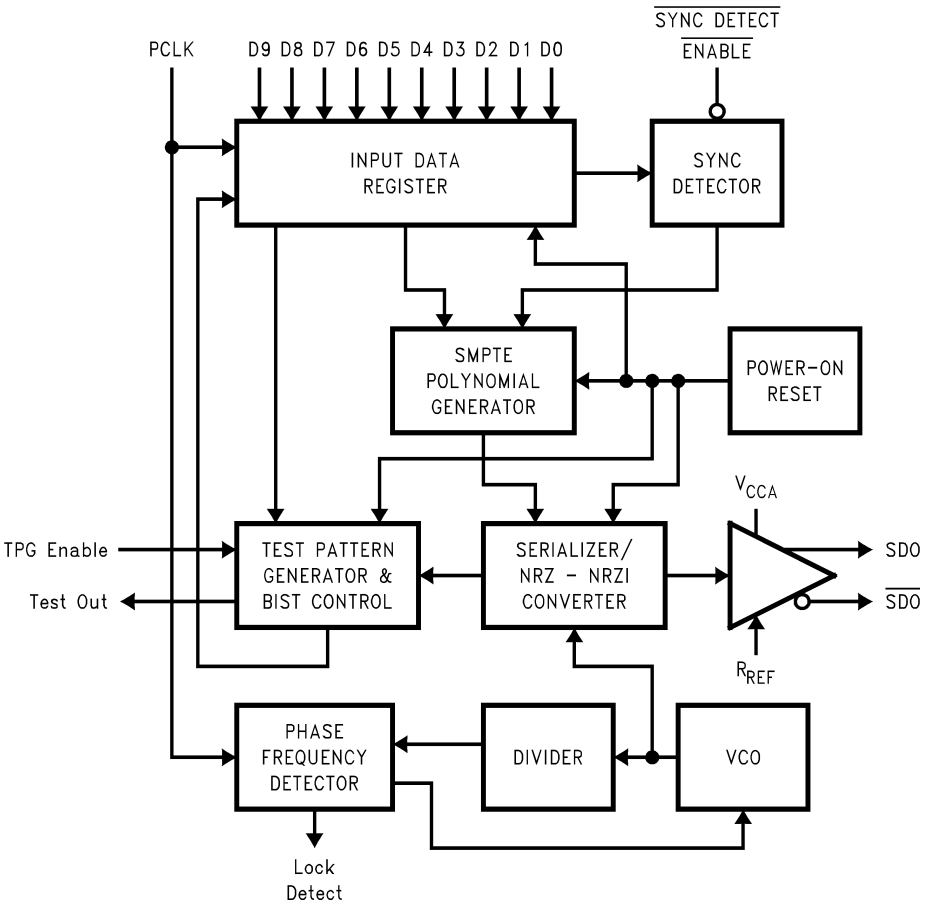
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BLOCK DIAGRAM



CONNECTION DIAGRAM

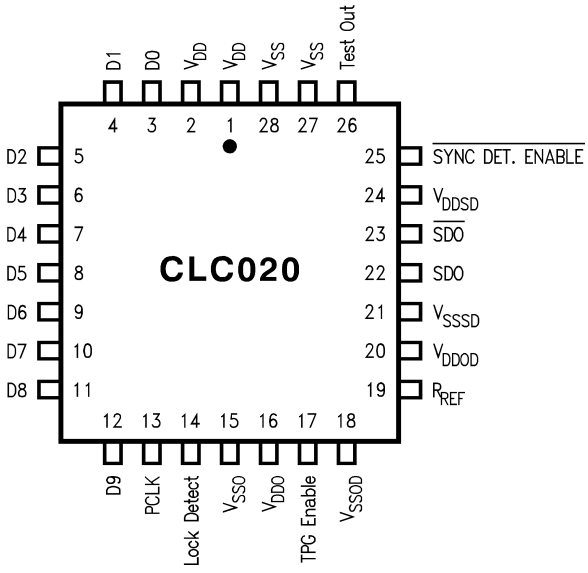


Figure 1. 28-Pin PLCC
See Package Number FN0028A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{DD}−V_{SS})		6.0V
CMOS/TTL Input Voltage (V_I)		−0.5V to (V_{DD} + 0.5V)
CMOS/TTL Output Voltage (V_O)		−0.5V to (V_{DD} + 0.5V)
CMOS/TTL Input Current (single input)	V_I = V_{SS} −0.5V	−5 mA
	V_I = V_{DD} +0.5V	+5 mA
Input Current, Other Inputs		±1 mA
CMOS/TTL Output Source/Sink Current		±10 mA
SDO Output Source Current		20 mA
Package Thermal Resistance	θ_{JA} 28-lead PLCC	85°C/W
	θ_{JC} 28-lead PLCC	35°C/W
Storage Temp. Range		−65°C to +150°C
Junction Temperature		+150°C
Lead Temperature (Soldering 4 Sec)		+260°C
ESD Rating (HBM)		>2.5 kV
ESD Rating (MM)		>200 V
Transistor Count		33,400

(1) Absolute Maximum Ratings are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of Electrical Characteristics specifies acceptable device operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{DD}−V_{SS})	5.0V ±10%
CMOS/TTL Input Voltage	V_{SS} to V_{DD}
P_{CLK} Frequency Range	10 to 40MHz
P_{CLK} Duty Cycle	45 to 55%
D_N and P_{CLK} Rise/Fall Time	1.0 to 3.0 ns
Maximum DC Bias on SDO pins	3.0V ±10%
Operating Free Air Temperature (T_A)	0°C to +70°C

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DC ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		D0 through D9, P_{CLK}, TPG_EN and Sync. Detect Enable	2.0		V_{DD}	V
V_{IL}	Input Voltage Low Level			V_{SS}		0.8	V
I_{IH}	Input Current High Level	$V_{IH} = V_{DD}$			+40	+60	µA
I_{IL}	Input Current Low Level	$V_{IL} = V_{SS}$			-1	-20	µA
V_{OH}	CMOS Output Voltage High Level	I_{OH} = −10 mA	Lock Detect, Test Out	2.4	4.7	V_{DD}	V
V_{OL}	CMOS Output Voltage Low Level	I_{OL} = +10 mA		0.0	0.3	V_{SS} + 0.5V	V
V_{SDO}	Serial Driver Output Voltage	R_L = 75Ω 1%, R_{REF} = 1.69 kΩ 1%, See Figure 3	SDO, $\overline{SDO}$	700	800	900	mV_{P-P}
I_{DD}	Power Supply Current, Total	R_L = 75Ω 1%, R_{REF} = 1.69 kΩ 1%, P_{CLK} = 27 MHz, See Figure 3, NTSC Colour Bar Pattern			47	60	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{SS} = 0V.
(2) Typical values are stated for V_{DD} = +5.0V and T_A = +25°C.

AC ELECTRICAL CHARACTERISTICS

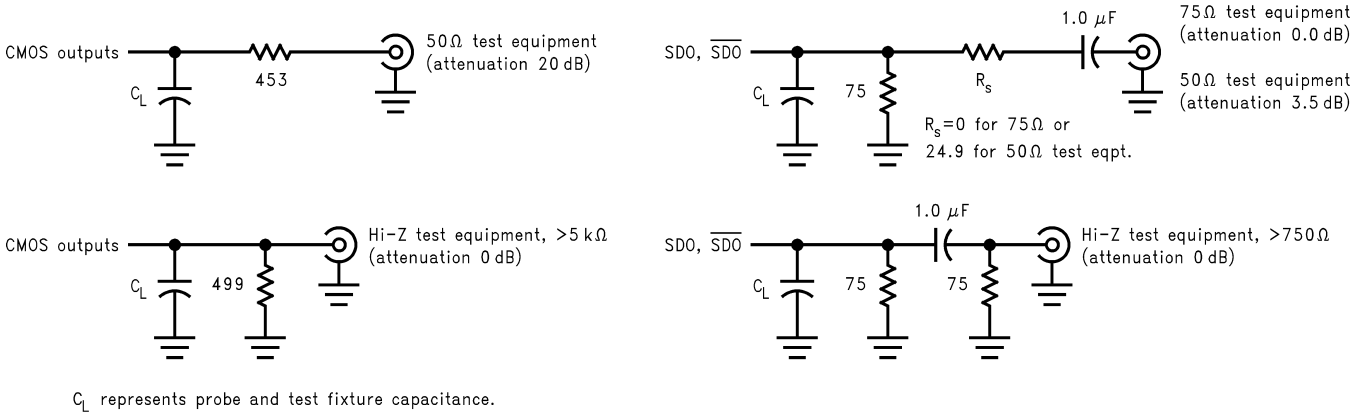
Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SDO}	Serial data rate	R_L = 75Ω, AC coupled(2)	SDO, $\overline{SDO}$	100		400	Mbps
F_{PCLK}	Reference Clock Input Frequency		P_{CLK}	10		40	MHz
	Reference Clock Duty Cycle		P_{CLK}	45	50	55	%
t_r, t_f	Rise time, Fall time	10%–90%	D_N, P_{CLK}	1.0	1.5	3.0	ns
t_j	Serial output jitter	270 Mbps(3), See Figure 3	SDO, $\overline{SDO}$		220		ps_{P-P}
t_{jit}	Serial output jitter	See(4)(2)			100	200	ps_{P-P}
t_r, t_f	Rise time, Fall time	20%–80%(2)(4)		500	800	1500	ps
	Output overshoot				1		%
t_{LOCK}	Lock time	270 Mbps(2)(5)			75		µs
t_{SU}	Setup time	See Figure 4	D_N to P_{CLK}	3	2		ns
t_{HLD}	Hold time	See Figure 4	D_N from P_{CLK}	1.5	1		ns
L_{GEN}	Output inductance	See(4)	SDO, $\overline{SDO}$		6		nH
R_{GEN}	Output resistance	See(4)			25k		Ω

(1) Typical values are stated for V_{DD} = +5.0V and T_A = +25°C.
(2) R_L = 75Ω, AC-coupled @ 270 M_{bps}, R_{REF} = 1.69 kΩ 1%, See TEST LOADS and Figure 3.
(3) CLC020 mounted in the SD020EVK board, configured in BIST mode (NTSC color bars) with P_{CLK} = 27MHz derived from Tektronix TG2000 black-burst reference. Timing jitter measured with Tektronix VM700T using jitter measurement FFT mode, frame rate, 1kHz filter bandwidth, Hanning window.
(4) Specification is ensured by design.
(5) Measured from rising-edge of first P_{CLK} cycle until Lock Detect output goes high (true).

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TEST LOADS



C_L represents probe and test fixture capacitance.

All resistors in Ohms, 1% tolerance.

Figure 2. Test Loads

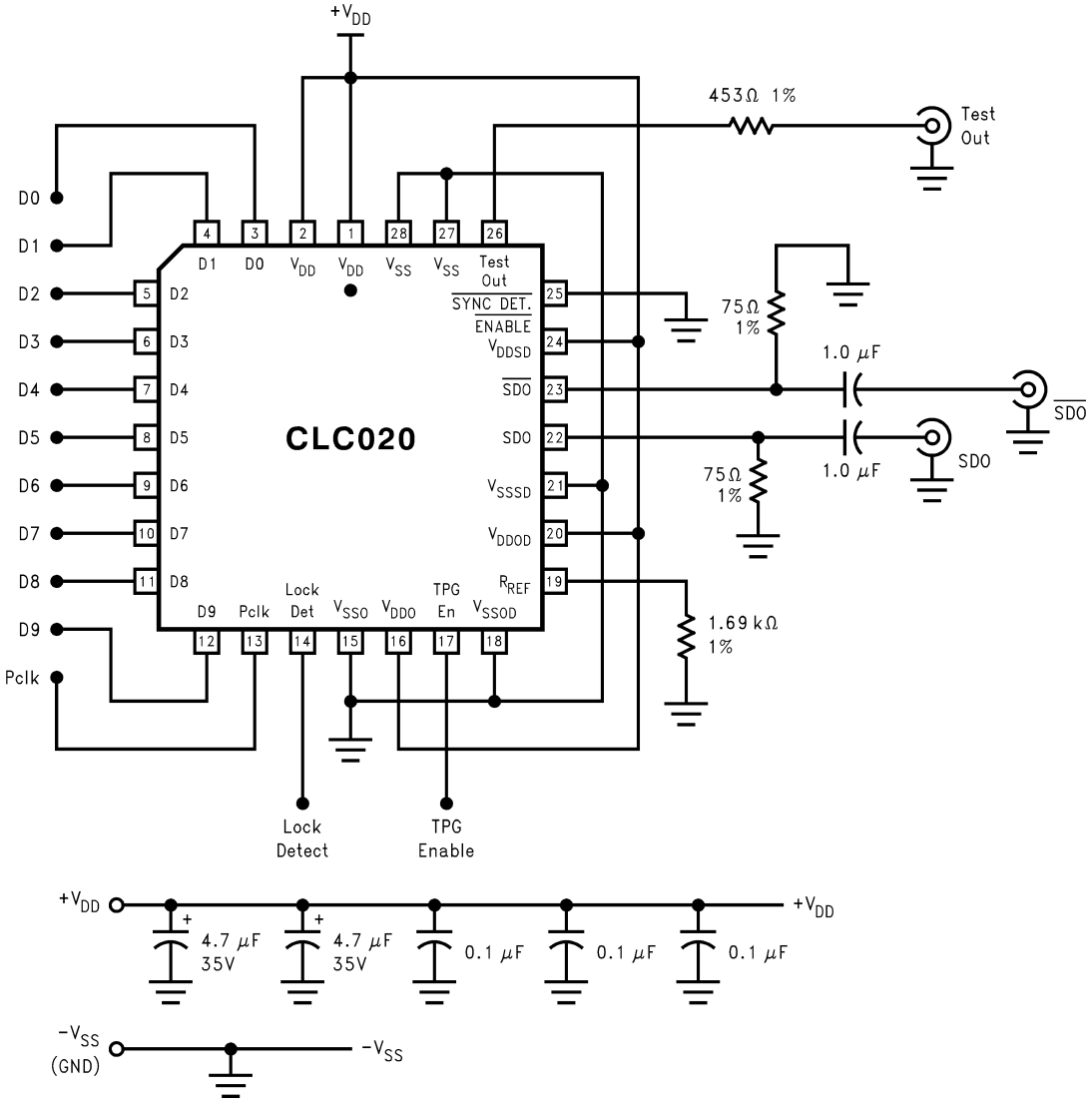


Figure 3. Test Circuit

TIMING DIAGRAM

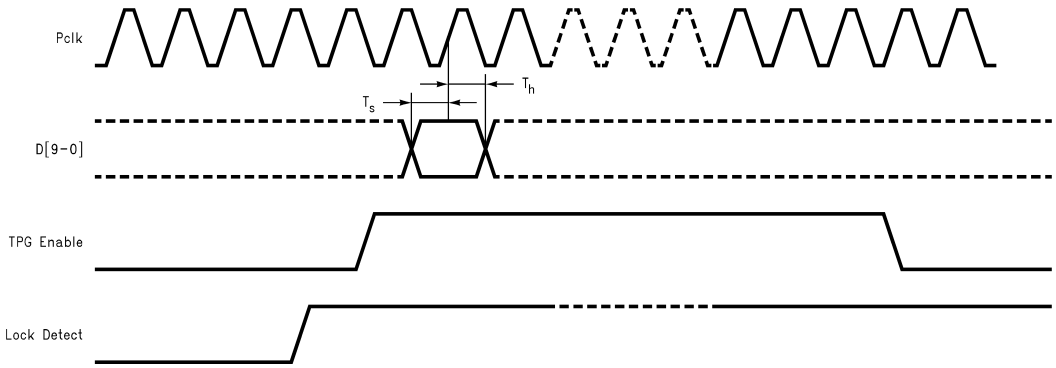


Figure 4. Setup and Hold Timing

DEVICE OPERATION

The CLC020 SMPTE 259M Digital Video Serializer is used in digital video signal origination and processing equipment: cameras, video tape recorders, telecines, video test equipment and others. It converts parallel component or composite digital video signals into serial format. Logic levels within this equipment are normally TTL-compatible as produced by CMOS or bipolar logic devices. The encoder outputs ECL-compatible serial digital video (SDV) signals conforming to SMPTE 259M-1997. The CLC020 operates at all standard SMPTE and ITU-R parallel data rates.

VIDEO DATA PROCESSING CIRCUITS

The **input data register** accepts 8 or 10-bit parallel data and clock signals having CMOS/TTL-compatible signal levels. Parallel data may conform to any of several standards: SMPTE 125M, SMPTE 267M, SMPTE 244M or ITU-R BT.601. If data is 8-bit, it is converted to a 10-bit representation according to the type of data being input: component 4:2:2 per SMPTE 259M paragraph 7.1.1, composite NTSC per paragraph 8.1.1 or composite PAL per paragraph 9.1.1. Output from this register feeds the SMPTE polynomial generator/serializer and sync detector. All CMOS inputs including the P_{CLK} input have internal pull-down devices.

The **sync detector** or TRS character detector accepts data from the input register. The detection function is controlled by Sync Detect Enable, a low-true, TTL-compatible, external signal. Synchronization words, the timing reference signals (TRS), start-of-active-video (SAV) and end-of-active-video (EAV) are defined in SMPTE 125M-1995 and 244M. The sync detector supplies control signals to the SMPTE polynomial generator that identify the presence of valid video data. The sync detector performs input TRS character LSB-clipping as prescribed in ITU-R-BT.601. LSB-clipping causes all TRS characters with a value between 000h and 003h to be forced to 000h and all TRS characters with a value between 3FCh and 3FFh to be forced to 3FFh. Clipping is done prior to encoding.

The **SMPTE polynomial generator** accepts the parallel video data and encodes it using the polynomial X^9+X^4+1 as specified in SMPTE 259M–1997, paragraph 5 and Annex C. The scrambled data is then serialized for output.

The **NRZ-to-NRZI converter** accepts serial NRZ data from the SMPTE polynomial genertor and converts it to NRZI using the polynomial X + 1 per SMPTE 259M–1997, paragraph 5.2 and Annex C. The transmission bit order is LSB first, per paragraph 6. The converter's output feeds the output driver amplifier.

PHASE-LOCKED LOOP AND VCO

The **phase-locked loop** (PLL) system generates the output serial data clock at 10× the parallel data clock frequency. This system consists of a VCO, divider chain, phase-frequency detector and internal loop filter. The VCO free-running frequency is internally set. The PLL automatically generates the appropriate frequency for the serial clock rate using the parallel data clock (P_{CLK}) frequency as its reference. Loop filtering is internal to the CLC020. The VCO has separate V_{SSO} and V_{DDO} power supply feeds, pins 15 and 16, which may be supplied power independently via an external low-pass filter, if desired. The PLL acquisition (lock) time is less than 75 µs @ 270 Mbps.

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LOCK DETECT

The **Lock Detect** output of the phase-frequency detector indicates the PLL lock condition. It is a logic HIGH when the loop is locked. The output is CMOS/TTL-compatible and is suitable for driving other CMOS devices or a LED indicator.

SERIAL DATA OUTPUT BUFFER

The current-mode **serial data outputs** provide low-skew complimentary or differential signals. The output buffer design can drive 75Ω coaxial cables (AC-coupled) or 10k/100k ECL/PECL-compatible devices (DC-coupled). Output levels are 800 mV_{P-P} ±10% into 75Ω AC-coupled, back-matched loads. The output level is 400 mV_{P-P} ±10% when DC-coupled into 75Ω (See APPLICATION INFORMATION for details). The 75Ω resistors connected to the SDO outputs are back-matching resistors. No series back-matching resistors should be used. SDO output levels are controlled by the value of R_{REF} connected to pin 19. The value of R_{REF} is normally 1.69 kΩ, ±1%. The output buffer is static when the device is in an out-of-lock condition. Separate V_{SSSD} and V_{DDSD} power feeds, pins 21 and 24, are provided for the serial output driver.

POWER-ON RESET

The CLC020 has an internally controlled, automatic, **power-on reset** circuit. This circuit clears TRS detection circuitry, all latches, registers, counters and polynomial generators and disables the serial output. The SDO outputs are tri-stated during power-on reset. The part will remain in the reset condition until the parallel input clock is applied.

It is recommended that P_{CLK} not be asserted until at least 30 µs after power has reached V_{DD}min. See Figure 5.

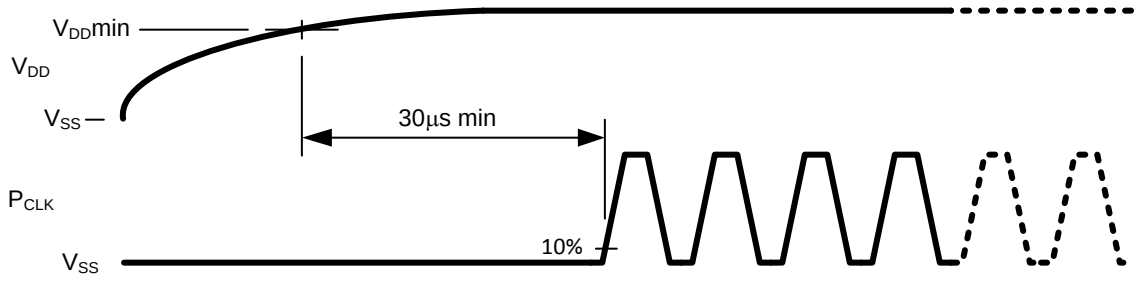


Figure 5. Power-On Reset Sequence

BUILT-IN SELF-TEST (BIST)

The CLC020 has a **built-in self-test (BIST)** function. The BIST performs a comprehensive go-no-go test of the device. The test uses either a full-field color bar for NTSC or a PLL pathological for PAL as the test data pattern. Data is input internally to the input data register, processed through the device and tested for errors. Table 1 gives device pin functions and Table 2 gives the test pattern codes used for this function. The signal level at Test_Output, pin 26, indicates a pass or fail condition.

The BIST is initiated by applying the code for the desired BIST to D0 throught D3 (D9 through D4 are 00h) and a 27 MHz clock at the P_{CLK} input. Since all parallel data inputs are equipped with an internal pull-down device, only those inputs D0 through D3 which require a logic-1 need be pulled high. After the Lock_Detect output goes high (true) indicating the VCO is locked on frequency, TPG_Enable, pin 17, is then taken to a logic high. TPG_Enable may be temporarily connected to the Lock_Detect output to automate BIST operation. Test_Output, pin 26, is monitored for a pass/fail indication. If no errors have been detected, this output will go to a logic high level approximately 2 field intervals after TPG_Enable is taken high. If errors have been detected in the internal circuitry of the CLC020, Test_Output will remain low until the test is terminated. The BIST is terminated by taking TPG_Enable to a logic low. Continuous serial data output is available during the test.

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TEST PATTERN GENERATOR

The CLC020 features an on-board **test pattern generator (TPG)**. Four full-field component video test patterns for both NTSC and PAL standards, and 4x3 and 16x9 raster sizes are produced. The test patterns are: flat-field black, PLL pathological, equalizer (EQ) pathological and a modified 75%, 8-color vertical bar pattern. The pathologicals follow recommendations contained in SMPTE RP 178–1996 regarding the test data used. The color bar pattern does not incorporate bandwidth limiting coding in the chroma and luma data when transitioning between the bars. For this reason, it may not be suitable for use as a visual test pattern or for input to video D-to-A conversion devices unless measures are taken to restrict the production of out-of-band frequency components.

The TPG is operated by applying the code for the desired test pattern to D0 through D3 (D4 through D9 are 00h). Since all parallel data inputs are equipped with an internal pull-down device, only those inputs D0 through D3 which require a logic-1 need be pulled high. Next, apply a 27 or 36 MHz signal, appropriate to the raster size desired, at the P_{CLK} input and wait until the Lock_Detect output goes true indicating the VCO is locked on-frequency. Then, take TPG_Enable, pin 17, to a logic high. The serial test pattern data appears on the SDO outputs. TPG_Enable may be temporarily connected to the Lock_Detect output to automate TPG operation. The TPG mode is exited by taking TPG_Enable to a logic low. Table 1 gives device pin functions for this mode. Table 2 gives the available test patterns and selection codes.

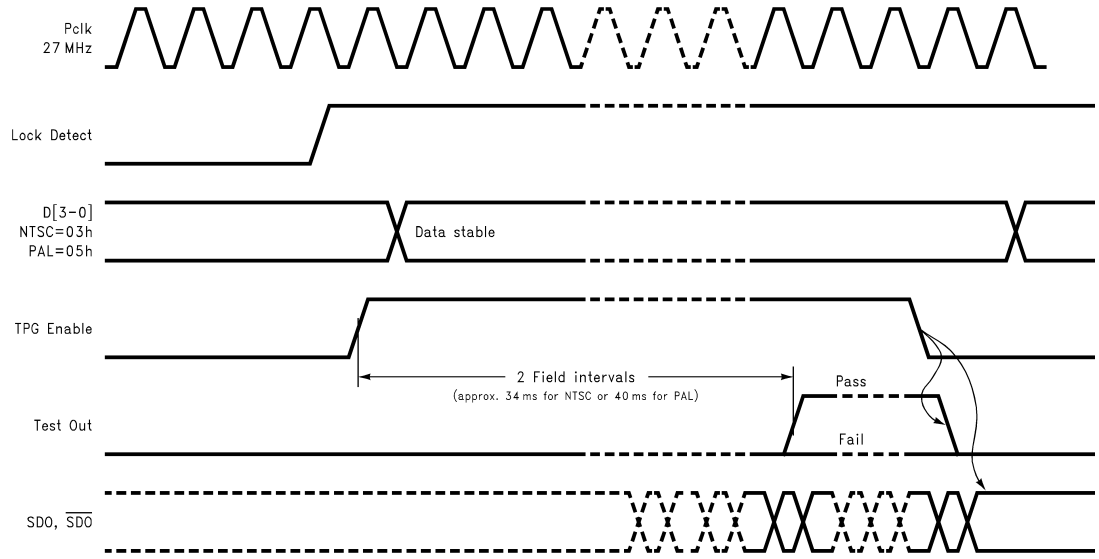


Figure 6. Built-In Self-Test Control Sequence

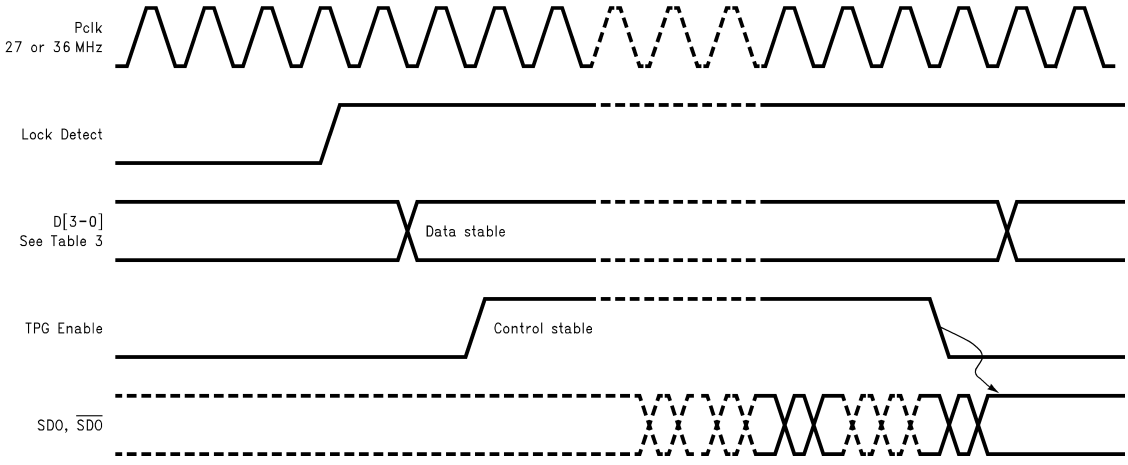


Figure 7. Test Pattern Generator Control Sequence

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Table 1. BIST and Test Pattern Generator Control Functions

Pin	Name	Function
3	D0	TPG code input LSB
4	D1	TPG code input
5	D2	TPG code input
6	D3	TPG code input MSB
17	TPG_EN	TPG Enable, active high true
26	Test_Out	BIST Pass/Fail output. Pass=High (See text for timing requirements)

Table 2. Component Video Test Pattern Selection(1)

Standard	Frame	Test Pattern	D3	D2	D1	D0
NTSC	4x3	Flat-field black	0	0	0	0
NTSC	4x3	PLL pathological	0	0	0	1
NTSC	4x3	EQ pathological	0	0	1	0
NTSC	4x3	Color bars, 75%, 8-bars (modified, see text), BIST	0	0	1	1
PAL	4x3	Flat-field black	0	1	0	0
PAL	4x3	PLL pathological, BIST	0	1	0	1
PAL	4x3	EQ pathological	0	1	1	0
PAL	4x3	Color bars, 75%, 8-bars (modified, see text)	0	1	1	1
NTSC	16x9	Flat-field black	1	0	0	0
NTSC	16x9	PLL pathological	1	0	0	1
NTSC	16x9	EQ pathological	1	0	1	0
NTSC	16x9	Color bars, 75%, 8-bars (modified, see text)	1	0	1	1
PAL	16x9	Flat-field black	1	1	0	0
PAL	16x9	PLL pathological	1	1	0	1
PAL	16x9	EQ pathological	1	1	1	0
PAL	16x9	Color bars, 75%, 8-bars (modified, see text)	1	1	1	1

(1) D9 through D4 = 0 (binary)

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PIN DESCRIPTIONS(1)

Pin #	Name	Description
1	V_{DD}	Positive power supply input (digital logic)
2	V_{DD}	Positive power supply input (digital logic)
3	D0	Parallel data input/Test pattern select (LSB)
4	D1	Parallel data input/Test pattern select
5	D2	Parallel data input/Test pattern select
6	D3	Parallel data input/Test pattern select (MSB)
7	D4	Parallel data input
8	D5	Parallel data input
9	D6	Parallel data input
10	D7	Parallel data input
11	D8	Parallel data input
12	D9	Parallel data input
13	PCLK	Parallel clock input
14	Lock Detect	VCO Lock Detect output (high-true)
15	V_{SSO}	Negative power supply input (PLL supply)
16	V_{DDO}	Positive power supply input (PLL supply)
17	TPG_EN	Test Pattern Generator (TPG) Enable input (high-true)
18	V_{SSOD}	Negative power supply input (PLL digital supply)
19	R_{REF}	Output driver level control
20	V_{DDOD}	Positive power supply input (PLL digital supply)
21	V_{SSSD}	Negative power supply input (Output driver)
22	SDO	Serial data true output
23	$\overline{SDO}$	Serial data complement output
24	V_{DDSD}	Positive power supply input (Output driver)
25	$\overline{\text{Sync Detect Enable}}$	Parallel data sync detection enable input (low true)
26	Test_Out	BIST Pass/Fail output
27	V_{SS}	Negative power supply input (digital logic)
28	V_{SS}	Negative power supply input (digital logic)

(1) All CMOS/TTL inputs have internal pull-down devices.

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APPLICATION INFORMATION

A typical application circuit for the CLC020 is shown in Figure 8. This circuit demonstrates the capabilities of the CLC020 and allows its evaluation in a variety of configurations. An assembled demonstration board with more comprehensive evaluation options is available, part number SD020EVK. The board may be ordered through any of Texas Instruments's sales offices. Complete circuit board layouts and schematics, for the SD020EVK are available on Texas Instruments' WEB site in the application information for this device.

APPLICATION CIRCUIT

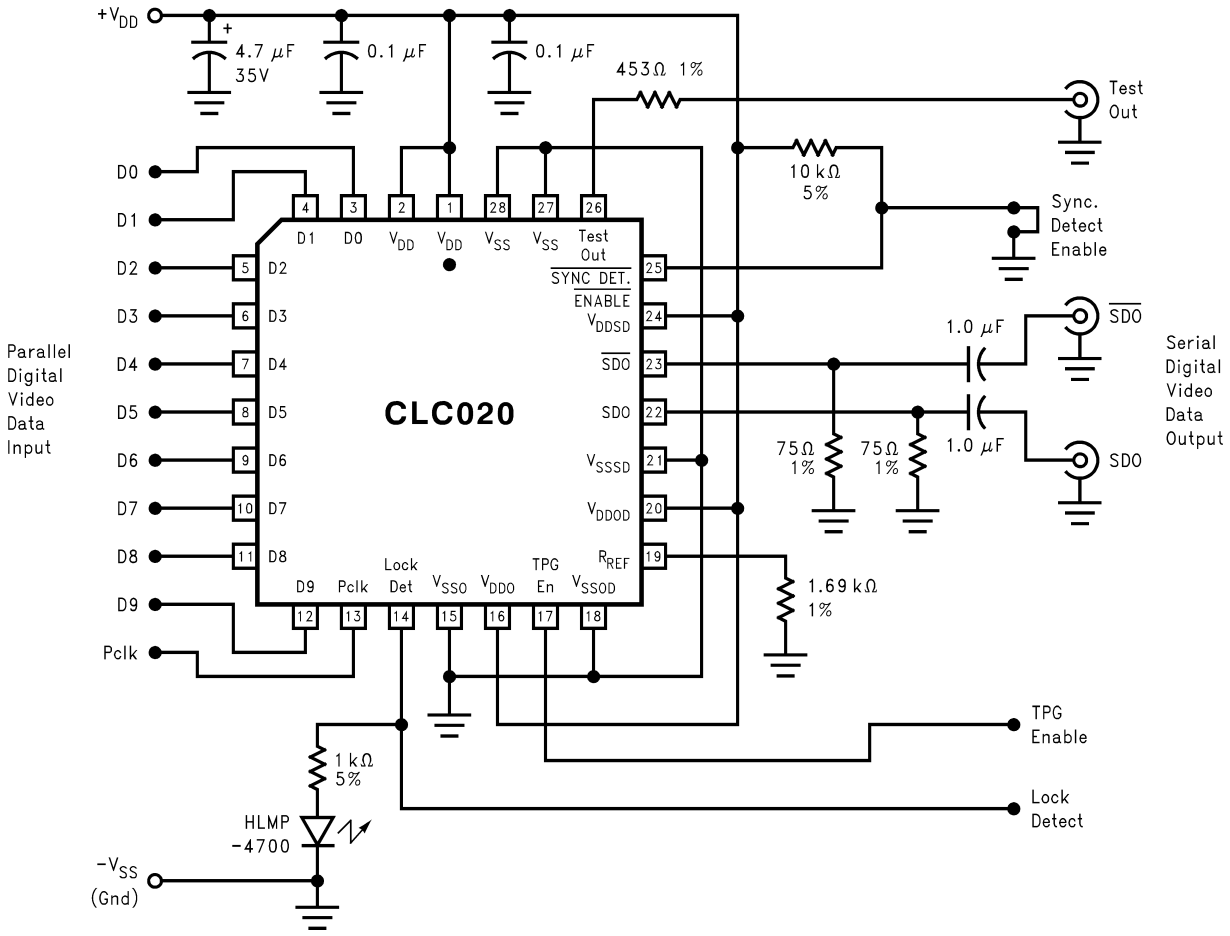


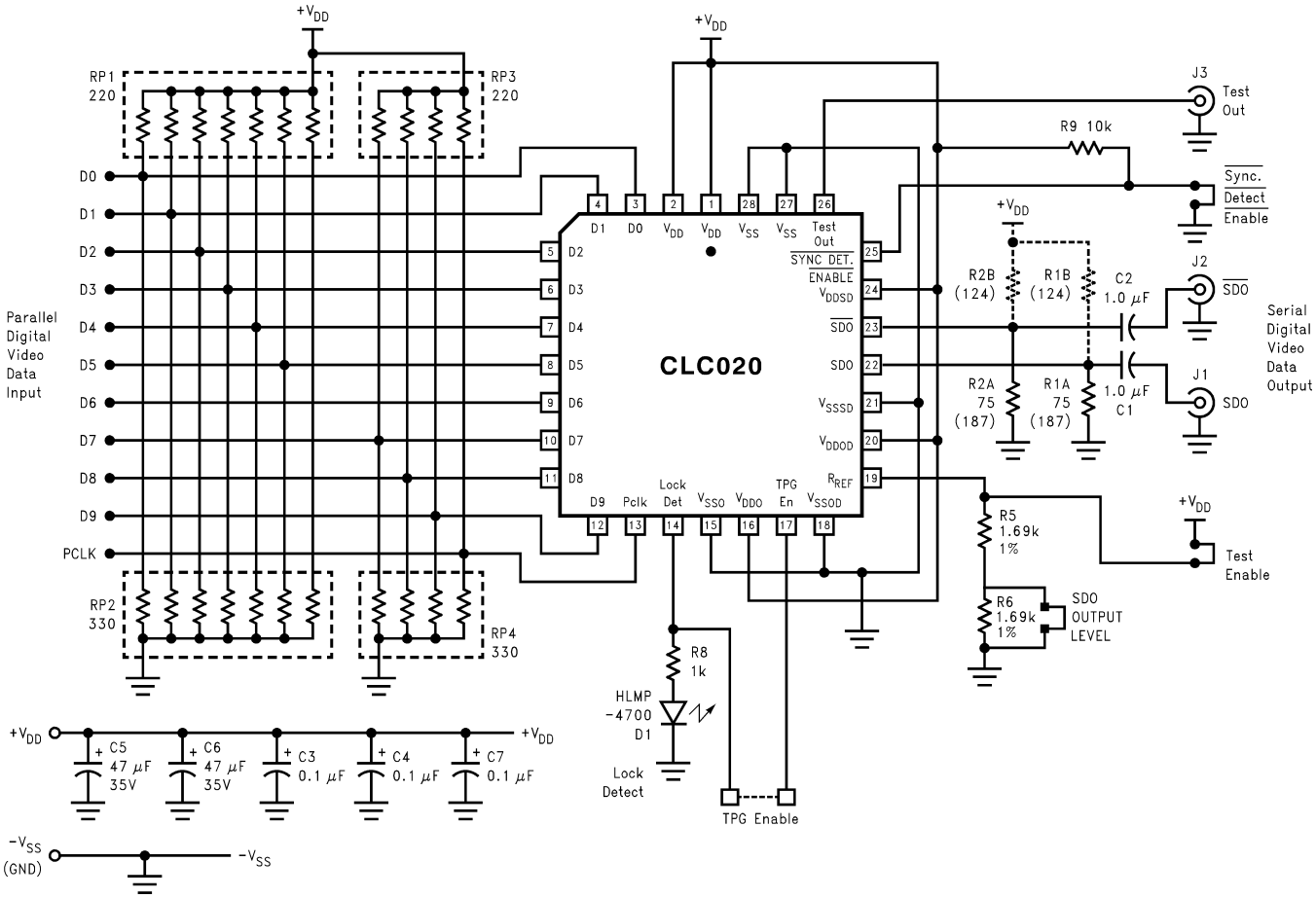
Figure 8. Typical Application Circuit

Several different input and output drive and loading options can be constructed on the SD020EVK application circuit board, Figure 9. Pin headers are provided for input cabling and control signal access. The appropriate value resistor packs, 220 and 330Ω for TTL or 50Ω for signal sources requiring such loading, should be installed at RP1-4 before applying input signals.

The board's outputs may be DC interfaced to PECL inputs by first installing 124Ω resistors at R1B and R2B, changing R1A and R2A to 187Ω and replacing C1 and C2 with short circuits. The PECL inputs should be directly connected to J1 and J2 without cabling. If 75Ω cabling is used to connect the CLC020 to the PECL inputs, the voltage dividers used on the CLC020 outputs must be removed and re-installed on the circuit board where the PECL device is mounted. This will provide correct termination for the cable and biasing for both the CLC020's outputs and the PECL inputs. It is most important to note that a 75Ω or equivalent DC loading (measured with respect to the negative supply rail) must always be installed at both of the CLC020's SDO outputs to obtain proper signal levels from device. When using 75Ω Thevenin-equivalent load circuits, the DC bias applied to the SDO outputs should not exceed +3V with respect to the negative supply rail. Serial output levels should be reduced to 400 mV_{p-p} by changing R_{REF} to 3.4 kΩ.

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The Test Out output is intended for monitoring by equipment presenting high impedance loading (>500Ω). When monitoring the Lock Detect output, the attached monitoring circuit should present a DC resistance greater than 5 kΩ so that Lock Detect indicator operation is not affected.



Connect LOCK DETECT to TPG ENABLE for test pattern generator function.
Remove RP1 & RP3 and replace RP2 & RP4 with 50Ω resistor packs for coax interfacing.
Install RP1-4 when using ribbon cable for input interfacing.
This board is designed for use with TTL power supplies only.
For optional ECL compatible load: R1A = R2A = 187; R1B = R2B = 124.
All resistances & impedances in Ohms. Values with 3 significant digits are 1%; with 2 digits 5%.

Figure 9. SD020EVK Schematic Diagram

MEASURING JITTER

The test method used to obtain the timing jitter value given in the AC Electrical Specification table is based on procedures and equipment described in SMPTE RP 192-1996. The recommended practice discusses several methods and indicator devices. An FFT method performed by standard video test equipment was used to obtain the data given in this data sheet. As such, the jitter characteristics (or jitter floor) of the measurement equipment, particularly the measurement analyzer, become integral to the resulting jitter value. The method and equipment were chosen so that the test can be easily duplicated by the design engineer using most standard digital video test equipment. In so doing, similar results should be achieved. The intrinsic jitter floor of the CLC020's PLL is approximately 25% of the typical jitter given in the electrical specifications. In production, device jitter is measured on automatic IC test equipment (ATE) using a different method compatible with that equipment. Jitter measured using this ATE yields values approximately 50% of those obtained using the video test equipment.

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The jitter test setup used to obtain values quoted in the data sheet consists of:

- Texas Instruments SD020EVK, CLC020 evaluation kit
- Tektronix TG2000 signal generation platform with DVG1 option
- Tektronix VM700T Option 1S Video Measurement Set
- Tektronix TDS 794D, Option C2 oscilloscope
- Tektronix P6339A passive probe
- 75 Ohm coaxial cable, 3ft., Belden 8281 or RG59 (2 required)
- ECL-to-TTL/CMOS level converter/amplifier, Figure 11

Apply the black-burst reference clock from the TG2000 signal generator's BG1 module 27MHz clock output to the level converter input. The clock amplitude converter schematic is shown in Figure 10. Adjust the input bias control to give a 50% duty cycle output as measured on the oscilloscope/probe system. Connect the level translator to the SD020EVK board, connector P1, P_{CLK} pins (the outer-most row of pins is ground). Configure the SD020EVK to operate in the NTSC colour bars, BIST mode. Configure the VM700T to make the jitter measurement in the jitter FFT mode at the frame rate with 1kHz filter bandwidth and Hanning window. Configure the setup as shown in Figure 10. Switch the test equipment on (from standby mode) and allow all equipment temperatures stabilize per manufacturer's recommendation. Measure the jitter value after allowing the instrument's reading to stabilize (about 1 minute). Consult the VM700T Video Measurement Set Option 1S Serial Digital Measurements User Manual (document number 071-0074-00) for details of equipment operation.

The VM700T measurement system's jitter floor specification at 270Mbps is given as 200ps ±20% (100ps ±5% typical) of actual components from 50Hz to 1MHz and 200ps +60%, -30% of actual components from 1MHz to 10MHz. To obtain the actual residual jitter of the CLC020, a root-sum-square adjustment of the jitter reading must be made to compensate for the measurement system's jitter floor specification. For example, if the jitter reading is 250ps, the CLC020 residual jitter is the square root of ($250^2 - 200^2$) = 150ps. The accuracy limits of the reading as given above apply.

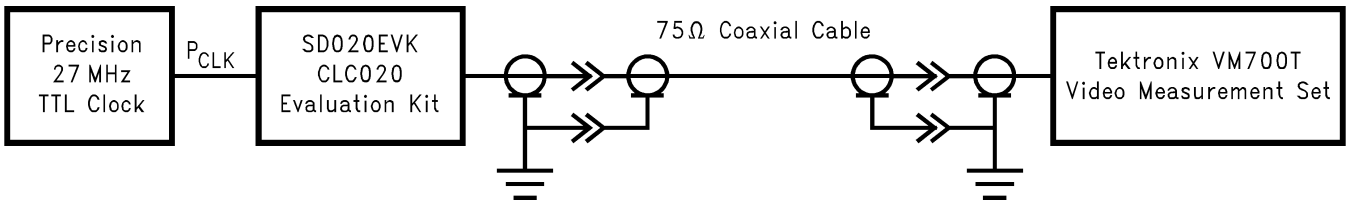


Figure 10. Jitter Test Circuit

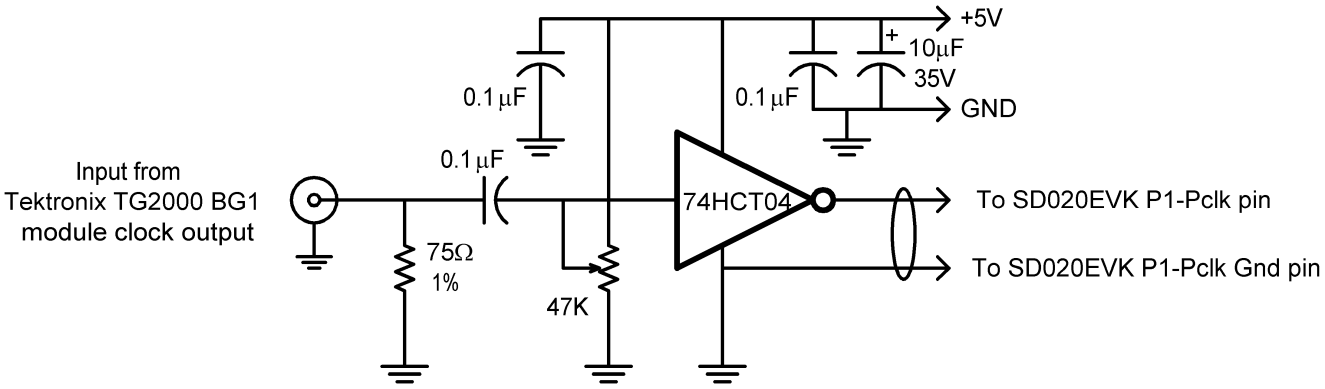


Figure 11. ECL-to-TTL/CMOS level converter/amplifer

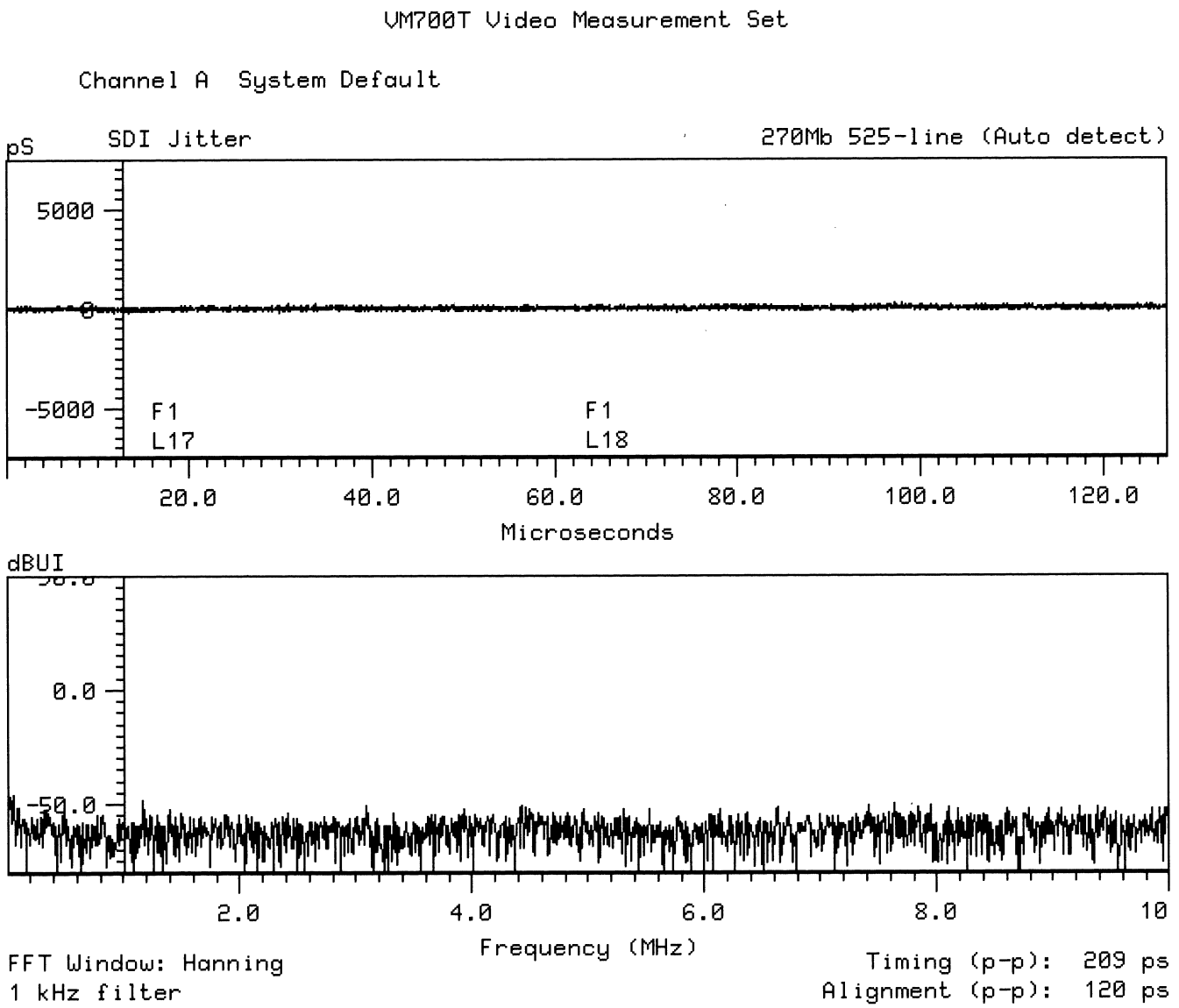


Figure 12. Jitter Plots

PCB LAYOUT AND POWER SYSTEM BYPASS RECOMMENDATIONS

Circuit board layout and stack-up for the CLC020 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5× the power supply voltage being used. It is recommended practice to use two vias at each power pin of the CLC020 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

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The outer layers of the PCB may be flooded with additional V_{SS} (ground) plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the V_{SS} power supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

In especially noisy power supply environments, such as is often the case when using switching power supplies, separate filtering may be used at the CLC020's VCO and output driver power pins. The CLC020 was designed for this situation. The digital section, VCO and output driver power supply feeds are independent (see PIN DESCRIPTIONS table and Pinout Drawing for details). Supply filtering may take the form of L-section or pi-section, L-C filters in series with these V_{DD} inputs. Such filters are available in a single package from several manufacturers. Despite being independent feeds, all device power supplies should be applied simultaneously as from a common source. The CLC020 is free from power supply latch-up caused by circuit-induced delays between the device's three separate power feed systems.

REPLACING THE GENNUM GS9022

The CLC020 is form-fit-function compatible with the Gennum GS9022. The CLC020 can improve the performance of GS9022 applications using the existing PCB layout with the removal of certain components or changes to component values. New layouts using the CLC020 will benefit from the greatly reduced ancilliary component count and more compact layout.

The CLC020 does not require external VCO filtering components. The external VCO filtering components at pin 17 of the GS9022 may remain connected to the CLC020 without complications. It is suggested that these be removed from the circuit board. The CLC020 uses pin 17 for its test pattern generator enable function. You will find the TPG function very useful when you make this change.

Remove the C_{OSC} capacitor used by the GS9022 at pin 26. The CLC020 uses pin 26 as the BIST pass/fail indicator output. You may attach a LED as an indicator to this pin, if desired. LED current should be limited to 10 mA maximum. The same LED type and current limiting resistor shown in Figure 9 at the Lock Detect output may be used for this indicator function.

Remove any capacitor attached to pin 19. A capacitor attached to pin 19 will cause distortion of the output V_{OH} level. The former data rate setting resistor, R_{VCO}, at pin 19 now functions as the output level setting resistor, R_{REF}. It must be changed to a 1.69 kΩ, 1% value for correct output level setting.

The input series resistors and the P_{CLK} risetime filter capacitor used with the GS9022 are not needed for the CLC020. These components should be removed from the circuit board and the resistors replaced by short circuits (0Ω resistors). These series resistors will increase input signal rise and fall times if left on the board.

The CLC020 has current-mode serial cable driver outputs. These outputs have very high internal generator resistance as one would expect of a current source. Though these current-mode outputs can produce the equivalent drive voltages into the load, it is necessary to change and simplify the typical GS9022 output circuit normally recommended for that device. The output load resistors at pins 22 and 23 must be changed to 75Ω, 1% values. These resistors become the back-matching loads across which the CLC020's outputs develop drive voltage. The series back-matching resistors used on the GS9022 should be removed and replaced with short circuits. The risetime compensating capacitors across these resistors should be removed.

Pin 28 on the CLC020 is V_{SS} and must be connected to the negative supply or ground. On layouts designed to mount the GS9022, the series R-C network connected to this pin should be replaced by short circuits (0Ω resistors). The pull-up resistor connected to the Lock Detect output, pin 14, should be removed. It may be replaced by a LED and current limiting resistor connected to V_{SS} if a visual lock indicator is desired.

The CLC020 has an internal pull-down at the $\overline{\text{Sync Detect Enable}}$ input and may be left unconnected in SMPTE video-only applications.

The CLC020 has independent power supply pins for the VCO, V_{SSO}, pin 15 and V_{DDO}, pin 16. The CLC020 has an output driver negative supply, V_{SSSD}, at pin 21. The output driver positive supply, V_{DDSD}, is pin 24 (as on the GS9022). On new layouts, additional power supply filtering may be added at these pins, if desired.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CLC020BCQ	ACTIVE	PLCC	FN	28	35	TBD	Call TI	Call TI	0 to 70	CLC020BCQ	Samples
CLC020BCQ/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	SN	Level-2A-245C-4 WEEK	0 to 70	CLC020BCQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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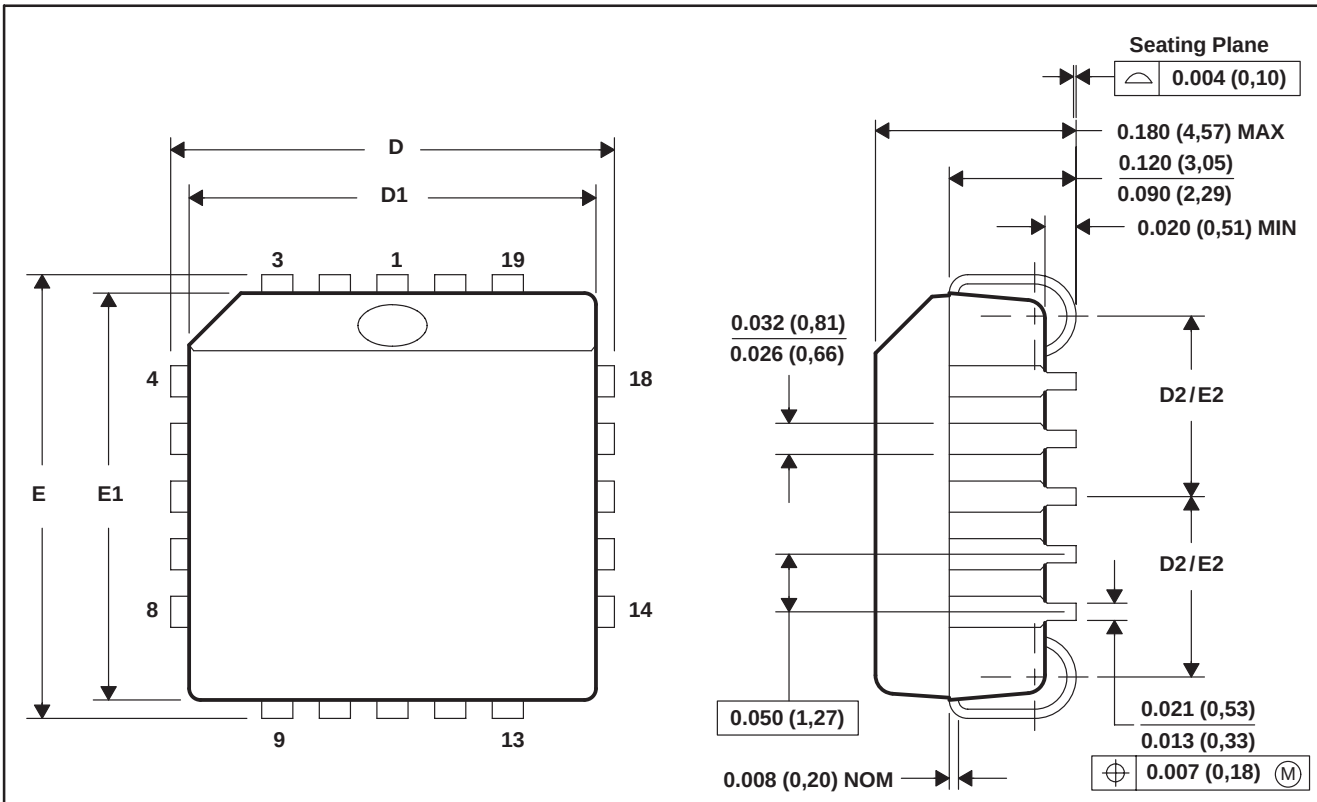
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MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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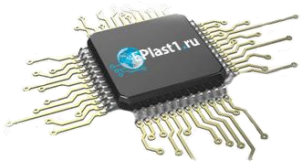
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