Operation temperature condition -40 °C ~85 °C

# SDRAM

# 2M x 16 Bit x 4 Banks Synchronous DRAM

### FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
- CAS Latency (2 & 3)
- Burst Length (1, 2, 4, 8 & full page)
- Burst Type ( Sequential & Interleave )
- All inputs are sampled at the positive going edge of the system clock
- Burst Read single write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

# ORDERING INFORMATION

| PRODUCT NO.      | MAX FREQ. | PACKAGE | COMMENTS |  |  |
|------------------|-----------|---------|----------|--|--|
| M12L128168A-5TIG | 200MHz    | TSOP II | Pb-free  |  |  |
| M12L128168A-5BIG | 200MHz    | BGA     | Pb-free  |  |  |
| M12L128168A-6TIG | 166MHz    | TSOP II | Pb-free  |  |  |
| M12L128168A-6BIG | 166MHz    | BGA     | Pb-free  |  |  |
| M12L128168A-7TIG | 143MHz    | TSOP II | Pb-free  |  |  |
| M12L128168A-7BIG | 143MHz    | BGA     | Pb-free  |  |  |

#### **GENERAL DESCRIPTION**

The M12L128168A is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 16 bits. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

#### **Pin Arrangement (Top View)**

|        |       |        | $\cap$ |            |                       |                          |   |   |   |                              |   |                   |
|--------|-------|--------|--------|------------|-----------------------|--------------------------|---|---|---|------------------------------|---|-------------------|
| Vdd 🗖  | 1 54  | 🗆 Vss  | 0      | 1          | 2                     | 3                        | 4 | 5 | 6 | 7                            | 8   | 9                 |
| DQ0 🗖  | 2 53  | DQ15   | ſ      | $\frown$   |                       |                          |   |   |   |                              |   | $\frown$          |
| Vddq 🗖 | 3 52  | 🗖 Vssq | Α      | (vss)      | (DQ15)                | (vssq)                   |   |   |   | (VDDQ)                       | (DQ0)                                     | (VDD)             |
| DQ1 🗖  | 4 51  | 🗖 DQ14 |        | $\bigcirc$ | $\smile$              | $\bigcirc$               |   |   |   | $\smile$                     | $\bigcirc$                                | $\smile$          |
| DQ2 🗖  | 5 50  | 🗖 DQ13 | _      | $\bigcap$  | $\bigcap$             |                          |   |   |   | $\square$                    | $\square$                                 |                   |
| Vssq 🗖 | 6 49  | 🗖 Vddq | в      | (DQ14)     | (DQ13)                | VDDQ                     |   |   |   | vssq                         | (DQ2)                                     |                   |
| DQ3 🗖  | 7 48  | DQ12   |        | $\sim$     | $\leq$                | $\leq$                   |   |   |   | $\leq$                       | $\leq$                                    | $\leq$            |
| DQ4 🗖  | 8 47  | 🗖 DQ11 | C      |            |                       | (vsso)                   |   |   |   |                              |   |                   |
| Vddq 🗖 | 9 46  | 🗖 Vssq | Ŭ      |            |                       |                          |   |   |   | $\bigcirc$                   | $\bigcirc$                                |                   |
| DQ5 🗖  | 10 45 | DQ10   |        | $\bigcirc$ | $\bigcirc$            | $\frown$                 |   |   |   | $\bigcirc$                   | $\frown$                                  | $\frown$          |
| DQ6 🗖  | 11 44 | DQ9    | D      | (DQ10)     | ( DQ9 )               | (VDDQ)                   |   |   |   | (vssq)                       | ( DQ6 )                                   | ( DQ5 )           |
| Vssq 🗖 | 12 43 | 🗖 Vddq |        | $\bigcirc$ | $\smile$              | $\bigcirc$               |   |   |   | $\smile$                     | $\bigcirc$                                | $\smile$          |
| DQ7 🗖  | 13 42 | DQ8    |        | $\bigcap$  | $\frown$              | $\frown$                 |   |   |   | $\frown$                     | $\frown$                                  | $\bigcirc$        |
| Vdd 🗖  | 14 41 | 🗆 Vss  | E      | ( DQ8 )    |                       | (vss)                    |   |   |   | (VDD)                        | (LDQM)                                    | (DQ7)             |
| LDQM 🗖 | 15 40 | D NC   |        | $\smile$   | $\smile$              | $\smile$                 |   |   |   | $\sim$                       | $\smile$                                  | $\smile$          |
| WE 🗆   | 16 39 | UDQM   | _      |            |                       |                          |   |   |   |                              |   |                   |
| CAS 🗆  | 17 38 |        | Г      | UDQM       |                       | CKE                      |   |   |   | CAS                          | RAS                                       | (WE)              |
| RAS 🗖  | 18 37 | CKE    |        | $\sim$     | $\sim$                | $\sim$                   |   |   |   | $\sim$                       | $\sim$                                    | $\sim$            |
| CS 🗆   | 19 36 | D NC   | G      | ( NC )     | (A11)                 | ( A9 )                   |   |   |   | (A13)                        | (A12)                                     | $(\overline{cs})$ |
| A13 🗖  | 20 35 | A11    |        | $\bigcirc$ | $\bigcirc$            | $\bigcirc$               |   |   |   | $\smile$                     | $\bigcirc$                                | $\bigcirc$        |
| A12 🗖  | 21 34 | ☐ A9   |        | $\bigcirc$ | $\frown$              | $\bigcirc$               |   |   |   | $\frown$                     | $\frown$                                  | $\bigcirc$        |
| A10/AP | 22 33 | 🗆 A8   | н      | ( A8 )     | ( A7 )                | ( A6 )                   |   |   |   | ( A0 )                       | (A1)                                      | ( A10 )           |
| A0 🗖   | 23 32 | 🗖 A7   |        | $\sim$     | $\leq$                | $\leq$                   |   |   |   | $\leq$                       | $\leq$                                    | $\leq$            |
| A1 🗖   | 24 31 | 🗖 A6   |        | (vee)      |                       | $\left( \Lambda \right)$ |   |   |   | $\left( \Lambda^{3} \right)$ | $\begin{pmatrix} \Lambda 2 \end{pmatrix}$ |                   |
| A2 🗖   | 25 30 | 🗖 A5   | J      | (100)      | $\left( ^{n}\right) $ |                          |   |   |   | $\langle \gamma \rangle$     | $\langle \gamma \rangle$                  |                   |
| Аз 🗖   | 26 29 | 🗆 A4   |        | $\sim$     | $\sim$                | $\sim$                   |   |   |   | $\sim$                       | $\sim$                                    | $\smile$          |
| Vdd 🗖  | 27 28 | 🗆 Vss  |        |            |                       |                          |   |   |   |                              |   |                   |
|        |       |        |        |            |                       |                          |   |   |   |                              |   |                   |

Elite Semiconductor Memory Technology Inc.

# ESMT

### **BLOCK DIAGRAM**



#### PIN DESCRIPTION

| PIN                                 | NAME                       | INPUT FUNCTION   |
|-------------------------------------|----------------------------|--|
| CLK                                 | System Clock               | Active on the positive going edge to sample all inputs   |
| CS                                  | Chip Select                | Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM  |
| СКЕ                                 | Clock Enable               | Masks system clock to freeze operation from the next clock cycle.<br>CKE should be enabled at least one cycle prior new command.<br>Disable input buffers for power down in standby. |
| A0 ~ A11                            | Address                    | Row / column address are multiplexed on the same pins.<br>Row address : RA0~RA11, column address : CA0~CA8   |
| A12 , A13                           | Bank Select Address        | Selects bank to be activated during row address latch time.<br>Selects bank for read / write during column address latch time.   |
| RAS                                 | Row Address Strobe         | Latches row addresses on the positive going edge of the CLK with $\overrightarrow{\text{RAS}}$ low. (Enables row access & precharge.)  |
| CAS                                 | Column Address Strobe      | Latches column address on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. (Enables column access.)  |
| WE                                  | Write Enable               | Enables write operation and row precharge.<br>Latches data in starting from $\overline{CAS}$ , $\overline{WE}$ active.   |
| L(U)DQM                             | Data Input / Output Mask   | Makes data output Hi-Z, $t_{SHZ}$ after the clock and masks the output. Blocks data input when L(U)DQM active.   |
| DQ0 ~ DQ15                          | Data Input / Output        | Data inputs / outputs are multiplexed on the same pins.  |
| V <sub>DD</sub> / V <sub>SS</sub>   | Power Supply / Ground      | Power and ground for the input buffers and the core logic.   |
| V <sub>DDQ</sub> / V <sub>SSQ</sub> | Data Output Power / Ground | Isolated power supply and ground for the output buffers to provide improved noise immunity.  |
| N.C                                 | No Connection              | This pin is recommended to be left No Connection on the device.  |

#### **ABSOLUTE MAXIMUM RATINGS**

| Parameter   | Symbol                             | Value      | Unit |
|---|------------------------------------|------------|------|
| Voltage on any pin relative to $V_{\mbox{\scriptsize SS}}$    | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6 | V    |
| Voltage on $V_{\text{DD}}$ supply relative to $V_{\text{SS}}$ | $V_{DD}, V_{DDQ}$                  | -1.0 ~ 4.6 | V    |
| Storage temperature   | TSTG                               | -55 ~ +150 | °C   |
| Power dissipation   | PD                                 | 1          | W    |
| Short circuit current   | I <sub>OS</sub>                    | 50         | mA   |

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded. Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

#### **DC OPERATING CONDITION**

Recommended operating conditions (Voltage referenced to  $V_{SS}$  = 0V,  $T_A$  = -40 to 85 °C )

| Parameter                 | Symbol            | Min  | Тур | Max     | Unit | Note              |
|---------------------------|-------------------|------|-----|---------|------|-------------------|
| Supply voltage            | $V_{DD}, V_{DDQ}$ | 3.0  | 3.3 | 3.6     | V    |                   |
| Input logic high voltage  | VIH               | 2.0  | 3.0 | VDD+0.3 | V    | 1                 |
| Input logic low voltage   | VIL               | -0.3 | 0   | 0.8     | V    | 2                 |
| Output logic high voltage | V <sub>OH</sub>   | 2.4  | -   | -       | V    | Іон <b>= -2mA</b> |
| Output logic low voltage  | V <sub>OL</sub>   | -    | -   | 0.4     | V    | lo∟ = 2mA         |
| Input leakage current     | IIL               | -5   | -   | 5       | μΑ   | 3                 |
| Output leakage current    | I <sub>OL</sub>   | -5   | -   | 5       | μΑ   | 4                 |

Note:

 $\begin{array}{ll} 1. \ V_{IH}(max) = 4.6V \ AC \ for \ pulse \ width \ \leq \ 10ns \ acceptable. \\ 2. \ V_{IL(min)} = -1.5V \ AC \ for \ pulse \ width \ \leq \ 10ns \ acceptable. \\ 3. \ Any \ input \ 0V \ \leq \ V_{IN} \ \leq \ V_{DD} + 0.3V, \ all \ other \ pins \ are \ not \ under \ test = \ 0V. \\ \end{array}$ 

4. Dout is disabled ,  $0V \leq v_{OUT} \leq V_{DD}$ .

### **CAPACITANCE** ( $V_{DD}$ = 3.3V, $T_A$ = 25 °C, f = 1MHZ)

| Parameter   | Symbol           | Min | Мах | Unit |
|---|------------------|-----|-----|------|
| Input capacitance (A0 ~ A11, A13 ~ A12)                     | C <sub>IN1</sub> | 2.5 | 4   | pF   |
| Input capacitance<br>(CLK, CKE, CS, RAS, CAS, WE & L(U)DQM) | C <sub>IN2</sub> | 2.5 | 4   | pF   |
| Data input/output capacitance (DQ0 ~ DQ15)                  | C <sub>OUT</sub> | 2   | 6.5 | pF   |

Operation temperature condition -40 °C ~85 °C

#### **DC CHARACTERISTICS**

Recommended operating condition unless otherwise noted  $\,\cdot\,$  T\_A = -40 to 85  $^\circ C$ 

| Parameter  | Symbol             | Test Condition  | CAS   |     | Versior | ı   | Unit | Note |
|--|--------------------|---|---|-----|---------|-----|------|------|
|  | -,                 |   | Latency   | -5  | -6      | -7  |      |      |
| Operating Current<br>(One Bank Active)           | I <sub>CC1</sub>   | Burst Length = 1, $t_{RC} \ge t_{RC(min)}$ , $I_{OL}$ =   | = 0 mA  | 170 | 160     | 140 | mA   | 1,2  |
| Precharge Standby Current                        | I <sub>CC2P</sub>  | $CKE \le V_{IL}(max), tcc = t_{CK(MIN)}$  |   |     | 2       |     | mA   |      |
| in power-down mode                               | I <sub>CC2PS</sub> | CKE & CLK $\leq$ V <sub>IL</sub> (max), t <sub>CC</sub> = $\infty$  |   |     | 2       |     |      |      |
| Precharge Standby Current                        | I <sub>CC2N</sub>  | $\label{eq:cke} \begin{split} CKE \geq & V_{IH(min)}, \ \overline{CS} \geq \ V_{IH(min)}, \ t_{CC} = \\ Input \ signals \ are \ changed \ one \ time \end{split}$ | = t <sub>CK(MIN)</sub><br>e during 2t <sub>ck</sub> |     | 45      | mA  |      |      |
| in non power-down mode                           | I <sub>CC2NS</sub> | $CKE \ge V_{IH(min)}, \ CLK \le V_{IL}(max), \ tcc \\ input \ signals \ are \ stable$   |   | 25  |         |     |      |      |
| Active Standby Current                           | I <sub>CC3P</sub>  | $CKE \le V_{IL}(max), t_{CC} = t_{CK(MIN)}$   |   | 6   |         | mΔ  |      |      |
| in power-down mode                               | I <sub>CC3PS</sub> | CKE & CLK $\leq$ V <sub>IL</sub> (max), t <sub>CC</sub> = $\infty$  |   | 6   | III V   |     |      |      |
| Active Standby Current<br>in non power-down mode | I <sub>CC3N</sub>  | $CKE \ge V_{H}(min), \ \overline{CS} \ge V_{H}(min), t$<br>Input signals are changed one time<br>All other pins $\ge V_{DD}$ -0.2V or $\le 0$                     | cc=15ns<br>e during 2clks<br>0.2V                   |     | 55      | mA  |      |      |
| (One Bank Active)                                | I <sub>CC3NS</sub> | $CKE \geq V_{IH(min)}, \ CLK \leq V_{IL}(max), \ t_{CC}$ input signals are stable   | = ∞   |     | 35      |     | mA   |      |
| Operating Current<br>(Burst Mode)                | I <sub>CC4</sub>   | I <sub>OL</sub> = 0 mA, Page Burst, 2 Banks a   | 280   | 210 | 180     | mA  | 1,2  |      |
| Refresh Current                                  | I <sub>CC5</sub>   | $t_{\text{RC}} \ge t_{\text{RC(min)}}$  | 280   | 210 | 180     | mA  |      |      |
| Self Refresh Current                             | I <sub>CC6</sub>   | CKE≤0.2V  |   | 2   |         |     | mA   |      |

Note : 1. Measured with outputs open.

2. Input signals are changed one time during 2 CLKS.

Operation temperature condition -40 ℃ ~85 ℃

### AC OPERATING TEST CONDITIONS (V\_{DD} = $3.3V\pm0.3V$ , $T_{A}$ = -40 to $85\,^{\circ}C$ )

| Parameter                                 | Value       | Unit |
|---|-------------|------|
| Input levels (Vih/Vil)                    | 2.4/0.4     | V    |
| Input timing measurement reference level  | 1.4         | V    |
| Input rise and fall-time                  | tr/tf = 1/1 | ns   |
| Output timing measurement reference level | 1.4         | V    |
| Output load condition                     | See Fig. 2  |      |







(Fig. 2) AC Output Load Circuit

### **OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

| Parar  | neter           | Symbol                |    | Version         |    | Unit            | Note |  |  |
|--|-----------------|-----------------------|----|-----------------|----|-----------------|------|--|--|
|  |                 | _                     | -5 | -6              | -7 |                 |      |  |  |
| Row active to row active delay                   |                 | t <sub>RRD(min)</sub> | 10 | 12              | 14 | ns              | 1    |  |  |
| RAS to CAS de                                    | elay            | t <sub>RCD(min)</sub> | 15 | 18              | 20 | ns              | 1    |  |  |
| Row precharge tir                                | ne              | t <sub>RP(min)</sub>  | 15 | ns              | 1  |                 |      |  |  |
| Row active time                                  |                 | t <sub>RAS(min)</sub> | 38 | ns              | 1  |                 |      |  |  |
|  | Now active time |                       |    | us              |    |                 |      |  |  |
| Row cycle time                                   | @ Operating     | t <sub>RC(min)</sub>  | 53 | 58              | 63 | ns              | 1    |  |  |
|  | @ Auto refresh  | t <sub>RFC(min)</sub> | 55 | 60              | 70 | ns              | 1,5  |  |  |
| Last data in to col                              | . address delay | t <sub>CDL(min)</sub> |    | 1               |    |                 |      |  |  |
| Last data in to row precharge                    |                 | t <sub>RDL(min)</sub> |    | 2               |    | t <sub>ск</sub> | 2    |  |  |
| Last data in to burst stop t <sub>BDL(min)</sub> |                 |                       |    | t <sub>ск</sub> | 2  |                 |      |  |  |
| Refresh period (4,                               | ,096 rows)      | t <sub>REF(max)</sub> |    | 64              |    | ms              | 6    |  |  |



Operation temperature condition -40 ℃ ~85 ℃

| Parameter                          |        | Symbol                |    | Unit            | Note |      |      |
|------------------------------------|--------|-----------------------|----|-----------------|------|------|------|
|                                    |        | Cymbol                | -5 | -6              | -7   | Onic | NOLE |
| Col. address to col. address delay |        | t <sub>CCD(min)</sub> |    | t <sub>CK</sub> | 3    |      |      |
| Number of valid                    | CAS la | atency = 3            |    | 2               |      | еа   | 4    |
| Output data                        | CAS la | atency = 2            |    | 1               |      | u    | •    |

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

- 5. A new command may be given  $t_{RFC}$  after self refresh exit.
- 6. A maximum of eight consecutive AUTO REFRESH commands (with t<sub>RFCmin</sub>) can be posted to any given SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8x15.6 μ s.)

#### AC CHARACTERISTICS (AC operating condition unless otherwise noted)

| Para                     | neter           | Symbol           | -   | 5    | -6  |      | -7  |      | Unit | Note |
|--------------------------|-----------------|------------------|-----|------|-----|------|-----|------|------|------|
|                          |                 |                  | MIN | MAX  | MIN | MAX  | MIN | MAX  |      |      |
| CLK ovelo timo           | CAS latency = 3 | taa              | 5   | 1000 | 6   | 1000 | 7   | 1000 | 200  | 1    |
|                          | CAS latency = 2 | LCC              | 10  | 1000 | 10  | 1000 | 10  | 1000 | 115  |      |
| CLK to valid             | CAS latency = 3 | •                |     | 4.5  |     | 5.4  |     | 5.4  | ns   | 1.0  |
| output delay             | CAS latency = 2 | LSAC             |     | 6    |     | 6    |     | 6    |      | 1,2  |
| Output data<br>hold time | CAS latency = 3 |                  | 2   |      | 2.5 |      | 2.5 |      | ns   | 2    |
|                          | CAS latency = 2 | LOH              | 2   |      | 2.5 |      | 2.5 | 2.5  |      | 2    |
| CLK high pulsh widt      | h               | t <sub>CH</sub>  | 2   |      | 2.5 |      | 2.5 |      | ns   | 3    |
| CLK low pulsh width      | ı               | t <sub>CL</sub>  | 2   |      | 2.5 |      | 2.5 |      | ns   | 3    |
| Input setup time         |                 | t <sub>ss</sub>  | 1.5 |      | 1.5 |      | 1.5 |      | ns   | 3    |
| Input hold time          |                 | t <sub>SH</sub>  | 1   |      | 1   |      | 1   |      | ns   | 3    |
| CLK to output in Low-Z   |                 | t <sub>SLZ</sub> | 1   |      | 1   |      | 1   |      | ns   | 2    |
| CLK to output            | CAS latency = 3 | touz             |     | 4.5  |     | 5.4  |     | 5.4  | ne   | _    |
| in Hi-Z                  | CAS latency = 2 | <sup>COHZ</sup>  |     | 6    |     | 6    |     | 6    | 115  | _    |

Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns. (tr/2 - 0.5) ns should be considered.

3. Assumed input rise and fall time (tr & tf) =1ns. If tr & tf is longer than 1ns. transient time compensation should be considered. i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.

Operation temperature condition -40 °C ~85 °C

#### SIMPLIFIED TRUTH TABLE

|                                     | COMMAND                        |                | CKEn-1 | CKEn | CS | RAS | CAS | WE | DQM | A13<br>A12 | A10/AP  | A11<br>A9~A0      | Note |
|-------------------------------------|--------------------------------|----------------|--------|------|----|-----|-----|----|-----|------------|---------|-------------------|------|
| Register                            | Mode Regis                     | ster set       | Н      | Х    | L  | L   | L   | L  | Х   |            | OP CO   | DE                | 1,2  |
|                                     | Auto Refres                    | sh             | Ц      | Н    |    |     |     | Г  | v   |            | v       |                   | 3    |
| Pefresh                             | Solf                           | Entry          | 11     | L    | L  | L   | L   | 11 | ^   |            | ^       |                   | 3    |
| Reliesh                             | Refresh                        | Evit           |        | н    | L  | Н   | Н   | Н  | Х   |            | x       |                   | 3    |
|                                     | Refredit                       | Exit           |        |      | Н  | Х   | Х   | Х  | Х   |            | ~       |                   | 3    |
| Bank A                              | ctive & Row                    | Addr.          | Н      | Х    | L  | L   | Н   | Н  | Х   | V          | Row     | Address           |      |
| Read &                              | Auto Pre                       | charge Disable | н      | x    |    | н   |     | н  | x   | v          | L       | Column<br>Address | 4    |
| Column Address Auto Prech           | charge Enable                  |                | ~      |      |    | -   |     | ^  | •   | н          | (A0~A8) | 4,5               |      |
| Write &                             | Write & Auto Precharge Disable |                | н      | x    |    | н   | L   |    | ×   | v          | L       | Column            | 4    |
| Column Address Auto Prech           |                                | charge Enable  |        | ^    | L  |     |     | L  | ^   | V          | Н       | (A0~A8)           | 4,5  |
| Burst Stop                          |                                | Н              | Х      | L    | Н  | Н   | L   | Х  |     | Х          | -       | 6                 |      |
| Bank Sele                           |                                | ection         | н      |      |    | ī   | н   |    | ×   | V          | L X     |                   |      |
| Treenarge                           | All Banks                      |                |        | ~    |    |     |     | -  |     | Х          | Н       |                   |      |
|                                     |                                | Entry          | н      |      | Н  | Х   | х   | х  | x   |            |         |                   |      |
| Clock Suspend of<br>Active Power Do | or<br>wn                       | Lituy          |        | L    | L  | V   | V   | V  |     |            | х       |                   |      |
|                                     |                                | Exit           | L      | н    | х  | х   | х   | х  | х   |            |         |                   |      |
|                                     |                                | Entry.         | ц      |      | Н  | х   | х   | Х  | v   |            |         |                   |      |
| Dracheres Devis                     |                                | Entry          |        | L    | L  | н   | Н   | Н  |     |            |         |                   |      |
| Precharge Powe                      | r Down Mod                     |                |        |      | н  | х   | х   | х  | V   |            | Х       |                   |      |
|                                     |                                | Exit           |        | н    | L  | V   | V   | V  |     |            |         |                   |      |
| DQM                                 |                                |                | Н      |      |    | Х   |     |    | V   |            | Х       |                   | 7    |
| No Operating Co                     | mmand                          |                | Ц      | v    | Н  | Х   | Х   | Х  | ~   |            | v       |                   |      |
| No Operating Co                     |                                |                |        | ^    | L  | Н   | Н   | Н  |     |            | X       |                   |      |

(V = Valid , X = Don't Care. H = Logic High , L = Logic Low )

Note : 1.OP Code : Operating Code

A0~A11 & A13~A12 : Program keys. (@ MRS)

2.MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3.Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge of command is meant by "Auto".

Auto/self refresh can be issued only at all banks idle state.

4.A13~A12 : Bank select addresses.

If A13 and A12 are "Low" at read ,write , row active and precharge ,bank A is selected.

If A13 is "Low" and A12 is "High" at read ,write , row active and precharge ,bank B is selected.

If A13 is "High" and A12 is "Low" at read ,write , row active and precharge ,bank C is selected.

If A13 and A12 are "High" at read ,write , row active and precharge ,bank D is selected

If A10/AP is "High" at row precharge , A13 and A12 is ignored and all banks are selected.

5. During burst read or write with auto precharge. new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6.Burst stop command is valid at every burst length.

7.DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)

Operation temperature condition -40 °C ~85 °C

#### MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

| Address  | A13~A12 | A11~A10/AP | A9     | A8 | A7 | A6          | A5 | A4 | A3 | A2           | A1 | A0  |
|----------|---------|------------|--------|----|----|-------------|----|----|----|--------------|----|-----|
| Function | RFU     | RFU        | W.B.L. | ТМ |    | CAS Latency |    |    | BT | Burst Length |    | gth |

| Test Mode |    |                   | CAS Latency |    |    |          | Bu | rst Type   | Burst Length |    |    |           |          |  |
|-----------|----|-------------------|-------------|----|----|----------|----|------------|--------------|----|----|-----------|----------|--|
| A8        | A7 | Туре              | A6          | A5 | A4 | Latency  | A3 | Туре       | A2           | A1 | A0 | BT = 0    | BT = 1   |  |
| 0         | 0  | Mode Register Set | 0           | 0  | 0  | Reserved | 0  | Sequential | 0            | 0  | 0  | 1         | 1        |  |
| 0         | 1  | Reserved          | 0           | 0  | 1  | Reserved | 1  | Interleave | 0            | 0  | 1  | 2         | 2        |  |
| 1         | 0  | Reserved          | 0           | 1  | 0  | 2        |    |            | 0            | 1  | 0  | 4         | 4        |  |
| 1         | 1  | Reserved          | 0           | 1  | 1  | 3        |    |            | 0            | 1  | 1  | 8         | 8        |  |
|           |    |                   | 1           | 0  | 0  | Reserved |    |            | 1            | 0  | 0  | Reserved  | Reserved |  |
|           |    |                   | 1           | 0  | 1  | Reserved |    |            | 1            | 0  | 1  | Reserved  | Reserved |  |
|           |    |                   | 1           | 1  | 0  | Reserved |    |            | 1            | 1  | 0  | Reserved  | Reserved |  |
|           |    |                   | 1           | 1  | 1  | Reserved |    |            | 1            | 1  | 1  | Full Page | Reserved |  |

Full Page Length : 512

#### POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pin are NOP condition at the inputs.

2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3. Issue precharge commands for all banks of the devices.

4. Issue 2 or more auto-refresh commands.

5. Issue mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. RFU(Reserved for future use) should stay "0" during MRS cycle.

2. If A9 is high during MRS cycle, "Burst Read single write" function will be enabled.

Operation temperature condition -40 °C ~85 °C

### **BURST SEQUENCE (BURST LENGTH = 4)**

| Initial Adrress |    |   | Sequ | ential |   | Interleave |   |   |   |  |  |
|-----------------|----|---|------|--------|---|------------|---|---|---|--|--|
| A1              | A0 |   |      |        |   |            |   |   |   |  |  |
| 0               | 0  | 0 | 1    | 2      | 3 | 0          | 1 | 2 | 3 |  |  |
| 0               | 1  | 1 | 2    | 3      | 0 | 1          | 0 | 3 | 2 |  |  |
| 1               | 0  | 2 | 3    | 0      | 1 | 2          | 3 | 0 | 1 |  |  |
| 1               | 1  | 3 | 0    | 1      | 2 | 3          | 2 | 1 | 0 |  |  |

### **BURST SEQUENCE (BURST LENGTH = 8)**

| Initial |    |    | Sequential |   |   |   |   |   | Interleave |   |   |   |   |   |   |   |   |   |
|---------|----|----|------------|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|
| A2      | A1 | A0 |            |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |
| 0       | 0  | 0  | 0          | 1 | 2 | 3 | 4 | 5 | 6          | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0       | 0  | 1  | 1          | 2 | 3 | 4 | 5 | 6 | 7          | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0       | 1  | 0  | 2          | 3 | 4 | 5 | 6 | 7 | 0          | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0       | 1  | 1  | 3          | 4 | 5 | 6 | 7 | 0 | 1          | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1       | 0  | 0  | 4          | 5 | 6 | 7 | 0 | 1 | 2          | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1       | 0  | 1  | 5          | 6 | 7 | 0 | 1 | 2 | 3          | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1       | 1  | 0  | 6          | 7 | 0 | 1 | 2 | 3 | 4          | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1       | 1  | 1  | 7          | 0 | 1 | 2 | 3 | 4 | 5          | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

#### **DEVICE OPERATIONS**

#### CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V<sub>IL</sub> and V<sub>IH</sub>. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

### **CLOCK ENABLE(CKE)**

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK +  $t_{SS}$ " before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

#### BANK ADDRESSES (A13~A12)

This SDRAM is organized as four independent banks of 2,097,152 words x 16 bits memory arrays. The A13~A12 inputs are latched at the time of assertion of  $\overline{RAS}$  and  $\overline{CAS}$  to select the bank to be used for the operation. The banks addressed A13~A12 are latched at bank active, read, write, mode register set and precharge operations.

#### ADDRESS INPUTS (A0~A11)

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with  $\overline{RAS}$  and A13~A12 during bank active command. The 9 bit column addresses are latched along with  $\overline{CAS}$ ,  $\overline{WE}$  and A13~A12 during read or with command.

#### NOP and DEVICE DESELECT

When  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  are high , The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting  $\overline{CS}$  high.  $\overline{CS}$  high disables the command decoder so that  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and all the address inputs are ignored.

#### **POWER-UP**

- 1.Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
- 2.Maintain stable power, stable clock and NOP input condition for minimum of 200us.
- 3.Issue precharge commands for both banks of the devices.
- 4.Issue 2 or more auto-refresh commands.
- 5.Issue a mode register set command to initialize the mode register.
  - cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

#### **MODE REGISTER SET (MRS)**

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,

 $\overrightarrow{CAS}$  and  $\overrightarrow{WE}$  (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and A13~A12 in the

same cycle as  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and A13~A12. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and A13~A12 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

#### **BANK ACTIVATE**

The bank activate command is used to select a random row in an idle bank. By asserting low on  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of  $t_{\text{RCD}(\text{min})}$  from the time of bank activation.  $t_{\text{RCD}}$  is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by

### **DEVICE OPERATIONS (Continued)**

dividing t<sub>RCD(min)</sub> with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. t<sub>RRD(min)</sub> specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to  $t_{\text{RCD}}$  specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t<sub>RAS(min)</sub>. Every SDRAM bank activate command must satisfy t<sub>RAS(min)</sub> specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t<sub>RAS</sub> (max) and t<sub>RAS</sub>(max) can be calculated similar to t<sub>RCD</sub> specification.

#### **BURST READ**

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank.

The burst read command is issued by asserting low on CS

and RAS with WE being high on the positive edge of the clock. The bank must be active for at least t<sub>RCD(min)</sub> before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

#### **BURST WRITE**

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on  $\overline{\text{CS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and precharge the bank  $t_{\text{RDL}}$  after the last data input to be written into the active row. See DQM OPERATION also.

#### **DQM OPERATION**

The DQM is used mask input and output operations. It works similar to  $\overline{OE}$  during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

#### PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{WE}$  and A10/AP with valid A13~A12 of the bank to be procharged. The precharge command can be asserted anytime after  $t_{RAS(min)}$  is satisfy from the bank active command in the desired bank. t<sub>RP</sub> is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t<sub>RP</sub> with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t<sub>RAS</sub>(max). Therefore, each bank has to be precharge with t<sub>RAS</sub>(max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

#### AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy  $t_{RAS(min)}$  and " $t_{RP}$ " for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

#### FOUR BANKS PRECHARGE

Four banks can be precharged at the same time by using Precharge all command. Asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,

and  $\overline{\text{WE}}$  with high on A10/AP after all banks have satisfied  $t_{\text{RAS}(\text{min})}$  requirement, performs precharge on all banks. At the end of  $t_{\text{RP}}$  after performing precharge all, all banks are in idle state.

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### **DEVICE OPERATIONS (Continued)**

#### AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on CS, RAS and CAS with high on CKE and WE. The auto refresh command can only be asserted with all banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by  $t_{\text{RFC}(\text{min})}$ . The minimum number of clock cycles required can be calculated by driving t<sub>REC</sub> with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us.

#### SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state

by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and CKE with

high on WE. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of  $t_{RFC}$  before the SDRAM reaches idle state to begin normal operation. It is recommended to use burst 4096 auto refresh cycles immediately before and after self refresh.



#### COMMANDS

#### Mode register set command

 $(\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE} = Low)$ 

The M12L128168A has a mode register that defines how the device operates. In this command, A0 through A13 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when all banks are in idle state.

During 2CLK following this command, the M12L128168A cannot accept any other commands.



**Precharge command** 

 $(\overline{CS}, \overline{RAS} = Low, \overline{CAS}, \overline{WE} = High)$ 

The M12L128168A has four banks, each with 4,096 rows.

This command activates the bank selected by A12 and A13 (BS) and a row address selected by A0 through A11.

This command begins precharge operation of the bank selected by A12 and A13

After this command, the M12L128168A can't accept the activate command to the

(BS). When A10 is High, all banks are precharged, regardless of A12 and A13. When

A10 is Low, only the bank selected by A12 and A13 is precharged.

precharging bank during t<sub>RP</sub> (precharge to activate command period).

This command corresponds to a conventional DRAM's RAS rising.

This command corresponds to a conventional DRAM's RAS falling.



Fig. 2 Row address strobe and bank active command

### CLK CKE H CS RAS CAS WE A12, A13 (Bank select) A10 (Precharge select) Add

Fig. 3 Precharge command

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 $(\overline{CS}, \overline{RAS}, \overline{WE} = Low, \overline{CAS} = High)$ 

#### Write command

#### $(\overline{CS}, \overline{CAS}, \overline{WE} = Low, \overline{RAS} = High)$

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst can be input with this command with subsequent data on following clocks.



Fig. 4 Column address and write command

#### **Read command**

 $(\overline{CS}, \overline{CAS} = Low, \overline{RAS}, \overline{WE} = High)$ 

CBR (auto) refresh command

address is generated internally.

row activate command.

 $(\overline{CS}, \overline{RAS}, \overline{CAS} = Low, \overline{WE}, CKE = High)$ 

Read data is available after  $\overline{CAS}$  latency requirements have been met. This command sets the burst start address given by the column address.

This command is a request to begin the CBR refresh operation. The refresh

After this cycle, all banks will be in the idle (precharged) state and ready for a

During t<sub>RC</sub> period (from refresh command to refresh or activate command), the

Before executing CBR refresh, all banks must be precharged.



Fig. 5 Column address and read command



Fig. 6 Auto refresh command

M12L128168A cannot accept any other command.

Operation temperature condition -40°C ~85°C

CLK

CKE

CS

#### Self refresh entry command

 $(\overline{CS}, \overline{RAS}, \overline{CAS}, CKE = Low, \overline{WE} = High)$ 

After the command execution, self refresh operation continues while CKE remains low. When CKE goes to high, the M12L128168A exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.

| CLK                       |  |
|---------------------------|--|
| CKE                       | Н  |
| CS                        |  |
| RAS                       |  |
| CAS                       |  |
| WE                        |  |
| A12, A13<br>(Bank select) |  |
| A10                       |  |
| Add                       | <i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i> |

Fig. 8 Burst stop command



Fig. 9 No operation

# Burst stop command

No operation

this command.

$$(\overline{CS}, \overline{WE} = Low, \overline{RAS}, \overline{CAS} = High)$$

This command terminates the current burst operation. Burst stop is valid at every burst length.



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 $(\overline{CS} = Low, \overline{RAS}, \overline{CAS}, \overline{WE} = High)$ 

This command is not a execution command. No operations begin or terminate by



Operation temperature condition -40 ℃ ~85 ℃

### **BASIC FEATURE AND FUNCTION DESCRIPTIONS**

#### 1. CLOCK Suspend



2. DQM masks data out Hi-Z after 2CLKs which should masked by CKE "L".
3. DQM masks both data-in and data-out.

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Operation temperature condition -40 °C ~85 °C

### 3. CAS Interrupt (I)



\*Note : 1. By "interrupt" is meant to stop burst read/write by external before the end of burst.

By "  $\overline{CAS}$  interrupt ", to stop burst read/write by  $\overline{CAS}$  access ; read and write.

- 2.  $t_{CCD}$  :  $\overline{CAS}$  to  $\overline{CAS}$  delay. (=1CLK)
- 3.  $t_{\text{CDL}}$  : Last data in to new column address delay. (=1CLK)

Operation temperature condition -40 °C ~85 °C



### 4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



Operation temperature condition -40 °C ~85 °C



\*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

#### 5. Write Interrupted by Precharge & DQM



\*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.

- 2. To inhibit invalid write, DQM should be issued.
  - 3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

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Operation temperature condition -40 ℃ ~85 ℃

### 6. Precharge



#### 7. Auto Precharge



\*Note: 1. t<sub>RDL</sub> : Last data in to row precharge delay.

- 2. Number of valid output data after row precharge : 1,2 for CAS Latency = 2,3 respectively.
- 3. The row active command of the precharge bank can be issued after t<sub>RP</sub> from this point. The new read/write command of other activated bank can be issued from this point. At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

ESMT

M12L128168A

Operation temperature condition -40 °C ~85 °C





#### 9. MRS



\*Note: 1.  $t_{BDL}$ : 1 CLK ; Last data in to burst stop delay.

- Read or write burst stop command is valid at every burst length.
- 2. Number of valid output data after burst stop : 1,2 for CAS latency = 2,3 respectively.
- 3. Write burst is terminated.  $t_{\mbox{\scriptsize BDL}}$  determinates the last data write.
- 4. DQM asserted to prevent corruption of locations D2 and D3.
- 5. Precharge can be issued here or earlier (satisfying t<sub>RAS</sub> min delay) with DQM.
- 6. PRE : All banks precharge, if necessary.
  - MRS can be issued only at all banks precharge state.

Operation temperature condition -40 °C ~85 °C

#### 10. Clock Suspend Exit & Power Down Exit



#### 11. Auto Refresh & Self Refresh



\*Note: 1. Active power down : one or more banks active state.

- 2. Precharge power down : all banks precharge state.
  - The auto refresh is the same as CBR refresh of conventional DRAM. No precharge commands are required after auto refresh command. During t<sub>RFC</sub> from auto refresh command, any other command can not be accepted.
- 4. Before executing auto/self refresh command, all banks must be idle state.
- 5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
- 6. During self refresh entry, refresh interval and refresh operation are performed internally. After self refresh entry, self refresh mode is kept while CKE is low. During self refresh entry, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state. For the time interval of t<sub>RFC</sub> from self refresh exit command, any other command can not be accepted. Before/After self refresh mode, burst auto refresh (4096 cycles) is recommended.



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#### Как с нами связаться

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