# HPUSB, USB, HPPCI and MSP430 Emulators Users Guide

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ANALOG DEVICES

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The USB- and PCI-based emulators have been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The USB- and PCI-based emulators have been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

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# PREFACE

Thank you for purchasing an Analog Devices USB- or PCI-based JTAG emulator. The USB-based emulator family consists of the High-Performance USB JTAG emulator, the USB JTAG emulator, and the MS430 emulator. The USB- and PCI-based emulators are used in conjunction with the VisualDSP++® development environment to create, test, and debug advanced processor application software on all of Analog Devices fixed point and floating point JTAG-based processors.

The HPUSB-ICE system provides state-of-the-art support for JTAG-compliant Analog Devices processors. Key features of the HPUSB-ICE include:

- Plug-n-Play, USB 2.0 compliant
- High-speed USB device
- Windows® 2000, Windows XP, or Windows Vista operation
- Multiple processor I/O voltage support
    - 1.8V, 2.5V, and 3.3V compliance
    - 5V tolerant in all ranges
- Multiprocessor support
- JTAG clock operation up to 50 MHz

The HPPCI-ICE system provides state-of-the-art support for JTAG-compliant Analog Devices processors. Key features of the HPPCI-ICE include:

- Plug-n-Play, PCI 2.2 compliant
- Windows 2000, Windows XP, or Windows Vista operation
- Multiple processor I/O voltage support
    - 1.8V, 2.5V, and 3.3V compliance
    - 5V tolerant in all ranges
- Multiprocessor support
- JTAG clock operation up to 50 MHz

The JTAG clock frequency is dependent on the delay characteristics of the JTAG interface and processor on the target board.

The USB-ICE system provides state-of-the-art support for selected processors within the Analog Devices MCP430 processor family. Key features of the USB-ICE include:

- Plug-n-Play, USB 2.0 compliant
- High-speed USB device
- Windows 2000, Windows XP, or Windows Vista operation
- Multiple processor I/O voltage support
    - 1.8V, 2.5V, and 3.3V compliance
    - 5V tolerant in all ranges
- Multiprocessor support
- JTAG clock operation of 10 MHz

The MSP430-ICE system provides state-of-the-art support for selected processors within the Analog Devices MSP430 processor family. Key features of the MSP430-ICE include:

- Plug-n-Play, USB 2.0 compliant
- Full-speed USB device
- Windows 2000, Windows XP, or Windows Vista operation
- Processor I/O voltage support
    - 3.3V compliance

Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators, go to:
http://www.analog.com/processors/

# Purpose of This Manual

The *HPUSB, USB, HPPCI and MSP430 Emulators User's Guide* provides directions for installing the High-Performance USB-ICE, USB ICE, High-Performance HPPCI-ICE, and MSP430-ICE hardware and software on your PC. The manual also describes how to configure and use the components of the USB- and PCI-based emulators.

# Intended Audience

This manual is intended to help the customer understand the features and operation of the HPUSB-ICE, HPPCI-ICE, USB-ICE, and MSP430-ICE so they can begin using VisualDSP++.

# Manual Contents

The manual consists of:

- Chapter 1, "Getting Started" on page 1-1
  Provides software and hardware installation procedures, PC system requirements, and basic board information.
- Chapter 2, "Hardware Description" on page 2-1
  Provides information on hardware aspects of the USB-based emulators.
- Chapter 3, "Support" on page 3-1
  Provides technical support contact information.
- Chapter 4, "References" on page 4-1
  Provides information on different resources available in developing an application based on an Analog Devices processor.

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  `processor.support@analog.com (World wide support)`
  `processor.europe@analog.com (Europe support)`
  `processor.china@analog.com (China support)`
- Phone questions to **1-800-ANALOGD**

- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

# 1 GETTING STARTED

This chapter provides the information needed to begin using Analog Devices USB- and PCI-based emulators.

This chapter includes the following sections.


- "Contents of Emulator Package" on page 1-2
  Provides a list of the components that are shipped with USB- and PCI-based emulators.
- "PC Configuration" on page 1-2
  Describes the minimal PC requirements.
- "Installation Tasks" on page 1-3
  Provides a step-by-step procedure for setting up the emulator hardware.
- "Attaching the Cable to the Emulation Target" on page 1-6
  Describes how to connect USB, PCI, and MSP43 emulators to your target board.
- "JTAG Frequency Selection" on page 1-9
  Describes how to change the JTAG frequency.
- "HPPCI JTAG I/O Voltage Detection" on page 1-12
  Describes the JTAG I/O voltage detection feature of the emulators.

# Contents of Emulator Package

**USB-Based Emulator:**

Your USB-based emulator package contains the following items.

- HPUSB-ICE, USB-ICE, or MSP430 assembly
- 5-volt power supply
- 3-meter USB type-A to mini-B cable

**HPPCI-ICE Emulator:**

Your High-Performance PCI emulator package contains the following items.

- HPPCI-ICE or JTAG daughter card
- HPPCI-ICE pod assembly

# PC Configuration

For correct operation of the USB- or PCI-based emulator, your computer must have the minimal configuration:

1. Windows 2000, Windows XP, or Windows Vista
2. VisualDSP++ 3.5 or later
3. USB full- or high-speed port (for USB-based emulators)
4. One available PCI slot (for PCI-based emulators)

# Installation Tasks

Perform the following tasks to safely install your USB- or PCI-based emulator. Follow these instructions in the presented order to ensure correct operation of your software and hardware.

## Installing USB-Based Emulators

1. Install VisualDSP++ 3.5 or later. VisualDSP++ includes the USB driver needed for your USB emulation hardware. If VisualDSP++ is already installed, you do not need to install it again. VisualDSP++ can be installed on Windows 2000, Windows XP, or Windows Vista. Refer to the *Installation Quick Reference Card* for details.

   **Note:** If you connect the ICE first, before installing VisualDSP++, the Windows driver wizard will not be able to find the drivers to install for the emulator to function.

2. Connect the USB cable between the USB assembly and a USB port of your computer.

3. Verify driver installation. Refer to "Verifying Driver Installation" on page 1-4.

Before connecting to a target, see the power-up/down procedures in "Attaching the Cable to the Emulation Target" on page 1-6.

## Installing PCI-Based Emulators

1. Install the HPPCI-ICE hardware. For instructions on installing a PCI card into your computer, consult the documentation provided by the computer manufacturer.
2. Install VisualDSP++ 3.5 or later. VisualDSP++ includes the HPPCI driver needed for your PCI emulation hardware. VisualDSP++ can be installed on Windows 2000, Windows XP, or Windows Vista. Refer to the *Installation Quick Reference Card* for details.
3. Verify driver installation. Refer to "Verifying Driver Installation" on page 1-4.

The driver must be installed before you start the HPPCI-ICE for the first time.

## Verifying Driver Installation

Before using your USB- or PCI-based emulator, verify that the driver software is installed properly.

Open the Windows **Device Manager** and verify that the HPUSB-ICE, HPPCI-ICE, USB-ICE, or MSP430-ICE appears under **ADI Development Tools** as shown in Figure 1-1

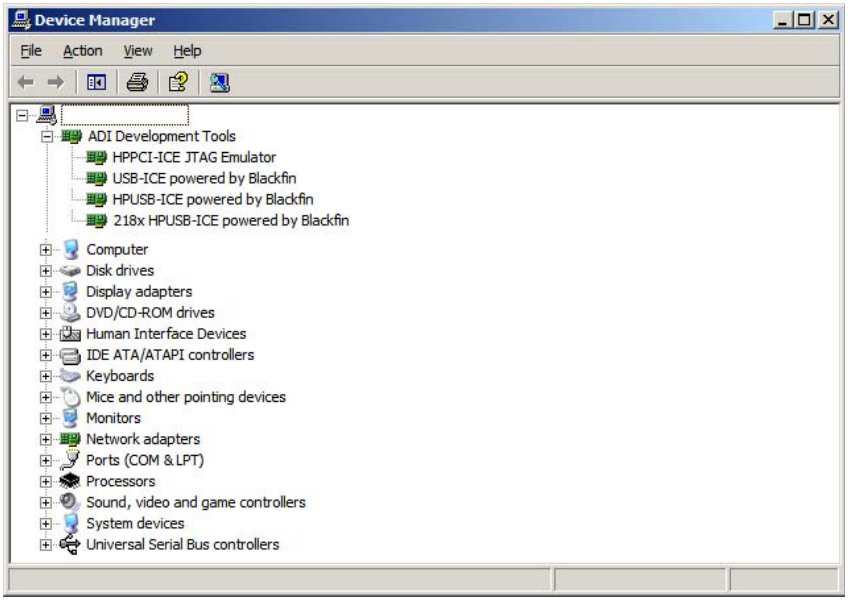


Figure 1-1. Verifying Driver Installation

# Attaching the Cable to the Emulation Target

## HPUSB, HPPCI, USB JTAG ICEs (not MSP430)

The final step is to connect the 14-pin header side of the pod cable to the target board via the debug interface. The 14-pin connector is keyed at pin 3 on the pod cable to ensure that the cable sits correctly on the 14-pin target emulation header. The target board should also have pin 3 keyed.

Never connect or disconnect a USB emulator JTAG header, whether powered up or not, to/from a powered target.

The following procedures apply only to USB-based emulators.

**Powering Up/Down an HPUSB or USB Emulator**

To power up the USB-based emulator:

1. Apply power to target board.
2. Apply power to ICE.
3. Connect the USB cable between the ICE and the PC.
4. Invoke VisualDSP++.

To power down the USB-based emulator:

1. Shut down (exit) VisualDSP++.
2. Disconnect the USB cable between the ICE and the PC.

3. Power down the ICE.
4. Power down the target board.

If the emulator has an "Enable/Power" LED, this should be green when power is applied. It should be amber when connected to a session or the ICE Test utility is being used.

If the emulator has an "Enable" LED only, this should be amber when connected to a session or while the ICE Test utility is being used.

At all other times, this LED should be off.

For custom processor boards still in design, refer to Engineer-to-Engineer Note, *Analog Devices JTAG Emulation Technical Reference (EE-68)*, available from the Analog Devices Web site. This document is a technical reference for implementing the JTAG interface on your target.

The emulator hardware is ready to be used in conjunction with VisualDSP++ to debug a processor target system.

## MSP430 ICEs

The final step is to connect the 14-pin header side of the pod cable to the target board via the JTAG interface. The 14-pin connector is keyed at pin 7 on the pod cable to ensure that the cable sits correctly on the 14-pin target emulation header. The target board must also have pin 7 keyed.

**Powering Up/Down an MSP430 Emulator**

To power up the MSP430 emulator:

1. Apply power to target board.
2. Apply power to ICE.

3. Connect the USB cable between the ICE and the PC.
4. Invoke VisualDSP++.

To power down the MSP430 emulator:

1. Shut down (exit) VisualDSP++.
2. Disconnect the USB cable between the ICE and the PC.
3. Power down the ICE.
4. Power down the target board.

The "ENABLE" LED is turned on when a VisualDSP++ debug session is running. The LED shuts off every time the VisualDSP++ session is closed. When this LED is off, it signifies all outputs of the pod logic connected to the target have been three-stated. Three-stating the outputs of the pod when VisualDSP++ is inactive prevents the target processor from entering an unknown state during the target power up sequencing.

For custom processor boards still in design, refer to Engineer-to-Engineer Note, *Analog Devices JTAG Emulation Technical Reference (EE-68)*, available from the Analog Devices Web site. This document is a technical reference for implementing the JTAG interface on your target.

The emulator hardware is ready to be used in conjunction with VisualDSP++ to debug a processor target system.

# VisualDSP++ Configurator

VisualDSP++ requires a description of your *platform* (JTAG chain). The platform definition is necessary for VisualDSP++ to communicate with the hardware through the emulator.

The VisualDSP++ Configurator's ICE Test utility allows you to configure and test your emulator hardware. ICE Test provides emulator detection, JTAG I/O voltage selection, and JTAG frequency selection. Use the ICE Test to test the target. If errors are encountered, they are reported immediately and the test ends. Each error message recommends a solution to the problem.

Refer to VisualDSP++ online Help for information about the VisualDSP++ Configurator and the ICE Test utility.

# JTAG Frequency Selection

High-Performance PCI-ICE and High-Performance USB-ICE emulators support a JTAG clock operation up to 50 MHz. USB-ICE emulators support a JTAG clock operation of 10 MHz.

There is a relationship between the JTAG frequency and the core clock frequency of the processor. Typically, the core clock runs at a frequency that is more than 2x the JTAG clock's frequency. On newer Analog Devices processors, the core clock is a variable that is sometimes set by switches or by software.

If the core/JTAG clock relation is not followed, scan failures may prevent the emulator from connecting to the processor.

Choosing the **JTAG Frequency Selection** from the **Settings** menu in VisualDSP++ opens the **JTAG Frequency Selection** dialog box shown in Figure 1-2 and Figure 1-3. The dialog box is used to change the rate at which the JTAG Test Clock signal (TCK) runs.

Not all frequencies listed above appear for all processor families. The displayed frequencies depend upon the processor family.

The tests listed in the **Status** box are run when you click the **Test** button on the **JTAG Frequency Selection** dialog box. The blue arrow points to the frequency currently being used. The arrow does not change after you

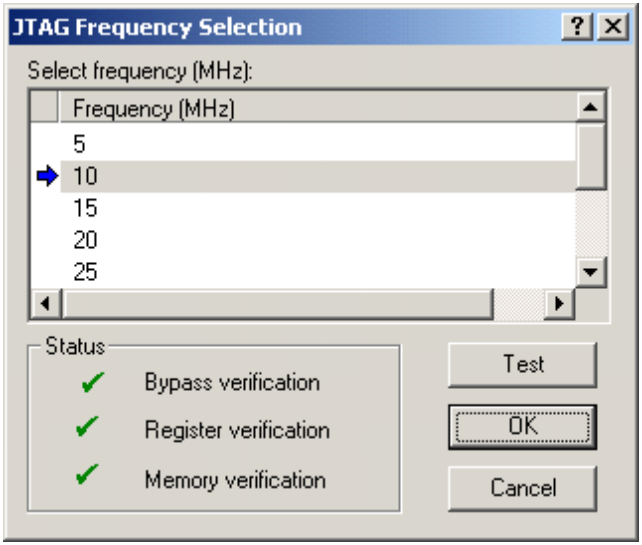


Figure 1-2. HPUSB-ICE JTAG Frequency Selection Dialog Box

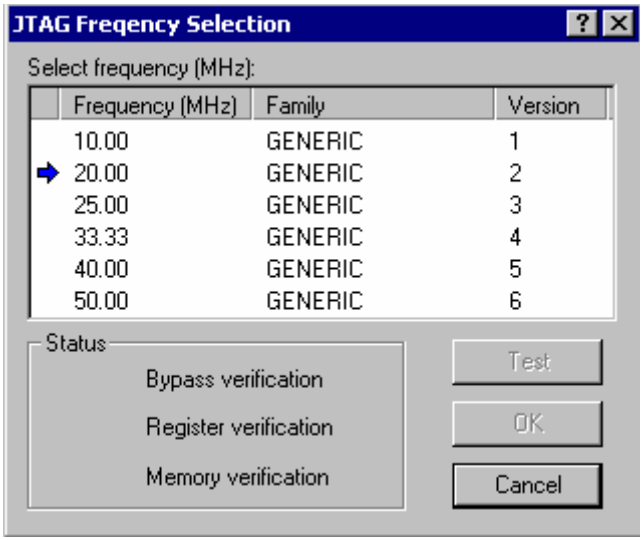


Figure 1-3. HPPCI-ICE JTAG Frequency Selection Dialog Box

run the tests because pressing the **Cancel** button goes back to using the frequency pointed to by the blue arrow. To use a different frequency, select the appropriate frequency from the list and click **Test**. Clicking **OK** uses the frequency that is highlighted and that has already been tested.

Table 1-1 lists and describes each of the available options.

Table 1-1. JTAG Frequency Selection Dialog Box Fields

| Item | Description |
|---|---|
| **Select frequency (MHz)** | Selects the frequency to run TCK. |
| **Status** | Updates status of the tests indicated within the test group. The test status indicator can show a "running" icon, "not running" icon, "pass" icon, or "fail" icon, depending on the test status. |
| **Test** | Tests the selected frequency by running the tests in the **Status** group. **NOTE:** If tests fail, you may have to shut down VisualDSP++ and restart your session. |
| **OK** | Saves the selected frequency. This should only be highlighted if all the tests have passed. |
| **Cancel** | Continues using the frequency pointed to by the blue arrow. |

If you encounter a problem launching VisualDSP++ at a certain frequency, delete your debug session in VisualDSP++ and create a new debug session. This will set TCK back to the default value of 10 MHz.

# HPPCI JTAG I/O Voltage Detection

The mode of operation supported by the PCI emulator is dependent on the connection method used for the 14-pin JTAG header on your target. Figure 1-4 and Figure 1-5 show how the target JTAG header connects for legacy and auto detection modes.

Voltage selection is not available on the MSP430 emulator. The MSP430 emulator is fixed at 3.3 volts and has a different pinout than shown in Figure 1-4 or Figure 1-5.

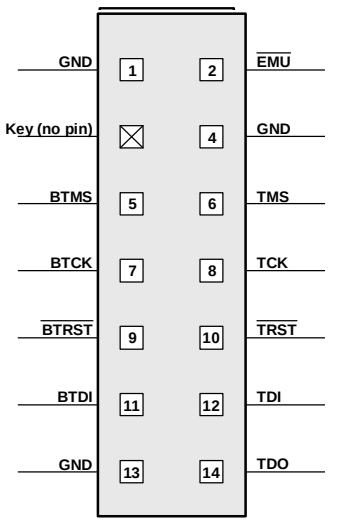


Figure 1-4. Legacy Pinout

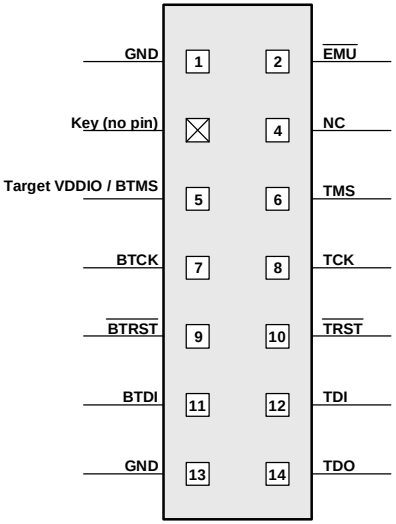


Figure 1-5. Auto Detection Pinout

## HPUSB/USB Legacy Mode

Legacy mode is used for older targets that do not provide a target VDDIO input for automatic voltage detection by the emulator. In this mode, the voltage at which the JTAG signals run is set manually through VisualDSP++ via the VisualDSP++ Configurator utility. The configurator utility provides a voltage selection setting when configuring the target.

HPUSB-ICE and USB-ICE emulators do not support auto voltage detection mode.

## HPPCI-ICE Legacy/Auto Detection Mode

The factory default for the pod shown in Figure 1-6 is legacy mode. For more information about available modes, refer to "Auto Detection Mode" on page 1-15.

In order to modify the factory default setting, remove the four screws on the bottom of the plastic enclosure. When opening the case, first remove the top of the enclosure with the top facing up. This must be done to ensure that the four light pipes used for the LEDs are not damaged. The default pod setting is shown in Figure 1-7. To determine whether the default setting of your HPPCI-ICE needs to be modified, refer to "Legacy Mode (Factory Default Setting)".

Figure 1-6. HPPCI-ICE Pod

## Legacy Mode (Factory Default Setting)

Legacy mode is used for older targets that do not support voltages less than 3.3V and do not provide an IOVDD input for automatic voltage detection by the pod. Consequently, the emulator in legacy mode is used for all previously designed 3.3V and 5V target boards. The HPPCI-ICE is 3.3V compliant and 5.0V tolerant in this mode and accepts both 3.3V and 5.0V signals but only drives 3.3V CMOS level signals. In legacy mode, the LED labeled **3.3/5V** is lit.

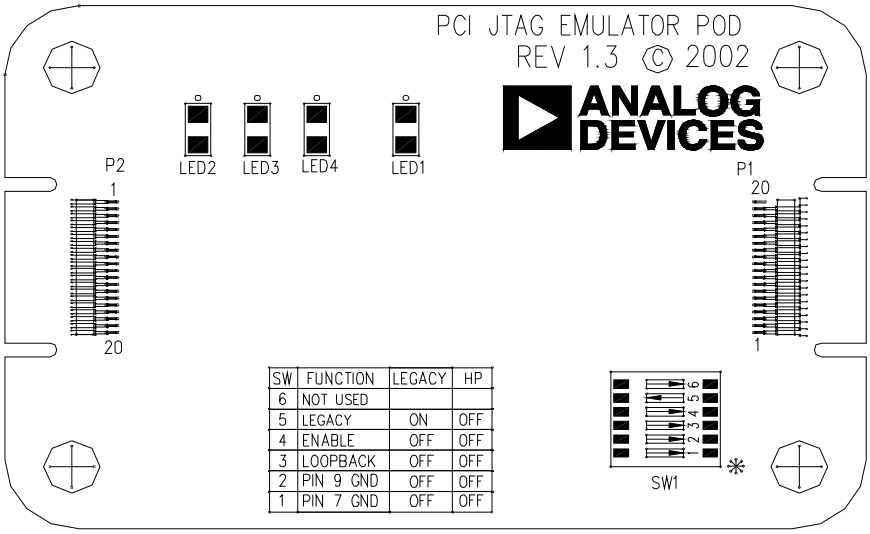


Figure 1-7. Default Switch Setting for HPPCI-ICE Pod

The emulator is set to Legacy mode before leaving the factory. The switch must be set in the manner shown in Figure 1-8 to verify that the emulator is in legacy mode, or to change the emulator to legacy mode.

## Auto Detection Mode

Auto detection mode is recommended for all newly designed target boards. This mode supports 1.8V, 2.5V, 3.3V, and 5V target boards. PCI-based emulators are 1.8V, 2.5V, and 3.3V-compliant in auto detection mode. This means that the emulator can accept 1.8V, 2.5V, and 3.3V signals and can also drive the respective 1.8V, 2.5V, and 3.3V CMOS level signals. The emulator is also 5V tolerant. Consequently, the emulator accepts 5V signals and drives 3.3V signals to the target.

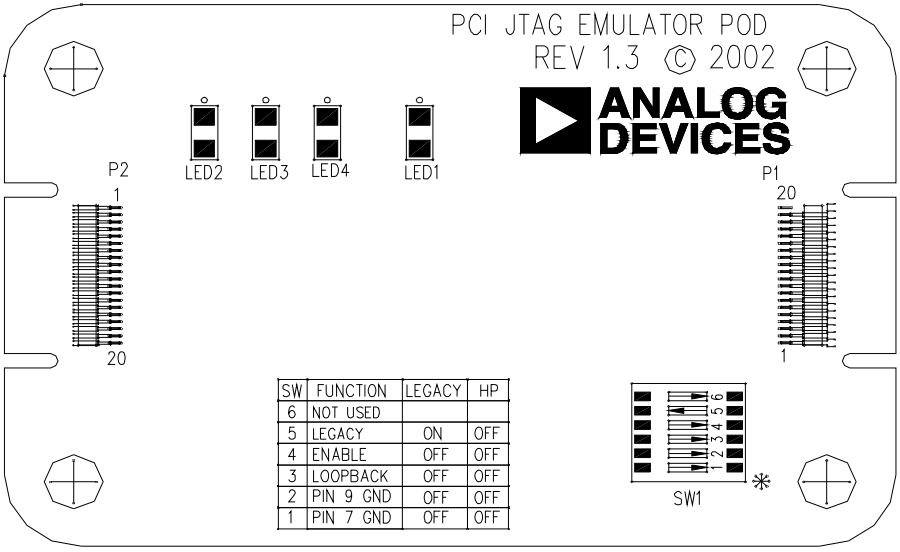


Figure 1-8. Legacy Switch Setting for HPPCI-ICE Pod

In auto detection mode, the emulator samples the target VDDIO signal (pin 5 on the JTAG header) and drives the JTAG signals from the emulator at the sampled voltage. The respective 1.8V, 2.5V, or 3.3/5V LED also lights up to indicate the voltage at which the JTAG signals are driven.

The emulator is set to legacy mode before leaving the factory. The switch must be set in the manner shown in Figure 1-9 to verify that the emulator is in auto detection mode, or to change the emulator to auto detection mode.

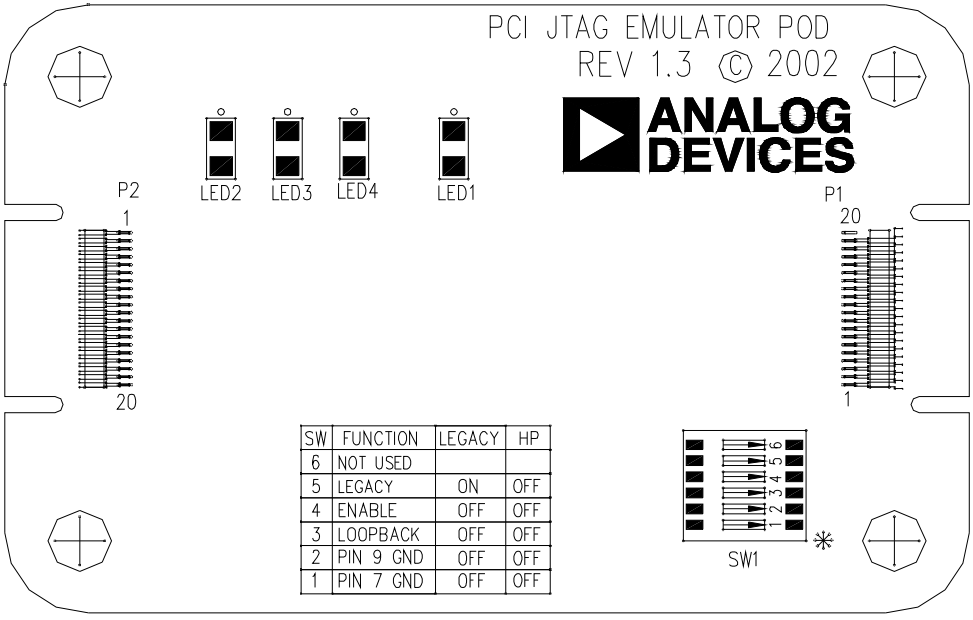


Figure 1-9. Auto Detection Switch Setting for HPPCI-ICE Pod

# Troubleshooting Emulator Problems

If you experience problems installing the emulator hardware or software, consult *Emulator Troubleshooting Guide (EE-175)*, which is available on the Analog Devices Web site.

# 2 HARDWARE DESCRIPTION

This chapter describes the hardware design of the USB- and PCI-based emulators.

## LEDs

### HPUSB-ICE/USB-ICE LEDs

Four LEDs are located on the enclosure:

- 1.8V LED – Signifies that the ICE drives all signals at 1.8V compliant levels.
- 2.5V LED – Signifies that the ICE drives all signals at 2.5V compliant levels.
- 3.3/5V LED – Signifies that the ICE drives all signals at 3.3V compliant levels.
- **ENABLE** – This LED is amber when the debugger is enabled. This means that the emulator is driving the JTAG signals, and the connector must not remove or plug onto a target when the light is amber. When the LED is green, the JTAG signals are not being driven, and it is safe to connect to a target. The green LED indicates that the board is powered up but not in emulation mode.

## HPPCI-ICE LEDs

Four LEDs are located on the pod enclosure (Figure 2-1), and five LEDs are located on the daughter board (Figure 2-2).

## Pod LEDs

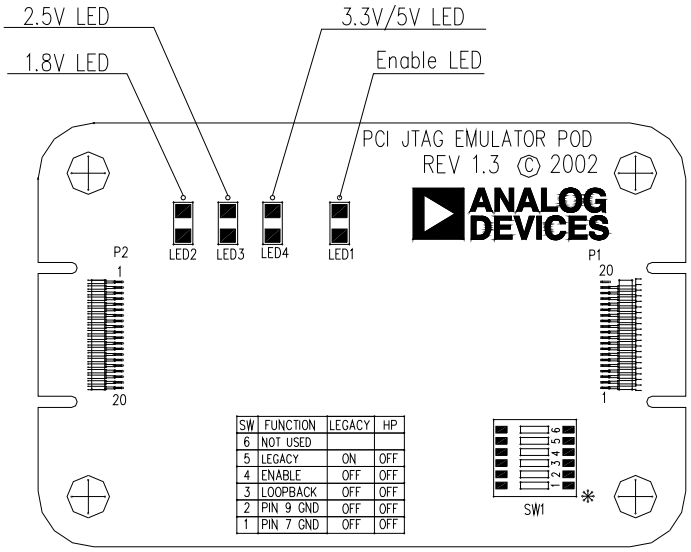


Figure 2-1. Pod LEDs

- 1.8V LED – In auto detection mode, this LED signifies that a target VDDIO of 1.8V has been detected on the JTAG header (pin 5) on the processor target board, and the HPPCI-ICE drives all signals at 1.8V compliant levels.
- 2.5V LED – In auto detection mode, this LED signifies that a target VDDIO of 2.5V has been detected on the JTAG header (pin 5) on the processor target board, and the HPPCI-ICE drives all signals at 2.5V compliant levels.

- 3.3/5V LED – In auto detection mode, this LED signifies that a target VDDIO of 3.3V or 5V has been detected on the JTAG header (pin 5) on the processor target board, and the HPPCI-ICE drives all signals at 3.3V compliant levels. In legacy mode, this LED is powered automatically, and pin 5 of the JTAG header on the target board is not used to detect the target VDDIO voltage.
- ENABLE – This LED is turned on when a VisualDSP++ debug session is running. This LED shuts off every time the VisualDSP++ session is closed. When this LED is off, it signifies all outputs of the pod logic connected to the target have been three-stated. Three-stating the outputs of the pod when VisualDSP++ is inactive prevents the target processor from entering an unknown state during the target power up sequencing.

## Board LEDs

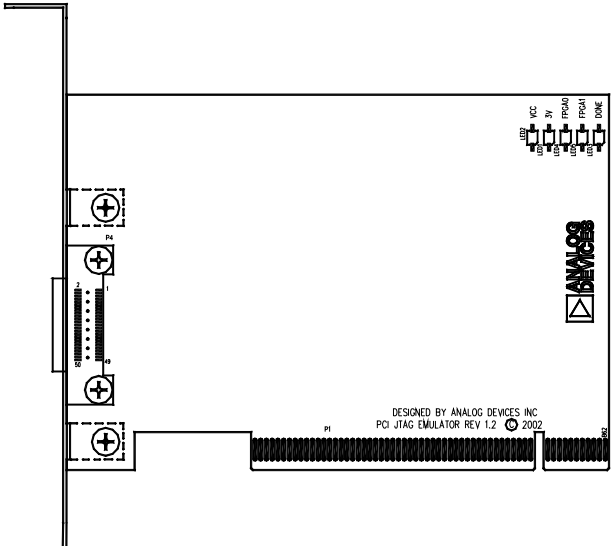


Figure 2-2. Board LEDs

- VCC – This LED signifies that the board is receiving 5V power. If this LED is not active, the HPPCI-ICE does not function properly.
- 3V – This LED signifies that the board is receiving 3.3V power. If this LED is not active, the HPPCI-ICE does not function properly.
- FPGA[1:0] – These two LEDs are used for factory purposes only.
- DONE – This LED is activated when a VisualDSP++ debug session is started. The LED should remain active even after the respective session has been terminated. The LED shuts off and re-activates at the beginning of every new VisualDSP++ session.

### MSP430-ICE LED

There is one LED located on the enclosure.

ENABLE – This LED is turned on when a VisualDSP++ debug session is running. The LED shuts off every time the VisualDSP++ session is closed. When this LED is off, it signifies all outputs of the pod logic connected to the target have been three-stated. Three-stating the outputs of the pod when VisualDSP++ is inactive prevents the target processor from entering an unknown state during the target power up sequencing.

## Designing Custom Processor Boards

When designing a custom processor board using Analog Devices processors and DSPs, special care must be taken to ensure that the JTAG interface is designed and laid out correctly. If the board is not designed correctly, communication via the JTAG port may not work. Another side effect may be that the interface works, but you are not able to run at the highest possible JTAG clock frequency. The JTAG clock frequency is dependant on the particular Analog Devices processor, as well as the delay characteristics of the custom processor board.

To ensure that the custom board's JTAG interface is designed and laid out correctly, refer to Engineer-to-Engineer Note, *Analog Devices JTAG Emulation Technical Reference (EE-68)*, available from the Analog Devices Web site. This document is a technical reference for implementing the JTAG interface on your target.

# Mechanical Specifications

## HPPCI-ICE

The HPPCI-ICE consists of a daughter board and a pod cable. The system is compliant with revision 2.2 of the PCI specification and plugs into 5V-only motherboards. It uses only the 5 volts from the PC's PCI slot. The pod cable consists of a small PCB that has a multi-conductor cable soldered at each end. The multi-conductor cable is constructed with individual coaxial cables that are encapsulated by shield ground. The PCB in the pod is fully enclosed in a copper-sprayed plastic enclosure. The multi-conductor cables and copper spray reduce system noise and electromagnetic interference. The mechanical dimensions of the daughter board, pod cable assembly, and pod enclosure are shown in Figure 2-3, Figure 2-4, and Figure 2-5, respectively. Unless specified, all dimensions are in inches.

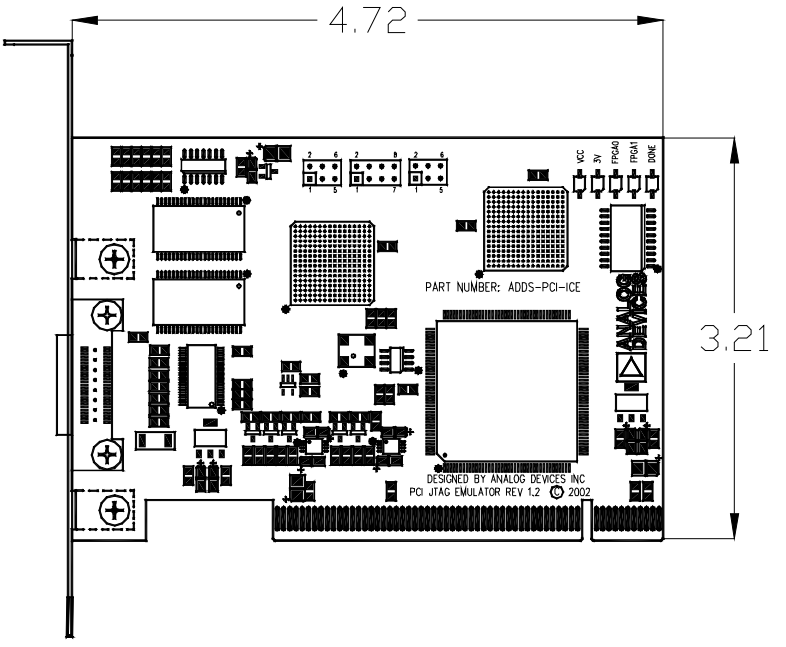


Figure 2-3. Daughter Board Dimensions (in inches)

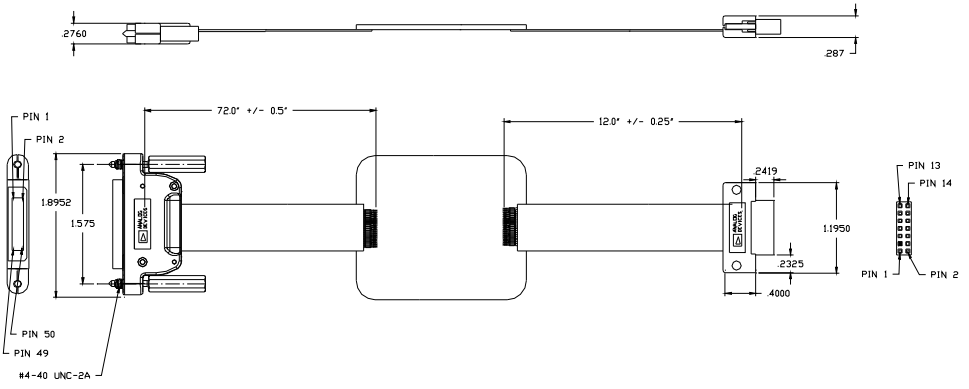


Figure 2-4. Pod Cable Dimensions (in inches)

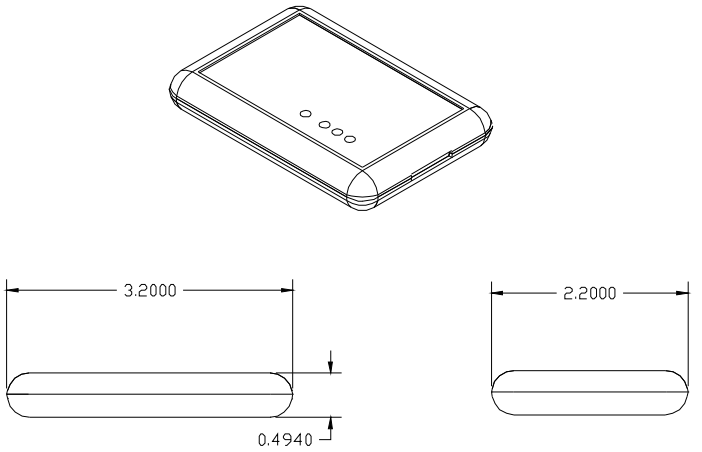


Figure 2-5. Pod Box Dimensions (in inches)

# 3 SUPPORT

Analog Devices provides free technical support.

## Technical Support

For technical support, you may contact the Analog Devices DSP Tools Technical Support group in any of the following ways.

- Fill out the Processor Tools Technical Support Web site form at `http://forms.analog.com/Form_Pages/DSP/tools/contactDSP.asp`
- Send a description of the problem by e-mail to `processor.tools.support@analog.com`
- Call the customer support hotline at 1-800-ANALOG-D (1-800-262-5643 U.S.A. only).

For direct support of the Analog Devices processors, call the Analog Devices DSP Applications Engineering group at 1-800-ANALOGD or e-mail `dsp.support@analog.com`.

## Quality Assurance

Analog Devices is committed to providing quality products and services. To continually provide this quality, please contact our Quality Assurance Department directly if you have any concerns at (603) 883-2430, Monday

through Friday during normal business hours, or via e-mail at: processor.tools@analog.com. Our Quality Assurance manager will listen to your concerns and provide a timely and effective solution.

# 4 REFERENCES

This section describes documentation resources helpful in your application development.

- For information on designing the interface between an Analog Devices SHARC processor and the emulation header on your custom processor target board, refer to Engineer-to-Engineer Note, *Analog Devices JTAG Emulation Technical Reference (EE-68)*, available from the Analog Devices Web site.
- For information on the architecture and system interface of the Analog Devices processor, refer to the appropriate Analog Devices processor's *Hardware Reference*.
- For processor timing specification and other hardware design information, refer to the appropriate processor's *Data Sheet*.
- For complete information on software development tools (assembler, compiler, linker, and so on), refer to documentation included with VisualDSP++. This information is available in PDF format and in VisualDSP++ online Help.
- For information about your development platform, refer to your operating system manuals and hardware system manuals.

- For information about digital signal processing theory and applications, consult:
    - Higgins. *Digital Signal Processing In VLSI*. Prentice-Hall, 1990.
    - Oppenheim and Schafer. *Digital Signal Processing*. Prentice-Hall, 1975.

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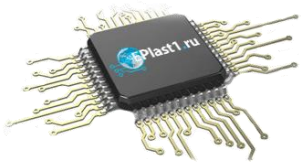


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