MAX35101 Time-to-Digital Converter with Analog Front-End

General Description

The MAX35101 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end (AFE) solution for the ultrasonic heat meter and flow meter markets.

With a time measurement accuracy of 20ps and automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements.

Multihit capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, an autozero amplifier/comparator, real-time clock (RTC), and programmable receiver sensitivity provide the analog interface and control for a minimal electrical bill of material solution. The RTC provides an event timing mode that is configurable and runs cyclic algorithms to minimize microprocessor interactivity and increase battery life.

Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access and thus minimize current consumption.

For temperature measurement, the MAX35101 supports up to four (4) 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

On-board 8KB user flash allows the MAX35101 to be nonvolatile-configurable and provide nonvolatile energy use data to be logged. Configuration can be recalled anytime with a SPI command.

Benefits and Features

- High Accuracy Flow Measurement for Billing and Leak Detection
  - Time-to-Digital Accuracy Down to 20ps
  - Measurement Range Up to 8ms
  - Two Channels: Single-Stop Channel
- High Accuracy Temperature Measurement for Precise Heat and Flow Calculations
  - Up to Four (4) 2-Wire Sensors
  - PT1000 and PT500 RTD Support
- Maximizes Battery Life with Low Device and Overall System Power
  - Low 10μA ToF measurement and < 125nA Duty-Cycled Temperature Measurement
  - Event Timing Mode Reduces Host μC
- Overhead to Minimize System Power Consumption
  - 2.3V to 3.6V Single-Supply Operation
- High-Integration Solution Minimizes Parts Count and Reduces BOM Cost
  - 8KB of Nonvolatile Flash Memory for Data Logging
  - Built-in Real Time Clock
  - Small, 5mm x 5mm, 32-Pin TQFP Package
  - -40°C to +85°C Operation

Applications

- Ultrasonic Heat Meters
- Ultrasonic Water Meters
- Ultrasonic Gas Meters

***Ordering Information* appears at end of data sheet.**

Absolute Maximum Ratings

(Voltages relative to ground.)
Voltage Range on V_{CC} Pins................................-0.5V to +4.0V
Voltage Range on All Other Pins
(not to exceed 4.0V)............................ -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 27.80mW/ºC above +70°C)...........2222.20mW

Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range........................... -55°C to +125°C
Lead Temperature (soldering, 10s)................................+300°C
Soldering Temperature (reflow).....................................+260°C
ESD Protection (All Pins, Human Body Model)..................±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA})..........36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....................4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.0	3.6	V
Input Logic 1 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.3	V
Input Logic 0 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IL}		-0.3		V_{CC} x 0.3	V
Input Logic 1 (32KX1)	$V_{IH32KX1}$		V_{CC} x 0.85		V_{CC} + 0.3	V
Input Logic 0 (32KX1)	$V_{IL32KX1}$		-0.3		V_{CC} x 0.15	V

Electrical Characteristics

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (CSW, $\overline{RST}$, SCK, DIN, $\overline{CE}$)	I_L		-0.1		+0.1	µA
Output Leakage ($\overline{INT}$, $\overline{WDO}$, T1,T2,T3,T4)			-0.1		+0.1	µA
Output Voltage Low (32KOUT)	V_{OL32K}	2mA			0.2 x V_{CC}	V
Output Voltage High (32KOUT)	V_{OH32K}	-1mA	0.8 x V_{CC}			V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	V_{OH}	-4mA	0.8 x V_{CC}			V
Output Voltage High (TC)	V_{OHTC}	V_{CC} = 3.3V, I_{OUT} = -4mA	2.9	3.1		V

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High (Launch_UP, Launch_DN)	$V_{OHLAUCH}$	V_{CC} = 3.3V, I_{OUT} = -50mA	2.8	3.0		V
Output Voltage Low ($\overline{WDO}$, $\overline{INT}$, DOUT, CMP_OUT/UP_DN)	V_{OL}	4mA			0.2 x V_{CC}	V
Pulldown Resistance (TC)	R_{TC}		650	1000	1500	Ω
Input Voltage Low (TC)	V_{ILTC}			0.36 x V_{CC}		V
Output Voltage Low (Launch_UP, Launch_DN)	$V_{OLLAUCH}$	V_{CC} = 3.3V, I_{OUT} = 50mA		0.2	0.4	V
Resistance (T1, T2, T3, T4)	R_{ON}			1		Ω
Input Capacitance ($\overline{CE}$, SCK, DIN, $\overline{RST}$, CSW)	C_{IN}	Not tested		7		pF
$\overline{RST}$ Low Time	t_{RST}				100	ns
CURRENT						
Standby Current	I_{DDQ}	No oscillators running, T_A = +25°C		0.1	1	μA
32kHz OSC Current	I_{32KHZ}	32kHz oscillator only (Note 4)		0.5	0.9	μA
4MHz OSC Current	I_{4MHZ}	4MHz oscillator only (Note 4)		40	85	μA
LDO Bias Current	I_{CCLDO}	I_{CCCPU} = 0 (Note 4)		15	35	μA
Time Measurement Unit Current	I_{CCTMU}	(Note 4)		4.5	8	mA
Calculator Current	I_{CCCPU}			2.5	5	mA
Device Current Drain	I_{CC3}	TOF_DIFF = 2 per second (3 hits), temperature = 1 per 30s		10		μA
	I_{CC6}	TOF_DIFF = 2 per second (6 hits), temperature = 1 per 30s		13		μA
FLASH Erase Current	I_{FLASH}			0.5	1	mA
ANALOG RECEIVER						
Analog Input Voltage (STOP_UP, STOP_DN)	V_{ANA}		10	700	2 x V_{CC} x (3/8)	mV_{P-P}
Input Offset Step Size	V_{STEP}			1		mV
STOP_UP/STOP_DN Bias Voltage	V_{BIAS}			V_{CC} x (3/8)		V
Receiver Sensitivity	V_{ANA}	Stop hit detect level (Note 5)	10			mV_{P-P}
TIME MEASUREMENT UNIT						
Measurement Range	t_{MEAS}	Time of flight	8		8000	μs
Time Measurement Accuracy	t_{ACC}	Differential time measurement		20		ps
Time Measurement Resolution	t_{RES}			3.8		ps

Electrical Characteristics (continued)

(V_{CC} = 2.3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.0V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH						
Data Retention	D_R	T_A = +25°C	100			Years
Flash Endurance	N_{FLASH}	T_A = +25°C	20k			Cycles
Block Flash Erase Time	t_{ERASE}				50	ms
LDO Stabilization Time	t_{STABLE}			135		µs
Word Write Time	t_{WRITE}			72	100	µs
Transfer Configuration to Flash Command Time	t_{CONFIG}			35		ms
EXECUTION TIMES						
Power-On-Reset Time	t_{RESET}	Reset to POR INT		275		µs
INIT Command Time	t_{INIT}	Command received when INIT bit set		2.5		ms
Case Switch Time	t_{CSW}	CSW pin logic-high until CSWI bit set		20		ns
CAL Command Time	t_{CAL}	Command received when CAL bit set		1.25		ms
SERIAL PERIPHERAL INTERFACE						
DIN to SCK Setup	t_{DC}				20	ns
SCK to DIN Hold	t_{CDH}			2	20	ns
SCK to DOUT Delay	t_{CDD}			5	20	ns
SCK Low Time	t_{CL}	V_{CC} ≥ 3.0V	25	4		ns
		V_{CC} = 2.3V	50	30		
SCK High Time	t_{CH}		25	4		ns
SCK Frequency	t_{CLK}	V_{CC} ≥ 3.0V			20	MHz
		V_{CC} = 2.3V			10	
$\overline{CE}$ to SCK Setup	t_{CC}			5	40	ns
SCK to $\overline{CE}$ Hold	t_{CCH}				20	ns
$\overline{CE}$ Inactive Time	t_{CWH}			2	40	ns
$\overline{CE}$ to DOUT High Impedance	t_{CCZ}			5	20	ns

Recommended External Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f_{32K}			32.768		kHz
32kHz Frequency Tolerance	$\Delta f_{32K}/f_{32K}$	T_A = +25°C	-20		+20	ppm
32kHz Load Capacitance	C_{L32K}			12.5		pF
32kHz Series Resistance	R_{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	F_{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	$\Delta f_{4M}/f_{4M}$	T_A = +25°C	-30		+30	ppm
4MHz Crystal Load Capacitance	C_{L4M}			12.0		pF
4MHz Crystal Series Resistance	R_{S4M}				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		T_A = +25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF
4MHz Ceramic Series Resistance					30	Ω

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: Currents are specified as individual block currents. Total current for a point in time can be calculated by taking the standby current and adding any block currents that are active at that time.

Note 5: Receiver sensitivity includes performance degradation contributed by STOP_UP and STOP_DN device pin input offset voltage and common mode drift.

Timing Diagrams

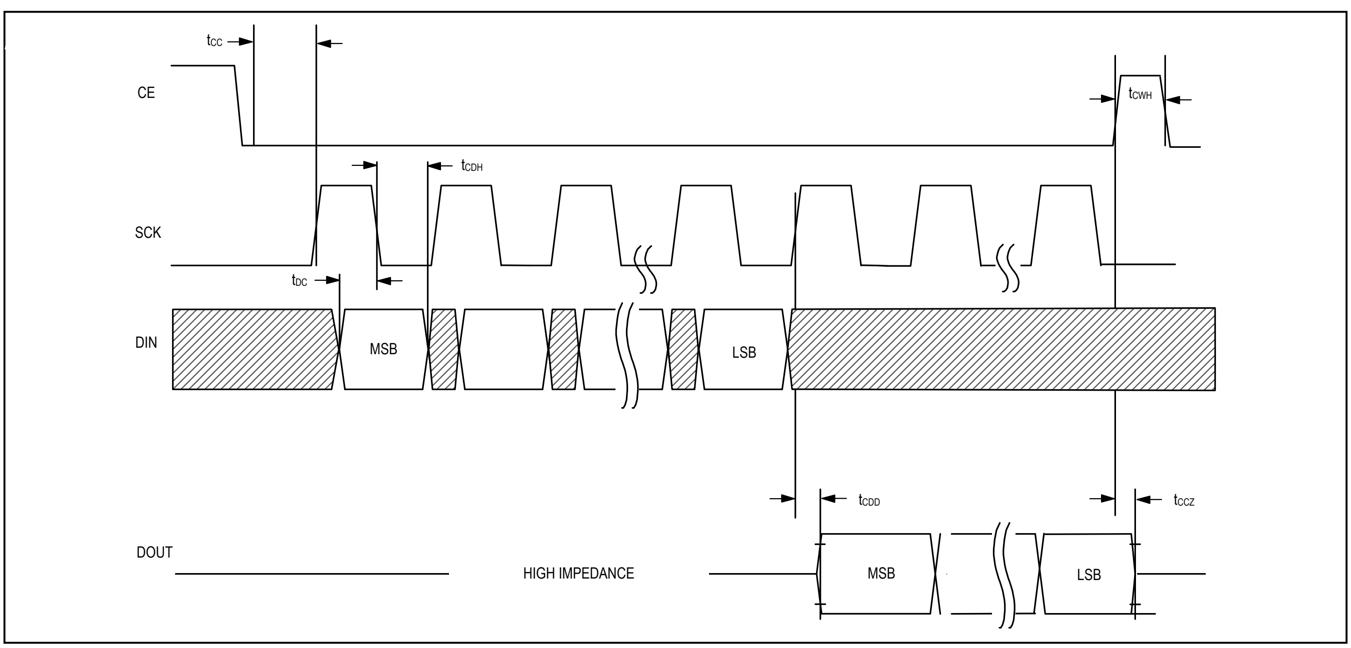


Figure 1. SPI Timing Diagram Read

Timing Diagrams (continued)

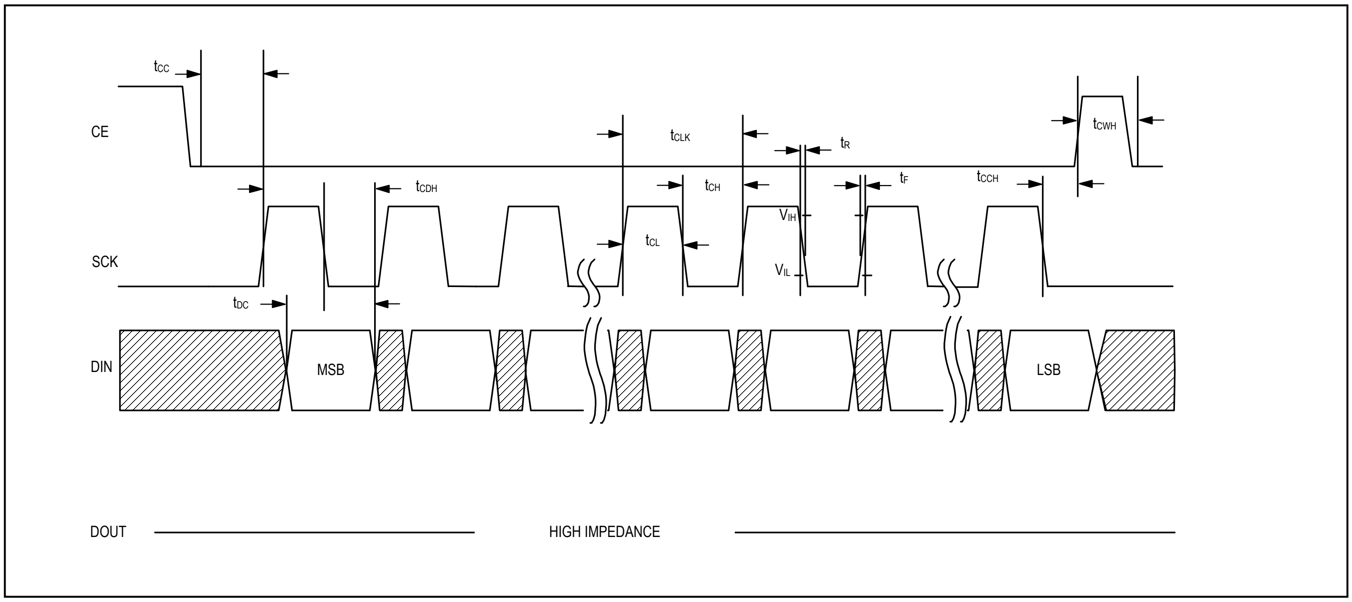
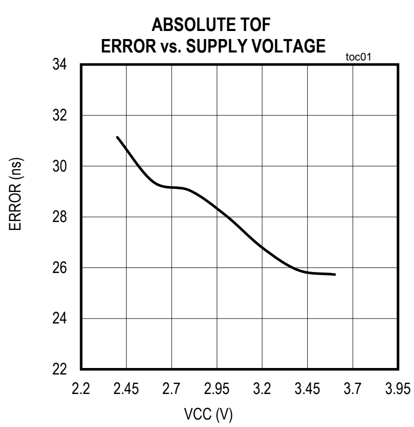
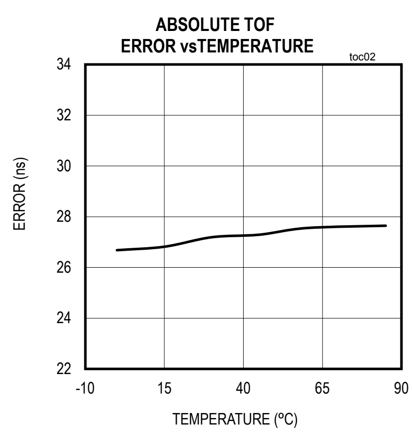


Figure 2. SPI Timing Diagram Write

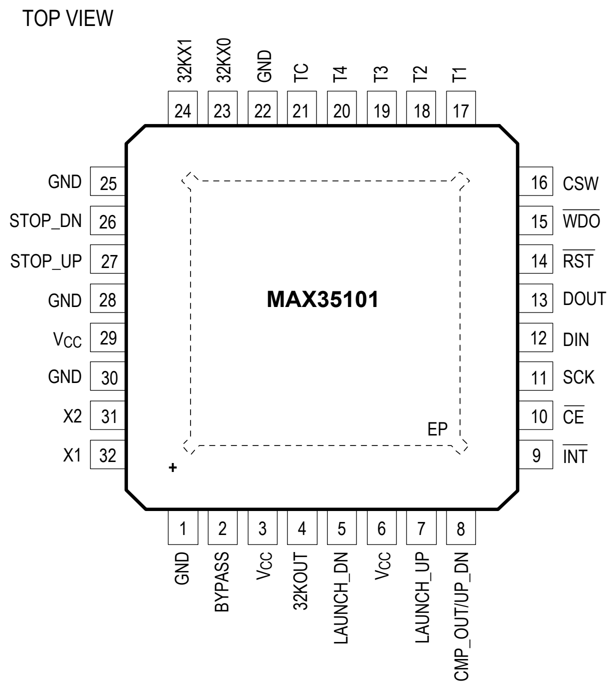
Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)





Pin Configuration



TQFP
(5mm x 5mm)

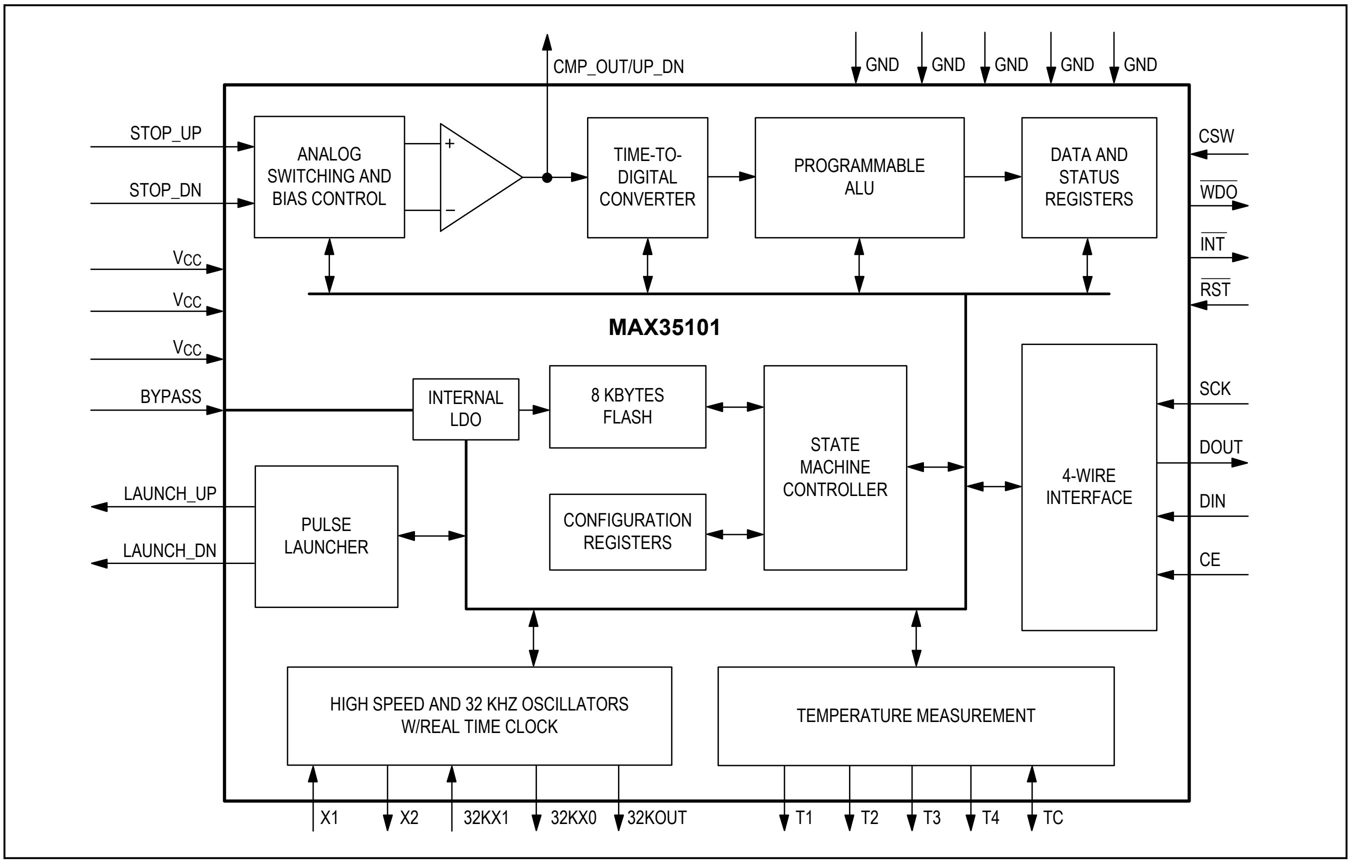
Pin Description

PIN	NAME	FUNCTION
1, 22, 25, 28, 30	GND	Device Ground
2	BYPASS	Connect this pin to ground with a capacitor (100nF) to provide stability for the on-board low-dropout regulator that is used to supply the flash circuitry. The effective series resistance of this capacitor needs to be in the 1Ω to 2Ω range.
3, 6, 29	V_{CC}	Main Supply. Typically sourced from a single lithium cell.
4	32KOUT	CMOS Output. Repeats the 32kHz crystal oscillator frequency.
5	LAUNCH_DN	CMOS Pulse Output Transmission in Downstream Direction of Water Flow
7	LAUNCH _UP	CMOS Pulse Output Transmission in Upstream Direction of Water Flow
8	CMP_OUT/UP_DN	CMOS Output. Indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output.
9	$\overline{INT}$	Active-Low Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
10	$\overline{CE}$	Active-Low CMOS Digital Input. Serial peripheral interface chip enable input.

Pin Description (continued)

PIN	NAME	FUNCTION
11	SCK	CMOS Digital Input. Serial peripheral interface clock input.
12	DIN	CMOS Digital Input. Serial peripheral interface data input.
13	DOUT	CMOS Output. Serial peripheral interface data output.
14	$\overline{RST}$	Active-Low CMOS Digital Reset Input
15	$\overline{WDO}$	Active-Low Open-Drain Watchdog Output
16	CSW	CMOS Digital Input. Case Switch. Active-high tamper detect input.
17	T1	Open-Drain Probe 1 Temperature Measurement
18	T2	Open-Drain Probe 2 Temperature Measurement
19	T3	Open-Drain Probe 3 Temperature Measurement
20	T4	Open-Drain Probe 4 Temperature Measurement
21	TC	Input/Output Temperature Measurement Capacitor Connection
23	32KX0	Connections for 32.768kHz Quartz Crystal. An external CMOS 32.768kHz oscillator can also drive the MAX35101. In this configuration, the 32KX1 pin is connected to the external oscillator signal and the 32KX0 pin is left unconnected.
24	32KX1	
26	STOP_DN	Downstream STOP Analog Input. Used for the signal that is received from the downstream transmission of a time-of-flight measurement.
27	STOP_UP	Upstream STOP Analog Input. Used for the signal that is received from the upstream transmission of a time-of-flight measurement.
31	X2	Connections for 4MHz Quartz Crystal. A ceramic resonator can also be used.
32	X1	
—	EP	Exposed Pad. Connect to GND.

Block Diagram



Detailed Description

The MAX35101 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end solution for the ultrasonic heat meter and flow meter markets.

With automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access.

For temperature measurement, the MAX35101 supports up to four (4) 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

The MAX35101 offers an event timing mode that is configurable and runs cyclic algorithms to minimize microprocessor interactivity and increase battery life.

The real-time clock (RTC) provides one programmable alarm and watchdog functionality.

A simple opcode based 4-Wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

On-board user flash allows the MAX35101 to be nonvolatile configurable and provides nonvolatile energy use data to be logged.

Time-of-Flight (TOF) Measurement Operations

TOF is measured by launching pulses from one piezoelectric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The MAX35101 contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The MAX35101 can measure two separate TOFs, which are defined as TOF up and TOF down.

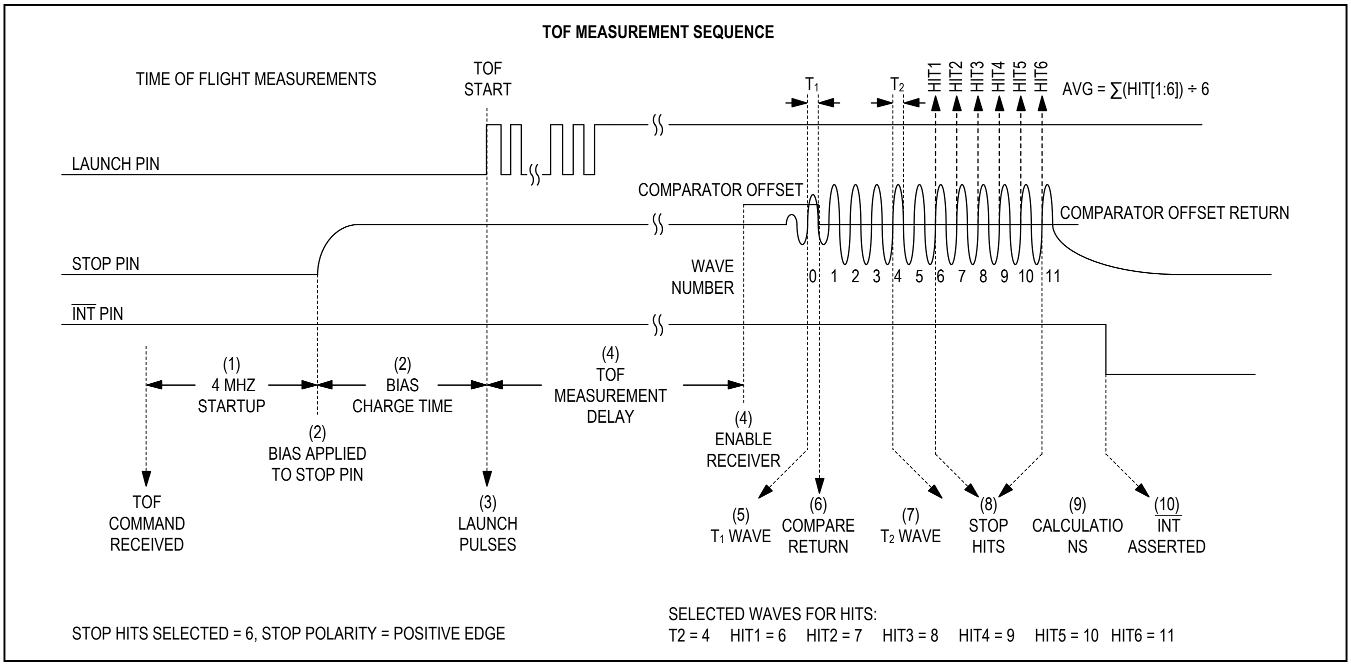


Figure 3. Time-of-Flight Sequence

A TOF up measurement has pulses launched from the LAUNCH_UP pin, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the STOP_UP pin. A TOF down measurement has pulses launched from the LAUNCH_DN pin, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the STOP_DN pin.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands. TOF_DIFF measurements can also be automatically executed using event timing mode commands EVTMG1 or EVTMG2.

The steps involved in a single TOF measurement are described here and shown in Figure 3.

1) The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
2) A common-mode bias is enabled on the STOP pin. This bias charge time is set by the CT[1:0] bits in the TOF1 register.
3) Once the bias charge time has expired, the pulse launcher drives the appropriate LAUNCH pin with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% duty-cycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses generates a start signal for the time-to-digital converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted by the start signal in the start/stop TDC timing (Figure 3).
4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate STOP pin are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
5) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the STOP pin according to the setting of the STOP_POL bit in the TOF1 register. The first stop hit is detected when a wave received at the STOP pin exceeds the comparator offset voltage, which is set in the TOF6 and TOF7 registers. This first detected wave is wave number 0. The width of the wave's pulse that exceeds the comparator offset voltage is measured and stored as the t1 time.
6) The offset of the comparator then automatically and immediately switches to the comparator return offset, which is set in the TOF6 and TOF7 registers.

7) The t_2 wave is detected and the width of the t_2 pulse is measured and stored as the t_2 time. The wave number for the measurement of the t_2 wave width is set by the T2WV[5:0] bits in the TOF2 register.

8) The preferred number of stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[2:0] bits in the TOF2 register. The wave number to measure for each stop hit is set by the HITx wave select bits in the TOF3, TOF4, and TOF5 registers.

9) After receiving all of the programmed hits, the MAX35101 calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t_1/t_2 and t_2/t_{ideal} are calculated and stored in the WVRUP or WVRDN register.

10) Once all of the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a read register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is 7FFFh or $(2^{15}-1) \times t_{4MHz}$ or ~ 8.19 ms. The maximum size of the fraction is:

FFFFh or $\frac{2^{16}-1}{2^{16}} \times t_{4MHz}$. or ~ 249.9961 ns.

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTER VALUE		CONVERTER VALUE
TOF_DIFFInt (hex)	**TOF_DIFFFrac (hex)**	**TOF DIFF VALUE (ns)**
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

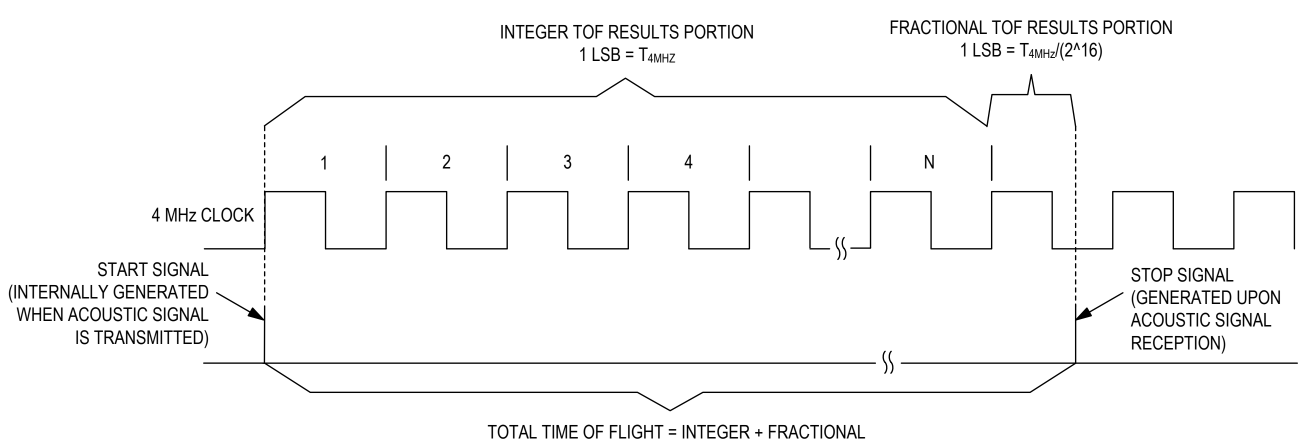


Figure 4.Start/Stop for Time-to-Digital Timing

Early Edge Detect

This early edge detect method of measuring the TOF of acoustic waves is used for all of the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the MAX35101 to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +127 LSBs if triggering on a positive edge and -127 LSBs if triggering on a negative edge, with 1 LSB = V_{CC}/3072. Separate input offset settings are available for the upstream received signal and the downstream received signal. The input offset for the upstream received signal is programmed using the C_OFFSETUP[6:0] bits in the TOF6 register. The input offset for the downstream received signal is programmed using the C_OFFSETDN[6:0] bits in the TOF7 register. Once the first hit is detected, the time t1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to a preprogrammed comparator offset value. This return offset value has a range of +127 LSBs to -128 LSBs in 1 LSB steps and is programmed into the C_OFFSETUPR[7:0] bits in the TOF6 register for the upstream received signal and programmed into the C_OFFSETDNR[7:0] bits in the TOF7 register. This preprogrammed comparator offset return value is provided to allow for common-mode shifts that can be present in the received acoustic wave.

The MAX35101 is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5, this is the 7th wave after the early edge detect wave. The selection of the t_2 wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{ideal} is calculated and registered for the user. For this calculation, t_{ideal} is1/2 the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all of the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. The TOF_DIFF_AVG Results registers do not include the error measurement. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

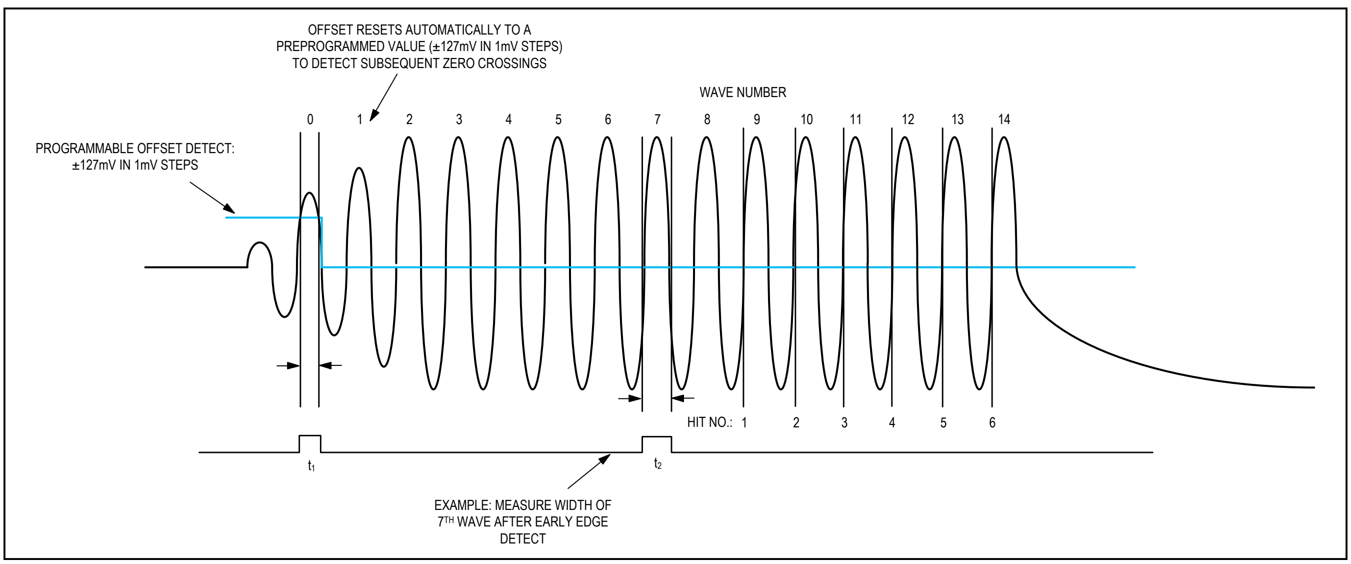


Figure 5. Early Edge Detect Received Wave Example

Temperature Measurement Operations

A temperature measurement is a time measurement of the RC circuit connected to the temperature port device pins T1 through T4 and TC. The TC device pin has a driver to charge the timing capacitor. The ports that are measured and the order in which the measurement is performed is selected with the TP[1:0] bits in the Event Timing 2 register.

Figure 6 depicts a 1000Ω platinum RTD with a 100nF NPO COG 30ppm/°C capacitor. It shows two dummy cycles with 4 temperature port evaluation measurements and 4 real temperature port measurements. This occurs when setting the TP[1:0] bits in the Event Timing 2 register to 11b.

The dummy 1 and dummy 2 cycles represent preamble measurements that are intended to eliminate the dielectric absorption of the temperature measurement capacitor. These dummy cycles are executed using a RTD Emulation resistor of 1000Ω internal to the MAX35101. This dummy path allows the dielectric absorption effects of the capacitor to be eliminated without causing any of the RTDs to be unduly self-heated. The number of dummy measurements to be taken ranges from 0 to 7. This parameter is configured by setting the PRECYC[2:0] bits in the Event Timing 2 register.

Following the dummy cycles, an evaluation, TXevaluate, is performed. This measurement allows the MAX35101 to maximize power efficiency by evaluating the temperature of the RTDs with a coarse measurement prior to a real measurement. The coarse measurement provides an approximation to the TDC converter. During the real measurement, the TDC can then optimize its measurement parameters to use power efficiently. These evaluate cycles are automatically inserted according to the order of ports selected with the of the Temperature Port bits. The time from the start of one port's temperature measurement to the next port's temperature measurement is set using with the PORTCYC[1:0] bits in the Event Timing 2 register.

Once all the temperature measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register is also set and the $\overline{INT}$ pin asserts (if enabled).

Actual temperature is determined by a ratiometric calculation. If T1 and T2 are connected to platinum RTDs and T3 and T4 are connected to the same reference resistor (as shown in the System Diagram), then the ratio of T1/T3 = R_{RTD1}/R_{REF} and T2/T4 = R_{RTD2}/R_{REF}. The ratios R_{RTD1}/R_{REF} and R_{RTD2}/R_{REF} can be determined by the host microprocessor and the temperature can be derived from a look-up table of Temperature vs. Resistance for each of the RTDs utilizing interpolation of table entries if required.

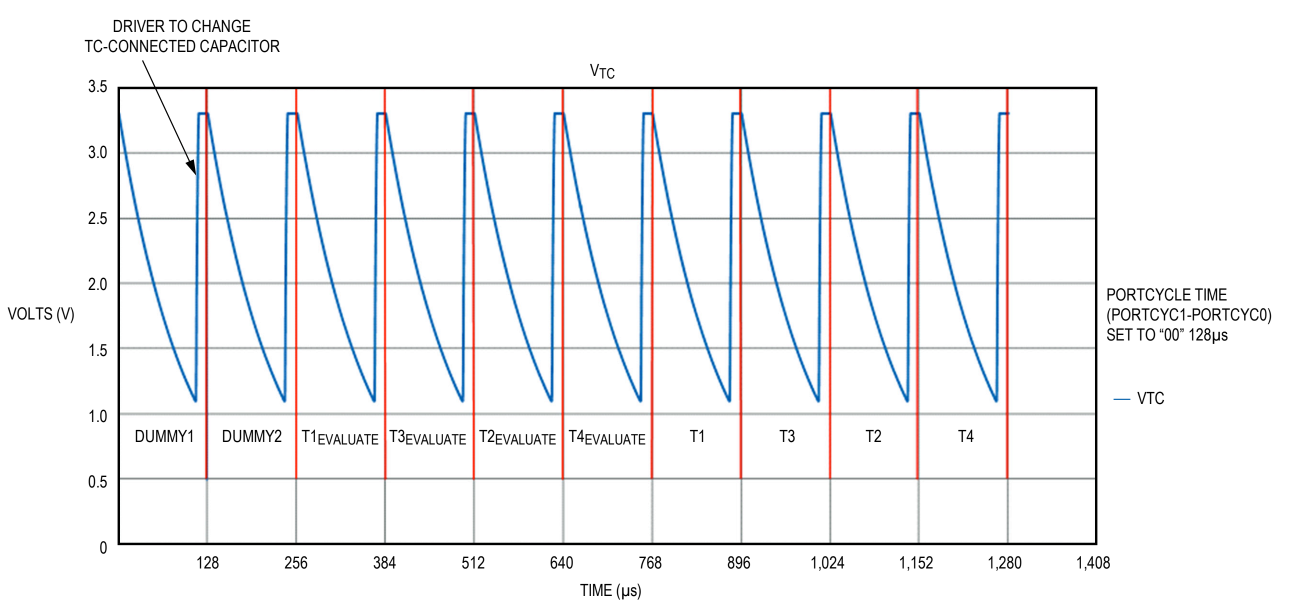


Figure 6. Temperature Command Execution Cycle Example

Temperature Error Handling

The temperature measurement unit can detect open and/or short-circuit temperature probes. If the resultant temperature reading in less than 8μs, then the MAX35101 writes a value of 0000h to the corresponding Results registers to indicate a short-circuit temperature probe. If the measurement process does not discharge the TC pin below the threshold of the internal temperature comparator within 2μs of the time set by the PORTCYC[1:0] bits in the Event Timing 2 register, then an open circuit temperature probe error is declared. The MAX35101 writes a value of FFFFh to the corresponding results registers to indicate an open circuit temperature probe, the TO bit in the Interrupt Status register is set, and the $\overline{\text{INT}}$ pin asserts (if enabled). If the temperature measurement error is caused by any other problems, then the MAX35101 writes a value of FFFFh to each of the temperature port results registers indicating that all of the temperature port measurements are invalid.

Event Timing Operation

The event timing mode of operation is an advanced feature that allows the user to configure the MAX35101 to perform automatic measurement cycles. This allows the host microcontroller to enter low-power mode and only awaken upon assertion of the MAX35101 $\overline{\text{INT}}$ pin (if enabled) when new measurement data is available. By using the TOF_DIFF and temperature commands and configuring the appropriate TOFx registers and the Event Timing registers, the event timing modes directs the MAX35101 to provide complete data for a sequence of measurements captured on a cyclical basis. There are three versions of the EVTMG commands.

- **EVTMG2:** Performs automatic TOF_DIFF measurements. The parameters and operation of the TOF measurement are described in the *Time-of-Flight (TOF) Measurement Operations* section.
- **EVTMG3:** Performs automatic Temperature measurements. The parameters and operation of the Temperature measurements are described in the *Temperature Measurement Operations* section.
- **EVTMG1:** Performs automatic TOF_DIFF and Temperature measurements.

Continuous Event Timing Operation

The MAX35101 can be configured to continue running event timing sequences at the completion of any sequence. If the ET_CONT bit in the Calibration and Control register is set, the currently executing EVTMGx command continues to execute until a HALT command is received by the MAX35101. If the ET_CONT bit is clear, automatic execution of event timing stops after the completion of a full sequence of measurements.

Continuous Interrupt Timing Operation

When operating in event timing mode, the $\overline{\text{INT}}$ pin can be asserted (if enabled) either after each TOF or temperature measurement, or at the completion of the sequence of measurements. If the CONT_INT bit in the Calibration and Control register is set to a 1, then the $\overline{\text{INT}}$ pin asserts (if enabled) at the completion of each TOF or temperature command. This allows the host microcontroller to interrogate the current event for accuracy of measurement. If the CONT_INT bit is set to a 0, then the $\overline{\text{INT}}$ pin only asserts (if enabled) at the completion of a sequence of measurements. This allows the host microcontroller to remain in a low-power sleep mode and only wake-up upon the assertion of the $\overline{\text{INT}}$ pin.

Error Handling During Event Timing Operation

During execution of event timing modes, any error that occurs during a TOF_DIFF or temperature measurement are handled as described in the corresponding error handling sections. Calibration can be executed during event timing operation, if programmed to do so with the calibration configuration bits in the Calibration and Control register. If a calibration error occurs, this is handled as described in the *Error Handling During Calibration* section. If any of these errors occur, the event timing operation does not terminate, but continues operation.

When making TOF measurements in event timing mode, the MAX35101 provides additional data in the TOF_Cycle_Count/TOF_Range register that can be used to check the validity of all of the TOF measurements. The TOF_Cycle_Count is the number of valid error-free TOF measurements that were recorded during an Event Timing Sequence. If a TOF error occurs, the TOF_Cycle_Count register will not be incremented. The TOF_Range is the range of all valid TOF measurements that were captured during a sequence.

When making temperature measurements in event timing mode, the MAX35101 provides additional data in the Temp_Cycle_Count register. This count increments after every valid error-free temperature measurement and can be used to check the validity of all of the temperature measurements. Also, the Temperature Average Results registers, TxAVG, are not updated with the error measurement if a temperature error occurs during event timing operation.

Event Timing Mode 2

The EVTMG2 command execution causes the TOF_DIFF command to be executed automatically with programmable repetition rates and programmable total counts as shown in Figure 7.

During execution of the EVTMG2 command, each TOF_DIFF command execution cycle causes the MAX35101 to compute a TOF_DIFF measurement (AVGUP register minus AVGDN register) as well as the running average of TOF_DIFF measurements (TOFF_DIFF_AVG register). The setting of the TDF[3:0] bits in the Event Timing 1 register selects the rate at which TOF_DIFF commands are executed. The setting of the TDM[4:0] bits in the Event Timing 1 register determines the number of TOF_DIFF measurements to be taken during the sequence.

Once all of the TOF_DIFF measurements in the sequence are captured, the TOF_DIFF_AVG register contains the average of the differences of the resultant AVGDN and AVGUP Results register content of each TOF_DIFF measurement. After the TOF_DIFF_AVG registers are updated, the TOF_EVTMG bit is set in the Interrupt Status register and the $\overline{\text{INT}}$ pin asserts (if enabled).

Event Timing Mode 3

The EVTMG3 command execution causes the temperature command to be executed automatically with programmable repetition rates and programmable total counts (Figure 9).

During execution of the EVTMG3 command, each Temperature command execution cycle computes the running average of the measurement of each temperature port. The results are provided in the Tx_AVGInt and TxAVGFrac Results registers.

The setting of the TMF[5:0] bits in the Event Timing 1 register selects the rate at which temperature commands are executed. The setting of the TMM[4:0] bits in the Event Timing 2 register determines the number of temperature measurements to be taken during the sequence.

Once all of the temperature measurements in the sequence are captured Tx_AVGInt and TxAVGFrac Results registers contains the average of all the temperature measurements in the sequence. After these registers are updated, the Temp_EVTMG bit is set in the Interrupt Status register and the $\overline{\text{INT}}$ pin asserts (if enabled).

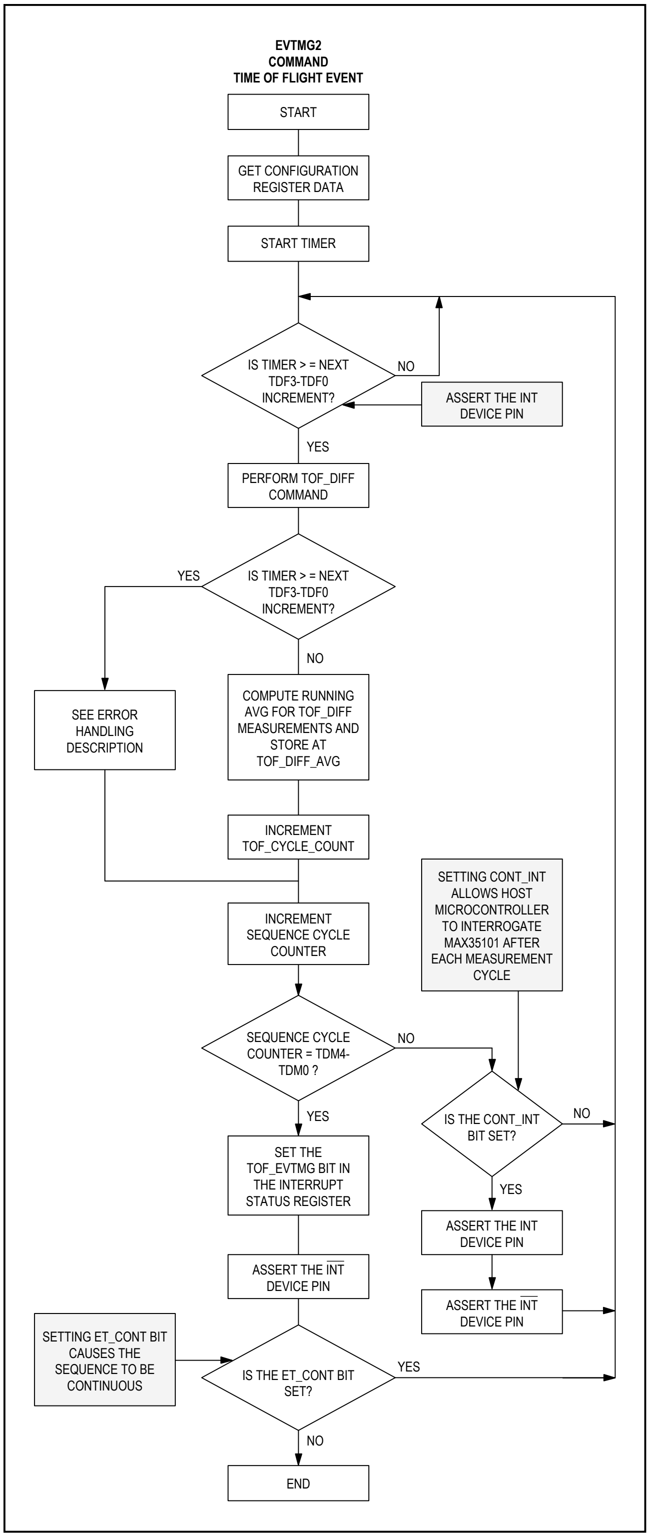


Figure 7. EVTMG2 Command

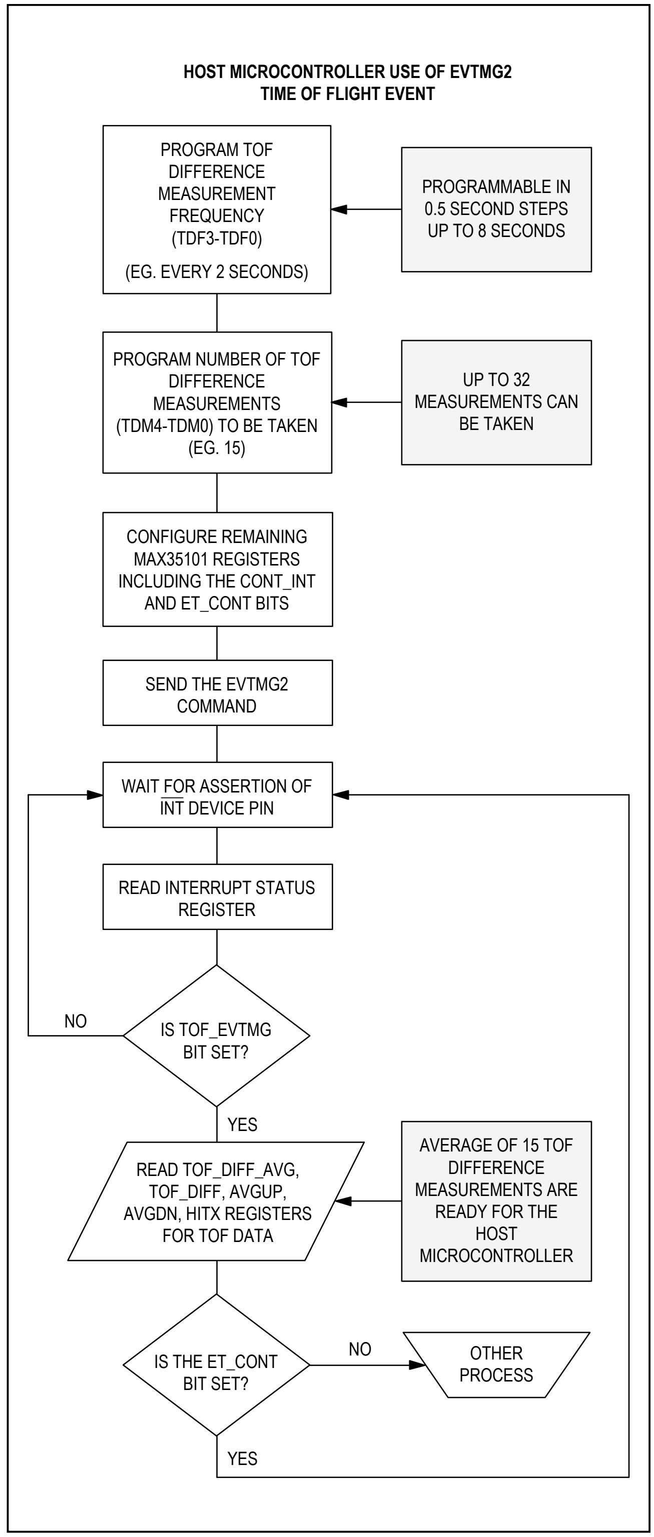


Figure 8. EVTMG2 Pseudo Code

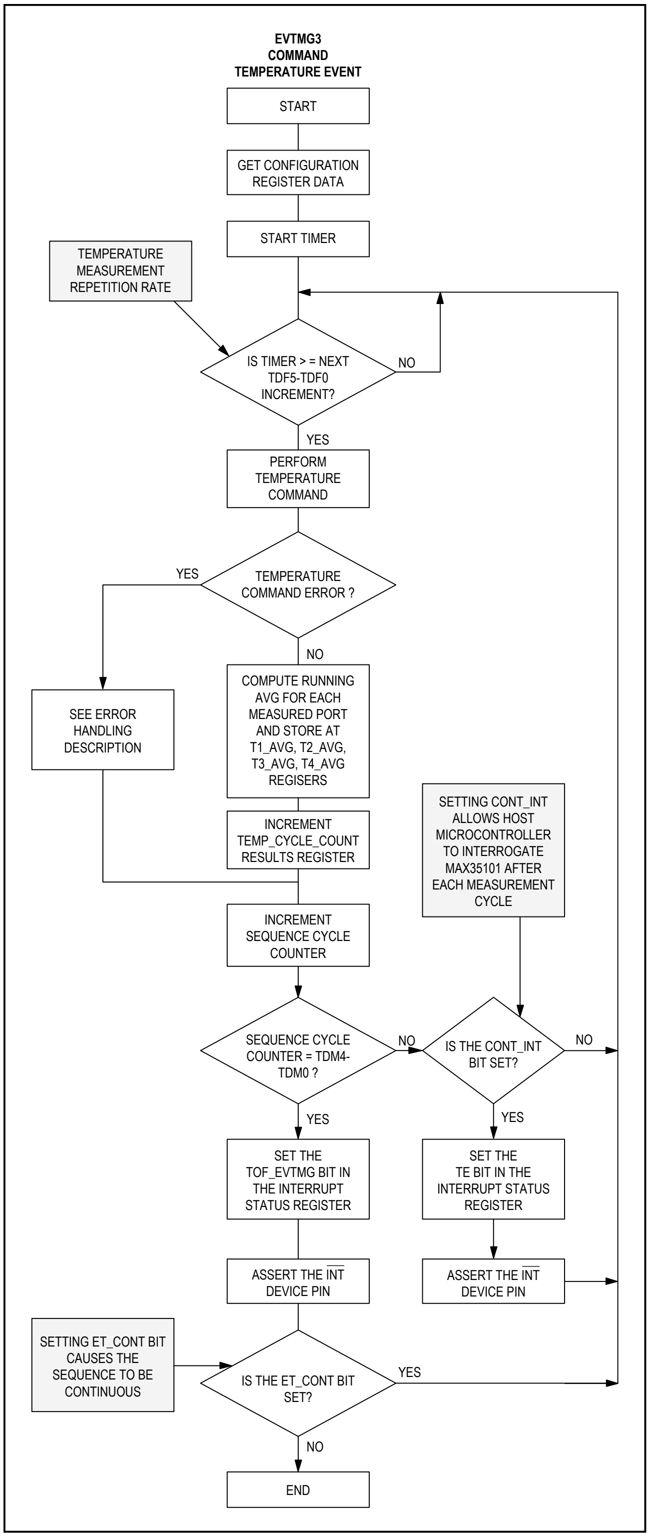


Figure 9. EVTMG3 Command

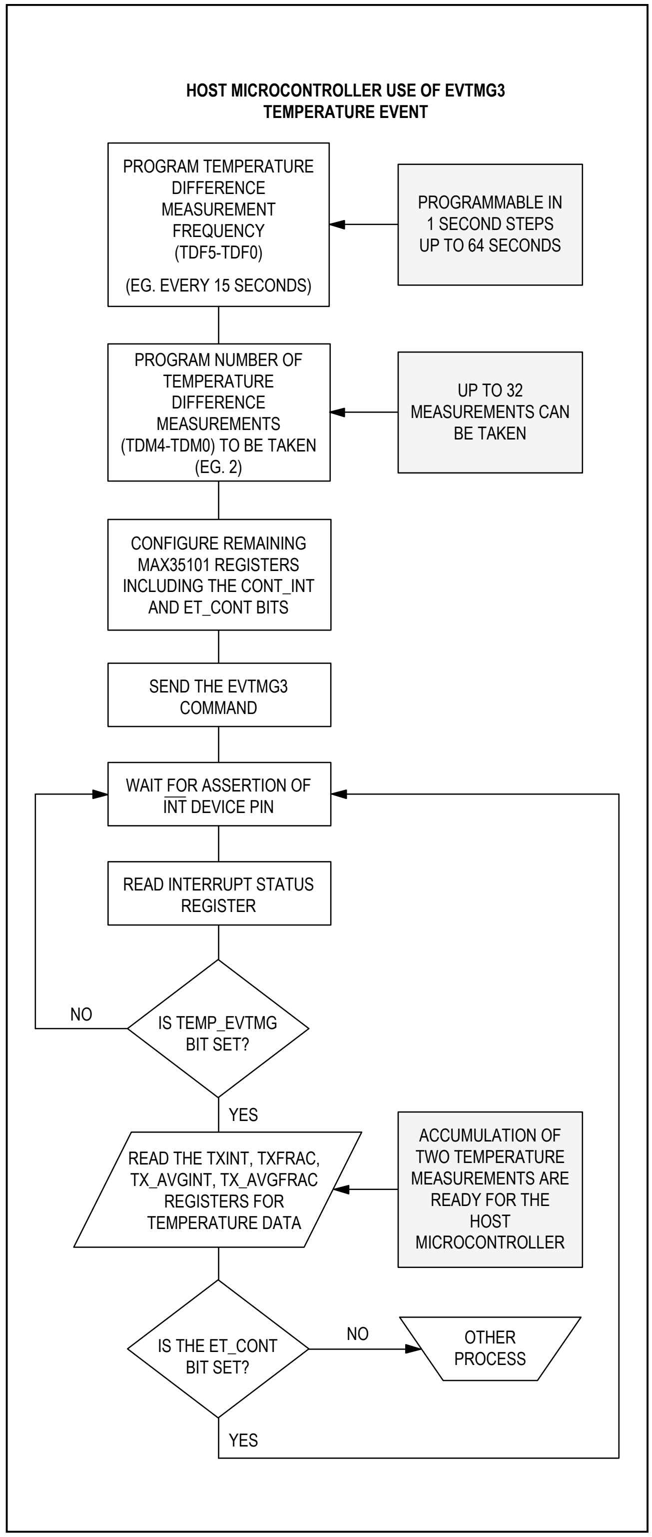


Figure 10. EVTMG3 Pseudo Code

Event Timing Mode 1

The EVTMG1 command execution causes the TOF_DIFF command and the temperature command to be executed automatically with programmable repetition rates and programmable total counts. In essence, both the EVTMG2 and EVTMG3 commands are simultaneously executed in a synchronous manner.

Setting up the TOF measurements for automatic execution in event timing mode 1 is identical to setting these up for execution with event timing mode 2. Likewise, setting up the temperature measurements is identical to setting these up for execution using event timing mode 3.

If the TOF_DIF command repetition rate and the temperature command repetition rate cause both measurements to be required at the same time, the TOFF_DIF command takes precedent. Upon completion of the TOFF_DIFF command, the pending temperature command is executed (Figure 12).

Once all of the TOF_DIFF measurements in the sequence are complete, the TOF_EVTMG bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled). Likewise, when all of the temperature measurements in the sequence are completed, the Temp_EVTMG bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled). It should be noted that depending upon the selected rates and number of cycles, the TOF_DIFF and temperature measurements can complete their sequences at different times. This causes the $\overline{\text{INT}}$ pin to assert (if enabled) before both sequences are complete.

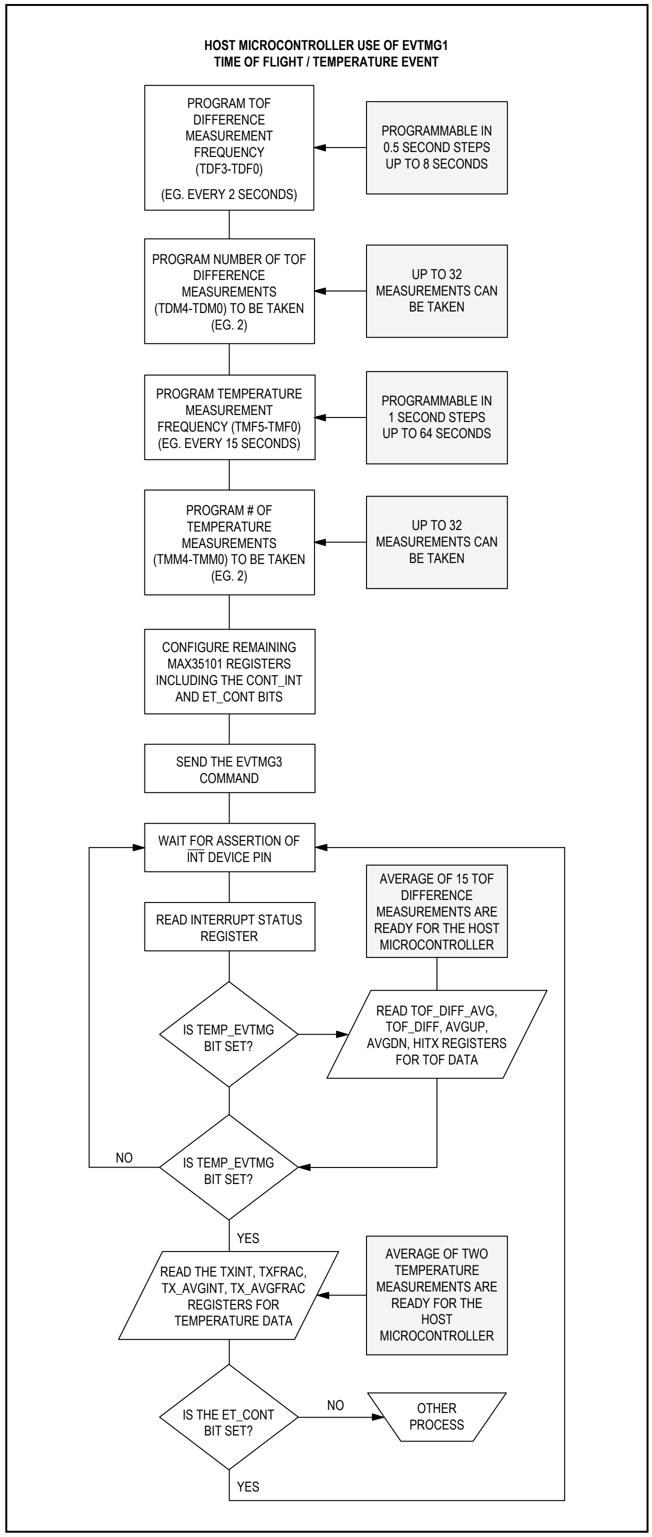


Figure 11. EVTMG1 Pseudo Code

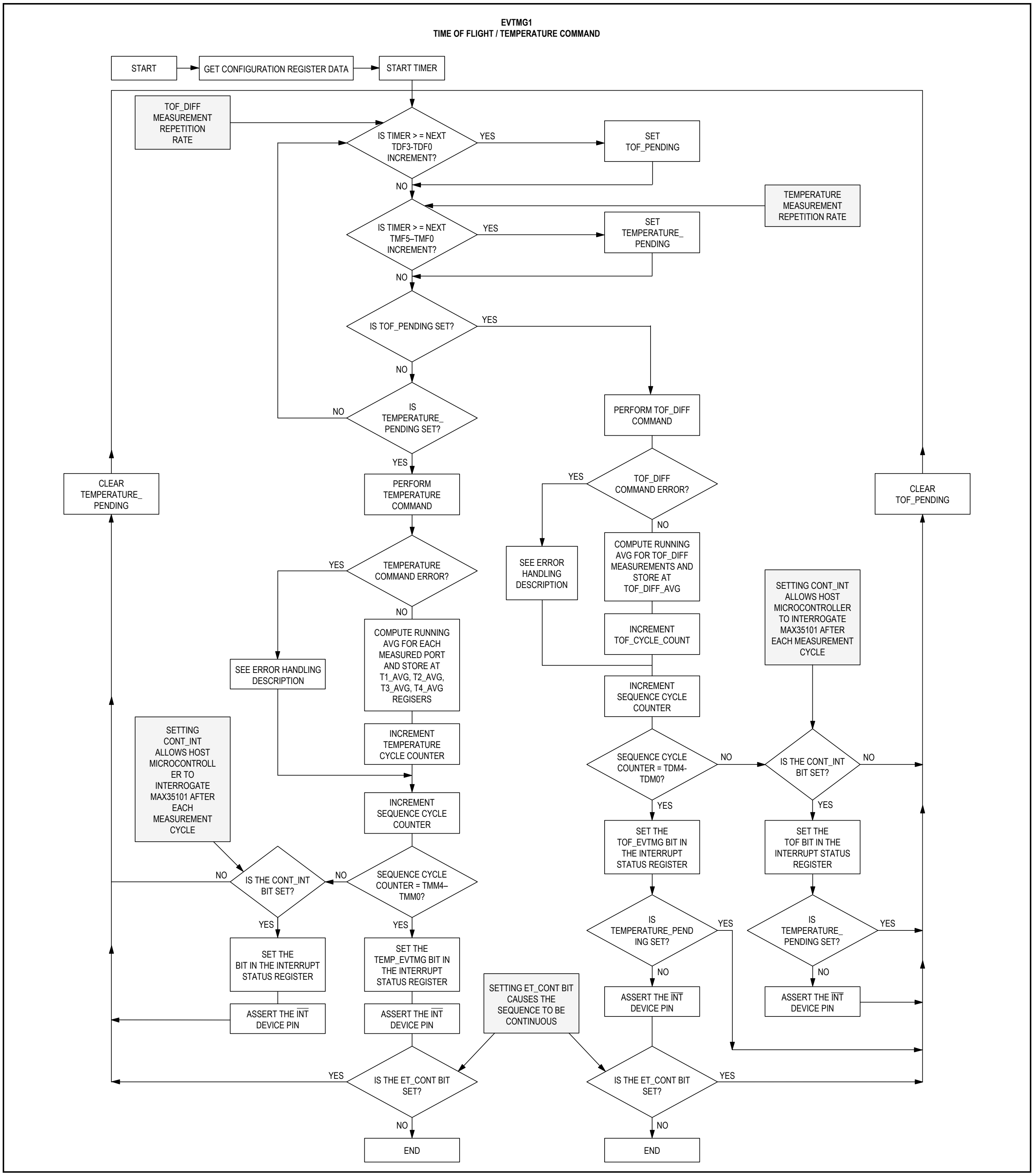


Figure 12. EVTMG1 Command

Calibration Operation

For more accurate results, calibration of the TDC can be performed. Calibration allows the MAX35101 to perform a calibration measurement that is based upon the 32.768kHz crystal, which is the most accurate clock in the system. This calibration is used when a ceramic oscillator is used in place of an AT-cut crystal for the 4MHz reference. The MAX35101 automatically generates START and STOP signals based upon edges of the 32.768kHz clock. The number of 32.768kHz clock periods that are used and then averaged are selected with the CAL_PERIOD[3:0] bits in the Calibration and Control register. The TDC measures the number of 4MHz clock pulses that occur during the 32.768kHz pulses. The measured time of a 32.768kHz clock pulse is reported in the CalibrationInt and CalibrationFrac Results registers. These results can then be used as a gain factor for calculating actual time-to-digital converter measurement if the CAL_USE bit in the Event Timing 2 Register is set.

Following is a description of an example calibration. Each TDC measurement is a 15-bit fixed-point integer value concatenated with a 16-bit fractional value binary representation of the number of t_{4MHz} periods that contribute to the time result, the actual period of t_{4MHz} needs to be known. If the CAL_PERIOD[3:0] bits in the Calibration and Control register are set to 6, then 6 measurements of 32.768kHz periods are measured by the TDC and then averaged. The expected measured value would be 30.5176μs/250ns = 122.0703125 t_{4MHz} periods. Assume that the 4MHz ceramic resonator is actually running at 4.02MHz. The TDC measurement unit would then measure 30.5176μs/248.7562ns = 122.6806641 t_{4MHz} periods and this result would be returned in the Calibration Results register. For all TDC measurements, a gain value of 122.0703125/122.6806641 = 0.995024876 would then be applied.

Calibration is performed at the following events:

- When the Calibration command is sent to the MAX35101. At the completion of this calibration, the CAL bit in the Interrupt Status register and the $\overline{INT}$ pin asserts (if enabled).
- During event timing operation, automatic calibrations can be performed before executing TOF or temperature measurements. This is selectable with the CAL_CFG[2:0] bits in the Event Timing 2 register. Upon completion of an automatic calibration during event timing, the result is updated in the Calibration Results register, but the CAL bit in the Interrupt Status register is not set and the $\overline{INT}$ pin does not assert.

Error Handling During Calibration

Since calibration can be set to be automatic by configuring the CAL_CFG[2:0] bits in the Event Timing 2 register, any errors that occur during the Calibrate command stop the CalibrationInt and the CalibrationFrac Results registers from being updated with new calibration coefficients. The results for the previous Calibration data remain in these two registers and are used for scaling measured results. If the calibration error is caused by the internal calibration time measurement exceeding the time set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

RTC, Alarm, Watchdog, and Tamper Operation

RTC Operation

The MAX35101 contains a real-time clock that is driven by a 32kHz oscillator. The time and calendar information is obtained by reading the appropriate register words. The time and calendar are set or initialized by writing the appropriate register words. The contents of the time and calendar registers are in the Binary-Coded Decimal (BCD) format. The clock/calendar provides hundredths of seconds, tenths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year valid up to 2100. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The MAX35101 real-time clock can be programmed for either 12-hour or 24-hour formats. If using the 24-hour format, Bit6 (12 HR MODE) of the Mins_Hrs register should be cleared to 0 and then Bit5 represents the 20-hour indicator. If using the 12-hour format, Bit6 should be set to 1 and Bit5 represents AM (if 0) or PM (if 1). The day-of-week register increments at midnight. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Alarm Operation

The MAX35101 real-time clock provides one programmable alarm. The alarm is activated when either the AM1 or AM2 bits in the Real-Time Clock register are set. Based upon these bits, an alarm can occur when either the minutes and/or hours programmed in the Alarm register match the current value in the Mins_Hrs register. When an alarm occurs, the AF bit in the Interrupt Status register is set and the $\overline{INT}$ device pin asserts (if enabled).

For proper alarm function, programming of the ALARM register HOURS bits must match the format (12- or 24-hour modes) used in the Mins_Hrs register.

Watchdog Operation

The MAX35101 also contains a watchdog alarm. The Watchdog Alarm Counter register is a 16-bit BCD counter that is programmable in 10ms intervals from 0.01s to 99.99s. A seed value may be written to this register representing the start value for the countdown. The watchdog counter begins decrementing when the WD_EN bit in the RTC register is set.

An immediate read of Watchdog Alarm Counter register returns the value just written. A read after a wait duration causes a value seed minus wait to be returned. For example if the seed value was 28.01s, an immediate read returns 28.01. A read after a 4s returns 24.01s. The value read out for any read operation is a snapshot obtained at the instant of a serial read operation.

A write operation to the Watchdog Alarm Counter register causes a reload with the newly written seed.

When the watchdog is enabled and a nonzero value is written into the Watchdog Alarm Counter register, the Watchdog Alarm Counter register decrements every 1/100s, until it reaches zero. At this point, the WF bit in the Real-Time Clock register is set and the $\overline{\text{WDO}}$ pin asserts low for typically 250ms. At the end of the pulse, the $\overline{\text{WDO}}$ pin becomes high impedance.

The WF flag remains set until cleared by writing WF to a logic 0 in the Real-Time Clock register. If the WF bit is cleared while the $\overline{\text{WDO}}$ device pin is being held low, the $\overline{\text{WDO}}$ device pin is immediately released to its high-impedance state. Writing a seed value of 0 does not cause the WF bit to assert.

Tamper Detect Operation

The MAX35101 provides a single input that can be connected to a device case switch and used for tamper detection. Upon detection of a case switch event the CSWA in the Control register and the CSWI bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ device pin is asserted (if enabled).

Device Interrupt Operations

The MAX35101 is designed to optimize the power efficiency of a flow metering application by allowing the host microprocessor to remain in a low-power sleep mode, instead of requiring the microprocessor to keep track of complex real-time events being performed by the MAX35101. Upon completion of any command, the MAX35101 alerts the host microprocessor using the $\overline{\text{INT}}$ pin. The assertion of the $\overline{\text{INT}}$ pin can be used to awaken the host microprocessor from its low power mode. Upon receiving an interrupt on the $\overline{\text{INT}}$ pin, the host microprocessor should read the Interrupt Status Register to determine which tasks were completed.

Interrupt Status Register

The interrupt status register contains flags for all for all commands and events that occur within the MAX35101. These flags are set when the event occurs or at the completion of the executing command. When the Interrupt Status Register is read, all asserted bits are cleared. If another interrupt source has generated an interrupt during the read, these new flags assert following the read.

$\overline{\text{INT}}$ Pin

The $\overline{\text{INT}}$ pin asserts when any of the bits in the Interrupt Status register are set. The $\overline{\text{INT}}$ pin remains asserted until the Interrupt Status register is read by the user and all bits in this register are clear. In order for the $\overline{\text{INT}}$ pin to operate, it must first be enabled by setting the INT_EN bit in the Calibration and Control register.

Serial Peripheral Interface Operation

Four pins are used for SPI-compatible communications: DOUT (serial-data out), DIN (serial-data in), $\overline{\text{CE}}$ (chip enable), and SCK (serial clock). DIN and DOUT are the serial data input and output pins for the devices, respectively. The $\overline{\text{CE}}$ input initiates and terminates a data transfer. SCK synchronizes data movement between the master (microcontroller) and the slave (MAX35101). The SCK, which is generated by the microcontroller, is active only when $\overline{\text{CE}}$ is low and during opcode and data transfer to any device on the SPI bus. The inactive clock polarity is logic-low. DIN is latched on the falling edge of SCK. There is one clock for each bit transferred. Opcode bits are transferred in groups of eight, MSB first. Data bits are transferred in groups of sixteen, MSB first.

The serial peripheral interface is used to access the features and memory of the MAX35101 using an opcode/command structure.

Opcode Commands

Table 2 shows the opcode/commands that are supported by the device.

Table 2. Opcode Commands

GROUP	COMMAND	OPCODE FIELD (HEX)	ADDRESS FIELD
Execution Opcode Commands	TOF_Up	00h	N/A
	TOF_Down	01h	N/A
	TOF_Diff	02h	N/A
	Temperature	03h	N/A
	Reset	04h	N/A
	Initialize	05h	N/A
	Transfer configuration to flash	06h	N/A
	EVTMG1	07h	N/A
	EVTMG2	08h	N/A
	EVTMG3	09h	N/A
	HALT	0Ah	N/A
	LDO_Timed	0Bh	N/A
	LDO_ON	0Ch	N/A
	LDO_OFF	0Dh	N/A
	Calibrate	0Eh	N/A
Register Opcode Commands	Read register	B0h through FFh. Each hex value represents the location of a single 16-bit register.	N/A
	Write register	30h through 43h. Each hex value represents the location of a single 16-bit register.	N/A
Flash Opcode Commands	Read flash	90h	0000h - 1FFFh 8 Kbytes Even Only
	Write flash	10h	0000h - 1FFFh 8 Kbytes Even Only
	Block erase flash	13h	0000h - 1FFFh

Execution Opcode Commands

The device supports several single byte opcode commands that cause the MAX35101 to execute various routines. All commands have the same SPI protocol sequence as shown in Figure 13. Once all 8 bits of the opcode are received by the MAX35101 and the $\overline{CE}$ device pin is deasserted, the MAX35101 begins execution of the specified command as described in that Command's description.

TOF_UP Command (00h)

The TOF_UP command generates a single TOF measurement in the upstream direction. Pulses launch from the LAUNCH_UP pin and are received by the STOP_UP pin. The measured hit results are reported in the HITxUPInt and HITxUPFrac registers, with the calculated average of all the measured hits being reported in the AVGUPInt and AVGUPFrac register. The t_1/t_2 and t_2/tideal wave ratios are reported in the WVRUP register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Note: The TOF_UP command yields a result that is only of use when used in conjunction with the TOF_DN command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

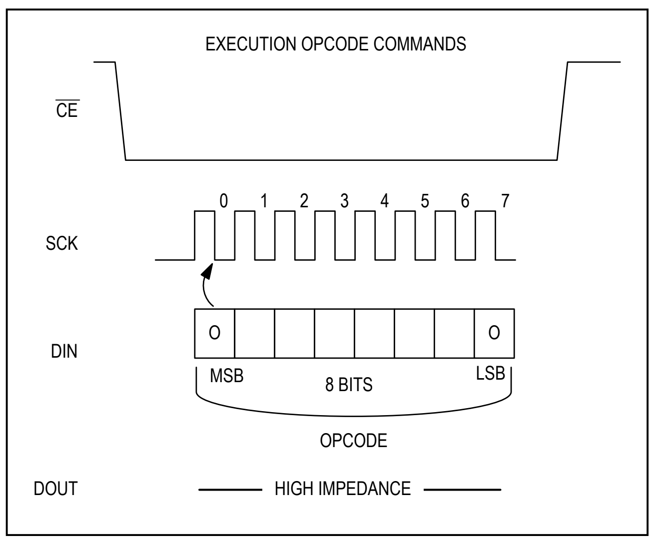


Figure 13. Execution Opcode Command Protocol

TOF_Down Command (01h)

The TOF_DOWN command generates a single TOF measurement in the downstream direction. Pulses launch from the LAUNCH_DN pin and are received by the STOP_DN pin. The measured hit results are reported in the HITxDnInt and HITxDnFrac registers, with the calculated average of all the measured hits being reported in the AVGDNInt and AVGDNFrac register. The t_1/t_2 and t_2/t_{ideal} wave ratios are reported in the WVRDN register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Note: The TOF_Down command yields a result that is only of use when used in conjunction with the TOF_UP command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

TOF_DIFF Command (02h)

The TOF_DIFF command performs back-to-back TOF_UP and TOF_DN measurements as required for a metering application. The TOF_UP sequence is followed by the TOF_DN sequence. The time between the start of the TOF_UP measurement and the start of the TOF_DN measurement is set by the TOF_CYC[2:0] bits in the TOF2 register. Upon completion of the TOF_DN measurement, the results of AVGUP minus AVGDN is computed and stored at the TOF_DIFFInt and TOF_DIFFFrac Results register locations. Once these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin asserts (if enabled).

Temperature Command (03h)

The temperature command initiates a temperature measurement sequence as described in the *Temperature Measurement Operations* section. The characteristics the temperature measurement sequence depends upon the settings in the Event Timing 1 register, and Event Timing 2 register. Once all the measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register also is set and the $\overline{INT}$ pin asserts (if enabled).

Reset Command (04h)

The reset command essentially performs the same function as a power-on reset (POR), and causes all of the Configuration registers to be set to their prior programmed values stored in flash and all of the Results registers and the Interrupt Status register to be cleared and set to zero.

Initialize Command (05h)

The initialize command must be executed after all configuration of the device is complete. This initializes the time-to-digital converter so that TOF and temperature commands can be executed. The MAX35101 sets the INIT bit in the Interrupt Status register and asserts the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the initialize command has completed and the next desired command can be sent to the MAX35101.

Transfer Configuration to Flash Command (06h)

This command causes the Configuration register map to be transferred to flash for nonvolatile (NV) storage. The MAX35101 automatically turns on the LDO for the duration of this transfer. Upon device reset, the content of this flash restores the Configuration registers. This flash is not part of the 8KB array, and is reserved solely for the transfer configuration to the flash command. The MAX35101 sets the flash bit in the Interrupt Status register and asserts the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the transfer configuration to the flash command has completed and the next command can be sent to the device.

EVTMG1 Command (07h)

The EVTMG1 command initiates the event timing mode 1 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF and Temperature measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, Event Timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG2 Command (08h)

The EVTMG2 command initiates the event timing mode 2 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG3 Command (09h)

The EVTMG3 command initiates the event timing mode 3 advanced automatic measurement feature. This timing mode performs automatic temperature measurements as described in the *Event Timing Operation* section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, Event timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

HALT Command (0Ah)

The HALT command is sent to the MAX35101 to stop any of the three EVTMG1/2/3 commands. All register data content is frozen and the SPI is then made available for access by the host microcontroller for commands, memory access, and register access. The HALT command takes time to execute. Since the EVTMGx commands are comprised of multiple TOF_DIFF and Temperature commands, the HALT command causes the MAX35101 to evaluate its own state and complete the currently executing TOF_DIFF or temperature command. Once the HALT command has completed, all registers update and the MAX35101 sets the halt bit in the Interrupt Status register and then asserts the $\overline{INT}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source.

LDO_Timed Command (0Bh)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_Timed command to the MAX35101 prior to the desired flash access command (read, write, block erase), the internal regulator is enabled and powers the flash circuitry. The LDO bit is set in the Interrupt Status register and the $\overline{INT}$ device pin asserts (if enabled) when the internal regulator has been turned on and is stable which takes approximately t_{STABLE}. The host microprocessor, upon detection of the asserted $\overline{INT}$ device pin, should read the Interrupt Status register LDO bit to determine that the internal regulator is stable and the flash is now ready to be accessed. The internal regulator remains enabled for a continuous period until the $\overline{CE}$ device pin is deasserted after any flash command (read, write, block erase). The LDO_Timed command is used in place of the LDO_ON command when a data access to the flash is required in a short burst. This minimizes SPI access since the LDO_OFF command is not required to be sent to the MAX35101 to turn off the internal regulator.

LDO_ON Command (0Ch)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_ON command to the MAX35101 prior to the desired flash access command (read, write, block erase), the internal regulator is enabled and powers the flash circuitry. The LDO bit is set in the Interrupt Status register and the $\overline{INT}$ device pin asserts (if enabled) when the internal regulator has been turned on and is stable which takes approximately t_{STABLE}. The host microprocessor, upon detection of the asserted $\overline{INT}$ device pin, should read the Interrupt Status register LDO bit to determine that the internal regulator is stable and the flash is now ready to be accessed. The internal regulator remains enabled for a continuous period until the LDO_OFF command is received by the MAX35101. The LDO_ON command is generally used when the host microprocessor needs to perform multiple-word writes to the MAX35101 since multiple-word writes require that the $\overline{CE}$ device pin be toggled after every word of data written. The LDO_ON command prevents the LDO from automatically disabling itself after each transition of the $\overline{CE}$ device pin.

LDO_OFF Command (0Dh)

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. By sending the LDO_OFF command to the MAX35101, the internal regulator is disabled and the Interrupt Status register LDO bit is cleared. The $\overline{INT}$ device pin is not asserted. The LDO_OFF command is used in conjunction with the LDO_ON command.

Calibrate Command (0Eh)

The calibrate command performs the calibration routine as described in the calibration operation section. When the calibrate command has completed the measurement, the Calibration Results register contains the measured 32kHz period measuremnt value, the MAX35101 sets the calibration bit in the Interrupt Status register and then asserts the $\overline{INT}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source and then read the Calibration Results register to be able to calculate the 4MHz ceramic oscillator gain factor.

Register Opcode Commands

To manipulate the register memory, there are two commands supported by the device: Read Register and Write register. Each register accessed with these commands is 16 bits in length. These commands are used to access all sections of the memory map including the RTC and Watchdog registers, Configuration registers, Conversion Results registers, and Status registers. The Conversion Results registers and the Interrupt Status register of the Status registers are all read only.

Read Register Command

The opcode must be clocked into the DIN device pin before the DOUT device pin produces the register data. The SPI protocol sequence is shown in Figure 14.

The read register command can also be used to read consecutive addresses. In this case, the data bits are continuously delivered in sequence starting with the MSB of the data register that is addressed in the opcode, and continues with each SCK rising edge until the $\overline{CE}$ device pin is deasserted as shown in Figure 15. The address counter automatically increments.

Write Register Command

This command applies to all writable registers. See the *Register Memory Map* for more detail. The SPI protocol sequence is shown in Figure 16.

The write register command can also be used to write consecutive addresses. In this case, the data bits are continuously received on the DIN device pin and bound for the initial starting address register that is addressed in the opcode. The address counter automatically increments after each 16 bits of data if the SCK device pin is continually clocked and the $\overline{CE}$ device pin remain asserted as shown in Figure 17.

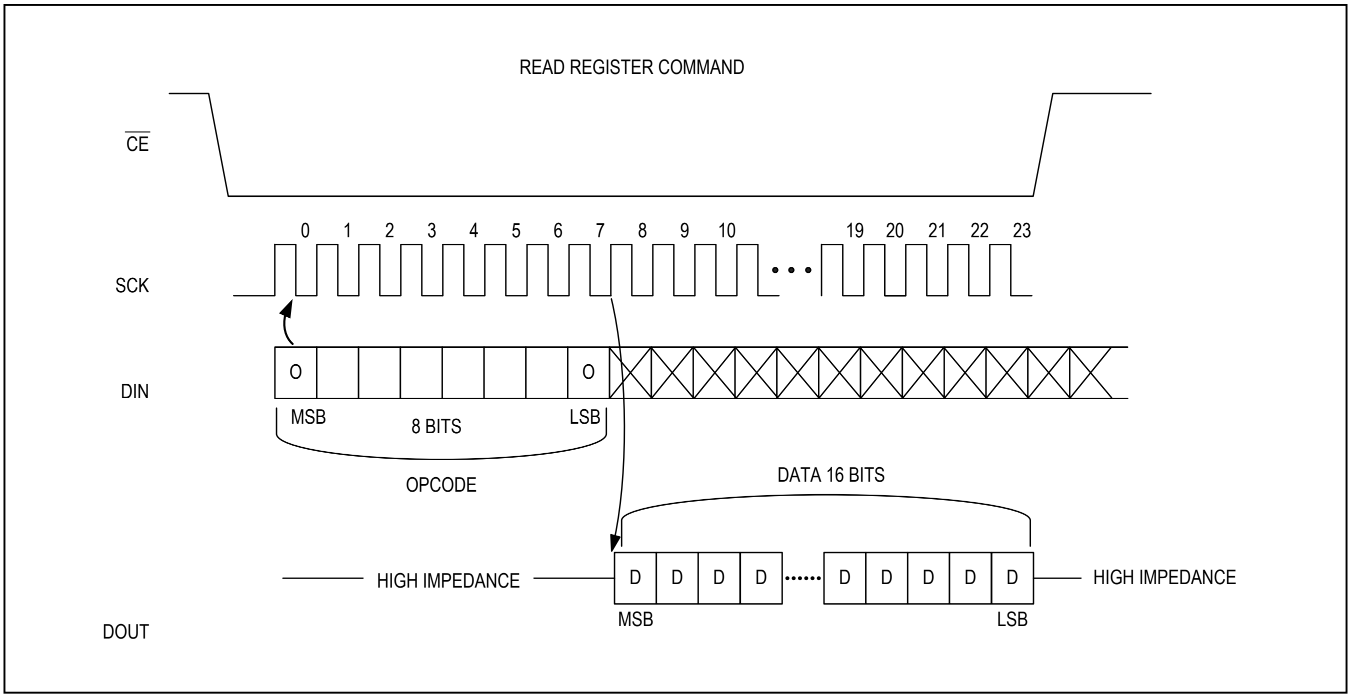


Figure 14. Read Register Opcode Command Protocol

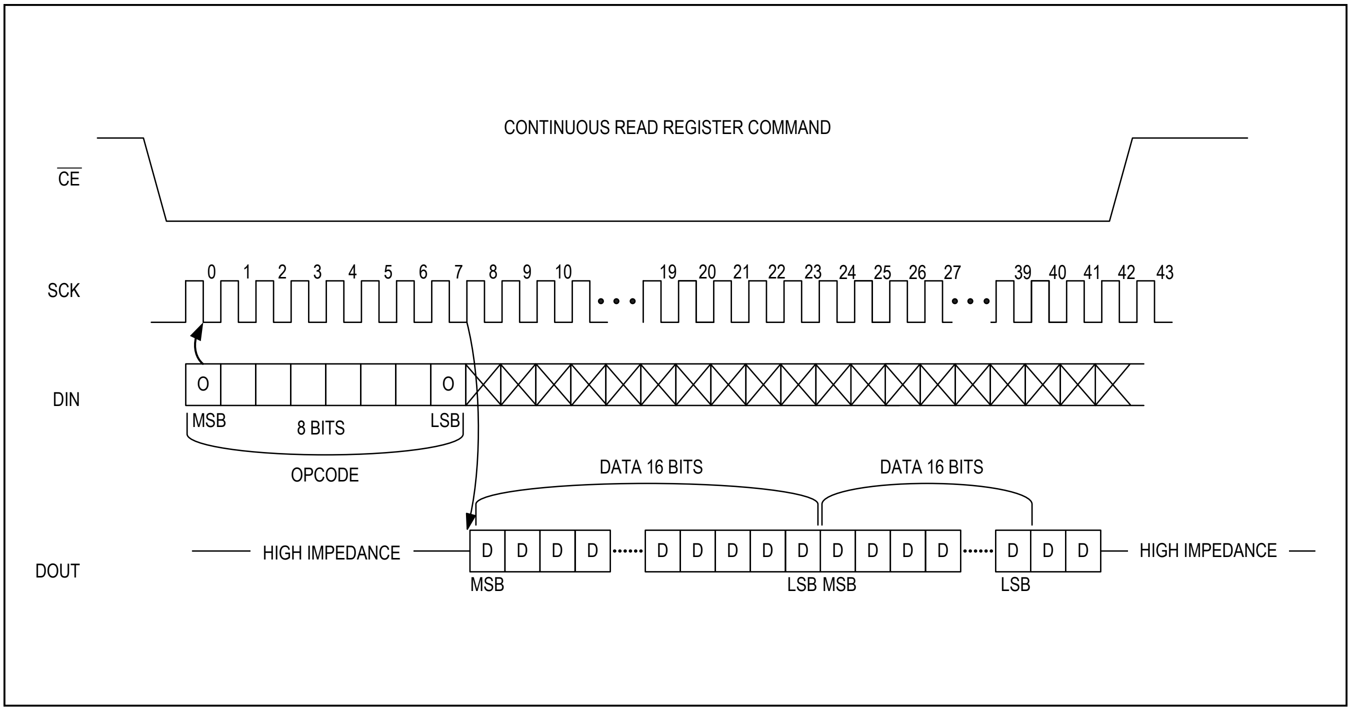


Figure 15. Continuous Read Register Opcode Command Protocol

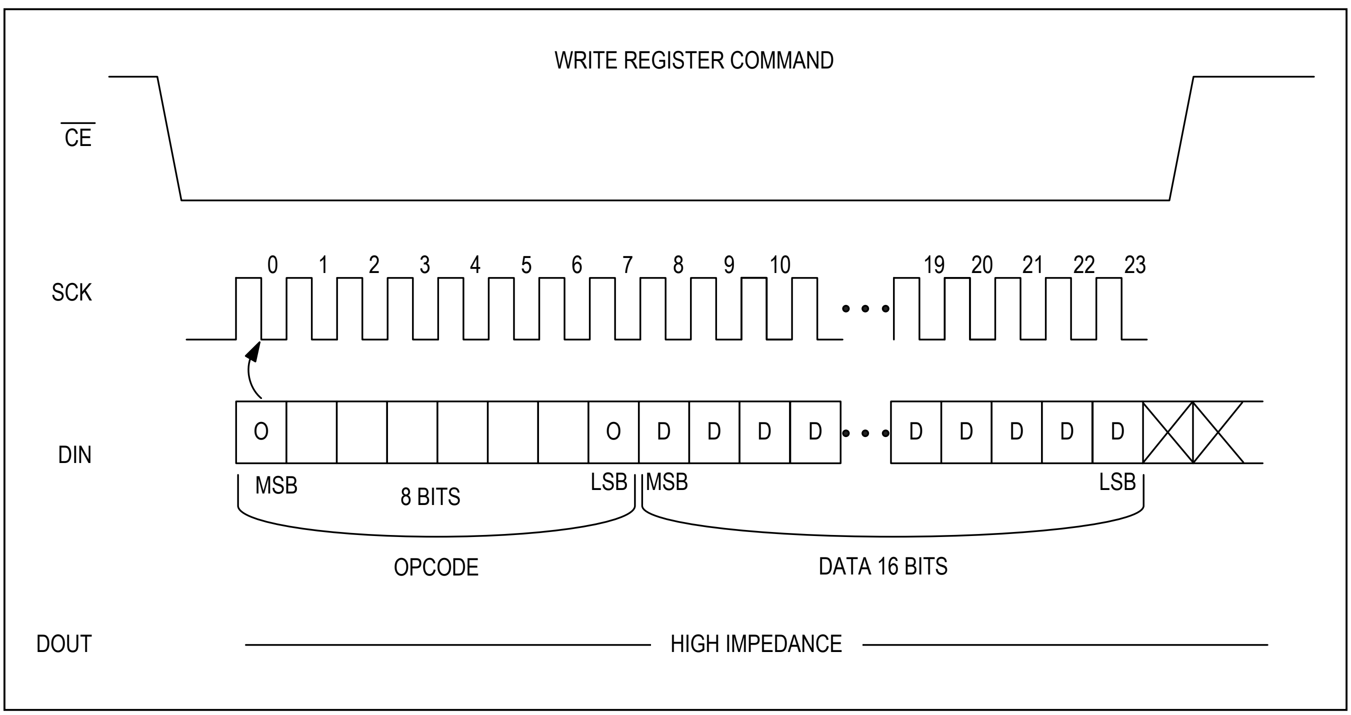


Figure 16. Write Register Opcode Command Protocol

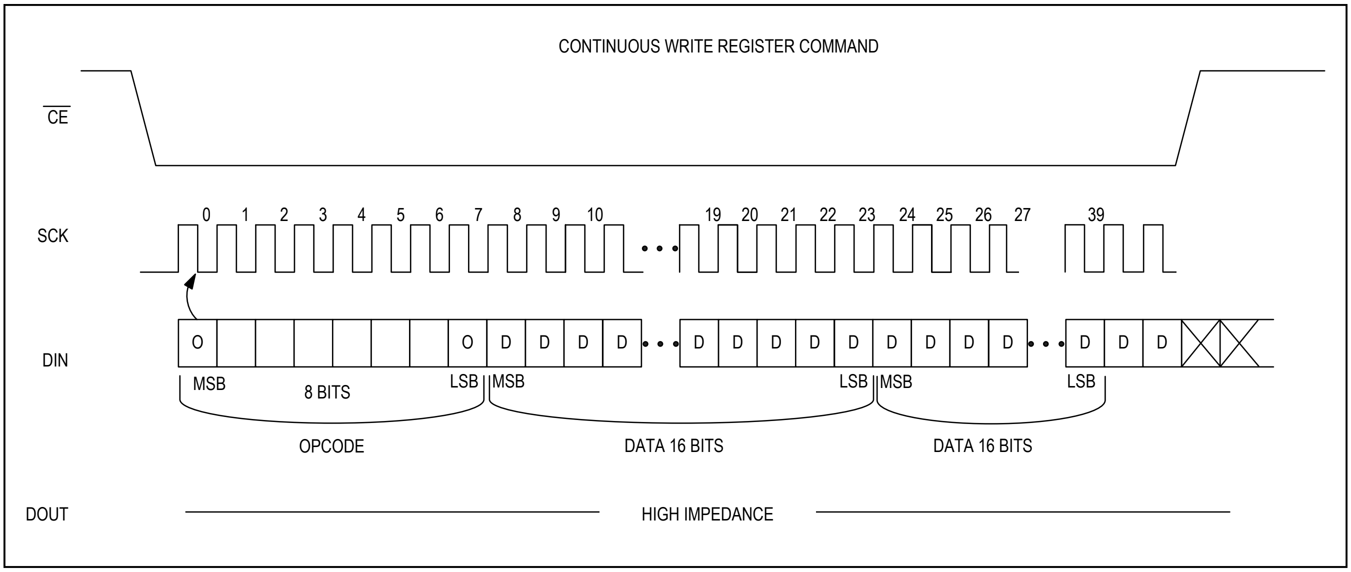


Figure 17. Continuous Write Register Opcode Command Protocol

Register Memory Map

These registers are accessed by the read register command and the Write Register command: “X” represents a reserved bit. Following a reset, all configuration variables are recalled from flash. The factory-stored flash default value for all configuration registers except TOF1 is 0000h.

The factory-stored flash configuration for TOF1 is 0010h. After a transfer to configuration to flash command, the new user configuration data is recalled from flash after a reset.

The RTC register, Results registers, Interrupt Status, and Control registers are all 0000h following a reset.

Table 3. Register Memory Map

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
RTC AND WATCHDOG REGISTERS																		
B0h	30h	Seconds	Tenths of Seconds				Hundredth Seconds				10 Seconds				Seconds			
B1h	31h	Mins_Hrs	10-Minutes				Minutes				0	12hr	20hr/AM/PM	10hr	Hours			
B2h	32h	Day_Date	Day								10-Date				Date			
B3h	33h	Month_ Year	10-Month				Month				10-Year				Year			
B4h	34h	Watchdog Alarm Counter	Tenths of Seconds				Hundredths of Seconds				10 Seconds				Seconds			
B5h	35h	Alarm	10-Minutes				Minutes				0	12hr	20hr/AM/PM	10hr	Alarm Hours			
CONFIGURATION REGISTERS These registers are restored from flash memory upon device reset. These registers are written to flash memory upon the issuance of the transfer configuration to flash command.																		
B6h	36h		Reserved															
B7h	37h		Reserved															
B8h	38h	TOF1	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DPL3	DPL2	DPL1	DPL0	STOP _POL	X	CT1	CT0
B9h	39h	TOF2	STOP 2	STOP 1	STOP 0	T2WV 5	T2WV 4	T2WV 3	T2WV 2	T2WV 1	T2WV0	TOF_ CYC2	TOF_ CYC1	TOF_ CYC0	EN_U P_DN	TIM OUT2	TIM OUT1	TIM OUT0
BAh	3Ah	TOF3	X	X	Hit1 WV5	Hit1 WV4	Hit1 WV3	Hit1 WV2	Hit1 WV1	Hit1 WV0	X	X	Hit2 WV5	Hit2 WV4	Hit2 WV3	Hit2 WV2	Hit2 WV1	Hit2 WV0
BBh	3Bh	TOF4	X	X	Hit3 WV5	Hit3 WV4	Hit3 WV3	Hit3 WV2	Hit3 WV1	Hit3 WV0	X	X	Hit4 WV5	Hit4 WV4	Hit4 WV3	Hit4 WV2	Hit4 WV1	Hit4 WV0
BCh	3Ch	TOF5	X	X	Hit5 WV5	Hit5 WV4	Hit5 WV3	Hit5 WV2	Hit5 WV1	Hit5 WV0	X	X	Hit6 WV5	Hit6 WV4	Hit6 WV3	Hit6 WV2	Hit6 WV1	Hit6 WV0
BDh	3Dh	TOF6	C_OF FSET RUP7	C_OF FSET RUP6	C_OF FSET RUP5	C_OF FSET RUP4	C_OF FSET RUP3	C_OF FSET RUP2	C_OF FSET RUP1	C_OF FSET RUP0	C_OF FSET UP7	C_OF FSET UP6	C_OF FSET UP5	C_OF FSET UP4	C_OF FSET UP3	C_OF FSET UP2	C_OF FSET UP1	C_OF FSET UP0
BEh	3Eh	TOF7	C_OF FSET RDN7	C_OF FSET RDN6	C_OF FSET RDN5	C_OF FSET RDN4	C_OF FSET RDN3	C_OF FSET RDN2	C_OF FSET RDN1	C_OF FSET RDN0	C_OF FSET DN7	C_OF FSET DN6	C_OF FSET DN5	C_OF FSET DN4	C_OF FSET DN3	C_OF FSET DN2	C_OF FSET DN1	C_OF FSET DN0
BFh	3Fh	Event Timing 1	TDF3	TDF2	TDF1	TDF0	TDM4	TDM3	TDM2	TDM1	TDM0	TMF5	TMF4	TMF3	TMF2	TMF1	TMF0	X

Table 3. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
C0h	40h	Event Timing 2	TMM4	TMM3	TMM2	TMM1	TMM0	Cal_ Use	Cal_ AUTO	Cal_ CFG1	Cal_ CFG0	TP1	TP0	PREC YC2	PREC YC1	PREC YC0	PORT CYC1	PORT CYC0
C1h	41h	TOF Measure-ment Delay	DLY15	DLY14	LY13	DLY12	DLY11	DLY10	DLY9	DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
C2h	42h	Calibration and Control	X	X	X	X	CMP_ EN	CMP_ SEL	INT_ EN	ET_ CONT	CONT _INT	CLK_ S2	CLK_ S1	CLK_ S0	Cal_P eriod3	Cal_P eriod2	Cal_P eriod1	Cal_P eriod0
C3h	43h	Real-Time Clock	X	X	X	X	X	X	X	X	X	32K_ BP	32K_ EN	EOSC	AM2	AM1	WF	WD_ EN
CONVERSION RESULTS REGISTERS																		
C4h	Read Only		WVRUP															
C5h	Read Only		Hit1UpInt															
C6h	Read Only		Hit1UpFrac															
C7h	Read Only		Hit2UpInt															
C8h	Read Only		Hit2UpFrac															
C9h	Read Only		Hit3UpInt															
CAh	Read Only		Hit3UpFrac															
CBh	Read Only		Hit4UpInt															
CCh	Read Only		Hit4UpFrac															
CDh	Read Only		Hit5UpInt															
CEh	Read Only		Hit5UpFrac															
CFh	Read Only		Hit6UpInt															

Table 3. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]	BITS[7:0]
D0h	Read Only		Hit6UpFrac	
D1h	Read Only		AVGUPInt	
D2h	Read Only		AVGUPFrac	
D3h	Read Only		WVRDN	
D4h	Read Only		Hit1DnInt	
D5h	Read Only		Hit1DnFrac	
D6h	Read Only		Hit2DnInt	
D7h	Read Only		Hit2DnFrac	
D8h	Read Only		Hit3DnInt	
D9h	Read Only		Hit3DnFrac	
DAh	Read Only		Hit4DnInt	
DBh	Read Only		Hit4DnFrac	
DCh	Read Only		Hit5DnInt	
DDh	Read Only		Hit5DnFrac	
DEh	Read Only		Hit6DnInt	
DFh	Read Only		Hit6DnFrac	
E0h	Read Only		AVGDNInt	

Table 3. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]	BITS[7:0]
E1h	Read Only		AVGDNFrac	
E2h	Read Only		TOF_DIFFInt	
E3h	Read Only		TOF_DIFFFrac	
E4h	Read Only		TOF_Cycle_Count	
E5h	Read Only		TOF_DIFF_AVGInt	
E6h	Read Only		TOF_DIFF_AVGFrac	
E7h	Read Only		T1Int	
E8h	Read Only		T1Frac	
E9h	Read Only		T2Int	
EAh	Read Only		T2Frac	
EBh	Read Only		T3Int	
ECh	Read Only		T3Frac	
EDh	Read Only		T4Int	
EEh	Read Only		T4Frac	
EFh	Read Only		Temp_Cycle_Count	
F0h	Read Only		T1_AVGInt	
F1h	Read Only		T1_AVGFrac	

Table 3. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
F2h	Read Only		T2_AVGInt															
F3h	Read Only		T2_AVGFrac															
F4h	Read Only		T3_AVGInt															
F5h	Read Only		T3_AVGFrac															
F6h	Read Only		T4_AVGInt															
F7h	Read Only		T4_AVGFrac															
F8h	Read Only		CalibrationInt															
F9h	Read Only		CalibrationFrac															
FAh	Read Only		Reserved															
FBh	Read Only		Reserved															
FCh	Read Only		Reserved															
FDh	Read Only		Reserved															
STATUS REGISTERS																		
FEh	Read Only	Interrupt Status	TO	AF	X	TOF	TE	LDO	TOF_ EVTMG	TEMP_ EVTMG	FLASH	CAL	HALT	CSWI	INIT	POR	X	X
FFh	Read Only	Control	X	X	X	X	X	X	AFA	CSWA	X	X	X	X	X	X	X	X

RTC and Watchdog Register Descriptions

Table 4. RTC Seconds Register

WRITE OPCODE 30h	READ OPCODE B0h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	Tenths of Seconds				Hundredths of Seconds			
Bit	7	6	5	4	3	2	1	0
Name	0	10 Seconds			Seconds			

BIT	NAME	DESCRIPTION
15:12	Tenths of Seconds	Range 0 to 9
11:8	Hundredths of Seconds	Range 0 to 9
7	0	This bit always returns 0
6:4	10 Second	Range 0 to 5
3:0	Seconds	Range 0 to 9

Table 5. RTC Mins_Hrs Register

WRITE OPCODE 31h	READ OPCODE B1h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	0	10 Minutes			Minutes			
Bit	7	6	5	4	3	2	1	0
Name	0	12/24	20HR/AM/PM	10HR	Hours			

BIT	NAME	DESCRIPTION
15	0	This bit always returns 0
14:12	10 Minutes	Range 0 to 5
11:8	Minutes	Range 0 to 9
7	0	This bit always returns 0

Table 5. RTC Mins_Hrs Register (continued)

BIT	NAME	DESCRIPTION
6	12/24	1 = 12-hour mode 0 = 24-hour mode
5	20HR/AM/PM	In 12-hour mode 1 = PM 0 = AM In 24-hour mode: 20-hour digit
4	10HR	Range 0 to 1
3:0	Hours	Range 0 to 9

Table 6. RTC Day_Date Register

WRITE OPCODE 32h	READ OPCODE B2h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	0	0	Day		
Bit	7	6	5	4	3	2	1	0
Name	0	0	10 Date		Date			

BIT	NAME	DESCRIPTION
15:11	0	These bits always return 0
10:8	Day	Range 0 to 7
7:6	0	These bits always return 0
5:4	10 Date	Range 0 to 3
3:0	Date	Range 0 to 9

Table 7. RTC Month_Year Register

WRITE OPCODE 33h	READ OPCODE B3h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	10 Month	Month			
Bit	7	6	5	4	3	2	1	0
Name	10 Year				Year			

BIT	NAME	DESCRIPTION
15:13	0	These bits always return 0
12	10 Month	Range 0 to 1
11:8	Month	Range 0 to 9
7:4	10 Year	Range 0 to 9
3:0	Year	Range 0 to 9

Table 8. Watchdog Alarm Counter Register

WRITE OPCODE 34h	READ OPCODE B4h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	Tenths of Seconds				Hundredths of Seconds			
Bit	7	6	5	4	3	2	1	0
Name	10 Seconds				Seconds			

BIT	NAME	DESCRIPTION
15:12	Tenths of Seconds	Range 0 to 9
11:8	Hundredths of Seconds	Range 0 to 9
7:4	10 Second	Range 0 to 9
3:0	Seconds	Range 0 to 9

Table 9. Alarm Register

WRITE OPCODE 35h	READ OPCODE B5h	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	10 Minutes			Minutes			
Bit	7	6	5	4	3	2	1	0
Name	X	12/24	20HR/AM/PM	10HR	Hours			

BIT	NAME	DESCRIPTION
15	X	Reserved
14:12	10 Minutes	Range 0 to 5
11:8	Minutes	Range 0 to 9
7	X	Reserved
6	12/24	1 = 12-hour mode 0 = 24-hour mode
5	20HR/AM/PM	In 12-hour mode 1 = PM 0 = AM In 24-hour mode: 20-hour digit
4	10HR	Range 0 to 1
3:0	Hours	Range 0 to 9

Configuration Register Descriptions

Table 10. TOF1 Register

WRITE OPCODE 38h	READ OPCODE B8h	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0010h

Bit	15	14	13	12	11	10	9	8
Name	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
Bit	7	6	5	4	3	2	1	0
Name	DPL3	DPL2	DPL1	DPL0	STOP_POL	X	CT1	CT0

Table 10. TOF1 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>15:8</td><td>PL[7:0]</td><td>Pulse Launcher Size: This is a hex value that defines the number of pulses that will be launched from the pulse launcher during transmission. The range of this hex value is 00h to FFh. When PL[7:0] is set to 00h, the Pulse Launcher is disabled. Up to 127 pulses can be launched. When PL7 is set, the pulse count is clamped at 127.</td></tr>
<tr><td>7:4</td><td>DPL[3:0]</td><td>Pulse Launch Divider: This is a hex value that defines the divider ratio of the internal clock signal used to drive the Pulse Launch signal. The 4MHz external reference oscillator is used as the source for the internal clock reference. The internal reference clock is first divided by 2 to produce a 2MHz clock. The range of this hex value is 1h to Fh, resulting in a range of division from ÷2 to ÷16 of the 2MHz clock. A value of 0h is not supported and should not be programmed
Pulse Launch Frequency = 2MHz/(1+DPL[3:0])
<table>
<tr><th>DPL[3:0]</th><th>PULSE LAUNCH FREQUENCY</th></tr>
<tr><td>0000b</td><td>RESERVED</td></tr>
<tr><td>0001b</td><td>1MHz</td></tr>
<tr><td>0002b</td><td>666kHz</td></tr>
<tr><td>….</td><td>….</td></tr>
<tr><td>1110b</td><td>133.33kHz</td></tr>
<tr><td>1111b</td><td>125kHz</td></tr>
</table></td></tr>
<tr><td>3</td><td>STOP_POL</td><td>Stop Polarity: This bit defines the edge sensitivity of the STOP_UP and STOP_DN channel. The signal received on the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the rising slope of this signal if this bit is set to 0. The signal received on the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the falling slope of this signal if this bit is set to 1.</td></tr>
<tr><td>2</td><td>X</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>CT[1:0]</td><td>Bias Charge Time: This is the time allotted for charging the external bias network on the STOP pins to produce common mode biasing for the analog receiver/comparator. It is based upon the 32.768 KHz crystal:
<table>
<tr><th rowspan="2">CT1</th><th rowspan="2">CT2</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES (decimal)</th><th>TYPICAL TIME (µs)</th></tr>
<tr><td>0</td><td>0</td><td>2</td><td>61</td></tr>
<tr><td>0</td><td>1</td><td>4</td><td>122</td></tr>
<tr><td>1</td><td>0</td><td>8</td><td>244</td></tr>
<tr><td>1</td><td>1</td><td>16</td><td>488</td></tr>
</table></td></tr>
</table>

Table 11. TOF2 Register

WRITE OPCODE 39h	READ OPCODE B9h	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	STOP2	STOP1	STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1
Bit	7	6	5	4	3	2	1	0
Name	T2WV0	TOF_CYC2	TOF_CYC1	TOF_CYC0	X	TIMOUT2	TIMOUT1	TIMOUT0

BIT	NAME	DESCRIPTION			
15:13	STOP[2:0]	**Stop Hits:** These bits set the number of stop hits to be expected and measured.			
		STOP2	**STOP1**	**STOP0**	**DESCRIPTION**
		0	0	0	1 Hit
		0	0	1	2 Hits
		0	1	0	3 Hits
		0	1	1	4 Hits
		1	0	0	5 Hits
		1	0	1	6 Hits
		1	1	0	6 Hits
		1	1	1	6 Hits
12:7	T2WV[5:0]	**Wave Selector for t_2:** These bits determine the wave number for which t_2 is measured. To ensure measurement accuracy, the first wave measurable after the early edge detect is wave 2. Waves are numbered as depicted in Figure 5.			
		T2WV[5:0] (decimal)		**DESCRIPTION**	
		0 through 2		Wave 2	
		3		Wave 3	
		4		Wave 4	
		5 through 63		Wave 5 through 63	

Table 11. TOF2 Register (continued)

<table>
<tr><td rowspan="10">6:4</td><td rowspan="10">TOF_CYC[2:0]</td><td colspan="4">TOF Duty Cycle: These bits determine the time delay between successive executions of TOF measurements. It is the start-to-start time of automatic execution of the TOF_UP and the TOF_DN and is applicable only for the TOF_DIFF command. It is based upon the 32.768kHz crystal. If the actual TOF of the acoustic path exceeds the programmed start-to-start time in this setting, then the TOF duty cycle performs as if the bit setting is 000b.</td></tr>
<tr><td rowspan="2">TOF_CYC[2:0]</td><td colspan="3">DESCRIPTION</td></tr>
<tr><td>32kHz CLOCK CYCLES (decimal)</td><td>TYPICAL TIME</td><td>4MHz ON BETWEEN TOF_ UP and TOF_DOWN</td></tr>
<tr><td>000b</td><td>0</td><td>0μs</td><td>Yes</td></tr>
<tr><td>001b</td><td>4</td><td>122μs</td><td>Yes</td></tr>
<tr><td>010b</td><td>8</td><td>244μs</td><td>Yes</td></tr>
<tr><td>011b</td><td>16</td><td>488μs</td><td>Yes</td></tr>
<tr><td>100b</td><td>24</td><td>732μs</td><td>Yes</td></tr>
<tr><td>101b</td><td>32</td><td>976μs</td><td>Yes</td></tr>
<tr><td>110b</td><td>546</td><td>16.65ms</td><td>No</td></tr>
<tr><td></td><td></td><td>111b</td><td>655</td><td>19.97ms</td><td>No</td></tr>
<tr><td>3</td><td>X</td><td colspan="4">Reserved</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">TIMOUT[2:0]</td><td colspan="4">Timeout: These bits force a timeout in the time-to-digital measurement block. If the hit required to measure t_1, t_2, or Hit1 through Hit6 of the received signal does not occur in this time, the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled). Additionally, any of the Conversion Results registers read FFFFh if the data for that register is invalid.</td></tr>
<tr><td>TIMOUT2</td><td>TIMOUT1</td><td>TIMOUT0</td><td>DESCRIPTION (μs)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>128</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>256</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>512</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1024</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>4096</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>8192</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>16384</td></tr>
</table>

Table 12. TOF3 Register

WRITE OPCODE 3Ah	READ OPCODE BAh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	HIT1WV5	HIT1WV4	HIT1WV3	HIT1WV2	HIT1WV1	HIT1WV0

Bit	7	6	5	4	3	2	1	0
Name	X	X	HIT2WV5	HIT2WV4	HIT2WV3	HIT2WV2	HIT2WV1	HIT2WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT1WV[5:0]	**Hit1 Wave Select:** These bits select the wave number for which the Hit1 stop time is measured. Wave numbers are depicted in Figure 5. The Hit1 wave select value must be at least 1 greater than the wave selected for t_2, which is configured in the TOF2 register. For example, if the wave selector for t_2 is set to wave number 7, then the Hit1 wave select must be set to delect wave number 8 or greater. The earliest wave for which Hit1 can be measured is wave 3.	
		HIT1WV[5:0] (decimal)	**DESCRIPTION**
		0 through 3	Wave 3
		4	Wave 4
		5	Wave 5
		6 through 63	Wave 6 through 63
7:6	X	Reserved	
5:0	HIT2WV[5:0]	**Hit2 Wave Select:** These bits select the wave number for which the Hit2 stop time is measured. Wave numbers are depicted in Figure 5. The Hit2 wave select value must be at least 1 greater than the Hit1 wave select value. For example, if Hit1 wave select value is set to measure wave number 9, then the Hit2 wave select must be set to detect wave number 10 or greater. The earliest wave for which Hit2 can be measured is Wave 4.	
		HIT2WV[5:0] (decimal)	**DESCRIPTION**
		0 through 4	Wave 4
		5	Wave 5
		6	Wave 6
		7 through 63	Wave 7 through 63

Table 13. TOF4 Register

WRITE OPCODE 3Bh	READ OPCODE BBh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	HIT3WV5	HIT3WV4	HIT3WV3	HIT3WV2	HIT3WV1	HIT3WV0

Bit	7	6	5	4	3	2	1	0
Name	X	X	HIT4WV5	HIT4WV4	HIT4WV3	HIT4WV2	HIT4WV1	HIT4WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT3WV[5:0]	**Hit3 Wave Select:** These bits select the wave number for which the Hit3 stop time is measured. Wave numbers are depicted in Figure 5. The Hit3 wave select value must be at least 1 greater than the Hit2 wave select value. For example, if the Hit2 wave select value is set to measure wave number 10, then the Hit3 wave select must be set to detect wave number 11 or greater. The earliest wave for which Hit3 can be measured is wave 5.	
		HIT3WV[5:0] (decimal)	**DESCRIPTION**
		0 through 5	Wave 5
		6	Wave 6
		7	Wave 7
		8 through 63	Wave 8 through 63
7:6	X	Reserved	
5:0	HIT4WV[5:0]	**Hit4 Wave Select:** These bits select the wave number for which the Hit4 stop time is measured. Wave numbers are depicted in Figure 5. The Hit4 wave select value must be at least 1 greater than the Hit3 wave select value. For example, if the Hit3 wave select value is set to measure wave number 11, then the Hit4 wave select must be set to detect wave number 12 or greater. The earliest wave for which Hit4 can be measured is wave 6.	
		HIT4WV[5:0] (decimal)	**DESCRIPTION**
		0 through 6	Wave 6
		7	Wave 7
		8	Wave 8
		9 through 63	Wave 9 through 63

Table 14. TOF5 Register

WRITE OPCODE 3Ch	READ OPCODE BCh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	HIT5WV5	HIT5WV4	HIT5WV3	HIT5WV2	HIT5WV1	HIT5WV0

Bit	7	6	5	4	3	2	1	0
Name	X	X	HIT6WV5	HIT6WV4	HIT6WV3	HIT6WV2	HIT6WV1	HIT6WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT5WV[5:0]	**Hit5 Wave Select**: These bits select the wave number for which the Hit5 stop time is measured. Wave numbers are depicted in Figure 5. The Hit5 wave select value must be at least 1 greater than the Hit4 wave select value. For example, if the Hit4 wave select value is set to measure wave number 12, then the Hit5 wave select must be set to detect wave number 13 or greater. The earliest wave for which Hit5 can be measured is wave 7.	
		HIT5WV[5:0] (decimal)	**DESCRIPTION**
		0 through 7	Wave 7
		8	Wave 8
		9	Wave 9
		10 through 63	Wave 10 through 63
7:6	X	Reserved	
5:0	HIT6WV[5:0]	**Hit6 Wave Select:** These bits select the wave number for which the Hit6 stop time is measured. Wave numbers are depicted in Figure 5. Hit6 wave select value must at least 1 greater than the Hit5 wave select value. For example, if Hit5 wave select value is set to measure wave number 13, then the Hit6 wave select must be set to detect wave number 14 or greater. The earliest wave for which Hit6 can be measured is wave 8.	
		HIT6WV[5:0] (decimal)	**DESCRIPTION**
		0 through 8	Wave 8
		9	Wave 9
		10	Wave 10
		11 through 63	Wave 11 through 63

Table 15. TOF6 Register

WRITE OPCODE 3Dh	READ OPCODE BDh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	C_OFFSET UPR7	C_OFFSET UPR6	C_OFFSET UPR5	C_OFFSET UPR4	C_OFFSET UPR3	C_OFFSET UPR2	C_OFFSET UPR1	C_OFFSET UPR0
Bit	7	6	5	4	3	2	1	0
Name	X	C_OFFSET UP6	C_OFFSET UP5	C_OFFSET UP4	C_OFFSET UP3	C_OFFSET UP2	C_OFFSET UP1	C_OFFSET UP0

BIT	NAME	DESCRIPTION	
15:8	C_OFFSETUPR [7:0]	**Comparator Return Offset Upstream:** When the device is measuring the t_2 wave, the programmed receive comparator offset is returned to a common-mode voltage automatically after the early edge, t_1, is detected. The actual offset return voltage is dependent upon and scales with the voltage present at the V_{CC} pins. The following formula defines the comparator return offset voltage setting, where C_OFFSETUPR is a two's-complement number: $\text{Comparator Return Offset Voltage} = V_{CC} \times \frac{(1152+\text{C\_OFFSETUPR})}{3072}$ where $1\ \text{LSB} = \frac{V_{CC}}{3072}$	
		C_OFFSETUPR[7:0]	**OFFSET (LSBs)**
		7Fh through 01h	127 through 1
		00h	0
		80h through FFh	-128 through -1
7	X	Reserved	

Table 15. TOF6 Register (continued)

BIT	NAME	DESCRIPTION
6:0	C_OFFSETUP [6:0]	**Comparator Offset Upstream:** These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1. The actual common-mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a positive value. When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a negative value. The following formulas define the comparator offset voltage setting $\text{STOP\_POL} = 0 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1152 + C_{OFFSETUP})}{3072}$ $\text{STOP\_POL} = 1 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1151 - C_{OFFSETUP})}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$

C_OFFSETUP[6:0]	OFFSET (LSBs)
00h through 7Fh	0 through 127

Table 16. TOF7 Register

WRITE OPCODE 3Eh	READ OPCODE BEh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	C_OFFSET DNR7	C_OFFSET DNR6	C_OFFSET DNR5	C_OFFSET DNR4	C_OFFSET DNR3	C_OFFSET DNR2	C_OFFSET DNR1	C_OFFSET DNR0
Bit	7	6	5	4	3	2	1	0
Name	X	C_OFFSET DN6	C_OFFSET DN5	C_OFFSET DN4	C_OFFSET DN3	C_OFFSET DN2	C_OFFSET DN1	C_OFFSET DN0

Table 16. TOF7 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="5">15:8</td><td rowspan="5">C_OFFSETDNR [7:0]</td><td colspan="2">Comparator Return Offset Downstream: When the MAX35101 is measuring the t_2 wave, the programmed receive comparator offset is returned to a common-mode voltage automatically after the early edge, t_1, is detected. The actual offset return voltage is dependent upon and scales with the voltage present at the V_{CC} pins. The following formula defines the comparator return offset voltage setting, where C_OFFSETDNR is a two's-complement number:

$$\text{Comparator Return Offset Voltage} = V_{CC} \times \frac{(1152 + \text{C\_OFFSETDNR})}{3072}$$

$$\text{where 1 LSB} = \frac{V_{CC}}{3072}$$</td></tr>
<tr><td>C_OFFSETDNR[7:0]</td><td>OFFSET (LSBs)</td></tr>
<tr><td>7Fh through 01h</td><td>127 through 1</td></tr>
<tr><td>00h</td><td>0</td></tr>
<tr><td>80h through FFh</td><td>-128 through -1</td></tr>
<tr><td>7</td><td>X</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="3">6:0</td><td rowspan="3">C_OFFSETDN [6:0]</td><td colspan="2">Comparator Offset Downstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1. The actual common-mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins.
When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a positive value.
When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the comparator offset is a negative value.
The following formulas define the comparator offset voltage setting:

$$\text{STOP\_POL} = 0 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1152 + C_{OFFSETDN})}{3072}$$

$$\text{STOP\_POL} = 1 \quad \text{Comparator Offset Voltage} = V_{CC} \times \frac{(1151 - C_{OFFSETDN})}{3072}$$

$$\text{where 1 LSB} = \frac{V_{CC}}{3072}$$</td></tr>
<tr><td>C_OFFSETDN[6:0]</td><td>OFFSET (LSBs)</td></tr>
<tr><td>00h through 7Fh</td><td>0 through 127</td></tr>
</table>

Table 17. Event Timing 1 Register

WRITE OPCODE 3Fh	READ OPCODE BFh	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	TDF3	TDF2	TDF1	TDF0	TDM4	TDM3	TDM2	TDM1

Bit	7	6	5	4	3	2	1	0
Name	TDM0	TMF5	TMF4	TMF3	TMF2	TMF1	TMF0	X

BIT	NAME	DESCRIPTION	
15:12	TDF[3:0]	**TOF Difference Measurement Frequency:** These bits define the rate at which TOF_DIFF measurements are executed when the EVTMG1 or EVTMG2 command is executed. Rate = 0.5s + (TDF[3:0] x 0.5s)	
		TDF[3:0] (decimal)	**RATE**
		0	0.5 s
		1	1.0s
		….	….
		14	7.5 s
		15	8.0 s
11:7	TDM[4:0]	**TOF Difference Measurements:** These bits define the number of TOF_DIFF measurement cycles to be executed when the EVTMG1 or EVTMG2 command is executed. Cycles = 1+ TDM[4:0]	
		TDM[4:0] (decimal)	**CYCLES**
		0	1
		1	2
		….	….
		30	31
		31	32
6:1	TMF[5:0]	**Temperature Measurement Frequency:** These bits define the time delay between temperature cycle measurements. It is a start-cycle to start-cycle time duration at which temperature measurement cycles are executed when the EVTMG1 or EVTMG3 command is executed. Rate = 1.0s + (TMF[3:0] x 1.0s)	
		TMF[5:0] (decimal)	**RATE**
		0	1 s
		1	2 s
		….	….
		62	63 s
		63	64 s
0	X	Reserved	

Table 18. Event Timing 2 Register

WRITE OPCODE 40h	READ OPCODE C0h	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	TMM4	TMM3	TMM2	TMM1	TMM0	CAL_USE	CAL_CFG2	CAL_CFG1
Bit	7	6	5	4	3	2	1	0
Name	CAL_CFG0	TP1	TP0	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC0

BIT	NAME	DESCRIPTION
15:11	TMM[4:0]	**Temperature Measurements:** These bits define the number of temperature measurement cycles to be executed when the EVTMG1 or EVTMG3 command is executed. Cycles = 1+ TMM[4:0]
10	CAL_USE	**Calibration Usage:** This bit, when set, causes the MAX35101 to use the calibration data in the CalibrationInt and CalibrationFrac registers during measurement, averaging and accumulation of data while executing the EVTMG commands. All time measurements are scaled using the calibration factors as described by the calibrate command.
9:7	CAL_CFG[2:0]	**Calibration Configuration:** These bits define the point in the EVTMGx cycle/sequence where the automatic calibration command is executed.

TMM[4:0] (bits 15:11):

TMM[4:0] (decimal)	CYCLES
0	1
1	2
….	….
30	31
31	32

CAL_CFG[2:0] (bits 9:7):

CAL_CFG[2:0]	DESCRIPTION DURING EVTMGX SEQUENCES, AUTOMATIC EXECUTION OF THE CALIBRATE COMMAND OCCURS AT:
000b through 011b	Autocalibration disabled
100b	The beginning of each TOF_DIFF cycle The beginning of each temperature cycle
101b	The beginning of each TOF_DIFF cycle The beginning of each temperature sequence
110b	The beginning of each TOF_DIFF sequence The beginning of each temperature cycle
111b	The beginning of each TOF_DIFF sequence The beginning of each temperature sequence

Table 18. Event Timing 2 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>6:5</td><td>TP[1:0]</td><td>Temperature Port: These bits set the number of temperature ports to stimulate during a temperature measurement sequence and the sequence in which the temperature ports are stimulated.
<table>
<tr><th>TP1</th><th>TP0</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>Measure ports T1 and T3</td></tr>
<tr><td>0</td><td>1</td><td>Measure ports T2 and T4</td></tr>
<tr><td>1</td><td>0</td><td>Measure ports T1, T3, and T2</td></tr>
<tr><td>1</td><td>1</td><td>Measure ports T1, T3, T2, and T4</td></tr>
</table></td></tr>
<tr><td>4:2</td><td>PRECYC[2:0]</td><td>Preamble Temperature Cycle: These 3 bits are used to set the number of cycles to use as preamble for reducing dielectric absorption of the temperature measurement capacitor. Each cycle comprises one temperature measurement sequence as defined by the TP[1:0] bits.
<table>
<tr><th>PRECYC2</th><th>PRECYC1</th><th>PRECYC0</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0 dummy cycle</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1 dummy cycles</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 dummy cycles</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3 dummy cycles</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4 dummy cycles</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5 dummy cycles</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6 dummy cycles</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7 dummy cycles</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>PORTCYC[1:0]</td><td>Port Cycle Time: These two bits define the time interval between successive individual temperature port measurements. It is a start-to-start time. These bits also define the timeout function of the temperature measurement ports. See the Temperature Operation section for timeout details.
<table>
<tr><th>PORTCYC1</th><th>PORTCYC0</th><th>DESCRIPTION (µs)</th></tr>
<tr><td>0</td><td>0</td><td>128</td></tr>
<tr><td>0</td><td>1</td><td>256</td></tr>
<tr><td>1</td><td>0</td><td>384</td></tr>
<tr><td>1</td><td>1</td><td>512</td></tr>
</table></td></tr>
</table>

Table 19. TOF Measurement Delay Register

WRITE OPCODE 41h	READ OPCODE C1h	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	DLY15	DLY14	DLY13	DLY12	DLY11	DLY10	DLY9	DLY8

Bit	7	6	5	4	3	2	1	0
Name	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0

BIT	NAME	DESCRIPTION
15:0	DLY[15:0]	This is hexadecimal value ranging from 0000h to FFFFh (decimal 0 to 65535). It is a multiple of the 4MHz crystal period (250ns). Settings less than 0012h are reserved and should not be used. The analog comparator driven by the STOP_UP and STOP_DN device pins does not generate a stop condition until this delay, counted from the internally generated start pulse for the acoustic wave, has expired. This delay applies to early edge detect wave. Care must be taken to set the TIMOUT bits in the TOF2 register so that a timeout interrupt does not occur before this delay expires.

Table 20. Calibration and Control Register

WRITE OPCODE 42h	READ OPCODE C2h	FLASH STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	CMP_EN	CMP_SEL	INT_EN	ET_CONT

Bit	7	6	5	4	3	2	1	0
Name	CONT_INT	CLK_S2	CLK_S1	CLK_S0	CAL_ PERIOD3	CAL_ PERIOD2	CAL_ PERIOD1	CAL_ PERIOD0

BIT	NAME	DESCRIPTION
15:12	X	Reserved
11	CMP_EN	**Comparator/UP_DN Output Enable:** 1 = CMP_OUT/UP_DN output device pin is enabled. 0 = CMP_OUT/UP_DN output device pin is driven low.

Table 20. Calibration and Control Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>10</td><td>CMP_SEL</td><td>Comparator/UP_DN Output Select: This bit selects the output function of the CMP_OUT/UP_DN pin and is only used when CMP_EN = 1.
1 = CMP_EN: The output monitors the receiver front end comparator output.
0 = UP_DN: The output monitors the launch direction of the pulse launcher.
High Output: Upstream measurement (Launch_UP to STOP_UP)
Low Output: Downstream measurement (Launch_DN to STOP_DN)</td></tr>
<tr><td>9</td><td>INT_EN</td><td>Interrupt Enable: This bit, when set, enables the $\overline{INT}$ pin. All interrupt sources are wire-ORed to the $\overline{INT}$ pin.</td></tr>
<tr><td>8</td><td>ET_CONT</td><td>Event Timing Continuous Operation: This bit, when set, causes the currently executing EVTMGx command to continuously execute until the HALT command is received by the MAX35101.
This bit, when cleared, causes:
• The currently executing EVTMG1 command to run one sequence of TOF_DIFF measurement cycles and/or one sequence of temperature measurement.
• The currently executing EVTMG2 command to run one sequence of TOF_DIFF measurements cycles.
• The currently executing EVTMG3 command to run one sequence of temperature measurement cycles.</td></tr>
<tr><td>7</td><td>CONT_INT</td><td>Continuous Interrupt: This bit, when set, causes the currently executing EVTMGx command to assert the $\overline{INT}$ pin (if enabled) after every TOF_DIFF or temperature measurement cycle. This allows the host microprocessor to interrogate the current event for accuracy of measurements and hit data.
When this bit is cleared, the currently executing EVTMGx command interrupt generation behavior is controlled only by the setting of the ET_CONT bit.</td></tr>
<tr><td>6:4</td><td>CLK_S[2:0]</td><td>Clock Settling Time: These bits define the time interval that the MAX35101 waits after enabling the 4MHz clock for it to stabilize before making any measurements of time or temperature.
<table>
<tr><th rowspan="2">CLK_S2</th><th rowspan="2">CLK_S1</th><th rowspan="2">CLK_S0</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES</th><th>TYPICAL TIME</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16</td><td>488µs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>48</td><td>1.46ms</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96</td><td>2.93ms</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128</td><td>3.9ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>168</td><td>5.13ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="2">4MHz oscillator on continuously</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td colspan="2">4MHz oscillator on continuously</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">4MHz oscillator on continuously</td></tr>
</table></td></tr>
</table>

Table 20. Calibration and Control Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="8">3:0</td><td rowspan="8">CAL_PERIOD[3:0]</td><td colspan="3">4MHz Ceramic Oscillator Calibration Period: These bits define the number of 32.768kHz oscillator periods to measure for determination of the 4MHz ceramic oscillator period.
32kHz clock cycles = 1+ CAL_PERIOD[3:0]</td></tr>
<tr><td rowspan="2">CAL_PERIOD[3:0] (decimal)</td><td colspan="2">DESCRIPTION</td></tr>
<tr><td>32kHz CLOCK CYCLES (decimal)</td><td>32kHz CLOCK CYCLES (µs)</td></tr>
<tr><td>0</td><td>1</td><td>30.5</td></tr>
<tr><td>1</td><td>2</td><td>61</td></tr>
<tr><td>….</td><td>….</td><td>….</td></tr>
<tr><td>14</td><td>15</td><td>457.7</td></tr>
<tr><td>15</td><td>16</td><td>488.0</td></tr>
</table>

Table 21. Real-Time Clock Register

WRITE OPCODE 43h	READ OPCODE C3h	FLASH-STORED Yes	FACTORY-STORED FLASH VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Name	X	32K_BP	32K_EN	EOSC	AM1	AM0	WF	WD_EN

BIT	NAME	DESCRIPTION
15:7	X	Reserved
6	32K_BP	**32kHz Bypass:** This bit, when set, allows an external CMOS-level 32.768kHz signal to be applied to the 32KX1 device pin. The internal 32.768kHz oscillator is bypassed and the external signal is driven into the MAX35101 core.
5	32K_EN	**32kHz Clock Output Enable:** This bit enables the 32KOUT device pin to drive a CMOS-level square wave representation of the 32kHz crystal.
4	EOSC	**Enable Oscillator:** This active-low bit when set to logic 0 starts the real-time clock oscillator. When this bit is set to logic 1, the oscillator is stopped.

Table 21. Real-Time Clock Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">AM[1:0]</td><td colspan="3">Alarm Control: The MAX35101 contains a time-of-day alarm. The alarm is activated when either the AM1 or AM2 bits are set. When the RTC’s hours or minutes value increments to a value equal to the alarm settings in Alarm registers, the AF bit in the Interrupt Status register is set and the $\overline{INT}$ device pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a read register command.</td></tr>
<tr><td>AM1</td><td>AM0</td><td>ALARM FUNCTION</td></tr>
<tr><td>0</td><td>0</td><td>No alarm</td></tr>
<tr><td>0</td><td>1</td><td>Alarm when minutes match</td></tr>
<tr><td>1</td><td>0</td><td>Alarm when hours match</td></tr>
<tr><td>1</td><td>1</td><td>Alarm when hours and minutes match</td></tr>
<tr><td>1</td><td>WF</td><td colspan="3">Watchdog Flag: This bit is set when the watchdog counter reaches zero. This bit must be written to a zero to clear the bit. Writing this bit to a zero when the $\overline{WDO}$ pin is asserted low releases the $\overline{WDO}$ pin to its inactive high-impedance state.</td></tr>
<tr><td>0</td><td>WD_EN</td><td colspan="3">Watchdog Enable:
1 = Watchdog timer is enabled.
0 = Watchdog time is disabled, and the $\overline{WDO}$ pin is high impedance.</td></tr>
</table>

Status Register Descriptions

Table 22. Interrupt Status Register

WRITE OPCODE Read Only	READ OPCODE FEh	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	TO	AF	X	TOF	TE	LDO	TOF_ EVTMG	TEMP_ EVTMG
Bit	7	6	5	4	3	2	1	0
Name	FLASH	CAL	HALT	CSWI	INIT	POR	X	X

Note: This register is read only and bits are self-clearing upon a read to this register. See the *Device Interrupt Operations* section for more information.

BIT	NAME	DESCRIPTION
15	TO	**Timeout:** The TO bit is set if any one of the t_1, t_2, Hit1 through Hit6, or temperature measurements do not occur within the associated timeout window.
14	AF	**Alarm Flag:** Set when the RTC’s hours or minutes value increments to a value equal to the alarm settings in Alarm registers.
13	X	Reserved

Table 22. Interrupt Status Register (continued)

BIT	NAME	DESCRIPTION
12	TOF	**Time of Flight:** Set when the TOF_UP, TOF_DN, or TOF_DIFF command has completed. During execution of The EVTMG1 or EVTMG2 command, this bit is set and the $\overline{\text{INT}}$ pin asserts (if enabled) upon completion of each of the cycles of the event defined by the TOF difference measurements setting if the CONT_INT bit in the Calibration and Control register has been set.
11	TE	**Temperature:** Set when the temperature command has completed. During execution of The EVTMG1 or EVTMG3 command, this bit is set and the $\overline{\text{INT}}$ pin asserts (if enabled) upon completion of each of the cycles of the event defined by the temperature measurements setting if the CONT_INT bit in the Calibration and Control register has been set.
10	LDO	**Internal LDO Stabilized:** Set when the internal low-dropout regulator is turned on by either the LDO_Timed or LDO_ON and has stabilized. Once asserted, a flash command can be sent to the MAX35101.
9	TOF_EVTMG	**Event Timing TOF Completed:** Set when either the EVTMG1 or EVTMG2 commands have completed its last TOF_DIFF measurement cycle. This indicates that the data in the TOF_DIFF, TOF_DIFF_AVG, AVGUP, and AVGDN Results registers is valid.
8	TEMP_EVTMG	**Event Timing Temperature Completed:** Set when the EVTMG1 or EVTMG3 commands have completed its last temperature measurements. This indicates that the data in the T1, T2, T3, T4, T1_AVG, T2AVG, T3AVG, and T4_AVG Results registers is valid.
7	FLASH	**Flash Ready:** Set when the flash memory is ready to be accessed. During execution of **any** command that requires write access to the flash memory (write flash, transfer configuration to flash, block erase, initialize), the SPI port is inactive and should not be exercised. The host microprocessor is interrupted by the assertion of the $\overline{\text{INT}}$ pin (if enabled) once the command has been completed and the SPI of the MAX35101 is available for access.
6	CAL	**Calibrate:** Set after completion of the Calibrate command when the command is manually sent by the host microprocessor. When calibration occurs as a result of the setting of the Cal_Use, Cal_AUTO and Cal_CFGx bits in the Event Timing 2 register and the MAX35101 is automatically executing calibration commands as required during execution of any of the EVTMGx commands, this bit is not set.
5	HALT	**HALT:** Set when the HALT command has completed.
4	CSWI	**Case Switch:** Set when a high logic level is detected on the CSW device pin.
3	INIT	**Initialize:** Set when the Initialize command has completed.
2	POR	**Power-On-Reset:** Set when the MAX35101 has been successfully powered by application of V_{CC}. Upon application of power, the SPI port becomes inactive until this bit has been set.
1:0	X	Reserved

Table 23. Control Register

WRITE OPCODE FFh	READ OPCODE 7Fh	FLASH STORED No	DEFAULT VALUE 0000h

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	AFA	CSWA

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
15:10	X	Reserved
9	AFA	**Alarm Flag Arm:** This bit is set when the RTC's hours and/or minutes value matched the alarm settings in the RTC register. This bit is set at the same time as the AF bit in the Interrupt Status register. After resetting the RTC alarm settings, a 0 must be written to this bit to rearm the RTC Alarm. This bit can only be written to a 0.
8	CSWA	**Case Switch Arm:** This bit is set when the CSW pin detects a logic-high, indicating the MAX35101 has detected a tamper condition. This bit is set at the same time as the CSWI bit in the Interrupt Status register. Once set, this bit must be written to a 0 to rearm the case switch detection. The case switch detection must be rearmed before the CSWI interrupt can be set again. This bit can only be written to a 0.
7:0	X	Reserved

Conversion Results Register Descriptions

The devices conversion results registers are all read-only volatile SRAM. Values are not stored in the flash memory and the POR value for all registers is 0000h.

Table 24. Conversion Results Registers Description

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="7">C4h</td><td rowspan="7">WVRUP</td><td colspan="8">Bit 15 through Bit 8 holds the 8-bit value of the pulse width ratio ($t_1 \div t_2$).for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 15</td><td>BIT 14</td><td>BIT 13</td><td>BIT 12</td><td>BIT 11</td><td>BIT 10</td><td>BIT 9</td><td>BIT 8</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 thru bit 0 holds the 8-bit value of the pulse width ratio ($t_2 \div t_{ideal}$) where t_{ideal} is equal to half the period of the Pulse Launch Frequency for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 7</td><td>BIT 6</td><td>BIT 5</td><td>BIT 4</td><td>BIT 3</td><td>BIT 2</td><td>BIT 1</td><td>BIT 0</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr><td>C5h</td><td>Hit1UPInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>C6h</td><td>Hit1UPFrac</td><td colspan="8">16-bit fractional value of the first hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>C7h</td><td>Hit2UPInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>C8h</td><td>Hit2UPFrac</td><td colspan="8">16-bit fractional value of the second hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>C9h</td><td>Hit3UPInt</td><td colspan="8">15-bit fixed-point integer value of the third hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>CAh</td><td>Hit3UPFrac</td><td colspan="8">16-bit fractional value of the third hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>CBh</td><td>Hit4UPInt</td><td colspan="8">15-bit fixed-point integer value of the fourth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>CCh</td><td>Hit4UPFrac</td><td colspan="8">16-bit fractional value of the fourth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
</table>

Table 24. Conversion Results Registers Description (continued)

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td>CDh</td><td>Hit5UPInt</td><td colspan="8">15-bit fixed-point integer value of the fifth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHz}.</td></tr>
<tr><td>CEh</td><td>Hit5UPFrac</td><td colspan="8">16-bit fractional value of the fifth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz}.</td></tr>
<tr><td>CFh</td><td>Hit6UPInt</td><td colspan="8">15-bit fixed-point integer value of the sixth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHz}.</td></tr>
<tr><td>D0Fh</td><td>Hit6UPFrac</td><td colspan="8">16-bit fractional value of the sixth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz}.</td></tr>
<tr><td>D1h</td><td>AVGUPInt</td><td colspan="8">15-bit fixed-point integer value of the average of the hits recorded in the upstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHz}.</td></tr>
<tr><td>D2h</td><td>AVGUPFrac</td><td colspan="8">16-bit fractional value of the average of the hits recorded in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz}.</td></tr>
<tr><td rowspan="8">D3h</td><td rowspan="8">WVRDN</td><td colspan="8">Bit 15 through Bit 8 holds the 8 bit value of the pulse width ratio (t_1/t_2).for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 15</td><td>BIT 14</td><td>BIT 13</td><td>BIT 12</td><td>BIT 11</td><td>BIT 10</td><td>BIT 9</td><td>BIT 8</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 thru bit 0 holds the 8 bit value of the pulse width ratio (t_2/t_{ideal}) where t_{ideal} is equal to half the period of the pulse launch frequency for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>BIT 7</td><td>BIT 6</td><td>BIT 5</td><td>BIT 4</td><td>BIT 3</td><td>BIT 2</td><td>BIT 1</td><td>BIT 0</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr></tr>
<tr><td>D4h</td><td>Hit1DNInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHz}.</td></tr>
<tr><td>D5h</td><td>Hit1DNFrac</td><td colspan="8">16-bit fractional value of the first hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz}.</td></tr>
<tr><td>D6h</td><td>Hit2DNInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHz}.</td></tr>
</table>

Table 24. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
D7h	Hit2DNFrac	16-bit fractional value of the second hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
D8h	Hit3DNInt	15-bit fixed-point integer value of the third hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
D9h	Hit3DNFrac	16-bit fractional value of the third hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
DAh	Hit4DNInt	15-bit fixed-point integer value of the fourth hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
DBh	Hit4DNFrac	16-bit fractional value of the fourth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
DCh	Hit5DNInt	15-bit fixed-point integer value of the fifth hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
DDh	Hit5DNFrac	16-bit fractional value of the fifth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
DEh	Hit6DNInt	15-bit fixed-point integer value of the sixth hit in the downstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
DFh	Hit6DNFrac	16-bit fractional value of the sixth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E0h	AVGDNInt	15-bit fixed-point integer value of the average of the hit times recorded in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} – 1) \times t_{4MHz}$.
E1h	AVGDNFrac	16-bit fractional value of the average of the hit times recorded in the downstream direction. This fractional portion is a binary representation of one period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} – 1)/2^{16} \times t_{4MHz}$.

Table 24. Conversion Results Registers Description (continued)

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>E2h</td><td>TOF_DIFFInt</td><td>16-bit fixed-point two’s-complement integer portion of the difference of the averages for the hits recorded in both the upstream and downstream directions. It is computed as:
AVGUP – AVGDN
This integer represents the number of t_{4MHz} periods that contribute to computation. The maximum size of the integer is 7FFFh or $(2^{15} – 1) \times t_{4MHz}$. The minimum size of this integer is 8000h or $-2^{15} \times t_{4MHz}$.</td></tr>
<tr><td>E3h</td><td>TOF_ DIFFFrac</td><td>16-bit fractional portion of the two’s complement difference of the averages for the hits recorded in both the upstream and downstream directions. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>E4h</td><td>TOF_Cycle_ Count /TOF_Range</td><td>Bit 15 through bit 8 holds the 8-bit value of the TOF_Range. The TOF_Range is an 8-bit binary integer that indicates the range of valid error-free TOF_DIFF measurements that were made during execution of either of the EVTMG1 or EVTMG2 commands. The maximum value of TOF_Range is equal to 2 times the actual pulse launch period as configured by the pulse launch divider bits in the TOF1 register.
<table>
<tr><th>BIT 15</th><th>BIT 14</th><th>BIT 13</th><th>BIT 12</th><th>BIT 11</th><th>BIT 10</th><th>BIT 9</th><th>BIT 8</th></tr>
<tr><td>MSB</td><td colspan="6">TOF_Range 8-bit binary integer</td><td>LSB</td></tr>
</table>
The formulas to calculate the range and resolution of the TOF_Range integer for a given DPL[3:0] bit setting are shown below:
Maximum range (µs) = DPL[3:0] + 1 Resolution = Maximum range/256
<table>
<tr><th>DPL[3:0]</th><th>LAUNCH FREQUENCY</th><th>MAXIMUM RANGE (µs)</th><th>RESOLUTION (ns)</th></tr>
<tr><td>0001b</td><td>1MHz</td><td>2</td><td>7.8175</td></tr>
<tr><td>0002b</td><td>666.6kHz</td><td>3</td><td>11.7185</td></tr>
<tr><td>….</td><td>….</td><td>….</td><td>….</td></tr>
<tr><td>1110b</td><td>133.3kHz</td><td>15</td><td>58.59375</td></tr>
<tr><td>1111b</td><td>125kHz</td><td>16</td><td>62.5</td></tr>
</table>
Bit 7 through bit 0 holds the 8-bit value of the TOF cycle count. The TOF cycle count is an 8-bit binary integer that indicates the number of valid error-free cycles that either of the EVTMG1 or EVTMG2 commands has executed. It also represents the number of TOF_DIFF cycles that have been totaled for the purpose of averaging, which affects the results provided in the TOF_DIFF_ AVGFrac and TOF_DIFF_AVGInt registers. It is incremented every time an error-free TOF_DIFF command is executed by either the EVTMG1 or EVTMG2 sequence. Because of this internal error checking, once the complete number of cycles defined by the TOF difference masurements bits in the Event Timing 1 register has been completed and the TOF_EVTMG bit has been set in the Interrupt Status register causing the $\overline{INT}$ device pin to be asserted (if enabled), the TOF Cycle Count may not be equal to the setting of the TOF difference measurements bits in the Event Timing 1 register.
<table>
<tr><th>BIT 7</th><th>BIT 6</th><th>BIT 5</th><th>BIT 4</th><th>BIT 3</th><th>BIT 2</th><th>BIT 1</th><th>BIT 0</th></tr>
<tr><td>MSB</td><td colspan="6">TOF cycle count 8-bit binary integer</td><td>LSB</td></tr>
</table>
</td></tr>
</table>

Table 24. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
E5h	TOF_DIFF_ AVGInt	16-bit fixed-point two's-complement integer portion of the average of the accumulated TOF_DIFF measurements. It is computed as: $$\frac{\sum_{n=1}^{TOF\_Cycle\_Count} TOF\_DIFF_n}{TOF\_Cycle\_Count}$$ This integer represents the number of t_{4MHz} periods that contribute to the computation. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$. The minimum size of this integer is 8000h or $-2^{15} \times t_{4MHz}$.
E6h	TOF_DIFF_ AVGFrac	16-bit fractional portion of the two's-complement average of the accumulated TOF_DIFF measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E7h	T1Int	15-bit fixed-point integer value of the time taken to discharge the timing capacitor through the RTD connected to the T1 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
E8h	T1Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T1 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E9h	T2Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This integer portion is a binary representation of the number of periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
EAh	T2Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
EBh	T3Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
ECh	T3Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
EDh	T4Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.

Table 24. Conversion Results Registers Description (continued)

<table>
<tr><th>READ ONLY ADDRESS</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td>EEh</td><td>T4Frac</td><td colspan="8">16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td rowspan="6">EFh</td><td rowspan="6">Temp_Cycle_Count</td><td colspan="8">The temp cycle count is an 8-bit binary integer that indicates the number of valid error-free cycles that either of the EVTMG1 or EVTMG3 commands has executed. It also represents the number of temperature cycles that have been totaled for the purpose of averaging, which affects the results provided in the Tx_AVGFrac and Tx_AVGInt registers. It is incremented every time an error-free temperature command is executed by either the EVTMG1 or EVTMG3 sequence. Because of this internal error checking, once the complete number of cycles defined by the temperature measurements bits in the Event Timing 2 register has been completed and the Temp_EVTMG bit has been set in the Interrupt Status register causing the $\overline{INT}$ device pin to be asserted (if enabled), the temperature cycle count may not be equal to the setting of the temperature measurements bits in the Event Timing 2 register.</td></tr>
<tr><td>BIT 15</td><td>BIT 14</td><td>BIT 13</td><td>BIT 12</td><td>BIT 11</td><td>BIT 10</td><td>BIT 9</td><td>BIT 8</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>BIT 7</td><td>BIT 6</td><td>BIT 5</td><td>BIT 4</td><td>BIT 3</td><td>BIT 2</td><td>BIT 1</td><td>BIT 0</td></tr>
<tr><td>MSB</td><td colspan="6">Temp Cycle Count</td><td>LSB</td></tr>
<tr><td>F0h</td><td>T1_AVGInt</td><td colspan="8">15-bit fixed-point integer value of the average of the T1 port measurements. It is computed as:
$$\frac{\sum_{n=1}^{Temp\_Cycle\_Count} T1_n}{Temp\_Cycle\_Count}$$
This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
<tr><td>F1h</td><td>T1_AVGFrac</td><td colspan="8">16-bit fractional portion of the average of the T1 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.</td></tr>
<tr><td>F2h</td><td>T2_AVGInt</td><td colspan="8">15-bit fixed-point integer value of the average of the T2 port measurements. It is computed as:
$$\frac{\sum_{n=1}^{Temp\_Cycle\_Count} T2_n}{Temp\_Cycle\_Count}$$
This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.</td></tr>
</table>

Table 24. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
F3h	T2_AVGFrac	16-bit fractional portion of the average of the T2 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
F4h	T3_AVGInt	15-bit fixed-point integer value of the average of the T3 port measurements. It is computed as: $\frac{\sum_{n=1}^{Temp\_Cycle\_Count} T3_n}{Temp\_Cycle\_Count}$ This integer portion is a binary representation of the number of periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
F5h	T3_AVGFrac	16-bit fractional portion of the average of the T3 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
F6h	T4_AVGInt	15-bit fixed-point integer value of the average of the T4 port measurements. It is computed as: $\frac{\sum_{n=1}^{Temp\_Cycle\_Count} T4_n}{Temp\_Cycle\_Count}$ This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
F7h	T4_AVGFrac	16-bit fractional portion of the average of the T4 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
F8h	Calibration Int	15-bit fixed-point integer value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
F9h	Calibration Frac	16-bit fractional value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
FAh		Reserved
FBh		Reserved
FCh		Reserved
FDh		Reserved

Flash Opcode Commands

To access the flash memory, the internal low-dropout voltage regulator that powers the flash circuitry must be enabled. This can be done two ways: sending the LDO_Timed command prior to the desired flash access or sending the LDO_ON command to the MAX35101 prior to desired flash access. See the LDO_Timed and LDO_ON command descriptions for details. To manipulate the flash memory, there are three commands supported by the device: read flash, write flash, and block erase flash.

Read Flash Command

The read flash command is used to sequentially read a continuous stream of data from the internal 8KB of flash using a built-in autoincrement address counter. For 8KB, 13 address bits are needed to indicate the starting address in memory to begin the read stream. Since the memory array is organized in X16 fashion, the starting address must fall on any even number address. The read stream continues until the $\overline{CE}$ signal is deasserted. Once the automatic internal address counter has been incremented to the last memory location in the array, it wraps around to the bottom of the memory array and the data for the first memory location of the array is read. Figure 18 illustrates the serial peripheral interface signaling associated with the read flash command.

Write Flash Command

The flash is written in the MAX35101 in a word-only manner. The architecture allows a single 16-bit word to be written to the array supporting the maximum access SPI clock speed of t_{SCK}. The location to be programmed must have previously been erased with the block erase flash command.

To perform a write flash command, the starting flash memory address must fall on an even flash memory address (i.e., the least significant bit of the address (A15–A0) must be 0). The 16-bit address word and at least one 16-bit word of data must be clocked into the device before the $\overline{CE}$ pin is deasserted. If more than 16 bits of data are clocked into the device during a single $\overline{CE}$ assertion, only the last bounded 16-bit data word is written. This is not a FIFO register. Any fraction of a 16-bit word is ignored, and the previous whole 16-bit word is written.

Once the 16 bits of data are clocked into the device, the host microprocessor deasserts the $\overline{CE}$ device pin and then waits. The MAX35101 sets the flash bit in the Interrupt Status register and assert the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the next write flash command can be sent to the MAX35101. The host microprocessor can then read the Interrupt Status register after the INT device pin is asserted. Figure 19 illustrates the serial peripheral interface signaling associated with the write flash command.

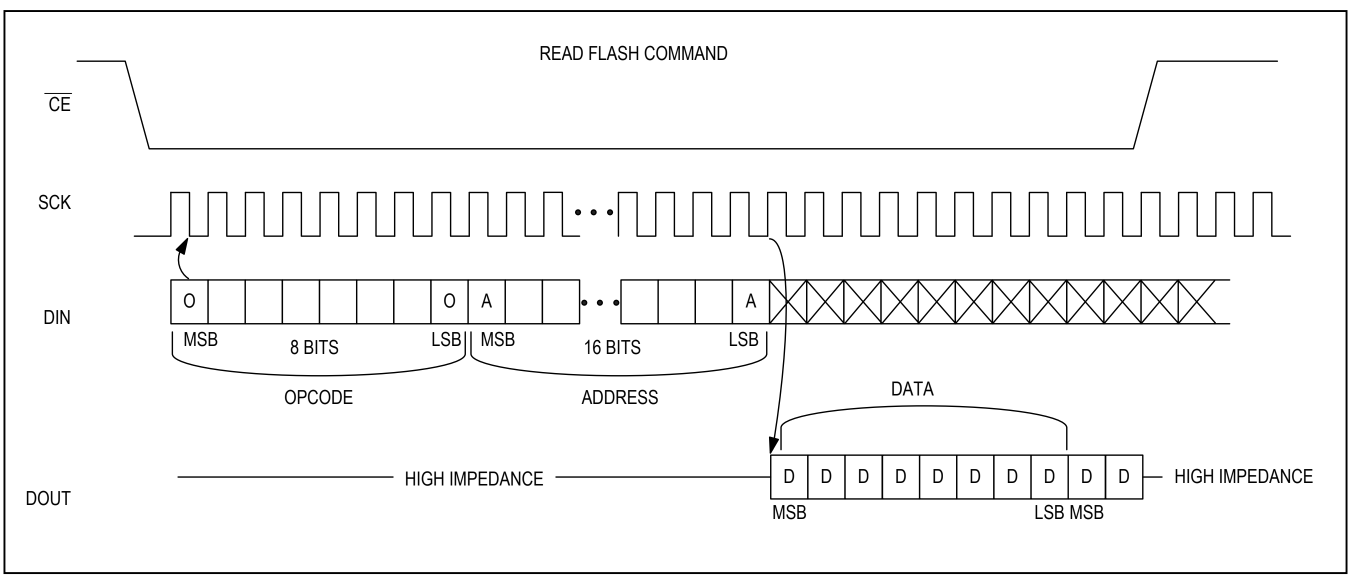


Figure 18. Read Flash Opcode Command Protocol

Block Erase Flash Command

A block of 128 words (256 bytes) can be erased in a single operation. For the 8KB array, there are 32 such 128 word (256 Byte) blocks. The block to be erased is selected by the 16-bit address word in the block erase flash SPI protocol sequence as illustrated in Figure 20.

The erased block is the block that contains the specified address. The time from $\overline{CE}$ deassert to $\overline{CE}$ assert for the next block erase flash command needs to be approximately t_{ERASE}. Also, the device sets the flash bit in the Interrupt Status register and asserts the $\overline{INT}$ device pin (if enabled) to tell the host microprocessor that the next block erase flash command can be sent. The host microprocessor can read the Interrupt Status register after the INT device pin is asserted instead of waiting for t_{ERASE}.

Flash Memory Map

This memory is accessed by the read flash, write flash, and the block erase flash commands. All flash memory is erased when the MAX35101 leaves the factory. This means that each flash location has a value of FFFFh until written by a user to a different value.

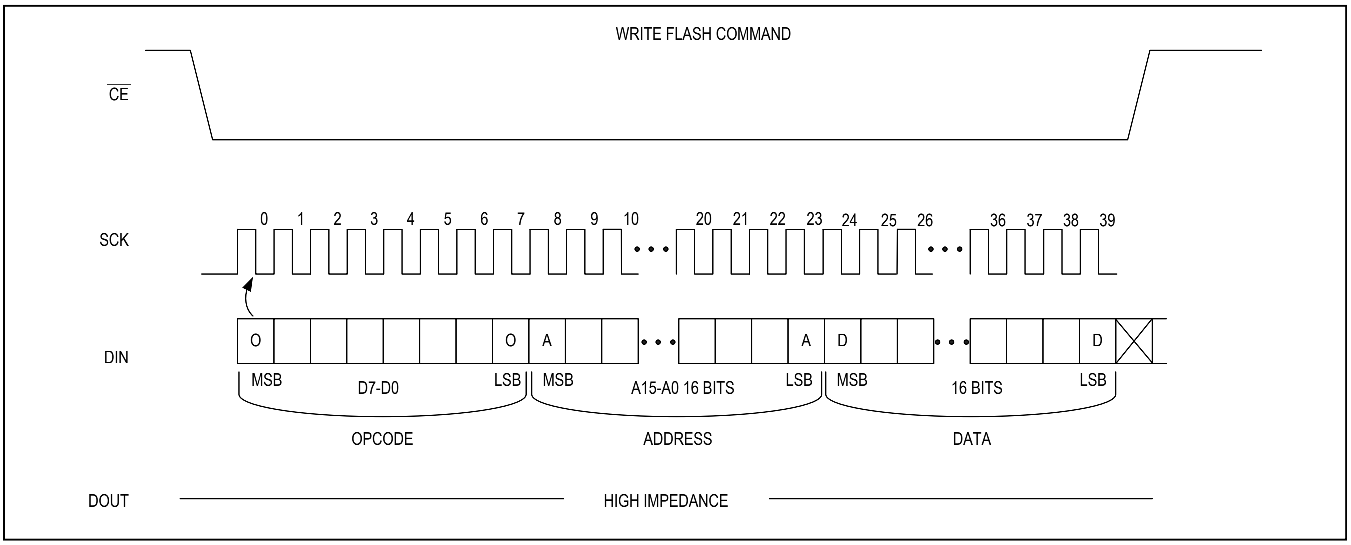


Figure 19. Write Flash Opcode Command Protocol

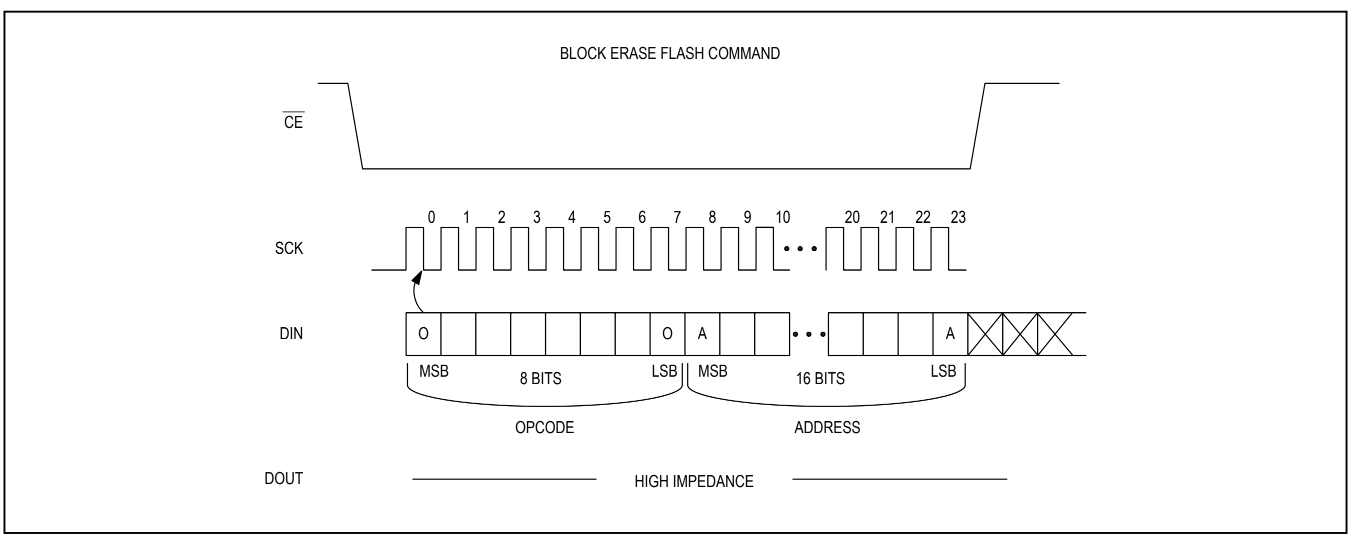
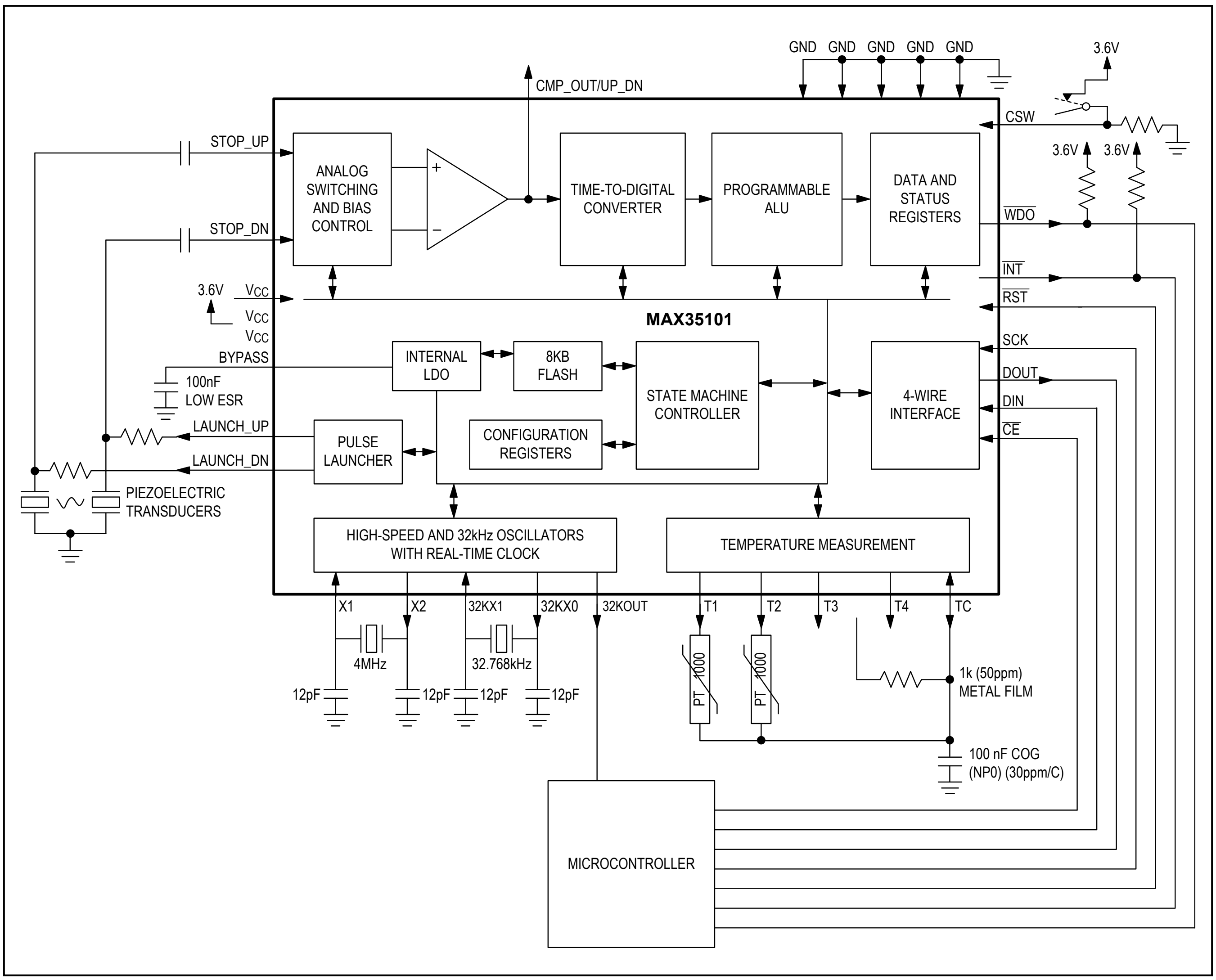


Figure 20. Block Erase Flash Opcode Command Protocol

Table 25. Flash Memory Map

FLASH ADDRESS (evens only)	BLOCK (decimal)	DESCRIPTION
0000h to 00FFh	0	User flash
0100h to 01FFh	1	User flash
0200h to 02FFh	2	User flash
….	….	User flash
1D00h to 1DFFh	29	User flash
1E00h to 1EFFh	30	User flash
1F00h to 1FFFh	31	User flash

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX35101EHJ+	-40°C to +85°C	32 TQFP-EP*
MAX35101EHJ+T	-40°C to +85°C	32 TQFP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFP-EP	H32E+6	21-0079	90-0326

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/14	Initial release	—
1	1/15	Updated *Benefits and Features* section and Figure 12	1, 19

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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