5 V, 3 A Current-Mode Constant On-Time Synchronous Buck Regulator

DESCRIPTION

The SiP12107 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 3 A continuous current at 4 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 2.8 V to 5.5 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiP12107's CM-COT architecture delivers ultra-fast transient response with minimum output capacitance and tight ripple regulation at very light load. No ESR or external ESR network is required for loop stability purpose. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output overvoltage protection (OVP), output under voltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and internal soft-start ramp.

The SiP12107 is available in lead (Pb)-free power enhanced MLP-16L package in 3 mm x 3 mm dimension.

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- 2.8 V to 5.5 V input voltage
- Adjustable output voltage down to 0.6 V
- 3 A continuous output current
- Programmable switching frequency up to 4 MHz
- 95 % peak efficiency
- Supports all ceramic capacitors No external ESR required
- Ultrafast transient response
- Selectable power saving mode or force current mode
- ± 1 % accuracy
- Pulse-by-pulse current limit
- Scalable with SiP12108 - 5A
- Fully protected with OTP, SCP, UVP, OVP
- P_{Good} Indicator
- Compliant to RoHS Directive 2011/65/EU

APPLICATIONS

- Notebook computers
- Desktop PCs and servers
- Handheld devices
- POLs for telecom
- Consumer electronics
- Industrial and automation

TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTIONS

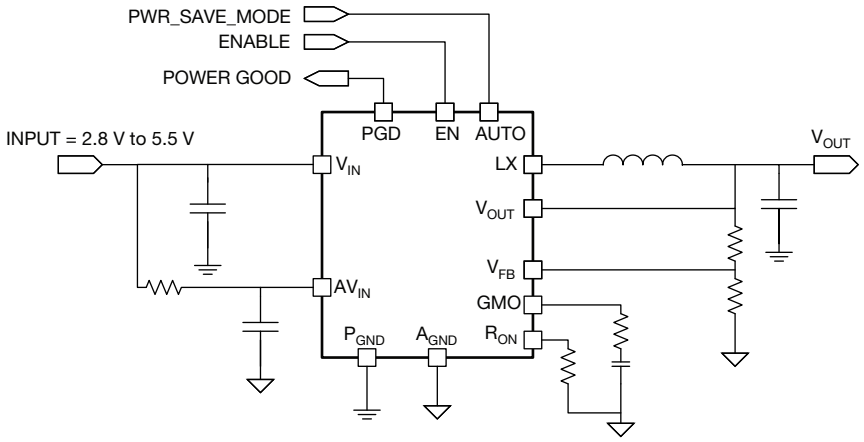


Fig. 1 - Typical Application Circuit for SiP12107

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
V_{IN}	Reference to P_{GND}	- 0.3 to 6	V
AV_{IN}	Reference to A_{GND}	- 0.3 to 6	
LX	Reference to P_{GND}	- 0.3 to 6	
A_{GND} to P_{GND}		- 0.3 to + 0.3	
All Logic Inputs	Reference to A_{GND}	- 0.3 to AV_{IN} + 0.3	
TEMPERATURE			
Max. Operating Junction Temperature		150	°C
Storage Temperature		- 65 to 150	
POWER DISSIPATION			
Junction to Ambient Thermal Impedance (R_{thJA})		36.3	°C/W
Maximum Power Dissipation	Ambient Temperature = 25 °C	3.4	W
	Ambient Temperature = 100 °C	1.3	
ESD PROTECTION			
	HBM	2	kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
V_{IN}	2.8	-	5.5	V
AV_{IN}	2.8	-	5.5	
LX	- 1	-	5.5	
V_{OUT}	0.6	-	0.85 x V_{IN}	
Ambient Temperature	- 40 to 85			°C

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED V_{IN} = AV_{IN} = 3.3 V, T_A = - 40 °C to 85 °C	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Power Input Voltage Range	V_{IN}		2.8	-	5.5	V
Bias Input Voltage Range	AV_{IN}		2.8	-	5.5	
Input Current	IV_{IN_NOLOAD}	Device switching, I_O = 0 A, R_{on} = 100 kΩ, AUTO = Low	-	1000	-	µA
Shutdown Current	IV_{IN_SHDN}	EN = 0 V	-	6	12	
AV_{IN} UVLO Threshold	AV_{IN}, U_{VLO}	AV_{IN} rising edge	-	2.55	-	V
AV_{IN} UVLO Hysteresis	U_{VLOHYS}		-	300	-	mV
PWM CONTROLLER						
Feedback Reference	V_{FB}	T_A = 0 °C to + 70 °C	0.594	0.600	0.606	V
		T_A = - 40 °C to + 85 °C	0.591	0.600	0.609	
V_{FB} Input Bias Current			-	2	200	nA
Transconductance			-	1	-	mS
COMP Source Current			-	50	-	µA
COMP Sink Current			-	50	-	
Switching Frequency Range		Guaranted by design	0.2	-	4	MHz
Minimum On-Time		Guaranted by design	-	50	-	ns
Minimum Off-Time		V_{OUT} = 1.2 V, R_{ON} = 100 kΩ	-	120	-	
Soft Start Time			-	1.5	-	ms
INTEGRATED MOSFETS						
High-Side On Resistance		V_{IN} = 3.3 V	-	56	-	mΩ
Low-Side On Resistance			-	33	-	
FAULT PROTECTIONS						
Over Current Limit		Inductor valley current	-	4.5	-	A
Output OVP Threshold		V_{FB} with respect to 0.6 V reference	-	20	-	%
Output UVP Threshold			-	- 25	-	
Over Temperature Protection		Rising temperature	-	160	-	°C
		Hysteresis	-	35	-	
POWER GOOD						
Power Good Output Threshold		V_{FB} rising above 0.6 V reference	-	20	-	%
		V_{FB} falling below 0.6 V reference	-	- 10	-	
Power Good On Resistance			-	30	-	Ω
Power Good Delay Time			-	6	-	µs
ENABLE THRESHOLD						
Logic High Level			1.5	-	-	V
Logic Low Level			-	-	0.4	

FUNCTIONAL BLOCK DIAGRAM

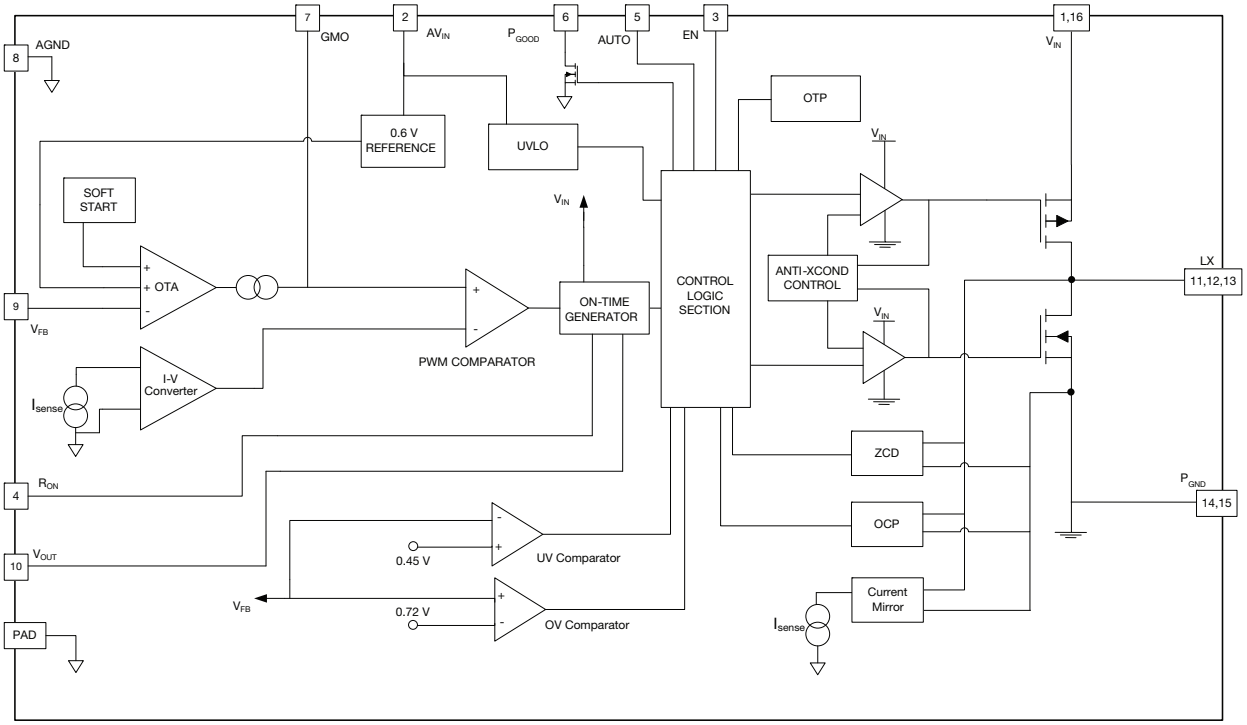
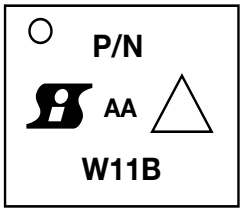


Fig. 2 - SiP12107 Functional Block Diagram

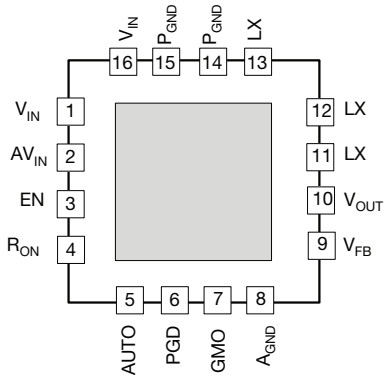
ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING (LINE 2: P/N)**
SIP12107DMP-T1-GE3	QFN33-16L	2107
SIP12107DB	Reference Board	



Format:

Line 1: Dot
Line 2: P/N
Line 2: Siliconix Logo + ESD Symbol
Line 3: Factory Code + Year Code + Work Week Code + Lot Code

PIN CONFIGURATION

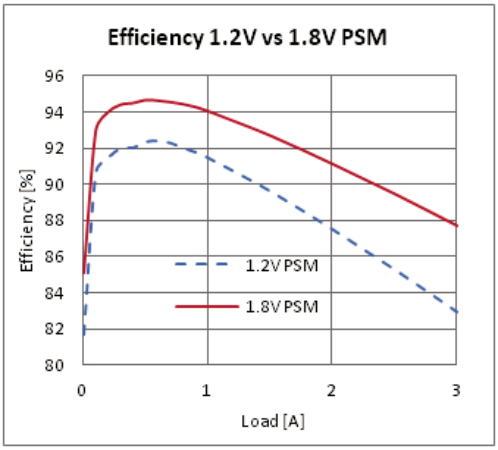


MLPQ 3 x 3 - 16L

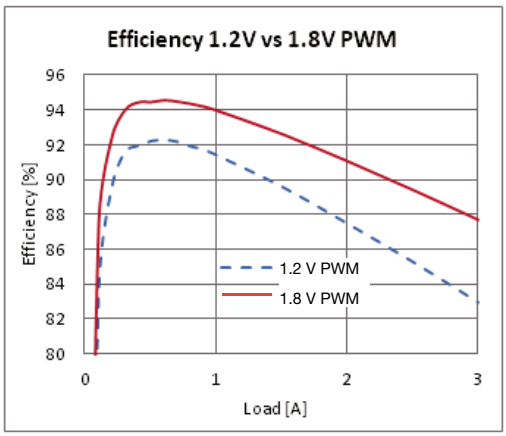
Fig. 3 - SiP12107 Pin Configuration (Top View)

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	V_{IN}	Input supply voltage for power MOS. V_{IN} = 2.8 V to 5.5 V
2	AV_{IN}	Input supply voltage for internal circuitry. AV_{IN} = 2.8 V to 5.5 V
3	EN	Enable pin. Enable > 1.5 V
4	R_{ON}	An external resistor between R_{ON} and GND sets the switching on time.
5	AUTO	Sets switching mode AUTO to AV_{IN} = PWM, AUTO to GND = light load mode
6	PGD	Power good output. Open drain.
7	GMO	Connect to an external RC network for loop compensation and droop function
8	A_{GND}	Analog ground
9	V_{FB}	Feedback voltage. 0.6 V (typ.)
10	V_{OUT}	V_{OUT}, output voltage sense connection
11	LX	Switching output, inductor connection point
12	LX	Switching output, inductor connection point
13	LX	Switching output, inductor connection point
14	P_{GND}	Power ground
15	P_{GND}	Power ground
16	V_{IN}	Input supply voltage for power MOS. V_{IN} = 2.8 V to 5.5 V

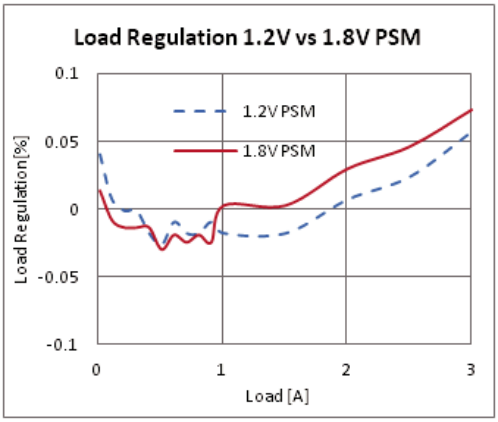
ELECTRICAL CHARACTERISTICS (V_{IN} = 3.3 V, L = 1 µH, C = 3 x 22 µF, f_{SW} = 1.2 MHz unless noted otherwise)



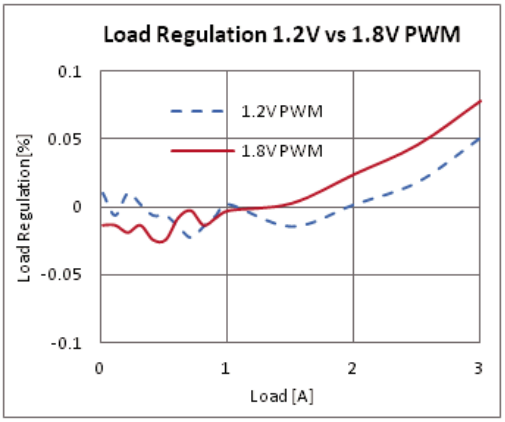
Efficiency vs. I_{OUT} (PSM)



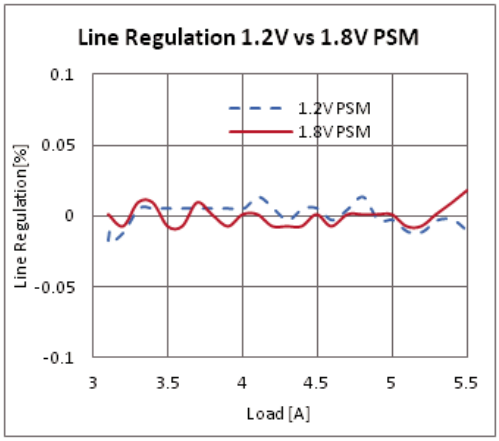
Efficiency vs. I_{OUT} (PWM)



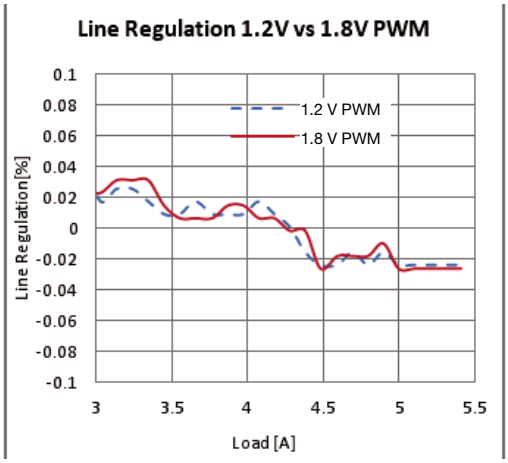
Load Regulation: % of V_{OUT} vs. I_{OUT} (PSM)



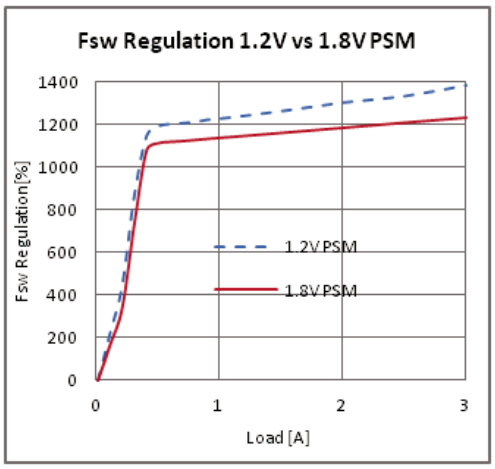
Load Regulation: % of V_{OUT} vs. I_{OUT} (PWM)



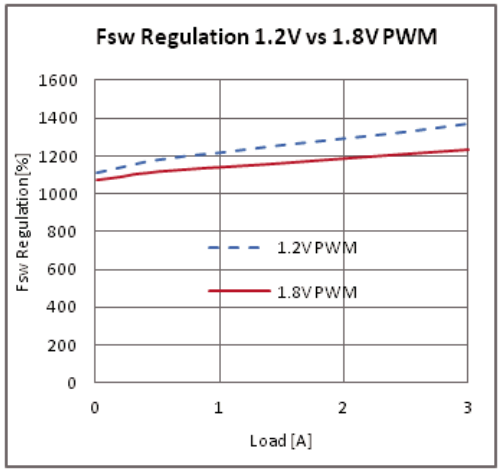
Line Regulation 1.2 V_{OUT} Nominal 0 A Load (PSM)



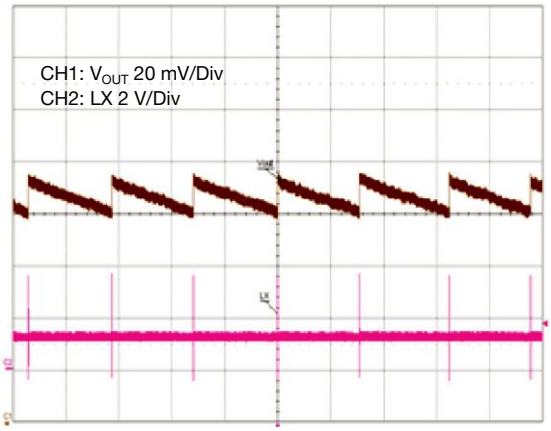
Line Regulation 1.2 V_{OUT} at 3 A Load (PWM)



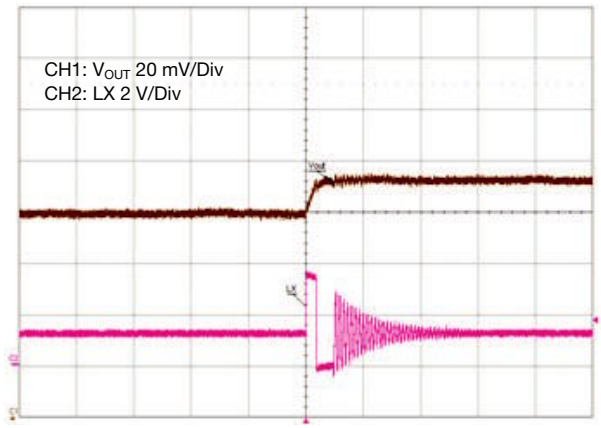
F_{SW} Variation vs. I_{OUT} (PSM)



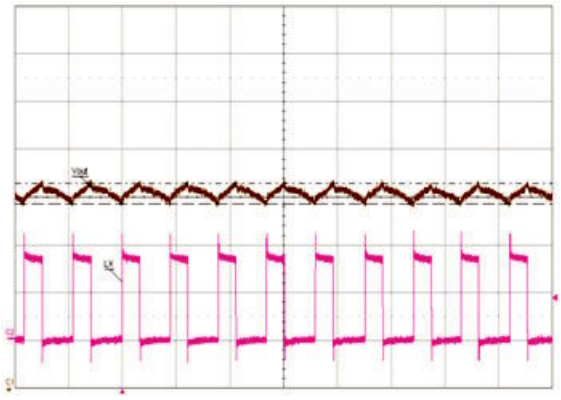
F_{SW} Variation vs. I_{OUT} (PWM)



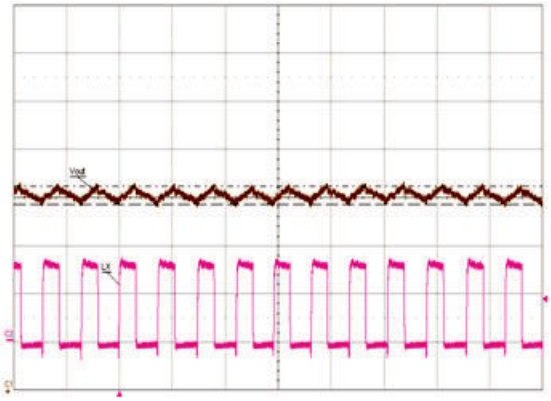
Output Ripple PSM: 0 A Load



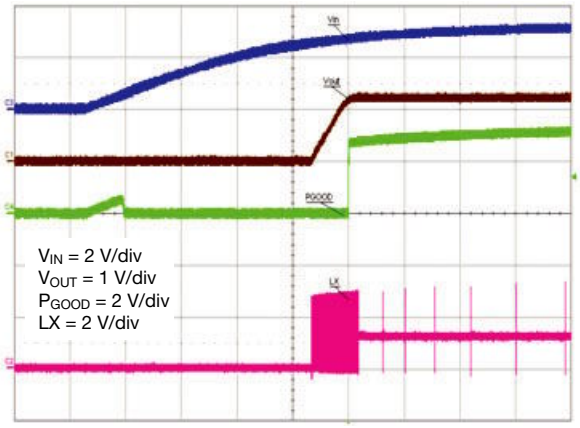
Output Ripple PSM: 0 A Load



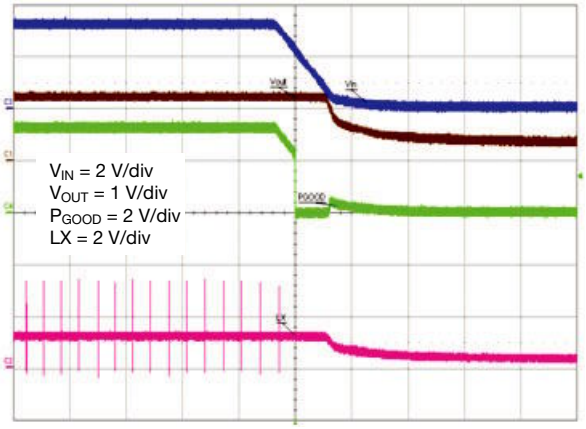
Output Ripple PWM: 0 A Load



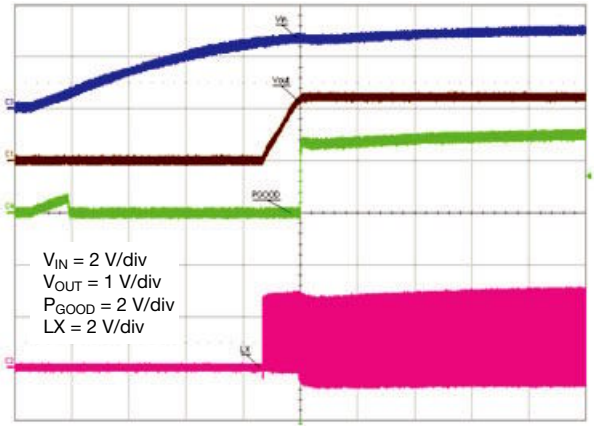
Output Ripple PWM: 3 A Load



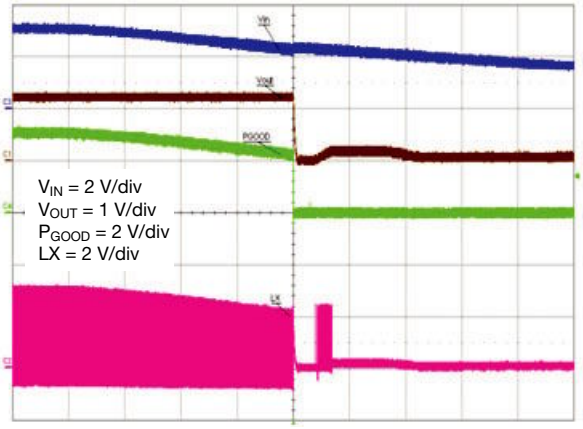
Startup PSM: 0 A Load



Shutdown PSM: 0 A Load



Startup PSM: 3 A Load



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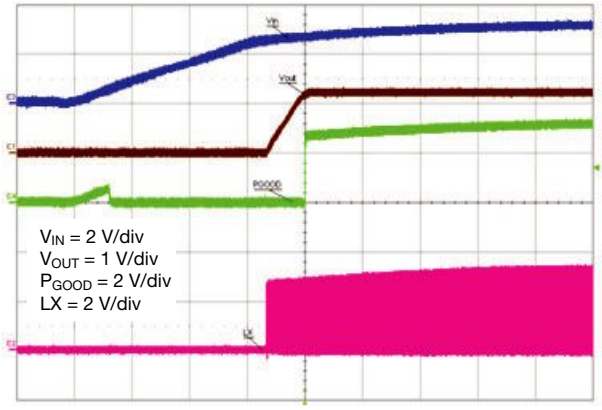

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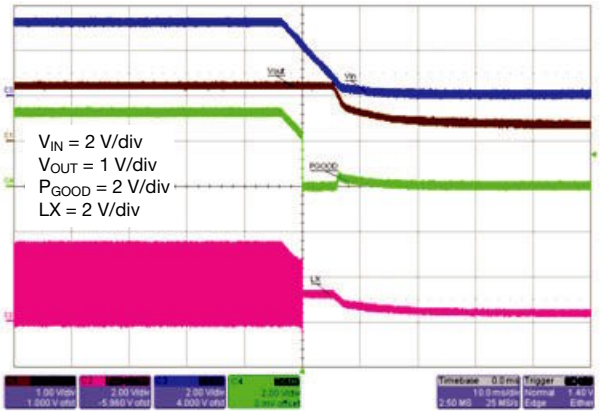
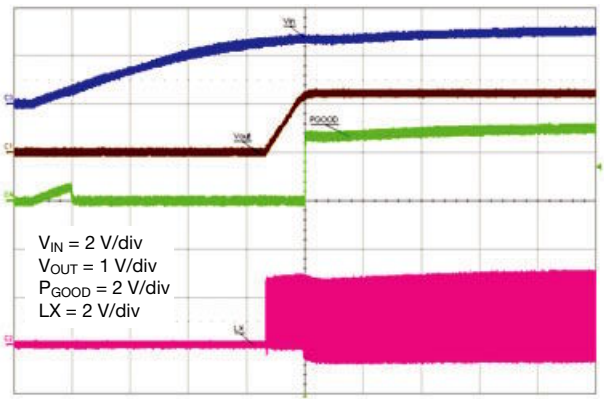
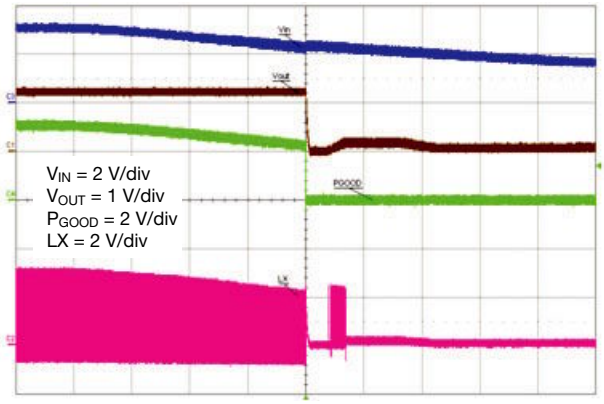


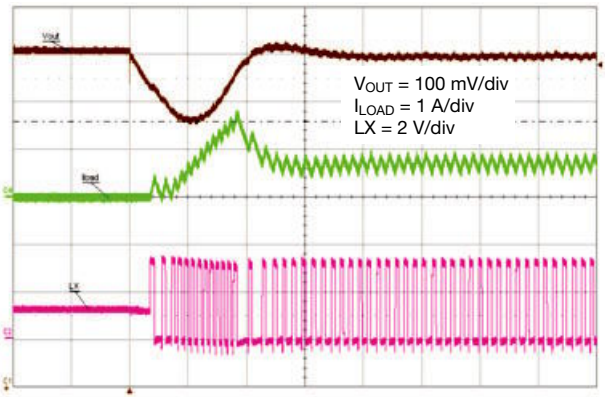
Shutdown PWM: 0 A Load



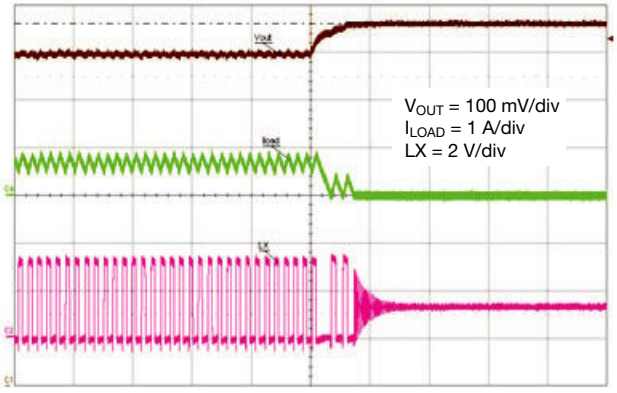
Startup PWM: 3 A Load



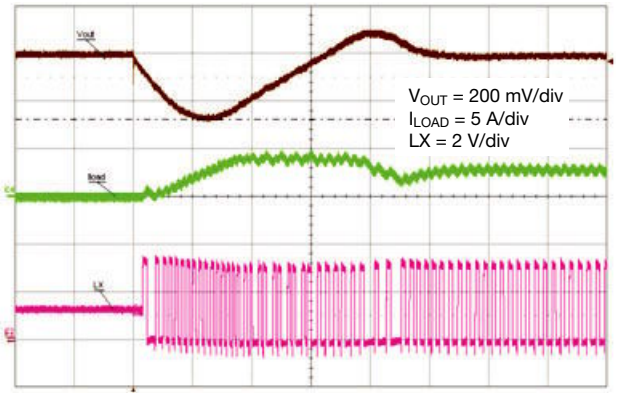
Shutdown PWM: 3 A Load



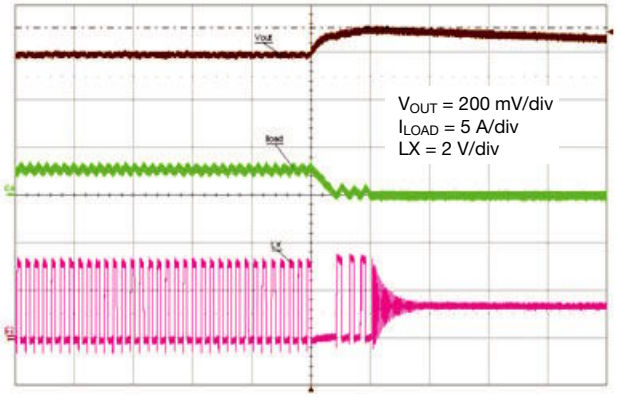
Load Step PSM: 0 A to 1.5 A Load (undershoot)



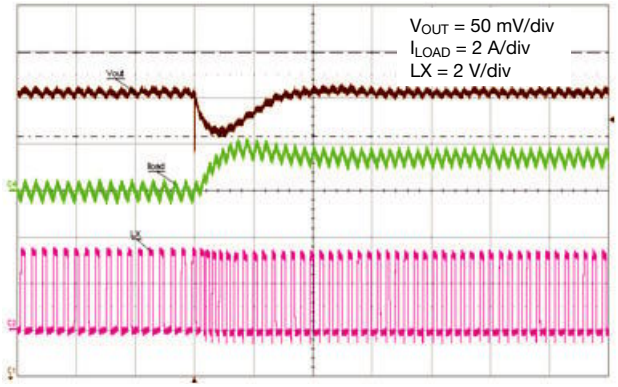
Load Step PSM 0 A to 1.5 A Load (overshoot)



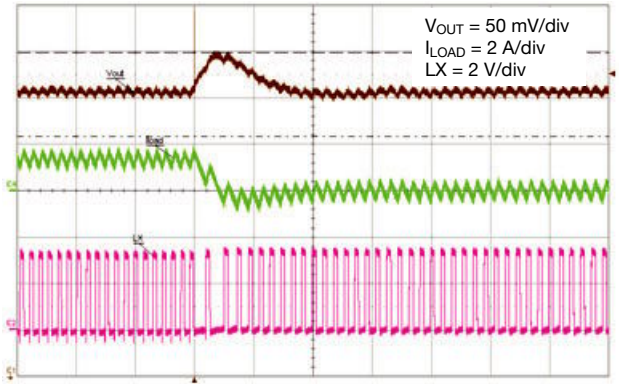
Load Step PSM: 0 A to 3 A Load (undershoot)



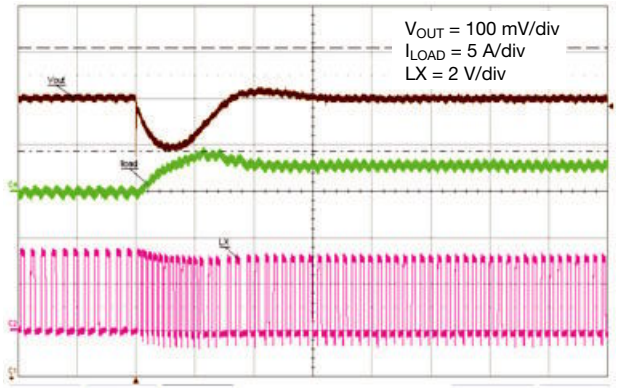
Load Step PSM: 0 A to 3 A Load (overshoot)



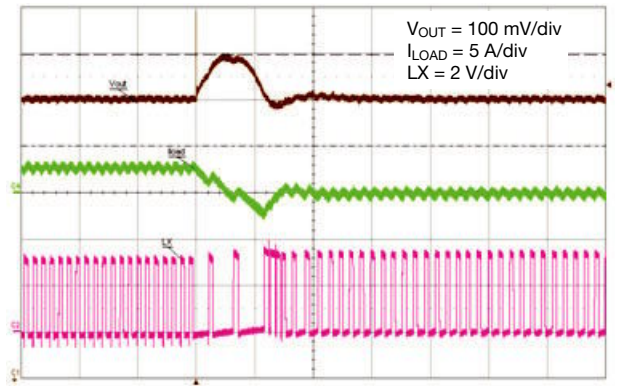
Load Step PWM: 0 A to 1.5 A Load (undershoot)



Load Step PWM 0 A to 1.5 A Load (overshoot)



Load Step PWM: 0 A to 3 A Load (undershoot)



Load Step PWM 0 A to 3 A Load (overshoot)

OPERATIONAL DESCRIPTION

Device Overview

SiP12107 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 3 A continuous current. The device has programmable switching frequency up to 4 MHz. The control scheme is based on current-mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates Power-Saving feature by enabling diode emulation mode and frequency foldback as load decrease.

SiP12107 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power Good open drain output

This device is available in MLPQ 3 x 3-16L package to deliver high power density and minimize PCB area.

Power Stage

SiP12107 integrates a high-performance power stage with a ~ 64 mΩ p-channel MOSFET and a ~ 33 mΩ n-channel MOSFET. The MOSFETs are optimized to achieve 95 % efficiency at 2 MHz switching frequency.

The power input voltage (V_{IN}) can go up to 5.5 V and down as low as 2.8 V for the power conversion. The logic bias voltage (AV_{IN}) ranges from 2.8 V to 5.5 V.

PWM Control Mechanism

SiP12107 employs a state-of-the-art current-mode COT control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated on the COMP pin. In the meantime, inductor valley current is sensed, and its slope (I_{sense}) is converted into a voltage signal ($V_{current}$) to be compared with V_{COMP}. Once $V_{current}$ is lower than V_{COMP}, a single shot on-time is generated for a fixed time programmed by the external R_{ON}. Figure 4 illustrates the basic block diagram for CM-COT architecture and figure 5 demonstrates the basic operational principle:

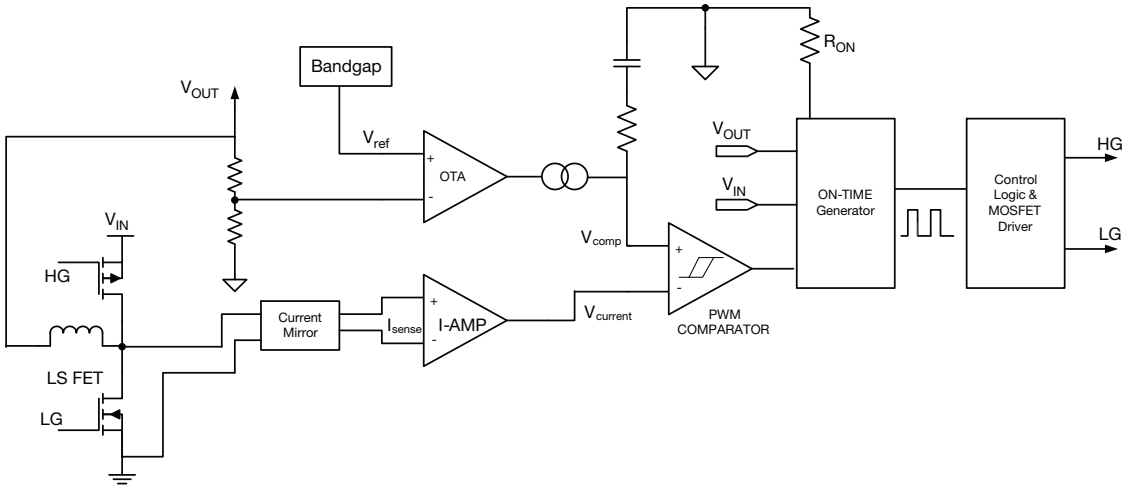


Fig. 4 - CM-COT Block Diagram

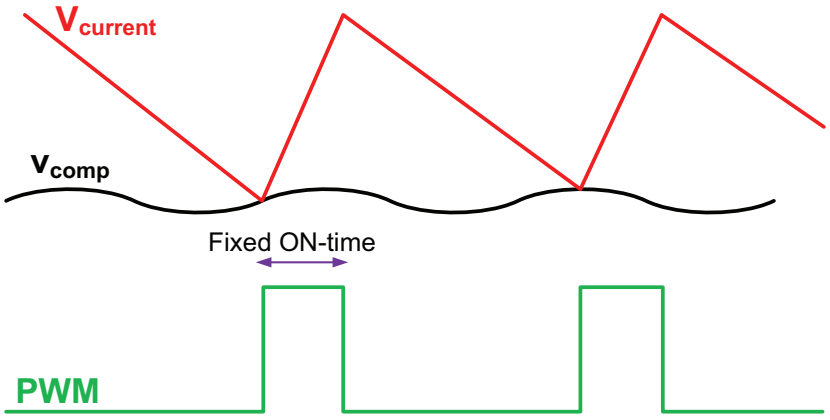


Fig. 5 - CM-COT Operational Principle

The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT} and R_{ON} value:

$$T_{ON} = R_{ON} \times K \times \frac{V_{OUT}}{V_{IN}}, \text{ where } K = 9.6 \times 10^{-12} \text{ a constant set internally}$$

Once on-time is set, the pseudo constant frequency is then determined by the following equation:

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{V_{OUT}}{V_{IN}} \times R_{ON} \times K} = \frac{1}{R_{ON} \times K}$$

Loop Stability and Compensator Design

Due to the nature of current mode control, a simple RC network (type II compensator) is required between COMP and A_{GND} for loop stability and transient response purpose. General concept of this loop design is to introduce a single zero through the compensator to determine the crossover frequency of overall close loop system.

The overall loop can be broken down into following segments.

Output feedback divider transfer function H_{fb}:

$$H_{fb} = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}}$$

Voltage compensator transfer function G_{COMP} (s):

$$G_{COMP}(s) = \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm$$

Modulator transfer function H_{mod} (s):

$$H_{mod}(s) = \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

The complete loop transfer function is given by:

$$H_{mod}(s) = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}} \times \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm \times \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

When:

C_{COMP} = Compensation capacitor
R_{COMP} = Compensation resistor
gm = Error amplifier transconductance
R_{load} = Load resistance
C_O = Output capacitor
$R_{DS(on)}$ = LS switch resistance
R_{fb1} = Feedback resistor connect to LX
R_{fb2} = Feedback resistor connect to ground
R_O = Output impedance of error amplifier = 20 MΩ
AV_1 = Voltage to current gain = 3

Power-Saving Mode Operation

To further improve efficiency at light-load condition, SiP12107 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal Zero Crossing Detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In power saving mode (PSM), as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

Whenever fixed frequency PWM operation is required over the entire load span, power saving mode feature can be disabled by connecting AUTO pin to V_{IN} or AV_{IN}.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiP12107 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined time, the valley current is compared with internal threshold (5 A typ.) to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output under-voltage protection (UVP), which latches the device off to prevent catastrophic thermal-related failure. UVP is described in the next section.

OCP is enabled immediately after AV_{IN} passes UVLO level.

Figure 6 illustrates the OCP operation.

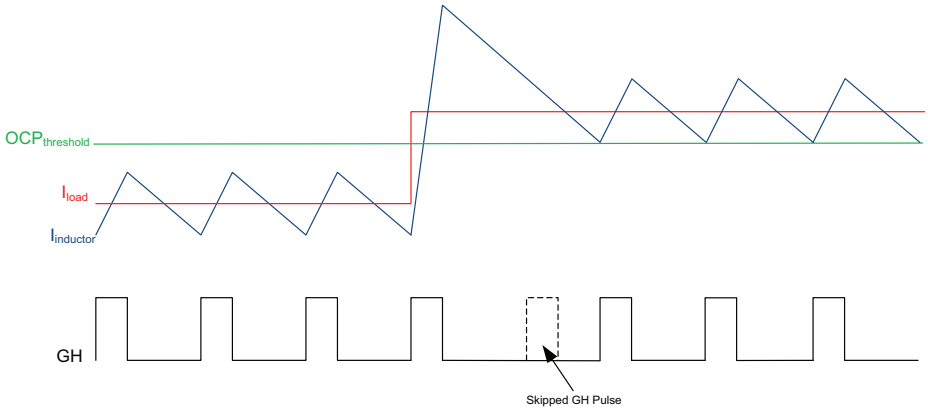


Fig. 6 - Over-Current Protection Illustration

Output Under-Voltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. Once the voltage level at V_{FB} is below 0.45 V for more than 20 µs, then UVP event is recognized and both HS and LS MOSFETs are turned off. UVP latches the device off until either AV_{IN} or EN is recycled.

UVP is only active after the completion of soft-start sequence.

Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft-start, if the voltage level at FB is above 20 % (typ.), OVP is triggered with HS FET turning off and LS FET turning on immediately to discharge the output. Normal operation is resumed once FB voltage drops back to 0.6 V.

OVP is active immediately after AV_{IN} passes UVLO level.

Over-Temperature Protection (OTP)

SiP12017 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 160 °C (typ.). A hysteresis of 30 °C is implemented, so when junction temperature drops below 130 °C, the device restarts by initiating the soft-start sequence again.

Soft Startup

SiP12107 deploys an internally regulated soft-start sequence to realize a monotonic startup ramp without any output overshoot. Once AV_{IN} is above UVLO level (2.55 V typ.). Both the reference and V_{OUT} will ramp up slowly to regulation in 1 ms (typ.) with the reference going from 0 V to 0.6 V and V_{OUT} rising monotonically to the programmed output voltage.

During soft-start period, OCP is activated. OVP and short-circuit protection are not active until soft-start is complete.

Pre-bias Startup

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

Power Good (PG)

SiP12107's Power Good is an open-drain output. Pull PG pin high up to 5 V through a 10K resistor to use this signal. Power Good window is shown in the below diagram. If voltage level on FB pin is out of this window, PG signal is de-asserted by pulling down to GND.

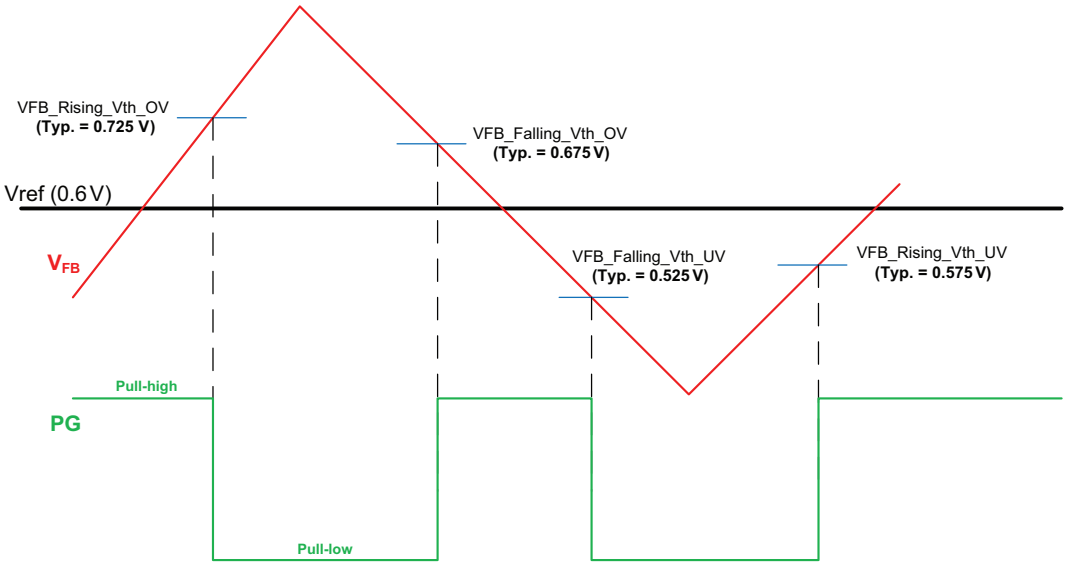


Fig. 7 - PG Window and Timing Diagram

DESIGN PROCEDURE

The design process of the SiP12107 is quite straight forward. Only few passive components such as output capacitors, inductor and R_{on} resistor need to be selected.

The following paragraph describes the selection procedure for these peripheral components for a given operating conditions.

In the next example the following definitions apply:

$V_{INmax.}$: the highest specified input voltage

$V_{INmin.}$: the minimum effective input voltage subject to voltage drops due to connectors, fuses, switches, and PCB traces

There are two values of load current to evaluate - continuous load current and peak load current.

Continuous load current relates to thermal stress considerations which drive the selection of the inductor and input capacitors.

Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following specifications are used in this design:

- V_{IN} = 3.3 V ± 10 %
- V_{OUT} = 1.2 V ± 1 %
- F_{SW} = 1 MHz
- Load = 3 A maximum

Setting Switching Frequency

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency. The desired switching frequency, 1 MHz was chosen based on optimizing efficiency while maintaining a small footprint and minimizing component cost.

In order to set the design for 1 MHz switching frequency, (R_{ON}) resistor which determines the on-time (indirectly setting the frequency) needs to be calculated using the following equation.

$$R_{ON} = \frac{1}{F_{SW} \times K} = \frac{1}{1 \times 10^{6} \times 9.6 \times 10^{-12}} \cong 105\ k\Omega$$

INDUCTOR SELECTION

In order to determine the inductance, the ripple current must first be defined. Cost, PCB size, output ripple, and efficiency are all used in the selection process. Low inductor values result in smaller size and allow faster transient performance but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current while compromising the efficiency (higher DCR) and transient response.

The ripple current will also set the boundary for power-save operation. The switcher will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 1 A then power-save operation will typically start at loads approaching 0.5 A. Alternatively, if ripple current is set at 40 % of maximum load current, then power-save will start for loads less than ~ 20 % of maximum current.

Setting the ripple current 20 % to 50 % of the maximum load current provides an optimal trade-off of the areas mentioned above.

The equation for determining inductance is shown next.

Example

In this example, the inductor ripple current is set equal to 30 % of the maximum load current. Thus ripple current will be 30 % x 3 A or 0.9 A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to $V_{INmax.}$

$$L = (V_{IN} - V_{OUT}) \times \frac{T_{ON}}{\Delta i}$$

Plugging numbers into the above equation we get

$$L = (3.63\ V - 1.2\ V) \times \frac{330 \times 10^{-9}\ s}{0.9\ A} = 0.891\ \mu H$$

A slightly larger value of 1 µH is selected which is a standard value. This will decrease the maximum ripple current by 10 %. Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current. The actual ripple current using the chosen 1 µH inductor comes out to be.

$$\Delta i = (3.63\ V - 1.2\ V) \times \frac{330\ ns}{1\ \mu H} = 0.8\ A$$

Output Capacitance Calculation

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < $1/F_{SW}$ µs), the output capacitor must absorb all the inductor's stored energy. This will approximately cause a peak voltage on the capacitor according to the following equation.

$$C_{OUTmin.} = \frac{L \times \left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEmax.}\right)^2}{(V_{peak})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.3 V (100 mV rise upon load release), and a 3 A load release, the required capacitance is shown by the next equation.

$$C_{OUTmin.} = \frac{1\ \mu H \times (3\ A + 0.5 \times (81\ A))^2}{(1.3\ V)^2 - (1.2\ V)^2} = 46.37\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced. Using MLCC ceramic capacitors we will use 3 x 22 µF or 66 µF as the total output capacitance.

STABILITY CONSIDERATIONS

Using the output capacitance as a starting point for compensation values. Then, taking Bode plots and transient response measurements we can fine tune the compensation values.

Setting the crossover frequency to 1/5 of the switching frequency:
$F_0 = F_{sw}/5 = 1\ MHz/5 = 200\ kHz$
Setting the compensation zero at 1/5 to 1/10 the crossover frequency for the phase boost:

$$F_Z = \frac{1}{2\pi \times R_C \times C_C} = \frac{F_0}{5}$$

Setting C_C = 1 nF and solve for R_C

$$R_C = \frac{5}{2\pi \times C_C \times F_0} = \frac{5}{2\pi \times 1\ nF \times 200K} = 4K$$

SWITCHING FREQUENCY VARIATIONS

The switching frequency variation in COT can be mainly attributed to the increase in conduction losses as the load increases. The on time is "ideally constant" so the controller must account for losses by reducing the off time which increases the overall duty cycle. Hence the F_{SW} will tend to increase with load.

In power save mode (PSM) the IC will run in pulse skip mode at light loads. As the load increases the F_{SW} will increase until it reaches the nominal set F_{SW}. This transition occurs approximately when the load reaches to 20 % of the full load current.

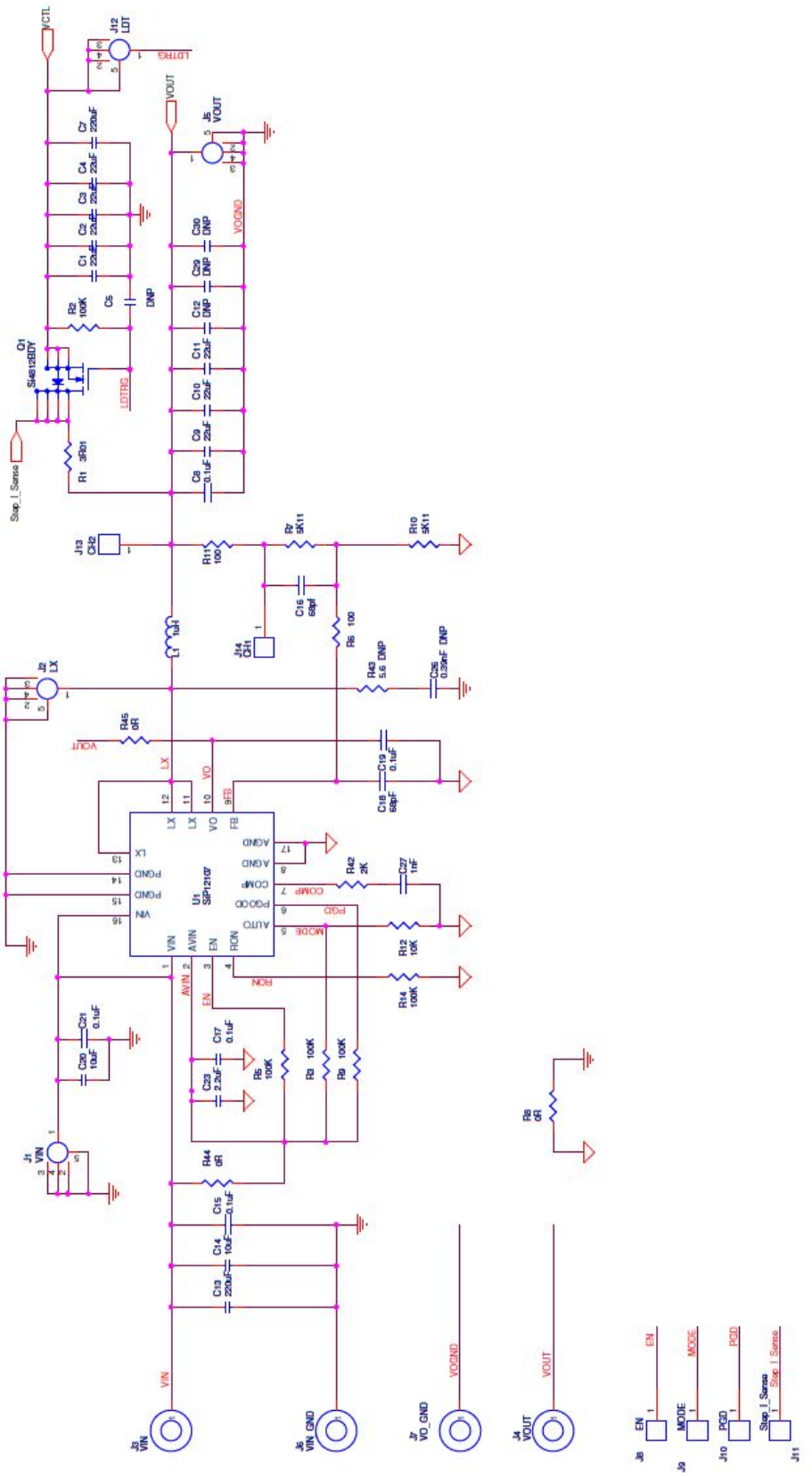


Fig. 8 - Reference Board Schematic

BILL OF MATERIALS

ITEM	QTY.	REFERENCE	PART	VOLTAGE	PCB FOOTPRINT	PART NUMBER	MANUFACTURER
1	4	C1, C2, C3, C4	22 µF	16 V	SM/C_1210	GRM32ER71C226ME18L	Murata
2	1	C5	DNP	50 V	SM/C_0603	-	-
3	2	C7, C13	220 µF	25 V	594D-R TYPE	594D227X0016R2T	Vishay
4	3	C8, C19, C21	0.1 µF	50 V	SM/C_0603	VJ0603Y104KXACW1BC	Vishay
5	3	C9, C10, C11	22 µF	6.3 V	SM/C_1210	GCM32ER70J476KE19L	Murata
6	3	C12, C29, C30	DNP	6.3 V	SM/C_1210	-	-
7	2	C14, C20	10 µF	16 V	SM/C_1206	C1206C106K4RACTU	Taiyo Yuden
8	1	C15	0.1 µF	50 V	SM/C_0402	VJ0603Y104KXACW1BC	Vishay
9	1	C16	68 pF	50 V	SM/C_0603	VJ0402A680JNAAJ	Vishay
10	1	C17	0.1 µF	50 V	SM/C_0402	VJ0402Y104KXACW1BC	Vishay
11	1	C18	68 pF	50 V	SM/C_0402	VJ0402A680JNAAJ	Vishay
12	1	C23	2.2 µF	10 V	SM/C_0603	GRM188R71A225KE15D	Murata
13	1	C26	DNP	50 V	SM/C_0402	-	-
14	1	C27	1 nF	50 V	SM/C_0402	VJ0402Y102KXACW1BC	Vishay
29	1	L1	1µH	-	IHLP2525	IHLP2525DZER1R0M01	Vishay
30	1	Q1	-	30 V	SO-8	Si4812BDY	Vishay
31	1	R1	3R01	200 V	C_2512	CRCW25123R01FKTA	Vishay
32	4	R2, R3, R5, R9	100K	50 V	SM/C_0603	CRCW0603100KFKEA	Vishay
33	1	R6	100	50 V	SM/C_0402	TNPW0402100RBEED	Vishay
34	1	R7	5K11	50 V	SM/C_0603	CRCW06035K11FKEA	Vishay
35	1	R8	0R	50 V	SM/C_0402	CRCW04020000FKTA	Vishay
36	1	R10	5K11	-	SM/C_0603	CRCW06035K11FKEA	-
37	1	R11	100	50 V	SM/C_0603	TNPW0402100RBEED	Vishay
38	1	R12	10K	50 V	SM/C_0603	CRCW060310K0FKEA	Vishay
39	1	R14	100K	50 V	SM/C_0603	CRCW0603100KFKEA	Vishay
40	1	R42	2K	50 V	SM/C_0603	CRCW06032K00FKEA	Vishay
41	1	R43	DNP	-	SM/C_0805	-	
42	1	R44	0R	50 V	SM/C_0603	CRCW06030000Z0EA	Vishay
43	1	R45	0R	50 V	SM/C_0402	CRCW04020000FKTA	Vishay
44	1	U1	-	-	QFN3X3_16 L	SiP12107	Vishay
45	1	J1	V_{IN}		PROBE PIN	PK007-015	Lecroy
46	1	J2	LX		PROBE PIN	PK007-015	Lecroy
47	1	J3	V_{IN}		Power connector	575-6	Keystone
48	1	J4	V_{OUT}		Power connector	575-6	Keystone
49	1	J5	V_{OUT}		PROBE PIN	PK007-015	Lecroy
50	1	J6	V_{IN}_GND		Power connector	575-6	Keystone
51	1	J7	V_O_GND		Power connector	575-6	Keystone
52	1	J8	EN		Control PIN	1573-3	Keystone
53	1	J9	MODE		Control PIN	1573-3	Keystone
54	1	J10	PGD		Probe PIN	1573-3	Keystone
55	1	J11	Step_I_Sense		Probe PIN	1573-3	Keystone
56	1	J12	LDT		SMA test connector	PK007-015	Lecroy
57	1	J13	CH2		Test point	1573-3	Keystone
58	1	J14	CH1		Test point	1573-3	Keystone

PCB LAYOUT OF REFERENCE BOARD

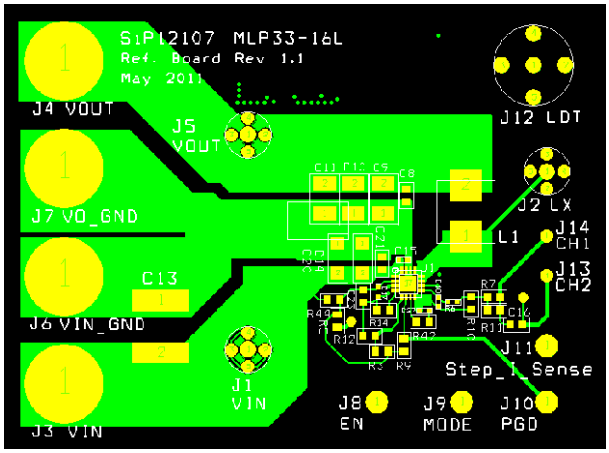


Fig. 9 - Top Layer

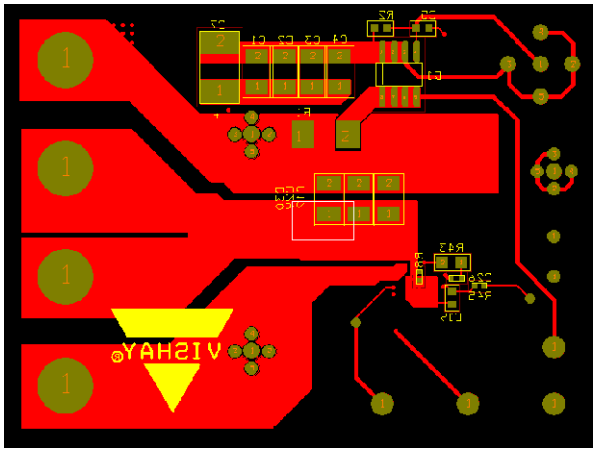


Fig. 11 - Bottom Layer

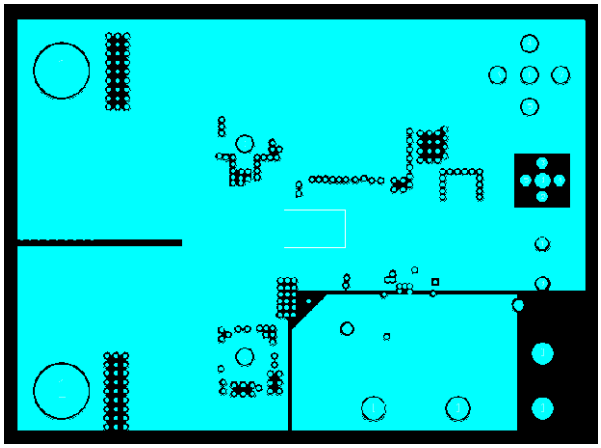


Fig. 10 - Inner Layer1

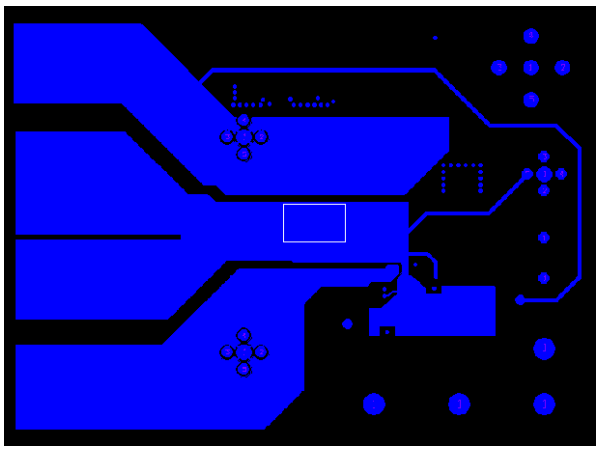


Fig. 12 - Inner Layer2

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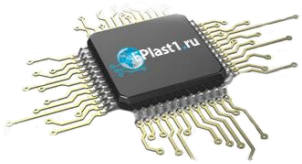

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