High Common-Mode Voltage, Difference Amplifier

AD629

FEATURES

Improved replacement for: INA117P and INA117KU
±270 V common-mode voltage range
Input protection to
±500 V common mode
±500 V differential mode
Wide power supply range (±2.5 V to ±18 V)
±10 V output swing on ±12 V supply
1 mA maximum power supply current

HIGH ACCURACY DC PERFORMANCE
3 ppm maximum gain nonlinearity (AD629B)
20 µV/°C maximum offset drift (AD629A)
10 µV/°C maximum offset drift (AD629B)
10 ppm/°C maximum gain drift

EXCELLENT AC SPECIFICATIONS
77 dB minimum CMRR @ 500 Hz (AD629A)
86 dB minimum CMRR @ 500 Hz (AD629B)
500 kHz bandwidth

APPLICATIONS

High voltage current sensing
Battery cell voltage monitors
Power supply current monitors
Motor controls
Isolation

FUNCTIONAL BLOCK DIAGRAM

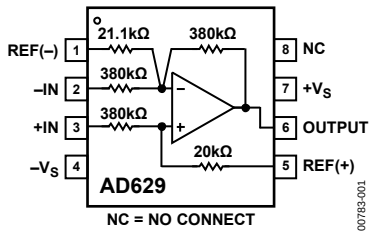


Figure 1.

GENERAL DESCRIPTION

The AD629 is a difference amplifier with a very high input, common-mode voltage range. It is a precision device that allows the user to accurately measure differential signals in the presence of high common-mode voltages up to ±270 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. The device operates over a ±270 V common-mode voltage range and has inputs that are protected from common-mode or differential mode transients up to ±500 V.

The AD629 has low offset, low offset drift, low gain error drift, low common-mode rejection drift, and excellent CMRR over a wide frequency range.

The AD629 is available in die and packaged form featuring 8-lead PDIP and 8-lead SOIC packages. For all packages (including die) and grades, performance is guaranteed over the industrial temperature range of −40°C to +85°C.

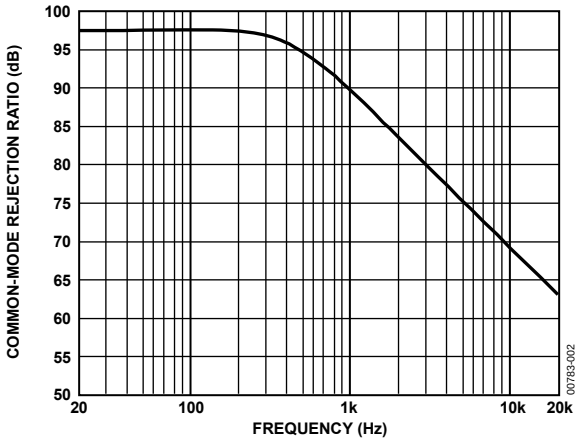


Figure 2. Common-Mode Rejection Ratio vs. Frequency

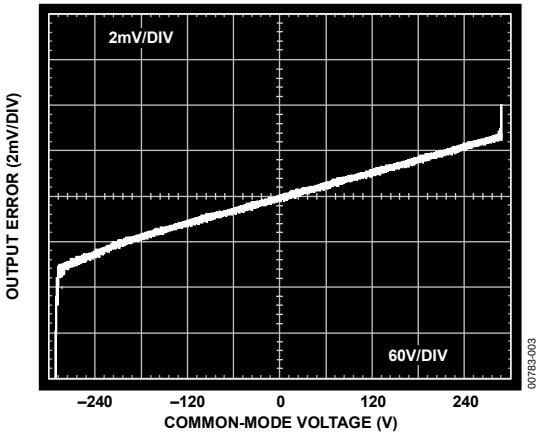


Figure 3. Error Voltage vs. Input Common-Mode Voltage

Rev. C
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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REVISION HISTORY

4/11—Rev. B to Rev. C

Changes to General Description Section ... 1
Added Endnote 1 in Table 1 ... 3
Added Figure 5; Renumbered Sequentially ... 4
Added Table 3; Renumbered Sequentially ... 4
Added Pin Configuration and Function Descriptions Section, Figure 6, and Table 4 ... 5
Changes to Ordering Guide ... 16

3/07—Rev. A to Rev. B

Updated Format and Layout ... Universal
Changes to Ordering Guide ... 15

3/00—Rev. 0 to Rev. A

10/99—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±15 V, unless otherwise noted.

Table 1.

		AD629A[1]			AD629B			
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN	V_{OUT} = ±10 V, R_L = 2 kΩ							
Nominal Gain			1			1		V/V
Gain Error			0.01	0.05		0.01	0.03	%
Gain Nonlinearity			4	10		4	10	ppm
	R_L = 10 kΩ		1			1	3	ppm
Gain vs. Temperature	$T_A = T_{MIN}$ to T_{MAX}		3	10		3	10	ppm/°C
OFFSET VOLTAGE								
Offset Voltage			0.2	1		0.1	0.5	mV
	V_S = ±5 V						1	mV
vs. Temperature	$T_A = T_{MIN}$ to T_{MAX}		6	20		3	10	µV/°C
vs. Supply (PSRR)	V_S = ±5 V to ± 15 V	84	100		90	110		dB
INPUT								
Common-Mode Rejection Ratio	V_{CM} = ±250 V dc	77	88		86	96		dB
	$T_A = T_{MIN}$ to T_{MAX}	73			82			dB
	V_{CM} = 500 V p-p, dc to 500 Hz	77			86			dB
	V_{CM} = 500 V p-p, dc to 1 kHz		88			90		dB
Operating Voltage Range	Common mode			±270			±270	V
	Differential			±13			±13	V
Input Operating Impedance	Common mode		200			200		kΩ
	Differential		800			800		kΩ
OUTPUT								
Operating Voltage Range	R_L = 10 kΩ	±13			±13			V
	R_L = 2 kΩ	±12.5			±12.5			V
	V_S = ±12 V, R_L = 2 kΩ	±10			±10			V
Output Short-Circuit Current			±25			±25		mA
Capacitive Load	Stable operation	1000			1000			pF
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth			500			500		kHz
Slew Rate		1.7	2.1		1.7	2.1		V/µs
Full Power Bandwidth	V_{OUT} = 20 V p-p		28			28		kHz
Settling Time	0.01%, V_{OUT} = 10 V step		15			15		µs
	0.1%, V_{OUT} = 10 V step		12			12		µs
	0.01%, V_{CM} = 10 V step, V_{DIFF} = 0 V		5			5		µs
OUTPUT NOISE VOLTAGE								
0.01 Hz to 10 Hz			15			15		µV p-p
Spectral Density, ≥100 Hz[2]			550			550		nV/√Hz
POWER SUPPLY								
Operating Voltage Range		±2.5		±18	±2.5		±18	V
Quiescent Current	V_{OUT} = 0 V		0.9	1		0.9	1	mA
	T_{MIN} to T_{MAX}		1.2			1.2		mA
TEMPERATURE RANGE								
For Specified Performance	$T_A = T_{MIN}$ to T_{MAX}	–40		+85	–40		+85	°C

[1] Specifications for the AD629 A grade are also valid for the die model (listed in the Ordering Guide as AD629AC-WP).
[2] See Figure 21.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	±18 V
Internal Power Dissipation[1]	
8-Lead PDIP (N)	See Figure 4
8-Lead SOIC (R)	See Figure 4
Input Voltage Range, Continuous	±300 V
Common-Mode and Differential, 10 sec	±500 V
Output Short-Circuit Duration	Indefinite
Pin 1 and Pin 5	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Maximum Junction Temperature	150°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] Specification is for device in free air:
8-Lead PDIP, θ_{JA} = 100°C/W;
8-Lead SOIC, θ_{JA} = 155°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

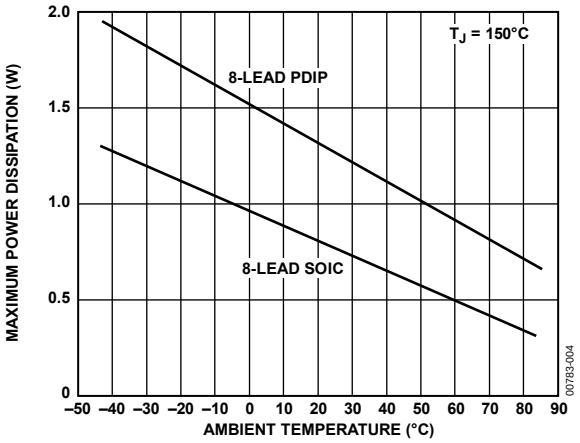


Figure 4. Maximum Power Dissipation vs. Temperature for SOIC and PDIP

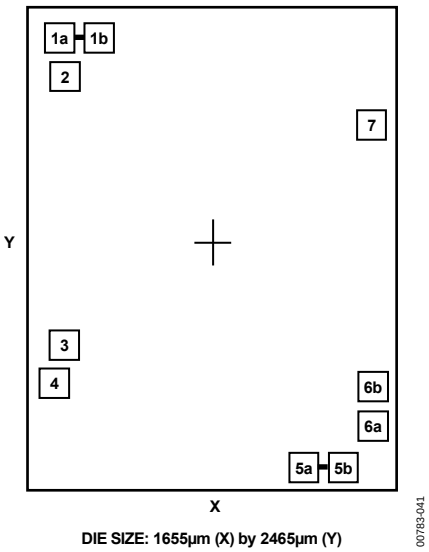


Figure 5. Metallization Photograph

Table 3. Pin Pad Coordinates

Pad	Pin	Coordinates[1] X	Coordinates[1] Y	Description
1a	REF(−)	−677	+1082	For the die model, either pad can be bonded because 1a and 1b are internally shorted.
1b		−534	+1084	
2	−IN	−661	+939	
3	+IN	−661	−658	
4	$-V_S$	+680	−800	
5a	REF(+)	+396	−1084	For the die model, either pad can be bonded because 5a and 5b are internally shorted.
5b		+538	−1084	
6a	OUTPUT	+681	−950	For the die model, both pads must be bonded because 6a and 6b are not internally shorted.
6b		+681	−807	
7	$+V_S$	+680	+612	

[1] All coordinates are with respect to the center of the die.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

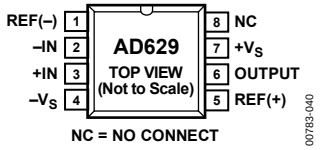


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF(–)	Negative Reference Voltage Input.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply Voltage.
5	REF(+)	Positive Reference Voltage Input.
6	OUTPUT	Output.
7	$+V_S$	Positive Supply Voltage.
8	NC	No Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V, unless otherwise noted.

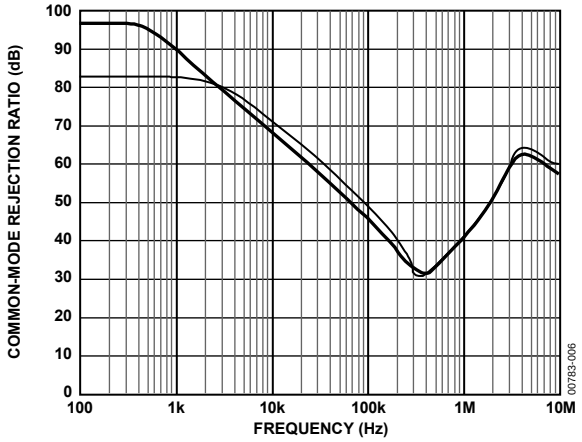


Figure 7. Common-Mode Rejection Ratio vs. Frequency

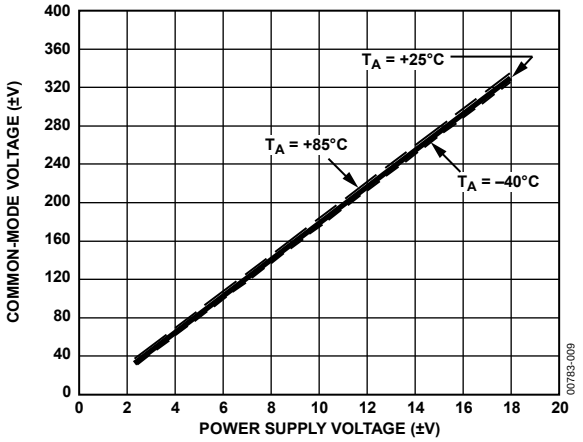


Figure 10. Common-Mode Operating Range vs. Power Supply Voltage

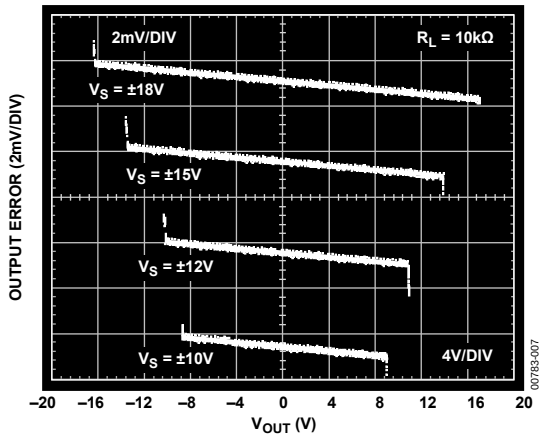


Figure 8. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 10 kΩ (Curves Offset for Clarity)

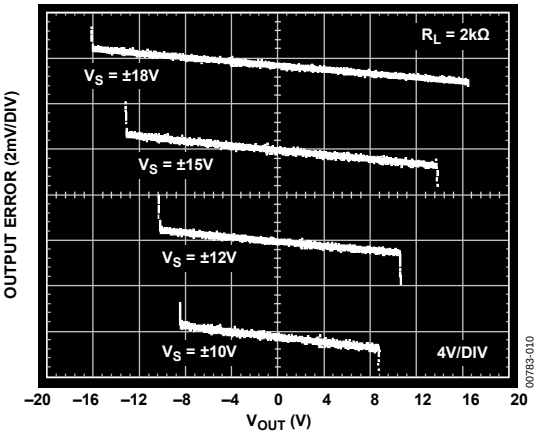


Figure 11. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 2 kΩ (Curves Offset for Clarity)

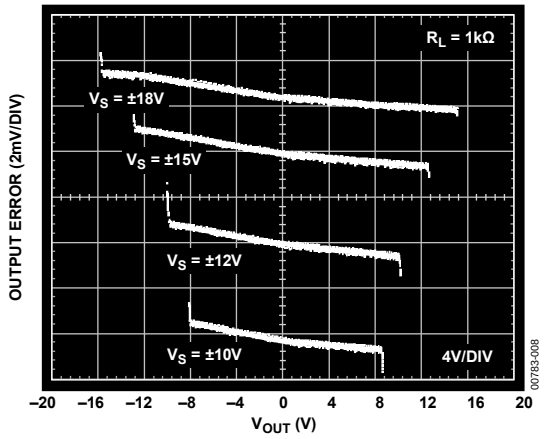


Figure 9. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 1 kΩ (Curves Offset for Clarity)

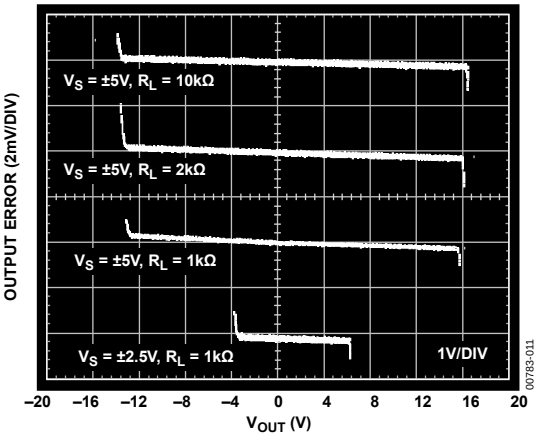


Figure 12. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage (Curves Offset for Clarity)

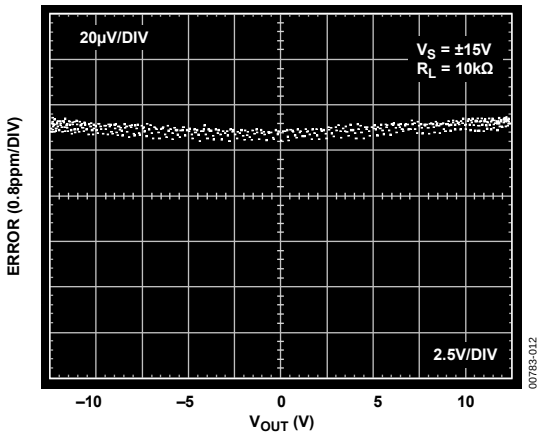


Figure 13. Gain Nonlinearity; V_S = ±15 V, R_L = 10 kΩ

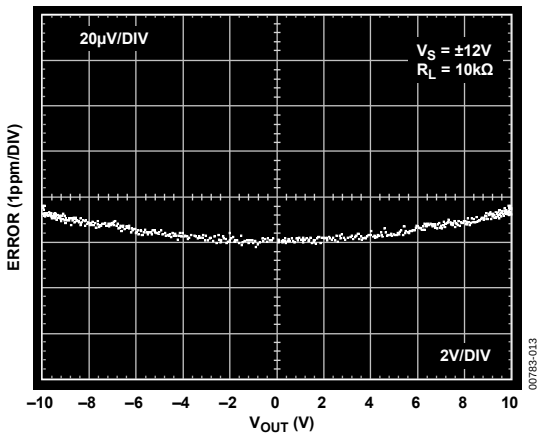


Figure 14. Gain Nonlinearity; V_S = ±12 V, R_L =10 kΩ

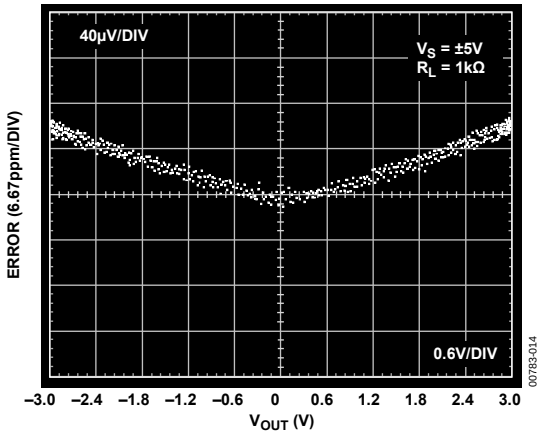


Figure 15. Gain Nonlinearity; V_S = ±5 V, R_L = 1 kΩ

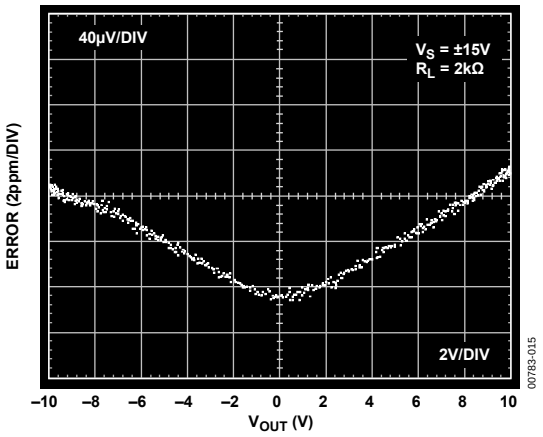


Figure 16. Gain Nonlinearity; V_S = ±15 V, R_L = 2kΩ

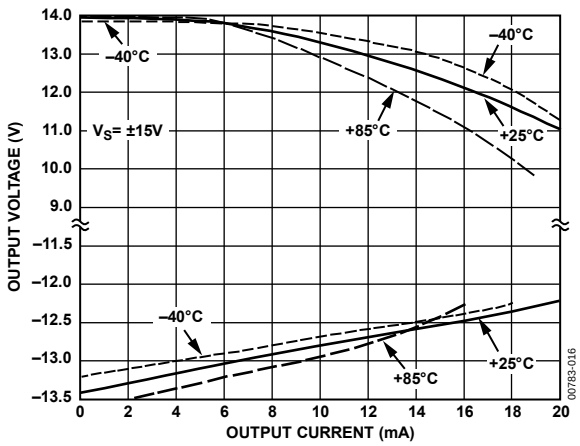


Figure 17. Output Voltage Operating Range vs. Output Current; V_S = ±15 V

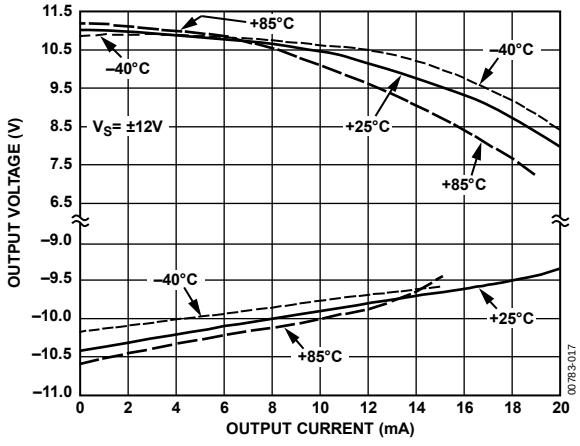


Figure 18. Output Voltage Operating Range vs. Output Current; V_S = ±12 V

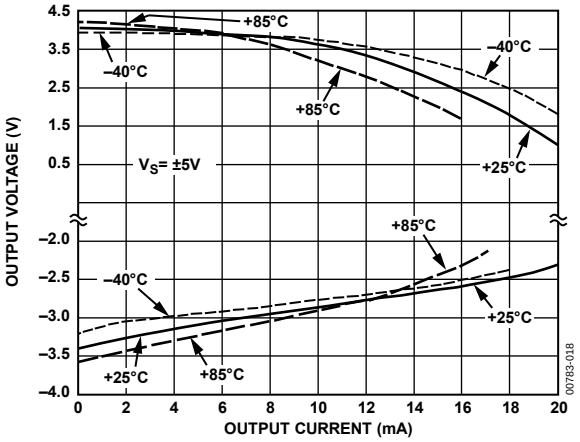


Figure 19. Output Voltage Operating Range vs. Output Current; V_S = ±5 V

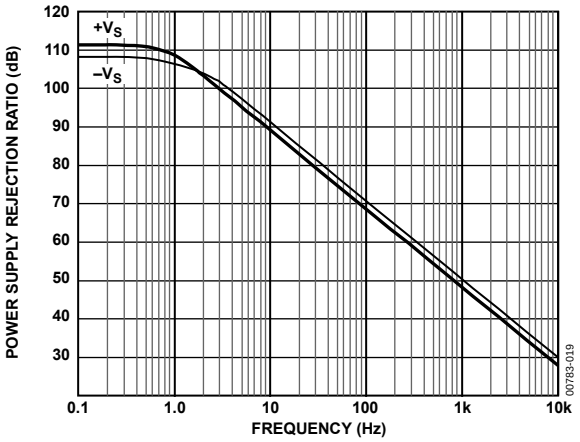


Figure 20. Power Supply Rejection Ratio vs. Frequency

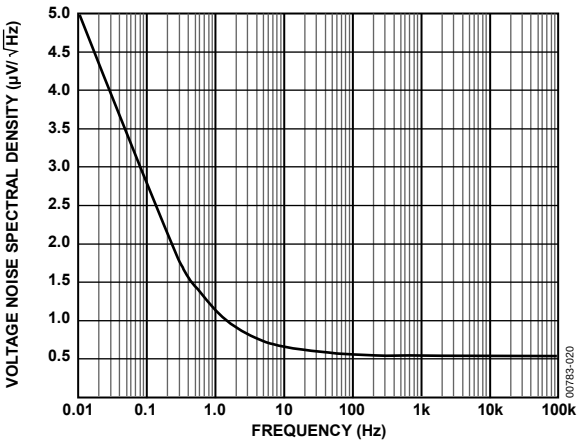


Figure 21. Voltage Noise Spectral Density vs. Frequency

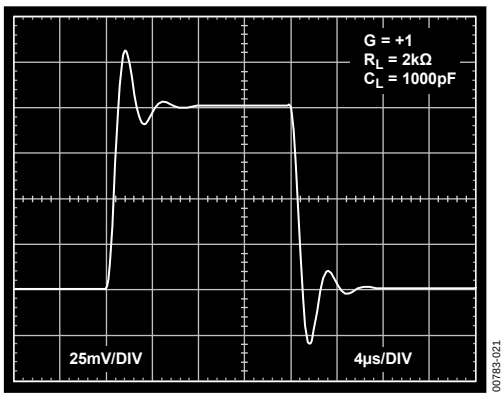


Figure 22. Small Signal Pulse Response

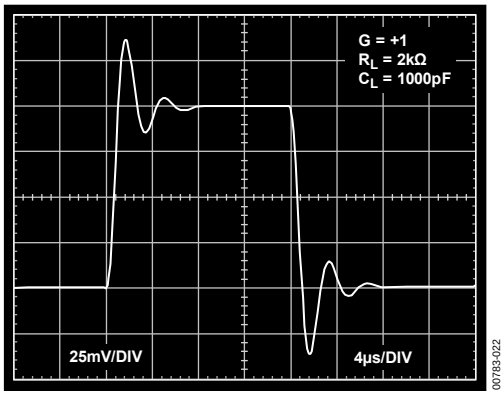


Figure 23. Small Signal Pulse Response

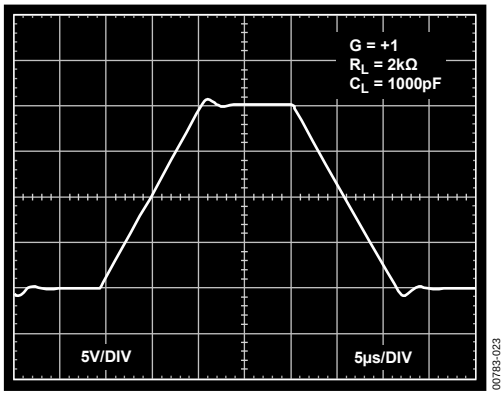


Figure 24. Large Signal Pulse Response

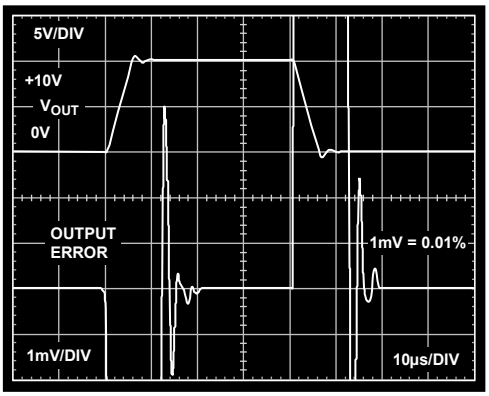


Figure 25. Settling Time to 0.01%, for 0 V to 10 V Output Step; G = −1, R_L = 2 kΩ

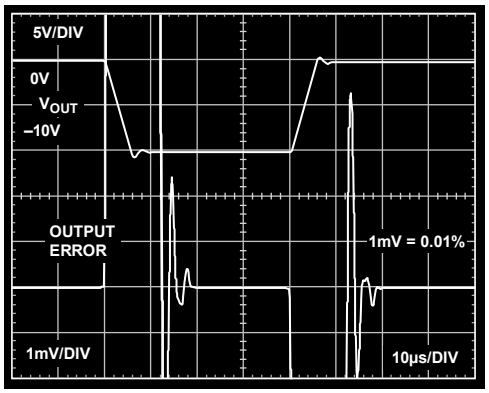


Figure 28. Settling Time to 0.01% for 0 V to −10 V Output Step; G = −1, R_L = 2kΩ

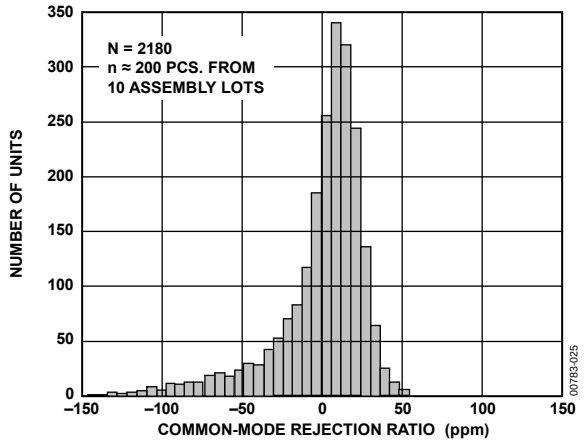


Figure 26. Typical Distribution of Common-Mode Rejection; Package Option N-8

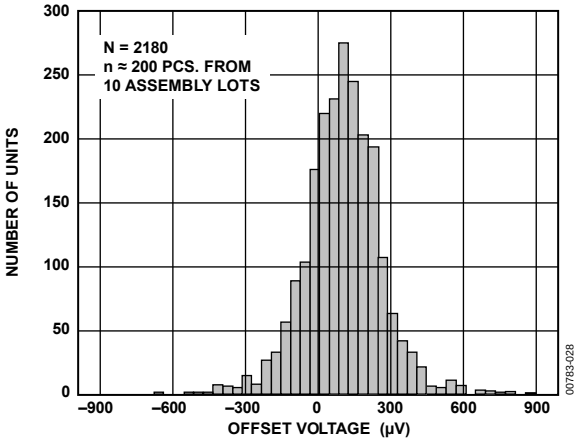


Figure 29. Typical Distribution of Offset Voltage; Package Option N-8

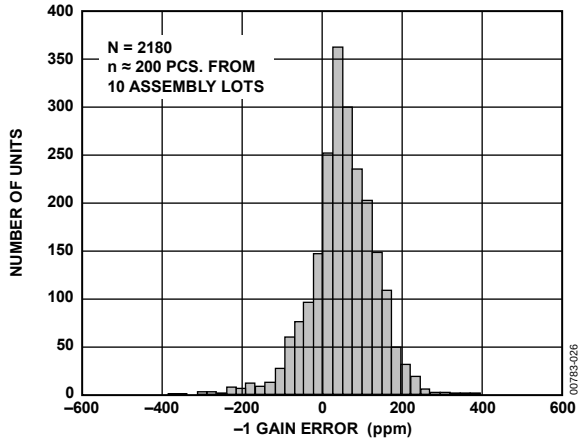


Figure 27. Typical Distribution of −1 Gain Error; Package Option N-8

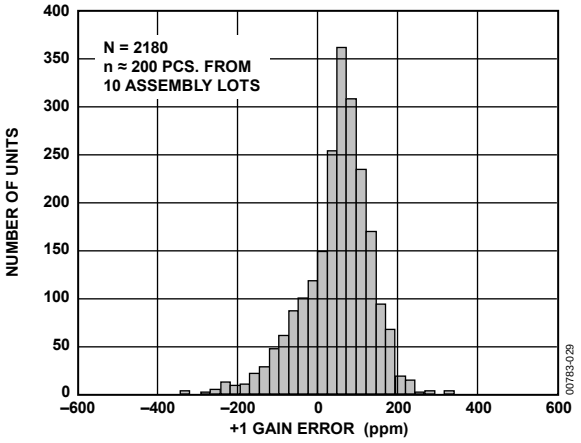


Figure 30. Typical Distribution of +1 Gain Error; Package Option N-8

THEORY OF OPERATION

The AD629 is a unity gain, differential-to-single-ended amplifier (diff amp) that can reject extremely high common-mode signals (in excess of 270 V with 15 V supplies). It consists of an operational amplifier (op amp) and a resistor network.

To achieve high common-mode voltage range, an internal resistor divider (Pin 3 or Pin 5) attenuates the noninverting signal by a factor of 20. Other internal resistors (Pin 1, Pin 2, and the feedback resistor) restore the gain to provide a differential gain of unity. The complete transfer function equals

$$V_{OUT} = \text{V}\,(+IN) - \text{V}\,(-IN)$$

Laser wafer trimming provides resistor matching so that common-mode signals are rejected while differential input signals are amplified.

To reduce output drift, the op amp uses super beta transistors in its input stage. The input offset current and its associated temperature coefficient contribute no appreciable output voltage offset or drift, which has the added benefit of reducing voltage noise because the corner where 1/f noise becomes dominant is below 5 Hz. To reduce the dependence of gain accuracy on the op amp, the open-loop voltage gain of the op amp exceeds 20 million, and the PSRR exceeds 140 dB.

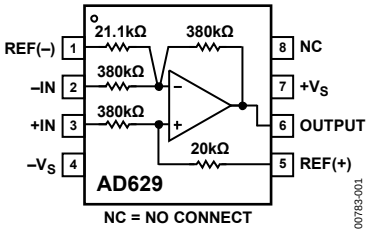


Figure 31. Functional Block Diagram

APPLICATIONS

BASIC CONNECTIONS

Figure 32 shows the basic connections for operating the AD629 with a dual supply. A supply voltage of between ±3 V and ±18 V is applied between Pin 7 and Pin 4. Both supplies should be decoupled close to the pins using 0.1 μF capacitors. Electrolytic capacitors of 10 μF, also located close to the supply pins, may be required if low frequency noise is present on the power supply. While multiple amplifiers can be decoupled by a single set of 10 μF capacitors, each in amp should have its own set of 0.1 μF capacitors so that the decoupling point can be located right at the IC's power pins.

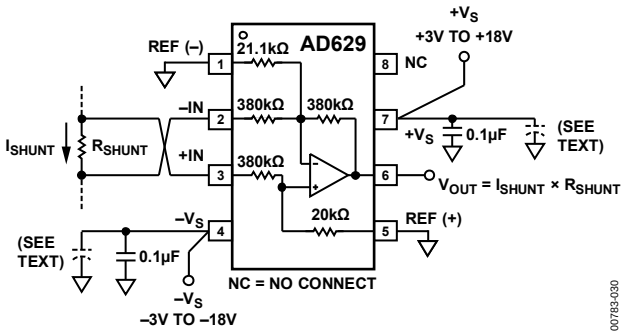


Figure 32. Basic Connections

The differential input signal, which typically results from a load current flowing through a small shunt resistor, is applied to Pin 2 and Pin 3 with the polarity shown to obtain a positive gain. The common-mode range on the differential input signal can range from −270 V to +270 V, and the maximum differential range is ±13 V. When configured as shown in Figure 32, the device operates as a simple gain-of-1, differential-to-single-ended amplifier; the output voltage being the shunt resistance times the shunt current. The output is measured with respect to Pin 1 and Pin 5.

Pin 1 and Pin 5 (REF(–) and REF(+)) should be grounded for a gain of unity and should be connected to the same low impedance ground plane. Failure to do this results in degraded common-mode rejection. Pin 8 is a no connect pin and should be left open.

SINGLE-SUPPLY OPERATION

Figure 33 shows the connections for operating the AD629 with a single supply. Because the output can swing to within only about 2 V of either rail, it is necessary to apply an offset to the output. This can be conveniently done by connecting REF(+) and REF(–) to a low impedance reference voltage (some ADCs provide this voltage as an output), which is capable of sinking current. Therefore, for a single supply of 10 V, V_{REF} may be set to 5 V for a bipolar input signal. This allows the output to swing ±3 V around the central 5 V reference voltage. Alternatively, for unipolar input signals, V_{REF} can be set to about 2 V, allowing the output to swing from 2 V (for a 0 V input) to within 2 V of the positive rail.

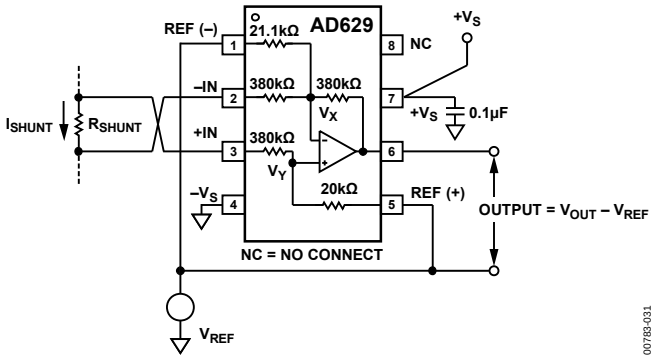


Figure 33. Operation with a Single Supply

Applying a reference voltage to REF(+) and REF(–) and operating on a single supply reduces the input common-mode range of the AD629. The new input common-mode range depends upon the voltage at the inverting and noninverting inputs of the internal operational amplifier, labeled V_X and V_Y in Figure 33. These nodes can swing to within 1 V of either rail. Therefore, for a (single) supply voltage of 10 V, V_X and V_Y can range between 1 V and 9 V. If V_{REF} is set to 5 V, the permissible common-mode range is +85 V to −75 V. The common-mode voltage ranges can be calculated by

$$V_{CM}(\pm) = 20\ V_X/V_Y(\pm) - 19\ V_{REF}$$

SYSTEM-LEVEL DECOUPLING AND GROUNDING

The use of ground planes is recommended to minimize the impedance of ground returns (and therefore the size of dc errors). Figure 34 shows how to work with grounding in a mixed-signal environment, that is, with digital and analog signals present. To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns. All ground pins from mixed-signal components, such as ADCs, should return through a low impedance analog ground plane. Digital ground lines of mixed-signal converters should also be connected to the analog ground plane. Typically, analog and digital grounds should be separated; however, it is also a requirement to minimize the voltage difference between digital and analog grounds on a converter, to keep them as small as possible (typically <0.3 V). The increased noise, caused by the converter's digital return currents flowing through the analog ground plane, is typically negligible. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. Note that Figure 34 suggests a "star" ground system for the analog circuitry, with all ground lines being connected, in this case, to the ADC's analog ground. However, when ground planes are used, it is sufficient to connect ground pins to the nearest point on the low impedance ground plane.

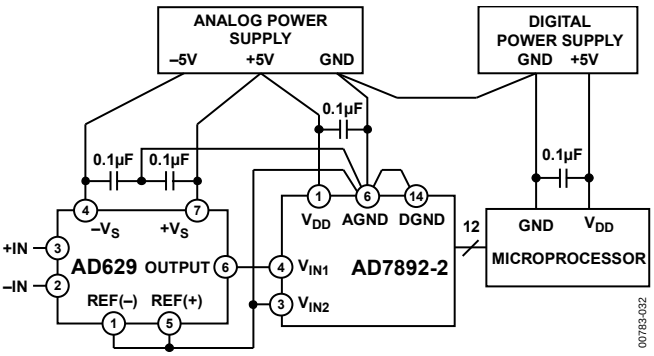


Figure 34. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

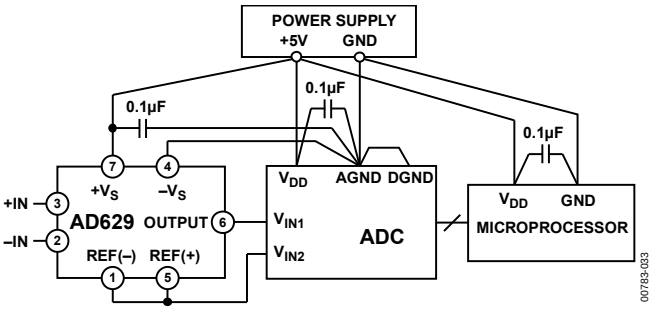


Figure 35. Optimal Ground Practice in a Single-Supply Environment

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 35 shows how to minimize interference between the digital and analog circuitry. In this example, the ADC's reference is used to drive Pin REF(+) and Pin REF(–). This means that the reference must be capable of sourcing and sinking a current equal to $V_{CM}/200\ k\Omega$. As in the previous case, separate analog and digital ground planes should be used (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should connect at the power supply's ground pin. Separate traces (or power planes) should run from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but these can be shared by a number of devices, as long as a single trace is not used to route current to both digital and analog circuitry.

USING A LARGE SENSE RESISTOR

Insertion of a large value shunt resistance across the input pins, Pin 2 and Pin 3, will imbalance the input resistor network, introducing a common-mode error. The magnitude of the error will depend on the common-mode voltage and the magnitude of R_{SHUNT}.

Table 5 shows some sample error voltages generated by a common-mode voltage of 200 V dc with shunt resistors from 20 Ω to 2000 Ω. Assuming that the shunt resistor is selected to use the full ±10 V output swing of the AD629, the error voltage becomes quite significant as R_{SHUNT} increases.

Table 5. Error Resulting from Large Values of R_{SHUNT} (Uncompensated Circuit)

R_S (Ω)	Error V_{OUT} (V)	Error Indicated (mA)
20	0.01	0.5
1000	0.498	0.498
2000	1	0.5

To measure low current or current near zero in a high common-mode environment, an external resistor equal to the shunt resistor value can be added to the low impedance side of the shunt resistor, as shown in Figure 36.

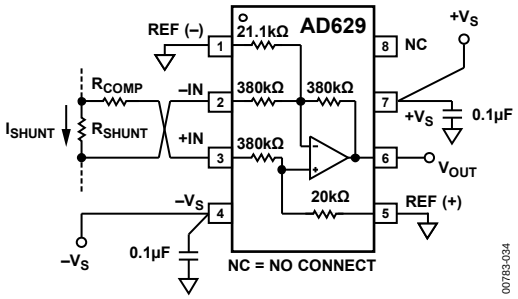


Figure 36. Compensating for Large Sense Resistors

OUTPUT FILTERING

A simple 2-pole, low-pass Butterworth filter can be implemented using the OP177 after the AD629 to limit noise at the output, as shown in Figure 37. Table 6 gives recommended component values for various corner frequencies, along with the peak-to-peak output noise for each case.

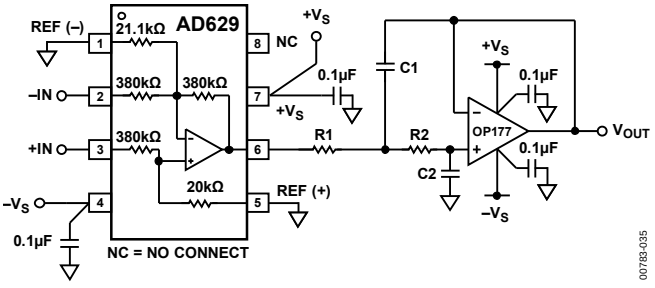


Figure 37. Filtering of Output Noise Using a 2-Pole Butterworth Filter

Table 6. Recommended Values for 2-Pole Butterworth Filter

Corner Frequency	R1	R2	C1	C2	Output Noise (p-p)
No Filter					3.2 mV
50 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	2.2 nF ± 10%	1 nF ± 10%	1 mV
5 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	22 nF ± 10%	10 nF ± 10%	0.32 mV
500 Hz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	220 nF ± 10%	0.1 µF ± 10%	100 µV
50 Hz	2.7 kΩ ± 10%	1.5 kΩ ± 10%	2.2 µF ± 20%	1 µF ± 20%	32 µV

OUTPUT CURRENT AND BUFFERING

The AD629 is designed to drive loads of 2 kΩ to within 2 V of the rails but can deliver higher output currents at lower output voltages (see Figure 17). If higher output current is required, the output of the AD629 should be buffered with a precision op amp, such as the OP113, as shown in Figure 38. This op amp can swing to within 1 V of either rail while driving a load as small as 600 Ω.

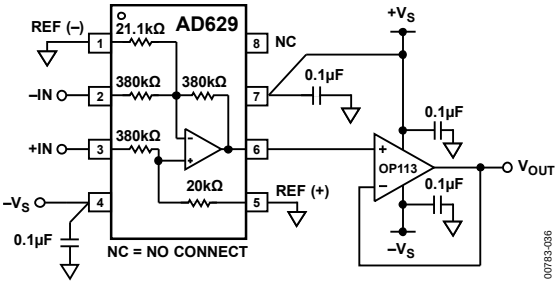


Figure 38. Output Buffering Application

A GAIN OF 19 DIFFERENTIAL AMPLIFIER

While low level signals can be connected directly to the –IN and +IN inputs of the AD629, differential input signals can also be connected, as shown in Figure 39, to give a precise gain of 19. However, large common-mode voltages are no longer permissible. Cold junction compensation can be implemented using a temperature sensor, such as the AD590.

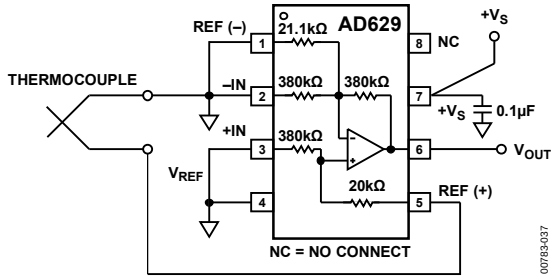


Figure 39. A Gain of 19 Thermocouple Amplifier

ERROR BUDGET ANALYSIS EXAMPLE 1

In the dc application that follows, the 10 A output current from a device with a high common-mode voltage (such as a power supply or current-mode amplifier) is sensed across a 1 Ω shunt resistor (see Figure 40). The common-mode voltage is 200 V, and the resistor terminals are connected through a long pair of lead wires located in a high noise environment, for example, 50 Hz/60 Hz, 440 V ac power lines. The calculations in Table 7 assume an induced noise level of 1 V at 60 Hz on the leads, in addition to a full-scale dc differential voltage of 10 V. The error budget table quantifies the contribution of each error source. Note that the dominant error source in this example is due to the dc common-mode voltage.

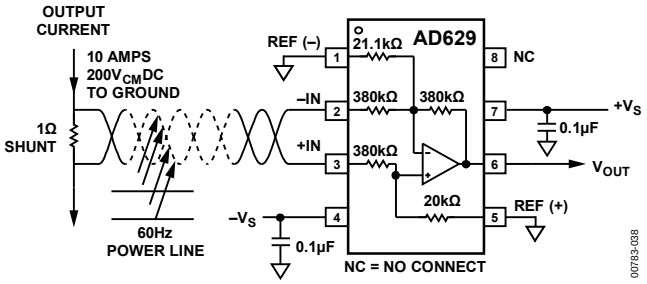


Figure 40. Error Budget Analysis Example 1: V_{IN} = 10 V Full-Scale, V_{CM} = 200 V DC, R_{SHUNT} = 1 Ω, 1 V p-p, 60 Hz Power-Line Interference

Table 7. AD629 vs. INA117 Error Budget Analysis Example 1 (V_{CM} = 200 V dc)

Error Source	AD629	INA117	Error, ppm of FS	
			AD629	INA117
ACCURACY, T_A = 25°C				
Initial Gain Error	(0.0005 × 10)/10 V × 10^6	(0.0005 × 10)/10 V × 10^6	500	500
Offset Voltage	(0.001 V/10 V) × 10^6	(0.002 V/10 V) × 10^6	100	200
DC CMR (Over Temperature)	(224 × 10^{-6} × 200 V)/10 V × 10^6	(500 × 10^{-6} × 200 V)/10 V × 10^6	4480	10,000
		Total Accuracy Error	5080	10,700
TEMPERATURE DRIFT (85°C)				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset Voltage	(20 µV/°C × 60°C) × 10^6/10 V	(40 µV/°C × 60°C) × 10^6/10 V	120	240
		Total Drift Error	720	840
RESOLUTION				
Noise, Typical, 0.01 Hz to 10 Hz, µV p-p	15 µV/10 V × 10^6	25 µV/10 V × 10^6	2	3
CMR, 60 Hz	(141 × 10^{-6} × 1 V)/10 V × 10^6	(500 × 10^{-6} × 1 V)/10 V × 10^6	14	50
Nonlinearity	(10^{-5} × 10 V)/10 V × 10^6	(10^{-5} × 10 V)/10 V × 10^6	10	10
		Total Resolution Error	26	63
		Total Error	5826	11,603

ERROR BUDGET ANALYSIS EXAMPLE 2

This application is similar to the previous example except that the sensed load current is from an amplifier with an ac common-mode component of ±100 V (frequency = 500 Hz) present on the shunt (see Figure 41). All other conditions are the same as before. Note that the same kind of power-line interference can happen as detailed in Example 1. However, the ac common-mode component of 200 V p-p coming from the shunt is much larger than the interference of 1 V p-p; therefore, this interference component can be neglected.

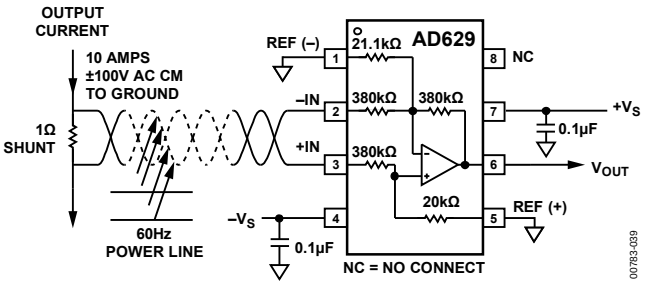
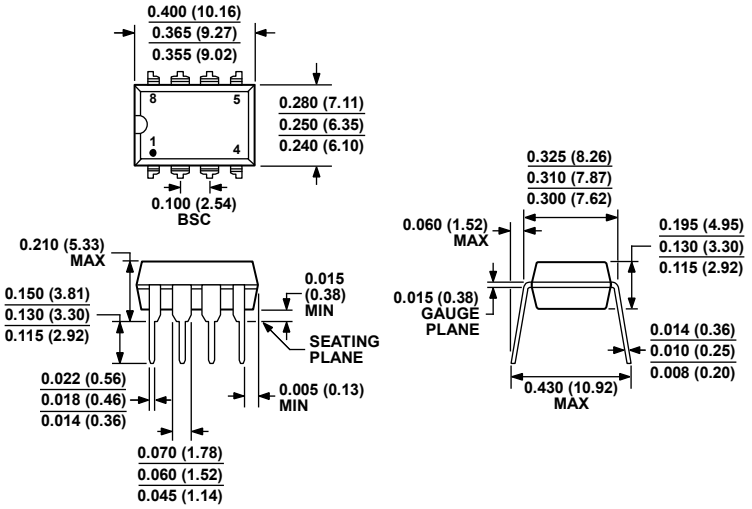


Figure 41. Error Budget Analysis Example 2: V_{IN} = 10 V Full-Scale, V_{CM} = ±100 V at 500 Hz, R_{SHUNT} = 1 Ω

Table 8. AD629 vs. INA117 AC Error Budget Example 2 (V_{CM} = ±100 V @ 500 Hz)

			Error, ppm of FS	
Error Source	**AD629**	**INA117**	**AD629**	**INA117**
ACCURACY, T_A = 25°C				
Initial Gain Error	(0.0005 × 10)/10 V × 10^6	(0.0005 × 10)/10 V × 10^6	500	500
Offset Voltage	(0.001 V/10 V) × 10^6	(0.002 V/10 V) × 10^6	100	200
		Total Accuracy Error	600	700
TEMPERATURE DRIFT (85°C)				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset Voltage	(20 µV/°C × 60°C) × 10^6/10 V	(40 µV/°C × 60°C) × 10^6/10 V	120	240
		Total Drift Error	720	840
RESOLUTION				
Noise, Typical, 0.01 Hz to 10 Hz, µV p-p	15 µV/10 V × 10^6	25 µV/10 V × 10^6	2	3
CMR, 60 Hz	(141 × 10^{-6} × 1 V)/10 V × 10^6	(500 × 10^{-6} × 1 V)/10 V × 10^6	14	50
Nonlinearity	(10^{-5} × 10 V)/10 V × 10^6	(10^{-5} × 10 V)/10 V × 10^6	10	10
AC CMR @ 500 Hz	(141 × 10^{-6} × 200 V)/10 V × 10^6	(500 × 10^{-6} × 200 V)/10 V × 10^6	2820	10,000
		Total Resolution Error	2846	10,063
		Total Error	4166	11,603

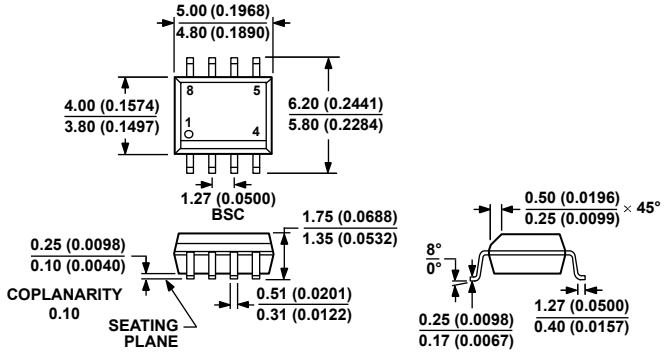
OUTLINE DIMENSIONS



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CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 42. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD629AN	−40°C to +85°C	8-Lead PDIP	N-8
AD629ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD629AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629ARZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13-Inch Tape and Reel, 2,500 pieces	R-8
AD629ARZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7-Inch Tape and Reel, 1,000 pieces	R-8
AD629BNZ	−40°C to +85°C	8-Lead PDIP	N-8
AD629BR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629BR-REEL	−40°C to +85°C	8-Lead SOIC_N, 13-Inch Tape and Reel, 2,500 pieces	R-8
AD629BR-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7-Inch Tape and Reel, 1,000 pieces	R-8
AD629BRZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD629BRZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13-Inch Tape and Reel, 2,500 pieces	R-8
AD629BRZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7-Inch Tape and Reel, 1,000 pieces	R-8
AD629AC-WP	−40°C to +85°C	Die	

[1] Z = RoHS Compliant Part.

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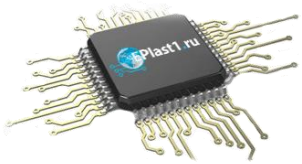
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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.