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S1R72U16
Data Sheet

SEIKO EPSON CORPORATION

Rev.2.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

Notice

Before using the S1R72U16, carefully read the sections “Special use case for S1R72U16” and “S1R72U16 Errata.”

Table of Contents

1. Overview

The S1R72U16 is an IDE device - USB 2.0 host bridge LSI that supports USB2.0-compliant high-speed mode. The main CPU is capable of controlling USB storage devices connected to this LSI as IDE devices. No USB driver is required. USB devices that can be connected to this LSI are bulk-only transport mass storage class devices (e.g., USB memory) and HUB devices.

2. Features

■ **Easy use/connect (IDE bus connection)**

Allows USB devices to be controlled as IDE devices

The main CPU is capable of controlling USB storage devices connected to this LSI as IDE devices. This LSI handles connection processing for the USB hub, no USB driver is required at the main CPU. An ATA/ATAPI driver should be installed at the main CPU.

A main CPU with an installed ATA/ATAPI driver is capable of controlling USB storage devices via this LSI.

■ **Easy use/connect (CPU bus connection)**

Also permits CPU bus connections (interface voltage: 1.8 V to 3.3 V)

The LSI can also be connected to a memory bus to connect to the main CPU without an IDE bus. An ATA/ATAPI driver should be installed in the main CPU. The registers used to control this LSI are ATA task file registers.

■ **High-speed transfer**

Transfer rate 31 MB/s (Seiko Epson figures)

Transfer rates of up to 31 MB/s can be achieved with ATA100 and USB High-Speed connection.

■ **Embedded Host silicon authentication**

High-quality USB signal

This LSI includes an Embedded Host function (including authentication software) for silicon authentication. The *S1R72U16 USB 2.0 PCB Design Guide* and *S1R72U16 Embedded Host Compliance Manual* are also provided to help the user obtain USB logo certification.

■ **Product (system) development support functions**

History display

LSI internal processing history can be displayed using the serial (asynchronous) interface. The *S1R72U16 Development Support Manual* provides detailed information on this function. This function and the manual provide support for product (system) development.

■ **Manuals and tools**

Development manuals and tools (bridge board)

The following manuals are provided in addition to this data sheet:

- *S1R72U16 Technical Manual*
- *S1R72U16 Application Note*
- *S1R72U16 Development Support Manual*
- *S1R72U16 USB 2.0 PCB Design Guide*
- *S1R72U16 Embedded Host Compliance Manual*

- *S1R72U16 Evaluation Board Manual*

An IDE device - USB 2.0 host bridge board is also provided for system evaluations in the early stages of product (system) development. *

* Please contact your nearest Seiko Epson sales office to obtain the IDE device - USB 2.0 host bridge board.

3. Block Diagram

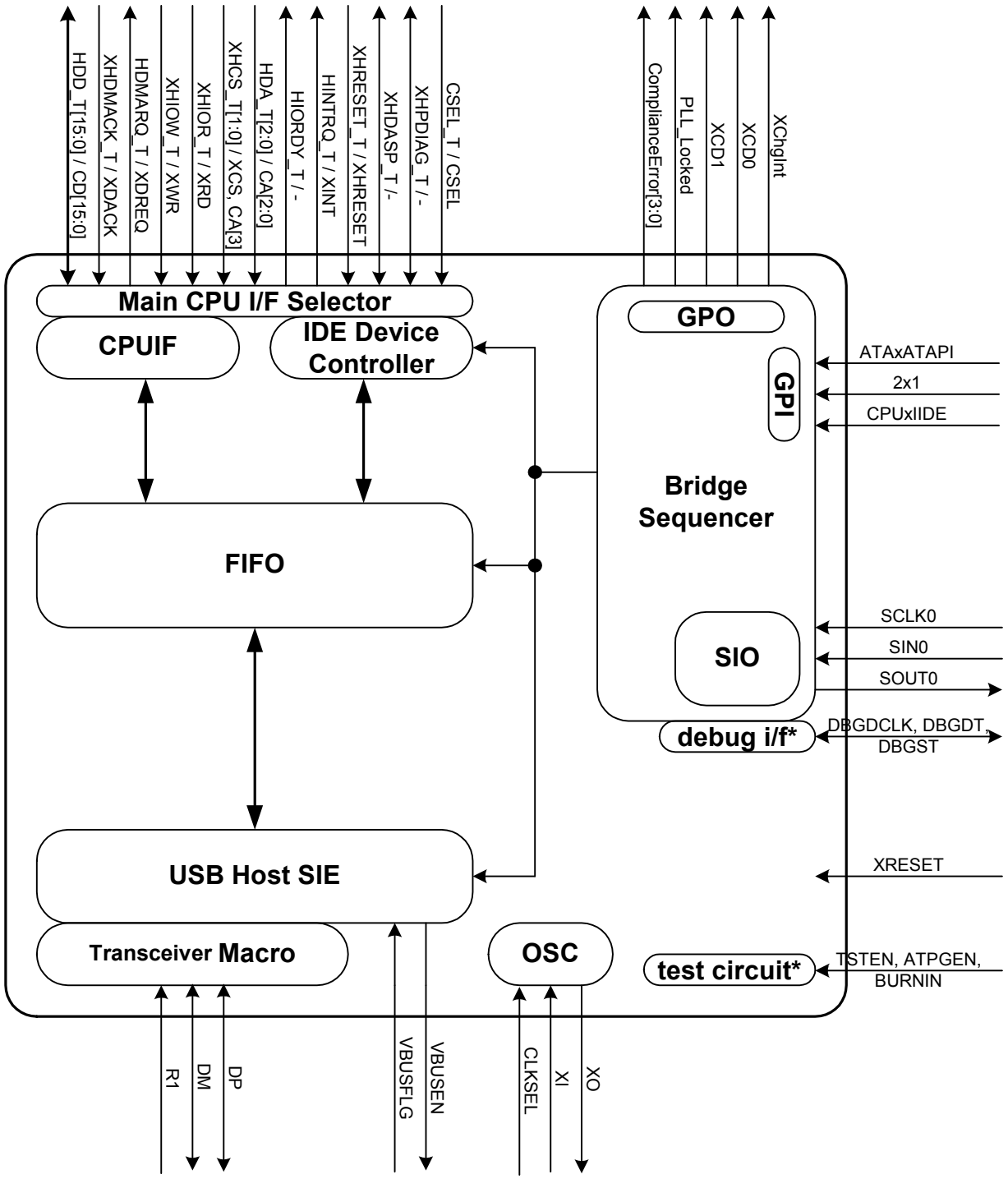


Figure 3.1 Block diagram

* Fix the debug I/F and test circuit pins strictly as described in "6. Pin Functions". They are not intended for use by users.

4. Functions

4.1 Main CPU I/F

This LSI can be used as either of the following connections to the main CPU.

- IDE bus connection (interface voltage: 3.3 V)
- CPU bus connection (interface voltage: 1.8 V to 3.3 V)

Bus connection is selected by using the mode setting pin CPUxIDE (PORT02).

4.1.1 IDE Device Controller

This block operates when IDE bus connection is selected. It supports ATA/ATAPI-6.

- PIO transfer modes 0 to 4
- Multi Word DMA transfer modes 0 to 2
- Ultra DMA transfer modes 0 to 5

4.1.2 CPUIF

This block operates when CPU bus connection is selected. The registers used to control this LSI are ATA task file registers. It supports PIO and DMA (*) transfer.

* For DMA transfer, the main CPU must provide a DMA master function that complies with the DMA specifications of this LSI.

4.2 USB Host

The USB host function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards. It supports HS (480 Mbps) and FS (12 Mbps) speed modes. USB host function is controlled by the Bridge Sequencer block inside the LSI. USB devices that can be connected to this LSI are bulk-only transport mass storage class devices (e.g., USB memory) and HUB devices.

4.3 GPI

These are the mode setting pins for selecting the command system, number of connected devices, and interface to the main CPU.

For detailed information, see the *S1R72U16 Technical Manual*.

4.4 GPO

These pins are used to issue notification of USB storage device connections, internal PLL operation status, and NSF (No Silent Failure).

For detailed information, see the *S1R72U16 Technical Manual*.

4.5 SIO

This block is used to display the product (system) development support function history.

For detailed information, see the *S1R72U16 Development Support Manual*.

4.6 OSC

This oscillator circuit supports a 12 MHz/24 MHz crystal oscillator. The 12 MHz or 24 MHz clock is selected using the CLKSEL pin.

5. Pin Layout Diagram

S1R72U16/PFBGA8UX81
Top View

	1	2	3	4	5	6	7	8	9	
A	TSTEN	ATPGEN	XO	XI	HDD3_T	IOVDD	HDD8_T	HDD10_T	NC	A
B	LVDD	VSS	LVDD	HDD0_T	HDD4_T	HDD6_T	HDD9_T	HDD11_T	LVDD	B
C	R1	VSS	CLKSEL	HDD1_T	HDD5_T	HDD7_T	HDD12_T	HDD13_T	HDD14_T	C
D	HVDD	BURNIN	VSS	HDD2_T	HDA0_T	HDA1_T	HDD15_T	HDA2_T	VSS	D
E	DM	VSS	VSS	PORT00	PORT01	XHCS1_T	XHCS0_T	XHDASP_T	XHRESET_T	E
F	DP	HVDD	VBUSFLG	PORT02	HINTRQ_T	PORT11	XHPDIAG_T	PORT17	CSEL_T	F
G	LVDD	VSS	VBUSEN	XRESET	XHIOW_T	PORT10	PORT13	PORT15	PORT16	G
H	DBGDCLK	DBGDT	DBGST	SIN0	HDMARQ_T	HIORDY_T	PORT12	PORT14	IOVDD	H
J	NC	HVDD	SOUT0	SCLK0	XHDMACK_T	XHIOR_T	VSS	LVDD	NC	J
	1	2	3	4	5	6	7	8	9	

Figure 5.1 PFBGA8UX81 package pin layout diagram (*)

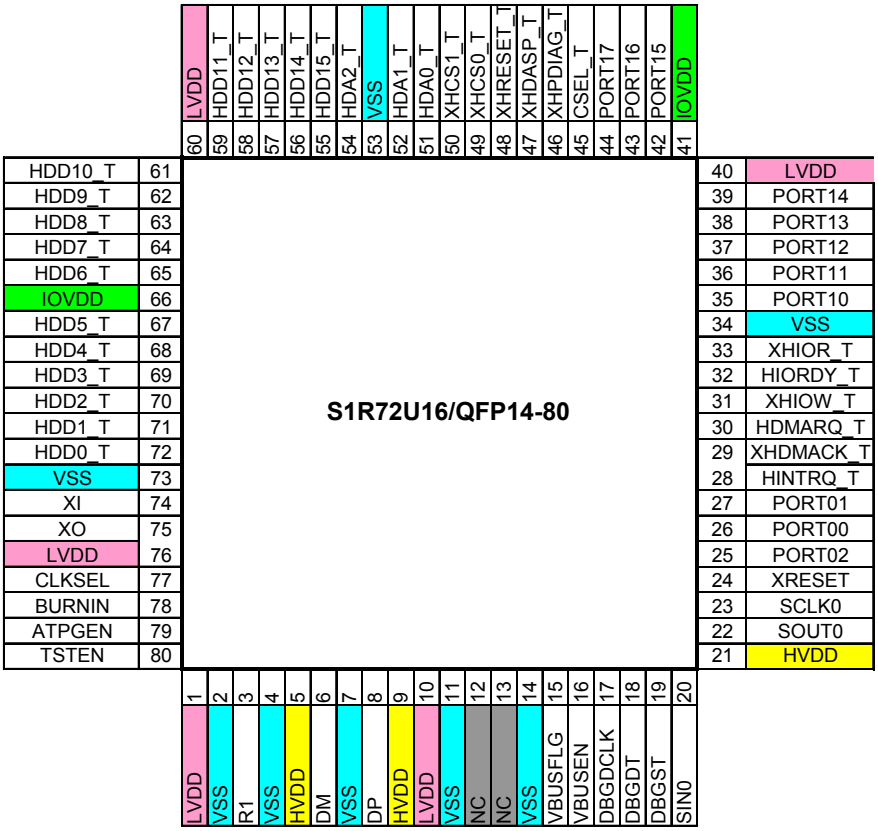


Figure 5.2 QFP14-80 package pin layout diagram (*)

* Shown here with pin names for IDE mode connection.

6. Pin Functions

6.1 IDE Mode

GENERAL (IOVDD system)

BGA	QFP	Name	I/O	RESET	Details
G4	24	XRESET	IN	-	Reset signal
C3	77	CLKSEL	IN		XI clock input selection 1: 24MHz 0: 12MHz

OSC (LVDD system)

BGA	QFP	Name	I/O	RESET	Details
A4	74	XI	IN	-	Internal oscillator circuit input 12MHz/24MHz
A3	75	XO	OUT	-	Internal oscillator circuit output

TEST (LVDD system)

BGA	QFP	Name	I/O	RESET	Details
A1	80	TSTEN	IN(PD)	-	Test pin (*)
A2	79	ATPGEN	IN(PD)	-	Test pin (*)
D2	78	BURNIN	IN(PD)	-	Test pin (*)

PD: Using pull-down I/O

* The LSI features internal pull-down, but low fixing is recommended on the circuit board.

USB

BGA	QFP	Name	I/O	RESET	Details
C1	3	R1	IN	-	Reference voltage setting pin Connect 6.2 kΩ ±1% resistor between VSS.
F1	8	DP	BI	Hi-Z	USB data line Data+
E1	6	DM	BI	Hi-Z	USB data line Data-
F3	15	VBUSFLG	IN(PU)	-	USB power switch fault detection signal 1: Normal, 0: Error CMOS Schmitt input
G3	16	VBUSEN	OUT	Low	USB power switch control signal

PU: Using pull-up I/O

IDE device I/F (IOVDD system)

BGA	QFP	Name	I/O	RESET	Details
D8	54	HDA2_T	IN	-	IDE register address
D6	52	HDA1_T	IN	-	
D5	51	HDA0_T	IN	-	
E6	50	XHCS1_T	IN	-	Control register access chip selection
E7	49	XHCS0_T	IN	-	Command block register access chip selection
J6	33	XHIOR_T	IN	-	IDE read strobe
G5	31	XHIOW_T	IN	-	IDE write strobe
H5	30	HDMARQ_T	OUT	Low	DMA transfer request
J5	29	XHDMACK_T	IN	-	DMA transfer acknowledge
H6	32	HIORDY_T	OUT (PU)	Hi-z	IDE register ready signal (*)
F5	28	HINTRQ_T	OUT	Low	IDE interrupt request
E9	48	XHRESET_T	IN	-	IDE bus reset
E8	47	XHDASP_T	BI(PU)	Hi-z	Drive enable/slave drive present (*)
F7	46	XHPDIAG_T	BI(PU)	Hi-z	**Diagnosis sequence end signal (*)**
F9	45	CSEL_T	IN	-	**Drive selection**
D7	55	HDD15_T	BI	Hi-Z	IDE data bus
C9	56	HDD14_T	BI	Hi-Z	
C8	57	HDD13_T	BI	Hi-Z	
C7	58	HDD12_T	BI	Hi-Z	
B8	59	HDD11_T	BI	Hi-Z	
A8	61	HDD10_T	BI	Hi-Z	
B7	62	HDD9_T	BI	Hi-Z	
A7	63	HDD8_T	BI	Hi-Z	
C6	64	HDD7_T	BI	Hi-Z	
B6	65	HDD6_T	BI	Hi-Z	
C5	67	HDD5_T	BI	Hi-Z	
B5	68	HDD4_T	BI	Hi-Z	
A5	69	HDD3_T	BI	Hi-Z	
D4	70	HDD2_T	BI	Hi-Z	
C4	71	HDD1_T	BI	Hi-Z	
B4	72	HDD0_T	BI	Hi-Z	

PU: Using pull-up I/O

* LSI internal pull-up is disabled in IDE mode.

Serial I/F (HVDD system)

BGA	QFP	Name	I/O	RESET	Details
J4	23	SCLK0	I(PU)		Not used (*)
H4	20	SIN0	I(PU)	-	Asynchronous serial data in
J3	22	SOUT0	O	High	Asynchronous serial data out

PU: Using pull-up I/O

* Set to open or pull-up.

DEBUG I/F (HVDD system)

BGA	QFP	Name	I/O	RESET	Details
H1	17	DBGDCLK	O	High	Not used (*1)
H2	18	DBGDT	BI(PU)	-	Not used (*2)
H3	19	DBGST	O	Low	Not used (*1)

PU: Using pull-up I/O

*1: Set to open or pull-up.

*2: The LSI features internal pull-up, but an external pull-up of approximately 10 kΩ is recommended.

GPIO (IOVDD system)

BGA	QFP	Name	I/O	RESET	Details
E4	26	PORT00 (ATAxATAPI)	I	-	Setting pin 1: ATA mode, 0: ATAPI mode
E5	27	PORT01 (2x1)	I	-	Setting pin 1: two-device mode, 0: one-device mode
F4	25	PORT02 (CPUxIDE)	I	-	Setting pin 1: CPU mode, 0: IDE mode
G6	35	PORT10 (XChgInt)	O	-	Storage device connection detection interrupt 1: -, 0: Connection detection
F6	36	PORT11 (XCD0)	O	-	Storage device 0 detection 1: -, 0: Detect
H7	37	PORT12 (XCD1)	O	-	Storage device 1 detection 1: -, 0: Detect
G7	38	PORT13 (PLL_Locked)	O	-	PLL oscillation start 1: Oscillation start, 0: No oscillation
H8	39	PORT14 (ComplianceErr0)	O	-	Unsupported Device 1: Error, 0: -
G8	42	PORT15 (ComplianceErr1)	O	-	Too Many Devices 1: Error, 0: -
G9	43	PORT16 (ComplianceErr2)	O	-	Too Many Hubs 1: Error, 0: -
F8	44	PORT17 (ComplianceErr3)	O	-	VBUS Over Current 1: Error, 0: -

POWER

BGA	QFP	Name	Voltage	Details
D1, F2, J2	5, 9, 21	HVDD	3.3V	USB, UART, DEBUG I/F power supply
A6, H9	41, 66	IOVDD	3.3V to 1.8V	IDE I/F and GPIO power supply
B1, G1, B3, J8, B9	1, 10, 40, 60, 76	LVDD	1.8V	Internal power supply, TEST power supply, OSC power supply
B2, C2, E2, G2, D3, E3, J7, D9	2, 4, 7, 11, 14, 34, 53, 73	VSS	0V	GND

6.2 CPU Mode

CPU memory bus I/F (IOVDD system)

BGA	QFP	Name	I/O	RESET	Details
D8	54	CA2	IN	-	Address
D6	52	CA1	IN	-	
D5	51	CA0	IN	-	
E6	50	XCS	IN	-	Chip selection
E7	49	CA3	IN	-	Address
J6	33	XRD	IN	-	Read strobe
G5	31	XWR	IN	-	Write strobe
H5	30	XDREQ	OUT	High	DMA transfer request
J5	29	XDACK	IN	-	DMA transfer acknowledge
H6	32	-	OUT(PU)	Hi-z	Not used (*)
F5	28	XINT	OUT	High	Interrupt request
E9	48	XHRESET	IN	-	Bus reset
E8	47	-	BI(PU)	Hi-z	Not used (*)
F7	46	-	BI(PU)	Hi-z	Not used (*)
F9	45	CSEL	IN	-	Drive selection
D7	55	CD15	BI	Hi-Z	Data bus
C9	56	CD14	BI	Hi-Z	
C8	57	CD13	BI	Hi-Z	
C7	58	CD12	BI	Hi-Z	
B8	59	CD11	BI	Hi-Z	
A8	61	CD10	BI	Hi-Z	
B7	62	CD9	BI	Hi-Z	
A7	63	CD8	BI	Hi-Z	
C6	64	CD7	BI	Hi-Z	
B6	65	CD6	BI	Hi-Z	
C5	67	CD5	BI	Hi-Z	
B5	68	CD4	BI	Hi-Z	
A5	69	CD3	BI	Hi-Z	
D4	70	CD2	BI	Hi-Z	
C4	71	CD1	BI	Hi-Z	
B4	72	CD0	BI	Hi-Z	

PU: Using pull-up I/O

* Set to open or pull-up. LSI internal pull-up resistor is enabled in CPU mode.

For detailed information on pins other than those described above, see “6.1 IDE Mode”.

7. Register

7.1 Register Map

7.1.1 IDE Mode Register Map

Pin					Register	
XHCS1_T	XHCS0_T	HDA2_T	HDA1_T	HDA0_T	Read	Write
H	L	L	L	L	Data (16bit)	
H	L	L	L	H	Error	Feature
H	L	L	H	L	Sector Count	
H	L	L	H	H	LBA Low	
H	L	H	L	L	LBA Mid	
H	L	H	L	H	LBA High	
H	L	H	H	L	Device	
H	L	H	H	H	Status	Command
L	H	L	L	L	none	
L	H	L	L	H	none	
L	H	L	H	L	none	
L	H	L	H	H	none	
L	H	H	L	L	none	
L	H	H	L	H	none	
L	H	H	H	L	Alternate Status	Device Control
L	H	H	H	H	none	

Figure 7.1 IDE mode register map

7.1.2 CPU Mode Register Map

Pin					Register	
XCS	CA3	CA2	CA1	CA0	Read	Write
L	L	L	L	L	Data (16bit)	
L	L	L	L	H	Error	Feature
L	L	L	H	L	Sector Count	
L	L	L	H	H	LBA Low	
L	L	H	L	L	LBA Mid	
L	L	H	L	H	LBA High	
L	L	H	H	L	Device	
L	L	H	H	H	Status	Command
L	H	L	L	L	none	
L	H	L	L	H	none	
L	H	L	H	L	none	
L	H	L	H	H	none	
L	H	H	L	L	none	
L	H	H	L	H	none	
L	H	H	H	L	Alternate Status	Device Control
L	H	H	H	H	none	

Figure 7.2 CPU mode register map

7.2 Registers

These are ATA task file registers. For detailed information, see *AT Attachment with Packet Interface – 6 (ATA/ATAPI-6)*.

7.2.1 Data Register

This register permits reads/writes. It is used for data transfers. It supports 16-bit access only.

bit15	bit14	Bit13	bit12	bit11	bit10	bit9	bit8
Data[15:8]							

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Data[7:0]							

7.2.2 Error Register

This is a read-only register. The register value is enabled when the Status register ERR bit is "1". Bit assignments and values vary, depending on the ATA/ATAPI command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
#	#	#	#	#	ABRT	#	#

7.2.3 Feature Register

This is a write-only register. Writing to this register depends on the ATA/ATAPI command. Bit assignments and values are defined for each command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Features Byte							

7.2.4 Sector Count Register

This register permits reads/writes and sets the number of sectors for data transfers.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector Count Byte							

7.2.5 LBA Low Register

This register permits reads/writes and sets LBA [7:0].

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LBA Low Byte							

7.2.6 LBA Mid Register

This register permits reads/writes and sets LBA [15:8].

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LBA Mid Byte							

7.2.7 LBA High Register

This register permits reads/writes and sets LBA [23:16].

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LBA High Byte							

7.2.8 Device Register

This register permits reads/writes. Bit assignments and values vary, depending on the ATA/ATAPI command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolute	#	Obsolute	DEV	#	#	#	#

7.2.9 Status Register

This read-only register is updated to indicate status when a command is executed. Reading this register when the HINTRQ_T signal is asserted cause to nagate the HINTRQ_T signal.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DF	#	DRQ	Obsolute	ChgInt	ERR

Bit 1 ChgInt

This bit, unique to this LSI, indicates whether a USB storage device is connected (using the bit dropped as of *AT Attachment with Packet Interface – 6 (ATA/ATAPI-6)*). The XChgInt signal status can be read off inverted. For detailed information, see the *S1R72U16 Technical Manual*.

7.2.10 Command Register

This is a write-only register. The register command is executed immediately on being written. Issuing the command (writing to this register) when the HINTRQ_T signal is asserted cause to nagate the HINTRQ_T signal.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Command Code							

7.2.11 Alternate Status Register

This read-only register is the same as the Status Register except when the HINTRQ_T signal is not altered.

7.2.12 Device Control Register

This write-only register is used to reset the HINTRQ_T signal control and software and to support Big Drive.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HOB	#	#	#	#	SRST	nIEN	#

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

(V_{SS}=0V)

Item	Code	Rating	Units
Power supply voltage	HVDD	VSS-0.3 to 4.0	V
	IOVDD	VSS-0.3 to 4.0	V
	LVDD	VSS-0.3 to 2.5	V
Input voltage (*)	HVI	VSS-0.3 to HVDD+0.5	V
	IOVI	VSS-0.3 to IOVDD+0.5	V
	LVI	VSS-0.3 to LVDD+0.5	V
Output voltage (*)	HVO	VSS-0.3 to HVDD+0.5	V
	IOVO	VSS-0.3 to IOVDD+0.5	V
Output current/pin	IOUT	±10	mA
Storage temperature	Tstg	-65 to 150	°C

* Check the power supply system information in “6. Pin Functions” for the corresponding pins.

8.2 Recommended Operating Conditions

Item	Code	MIN	TYP	MAX	Units
Power supply voltage	HVDD	3.00	3.30	3.60	V
	IOVDD (*1)	1.65	1.80 to 3.30	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage (*2)	HVI	-0.3	-	HVDD+0.3	V
	IOVI	-0.3	-	IOVDD+0.3	V
	LVI	-0.3	-	LVDD+0.3	V
Ambient temperature	T_a	-40	25	85	°C

*1: Use with 3.3 V (typ) in IDE mode.

*2: Check the power supply system information in “6. Pin Functions” for the corresponding pins.

[Precautions for power-on sequence]

Power to the HVDD and IOVDD should be turned on/off with LVDD confirmed. (*)

- Power-on: LVDD → (HVDD, IOVDD)
- Power-off: (HVDD, IOVDD) → LVDD

* Reliability issues may arise if LVDD is cut off and HVDD or IOVDD or both are on continuously for 1 second or longer.

8.3 DC Characteristics

8.3.1 Current Consumption

Item		Code	Conditions	MIN	TYP	MAX	Units
Power supply current (*)							
	Power current	IDDH	HVDD = 3.6V	-	17.0		mA
		IDDCH	IOVDD = 3.6V	-	2.0		mA
		IDDCL	IOVDD = 1.95V	-	1.5		mA
		IDDL	LVDD = 1.95V	-	65.0		mA
Static current							
	Power current	IDDS	VIN = HVDD,IOVDD,LVDD or VSS	-	-	70	μA
			HVDD = 3.6V				
			IOVDD = 3.6V				
			LVDD = 1.95V				
Input leak							
	Input leak current	IL	HVDD = 3.6V IOVDD = 3.6V LVDD = 1.95V HVIH = HVDD IOVIH = IOVDD LVIH = LVDD	-5	-	5	μA

* Mean operating current at recommended operating conditions (Ta = 25°C)

8.3.2 Input Characteristics

Item	Code	Conditions	MIN	TYP	MAX	Units
Input characteristics	Pin:	TSTEN, ATPGEN, BURNIN, XI				
"H" level input voltage	VIH1	LVDD = 1.95V	1.27	-	-	V
"L" level input voltage	VIL1	LVDD = 1.65V	-	-	0.57	V
Input characteristics	Pin:	HDD_T[15:0], HAD_T[2:0], XHCS_T[1:0], XHIOR_T, XHIOW_T, XHDMACK_T, XHRESET_T, XHDASP_T, XHPDIAG_T, CSEL_T				
"H" level input voltage	VIH2	IOVDD = 3.6V IOVDD = 1.95V	2.0 1.27	-	-	V
"L" level input voltage	VIL2	IOVDD = 3.0V IOVDD = 1.65V	-	-	0.8 0.57	V
Input characteristics	Pin:	XRESET, CLKSEL, PORT00, PORT01, PORT02				
"H" level input voltage	VIH3	IOVDD = 3.6V IOVDD = 1.95V	2.2 1.20	-	-	V
"L" level input voltage	VIL3	IOVDD = 3.0V IOVDD = 1.65V	-	-	0.8 0.50	V
Input characteristics (Schmitt)	Pin:	SCLK0, SIN0, DBGDT, VBUSFLG				
"H" level trigger voltage	VT1+	HVDD = 3.6V	1.4	-	2.7	V
"L" level trigger voltage	VT1-	HVDD = 3.0V	0.6	-	1.8	V
Hysteresis voltage	ΔV1	HVDD = 3.0V	0.3	-	-	V
Schmitt input characteristics (USB: FS)	Pin:	DP, DM				
"H" level trigger voltage	VTU+	HVDD = 3.6V	1.1	-	1.8	V
"L" level trigger voltage	VTU-	HVDD = 3.0V	1.0	-	1.5	V
Hysteresis voltage	ΔVU	HVDD = 3.0V	0.1	-	-	V
Input characteristics (USB:FS differential input)	Pin:	DP, DM pair				
Differential input sensitivity	VDSU	HVDD = 3.0V Differential input voltage 0.8V to 2.5V	-	-	0.2	V
Input characteristics	Pin:	SCLK0, SIN0, DBGDT				
Pull-up resistance	RPLU1H	VI = HVDD	25	50	120	kΩ
Input characteristics	Pin:	HINTRQ_T, XHDASP_T, XHPDIAG_T, VBUSFLG				
Pull-up resistance	RPLU2H	VI = HVDD or IOVDD	50	100	240	kΩ
Input characteristics	Pin:	ATPGEN, BURNIN				
Pull-down resistance	RPLD1L	VI = LVDD	24	60	150	kΩ
Input characteristics	Pin:	TSTEN				
Pull-down resistance	RPLD2L	VI = LVDD	48	120	300	kΩ
Input characteristics	Pin:	VBUS				
Pull-down resistance	RPLDB	VI = 5.0V	110	125	150	kΩ

8.3.3 Output Characteristics

(V_{SS}=0V)

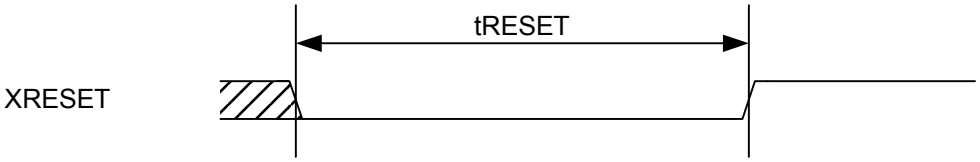
Item	Code	Conditions	MIN	TYP	MAX	Units
Output characteristics	Pin:	HDD_T[15:0], HDMARQ_T, HIORDY_T, HINTRQ_T, XHDASP_T, XHPDIAG_T				
"H" level output voltage	VOH1	IOVDD = 3.0V IOH = -4.0mA IOVDD = 1.65V IOH = -2.0mA	IOVDD - 0.4	-	-	V
"L" level output voltage	VOL1	IOVDD = 3.0V IOL = 4.0mA IOVDD = 1.65V IOL = 2.0mA	-	-	0.4	V
Output characteristics	Pin:	PORT10, PORT11, PORT12, PORT13, PORT14, PORT15, PORT16, PORT17				
"H" level output voltage	VOH2	IOVDD = 3.0V IOH = -2.0mA IOVDD = 1.65V IOH = -1.0mA	IOVDD - 0.4	-	-	V
"L" level output voltage	VOL2	IOVDD = 3.0V IOL = 2.0mA IOVDD = 1.65V IOL = 1.0mA	-	-	0.4	V
Output characteristics	Pin:	SOUT0, DBGDCLK, DBGDT, DBGST				
"H" level output voltage	VOH3	HVDD = 3.0V IOH = -4.0mA	HVDD - 0.4	-	-	V
"L" level output voltage	VOL3	HVDD = 3.0V IOL = 4.0mA	-	-	0.4	V
Output characteristics	Pin:	VBUSEN				
"H" level output voltage	VOH4	HVDD = 3.0V IOH = -2.0mA	HVDD - 0.4	-	-	V
"L" level output voltage	VOL4	HVDD = 3.0V IOL = 2.0mA	-	-	0.4	V
Output characteristics (USB:FS)	Pin:	DP, DM				
"H" level output voltage	VOHUF	HVDD = 3.0V	2.8	-	-	V
"L" level output voltage	VOLUF	HVDD = 3.6V	-	-	0.3	V
Output characteristics (USB:HS)	Pin:	DP, DM				
"H" level output voltage	VOHUH	HVDD = 3.0V	360	-	-	mV
"L" level output voltage	VOLUH	HVDD = 3.6V	-	-	10.0	mV
Output characteristics	Pin:	HDD_T[15:0], HDMARQ_T, HIORDY_T, HINTRQ_T, XHDASP_T, XHPDIAG_T, SCLK0, SIN0, DBGDT				
OFF-STATE leakage	IOZ	HVDD, IOVDD = 3.6V VOH = HVDD or IOVDD VOL = VSS	-5	-	5	μA

8.3.4 Pin Capacitance

Item		Code	Conditions	MIN	TYP	MAX	Units
Pin capacitance		Pin:	All input pins				
	Input pin capacitance	CI	f = 1MHz HVDD = IOVDD = LVDD = VSS	-	-	8	pF
Pin capacitance		Pin:	All output pins				
	Output pin capacitance	CO	f = 1MHz HVDD = IOVDD = LVDD = VSS	-	-	8	pF
Pin capacitance		Pin:	Input/output pins except DP and DM				
	Input/output pin capacitance	CB	f = 1MHz HVDD = IOVDD = LVDD = VSS	-	-	8	pF
Pin capacitance		Pin:	DP and DM				
	Input/output pin capacitance (USB)	CBU	f = 1MHz HVDD = IOVDD = LVDD = VSS	-	-	11	pF

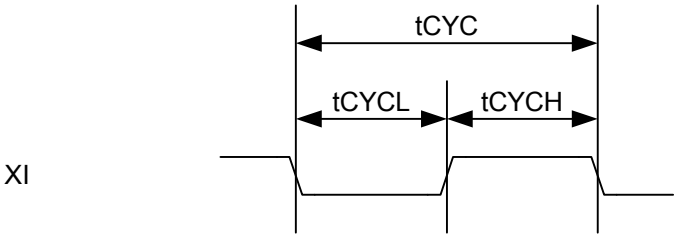
8.4 AC Characteristics

8.4.1 Reset Timing



Code	Details	Min	Typ	Max	Units
tRESET	Reset pulse width	40	-	-	ns

8.4.2 Clock Timing



Code	Details	Min	Typ	Max	Units
tCYC	Clock cycle (CLKSEL = "L")	11.9988	12.000	12.0012	MHz
tCYC	Clock cycle (CLKSEL = "H")	23.9976	24.000	24.0024	MHz
tCYCL tCYCH	Clock duty	45	50	55	%

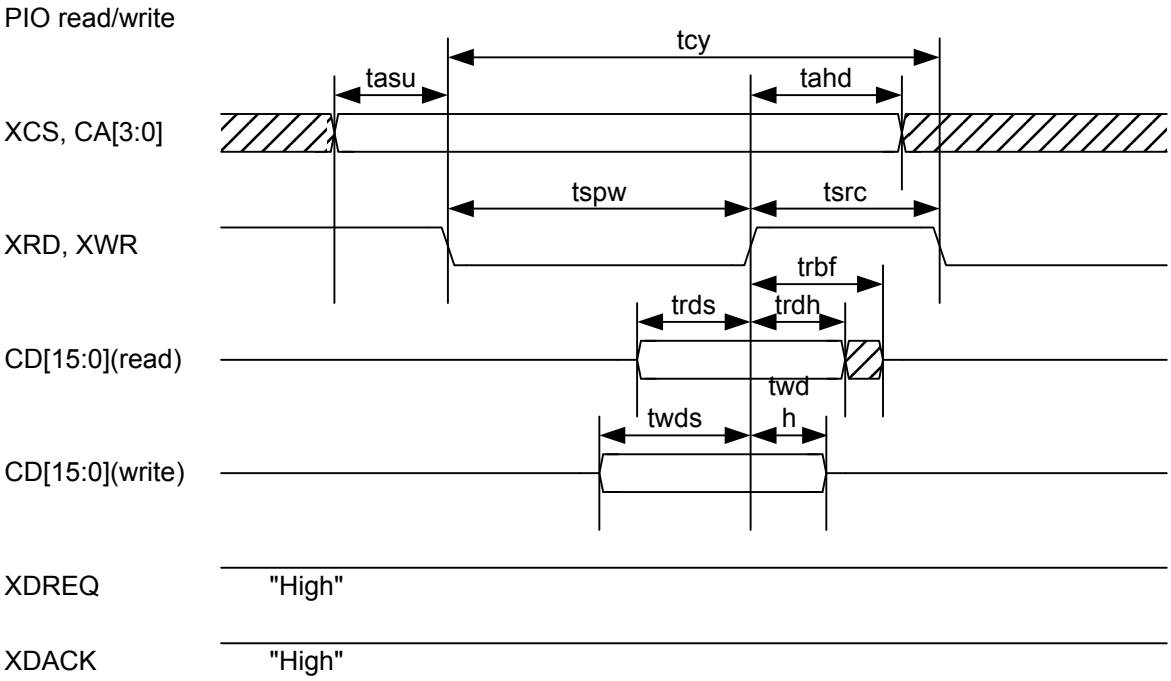
8.4.3 USB I/F Timing

Complies with *USB 2.0 Universal Serial Bus Specification Revision 2.0* tandards.

8.4.4 IDE Device I/F Timing

Complies with *AT Attachment with Packet Interface – 6 (ATA/ATAPI-6)* standards.

8.4.5 CPUIF Timing (PIO)



Code	Details	Min	Typ	Max	Units
tcy	Cycle	120/130	-	-	ns
tasu	Address setup	25/30	-	-	ns
tspw	XRD/XWR pulse width	70/75	-	-	ns
tsrc	XRD/XWR recovery	25/30	-	-	ns
trds	Read data setup	20/15	-	-	ns
trdh	Read data hold	5/5	-	-	ns
trbf	Bus release	-	-	30/30	ns
twds	Write data setup	20/25	-	-	ns
twdh	Write data set hold	10/10	-	-	ns
tahd	Address hold	10/10	-	-	ns

* When using IOVDD = 3.0 V to 3.6 V / When using IOVDD = 1.8 V to 3.0 V (wide range)

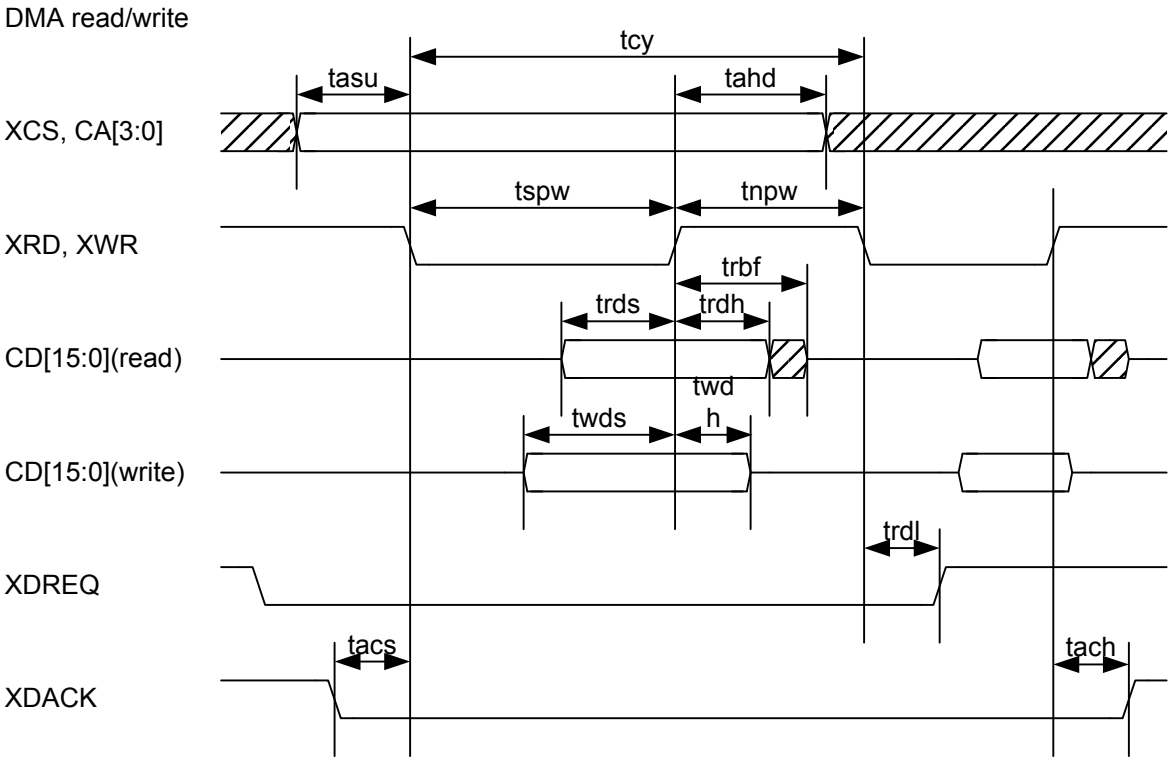
S1R72U16***E200 AC characteristics

Code	Details	Min	Typ	Max	Units
trdh	Read data hold time	5/5 *1	-	-	ns
tahd	Address hold time	0/0	-	-	ns

* When using IOVDD = 3.0 V to 3.6 V / When using IOVDD = 1.8 V to 3.0 V (wide range)
*1: The read data hold time will be 0 ns for address changes if the address hold time is less than 5 ns.

Note: The definition of AC shown above uses the description format specified in ATA standards. Consider the valid data output start time in a read operation as follows:
70 (XRD pulse width: min) -20 (read data setup: min) = 50 ns (when IOVDD = 3.0 to 3.6 V)

8.4.6 CPUIF Timing (DMA)



Code	Details	Min	Typ	Max	Units
tcy	Cycle	120/130	-	-	ns
tasu	Address setup	25/25	-	-	ns
tspw	XRD/XWR pulse width	70/75	-	-	ns
tspw	XRD/XWR negate pulse width	25/30	-	-	ns
trds	Read data setup	20/15	-	-	ns
trdh	Read data hold	5/5	-	-	ns
trbf	Bus release	-	-	30/30	ns
twds	Write data setup	20/25	-	-	ns
twdh	Write data set hold	10/10	-	-	ns
tahd	Address hold	10/10	-	-	ns
trdl	XDREQ delay	-	-	35/45	ns
tacs	XDACK setup	0/0	-	-	ns
tach	XDACK hold	5/5	-	-	ns

* When using IOVDD = 3.0 V to 3.6 V / When using IOVDD = 1.8 V to 3.0 V (wide range)

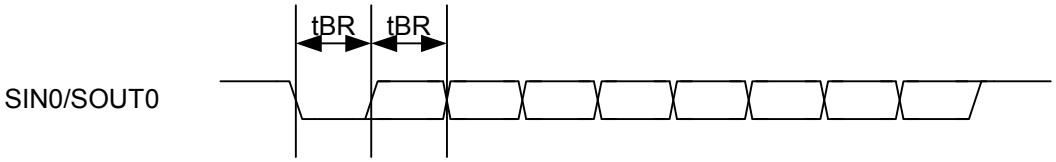
S1R72U16***E200 AC characteristics

Code	Details	Min	Typ	Max	Units
trdh	Read data hold time	5/5 *1	-	-	ns
tahd	Address hold time	0/0	-	-	ns

* When using IOVDD = 3.0 V to 3.6 V / When using IOVDD = 1.8 V to 3.0 V (wide range)
*1: The read data hold time will be 0 ns for address changes if the address hold time is less than 5 ns.

Note: The definition of AC shown above uses the description format specified in ATA standards. Consider the valid data output start time in a read operation as follows:
70 (XRD pulse width: min) -20 (read data setup: min) = 50 ns (when IOVDD = 3.0 to 3.6 V)

8.4.7 Serial I/F Timing



Code	Detail	Min	Typ	Max	Unit
tBR	Baud rate	-	19200	-	bps

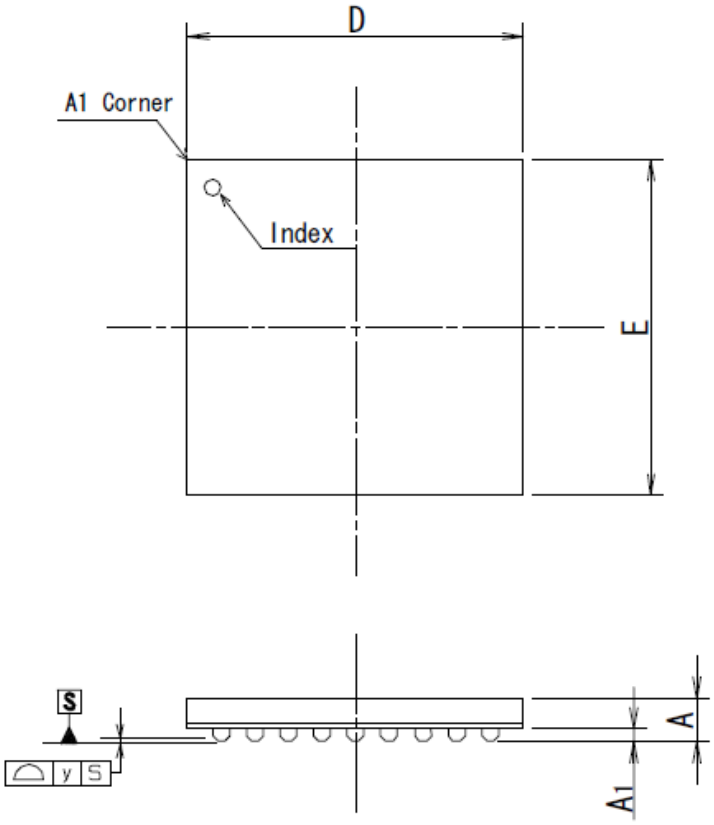
9. Connection Examples

Refer to the *S1R72U16 Evaluation Board Manual* for USB I/F, IDE I/F, CPU I/F (in CPU mode), and Serial I/F connection examples.

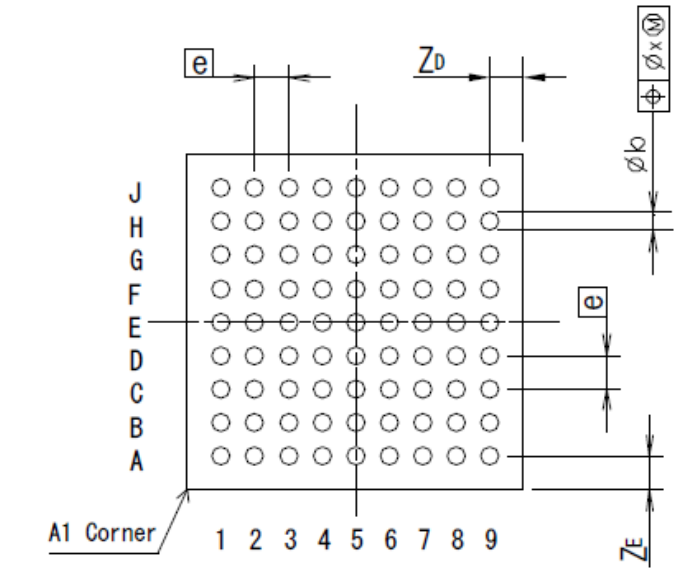
10. External Dimensions Diagram

10.1 PFBGA8UX81

Top View

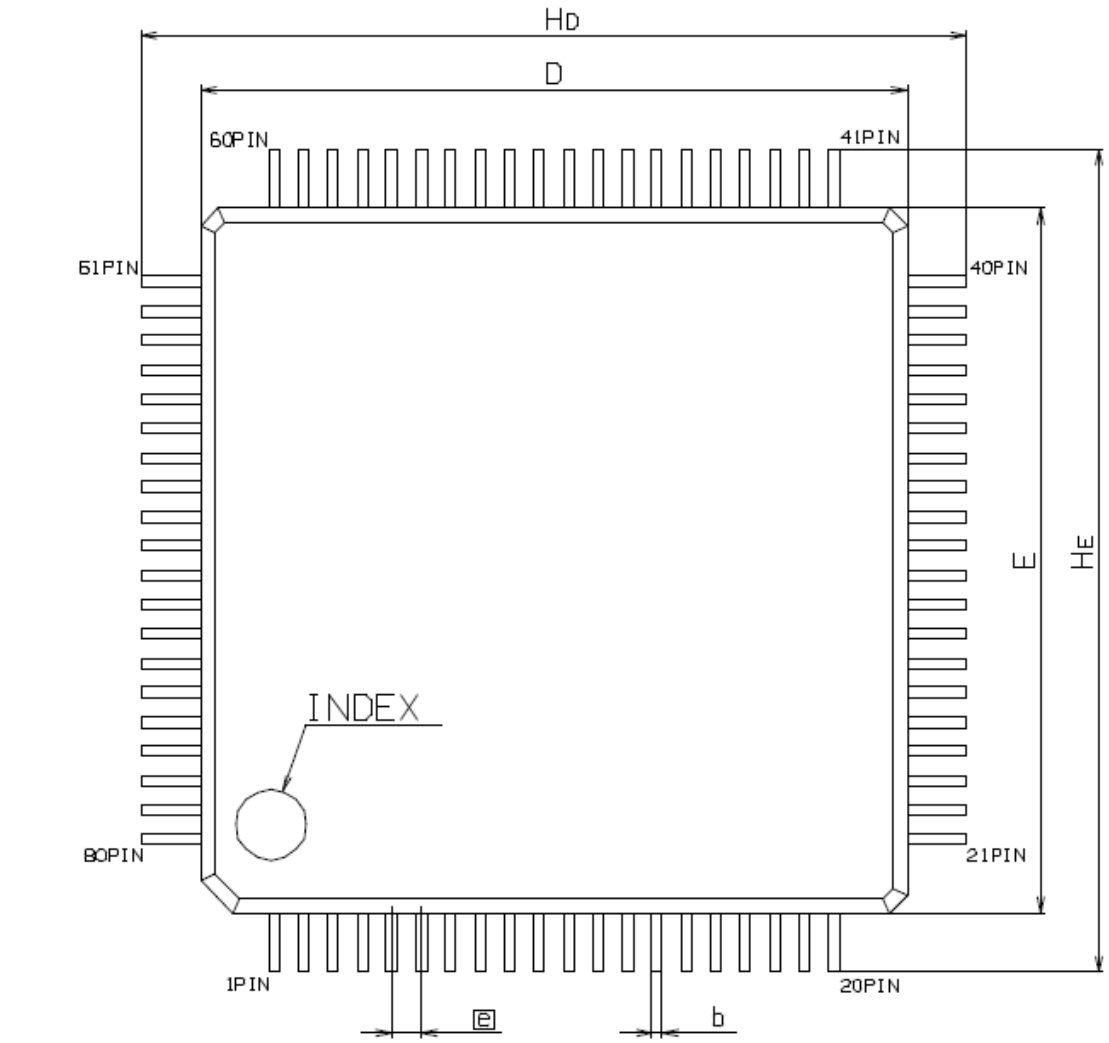


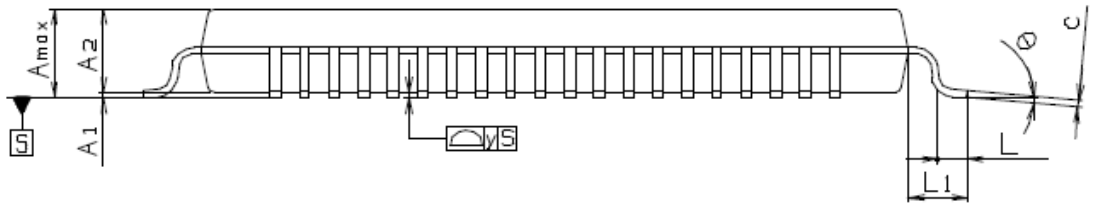
Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	–	8	–
E	–	8	–
A	–	–	1.2
A_1	–	0.3	–
e	–	0.8	–
b	0.38	–	0.48
x	–	–	0.08
y	–	–	0.1
Z_D	–	0.8	–
Z_E	–	0.8	–

10.2 QFP14-80





Symbol	Dimension in Millimters		
	Min	Nom	Max
E	-	12	-
D	-	12	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L_1	-	1	-
HE	-	14	-
HD	-	14	-
y	-	-	0.08

11. Product Codes

Table 11.1 Product codes

Product code	Details
S1R72U16B08E100 S1R72U16B08E200	PFBGA8UX81 package
S1R72U16F14E100 S1R72U16F14E200	QFP14-80 package

Revision History

	Rev.	Page	Type	Details
05/14/2007	0.79	All pages	New	Newly established
07/01/2007	1.00	8.3.1 8.3.2 8.3.3 8.4.5 8.4.6 8.4.7	Addition Addition Addition Addition Addition Addition	Spec. added Spec. added(IOVDD=1.8V) Spec. added(IOVDD=1.8V) Spec. added Spec. added Serial I/F Timing added
10/15/2007	1.10	Scope	Add	Added “notice.”
		2	Correct	Changed “IDE driver” to “ATA/ATAPI driver.”
		6.1 and 6.2	Correct	Changed setting of unused terminal from “open” to “open or pull-up.”
		8.4.2	Correct	Spec. corrected as follows: “11.999” to “11.9988” “12.001” to “12.0012 “23.998” to “23.9976” “24.002” to “24.0024”
		8.4.5 and 8.4.6	Add	Added note regarding valid data output start time.
04/21/2008	2.00	8.4.5 8.4.6	Addition	Added S1R72U16***E200 timing.
		11	Addition	Added S1R72U16***E200 product code.

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Document Code: 411135202
First Issue May 2007
Revised April 2008, JAPAN

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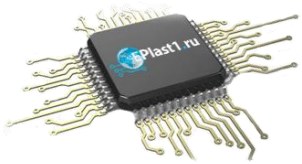

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