

# 74ALVC573

Octal D-type transparent latch; 3-state

Rev. 03 — 26 October 2007

Product data sheet

## 1. General description

---

The 74ALVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A latch enable (LE) input and an outputs enable ( $\overline{OE}$ ) input are common to all latches.

When pin LE is HIGH, data at the D-inputs (pins D0 to D7) enters the latches. In this condition, the latches are transparent, that is, a latch output will change each time its corresponding D-input changes. When pin LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of pin LE.

When pin  $\overline{OE}$  is LOW, the contents of the eight latches are available at the Q-outputs (pins Q0 to Q7). When pin  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of input pin  $\overline{OE}$  does not affect the state of the latches.

The 74ALVC573 is functionally identical to the 74ALVC373, but has a different pin arrangement.

## 2. Features

---

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A 115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC573D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC573PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC573BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram

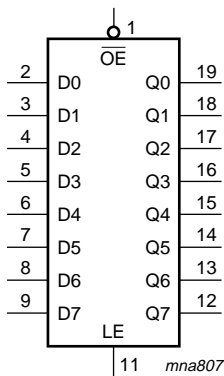


Fig 1. Logic symbol

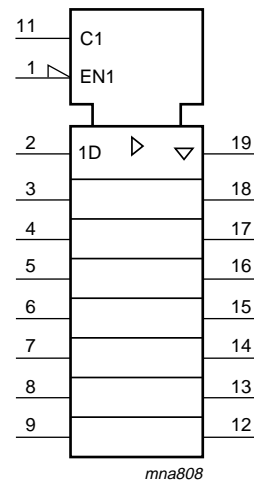


Fig 2. IEC logic symbol

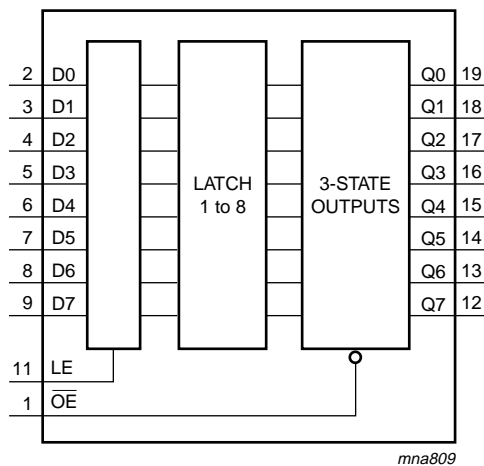


Fig 3. Functional diagram

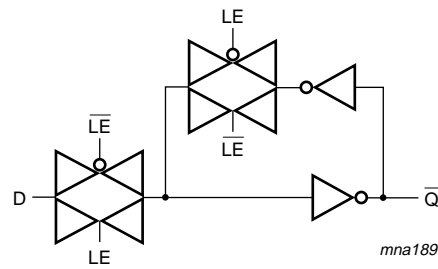


Fig 4. Logic diagram (one latch)

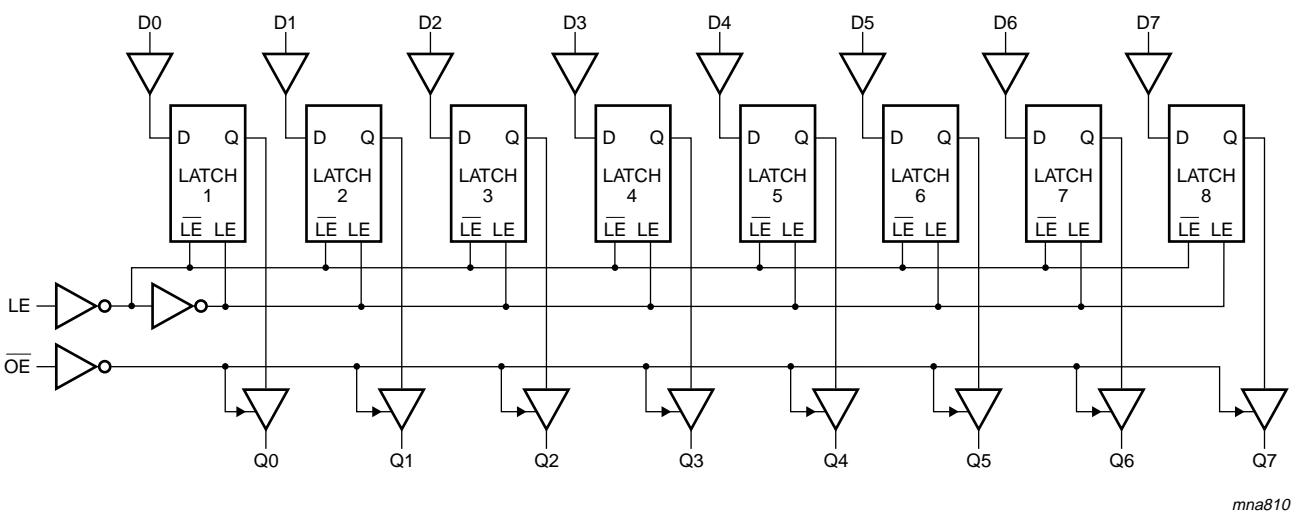


Fig 5. Logic diagram

## 5. Pinning information

### 5.1 Pinning

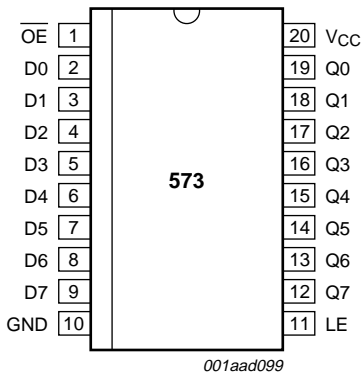
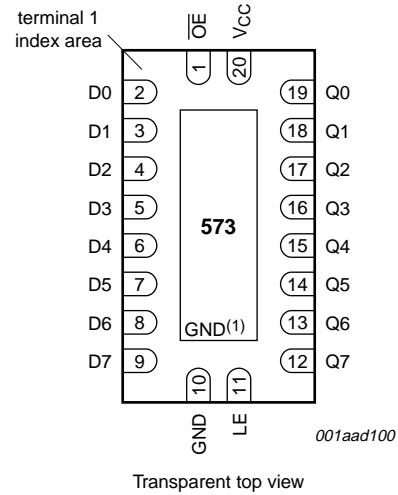


Fig 6. Pin configuration SO20 and TSSOP20



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 7. Pin configuration DHVQFN20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
LE	11	latch enable input (active HIGH)
OE	1	output enable input (active LOW)
Q[0:7]	19, 18, 17, 16, 15, 14, 13, 12	3-state latch output
V <sub>CC</sub>	20	supply voltage
GND	10	ground (0 V)

## 6. Functional description

**Table 3. Functional table<sup>[1]</sup>**

Operating modes	Input			Internal latch	Output Qn
	$\overline{OE}$	LE	Dn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

- [1] H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 Z = High-impedance OFF-state

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	<sup>[1]</sup> <sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		power-down mode, $V_{CC} = 0$ V	<sup>[2]</sup> -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	<sup>[3]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] When  $V_{CC} = 0$  V (power-down mode), the output voltage can be 3.6 V in normal operation.  
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
 For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	output HIGH or LOW state	0	$V_{CC}$	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	-	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.2	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	-	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	-	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	-	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	-	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	$\pm 0.1$	$\pm 5$	$\mu$ A

**Table 6.** Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 1.65 V to 3.6 V; V <sub>O</sub> = 3.6 V or GND;	-	±0.1	±10	µA
I <sub>OFF</sub>	power-off leakage supply	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	-	±0.1	±10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	10	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	-	5	750	µA
C <sub>I</sub>	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit		
			Min	Typ <sup>[1]</sup>	Max			
t <sub>pd</sub>	propagation delay	Dn to Qn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.5	5.4	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.0	3.5	ns		
		V <sub>CC</sub> = 2.7 V	1.0	2.3	3.6	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.2	3.3	ns		
		LE to Qn; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.8	6.0	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.1	3.8	ns		
		V <sub>CC</sub> = 2.7 V	1.0	2.4	3.7	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	3.3	ns		
		t <sub>en</sub>	enable time	OE to Qn; see <a href="#">Figure 10</a> <sup>[2]</sup>				
				V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	3.0	6.4	ns
V <sub>CC</sub> = 2.3 V to 2.7 V	1.0			2.4	4.5	ns		
V <sub>CC</sub> = 2.7 V	1.5			3.0	4.6	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	1.0			2.3	4.0	ns		
t <sub>dis</sub>	disable time	OE to Qn; see <a href="#">Figure 10</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	3.4	7.0	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	4.4	ns		
		V <sub>CC</sub> = 2.7 V	1.5	2.8	4.4	ns		
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	4.4	ns		

**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>W</sub>	pulse width	LE pulse width HIGH; see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.8	-	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.3	-	-	ns
		V <sub>CC</sub> = 2.7 V	3.3	-	-	ns
t <sub>su</sub>	set-up time	Dn to LE; see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.8	-	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	-	-	ns
		V <sub>CC</sub> = 2.7 V	0.8	-	-	ns
t <sub>h</sub>	hold time	Dn to LE; see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.8	-	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.8	-	-	ns
		V <sub>CC</sub> = 2.7 V	0.8	-	-	ns
C <sub>PD</sub>	power dissipation capacitance	per latch; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[3]</sup>				
		outputs HIGH or LOW state	-	37	-	pF
		outputs 3-state	-	7	-	pF

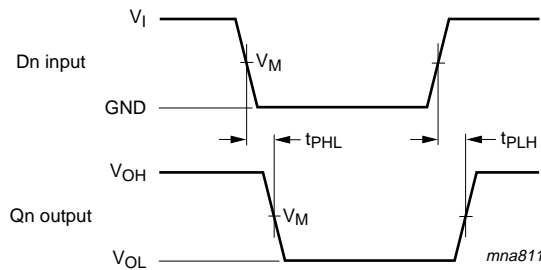
[1] Typical values are measured at T<sub>amb</sub> = 25 °C[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHzC<sub>L</sub> = output load capacitance in pFV<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs



### 11. Waveforms



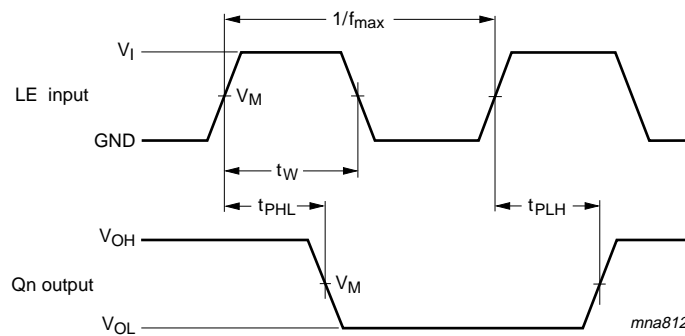
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 8. Input Dn to output Qn propagation delay times**

**Table 8. Measurement points**

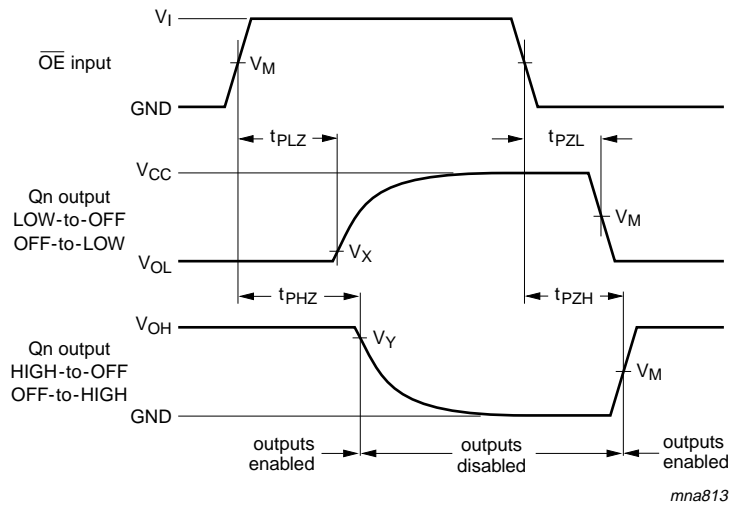
Supply voltage $V_{CC}$	$V_M$	Output	
		$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

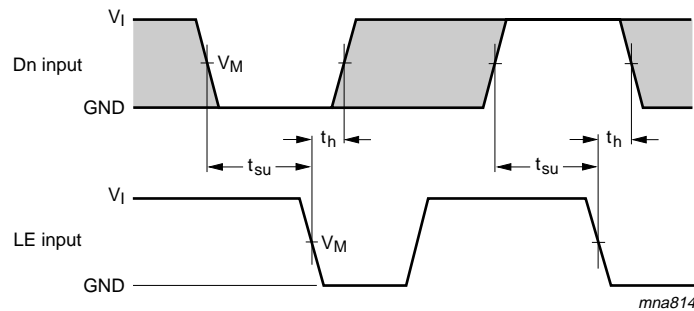
**Fig 9. Latch enable (LE) pulse width and latch enable input to output (Qn) propagation delays**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

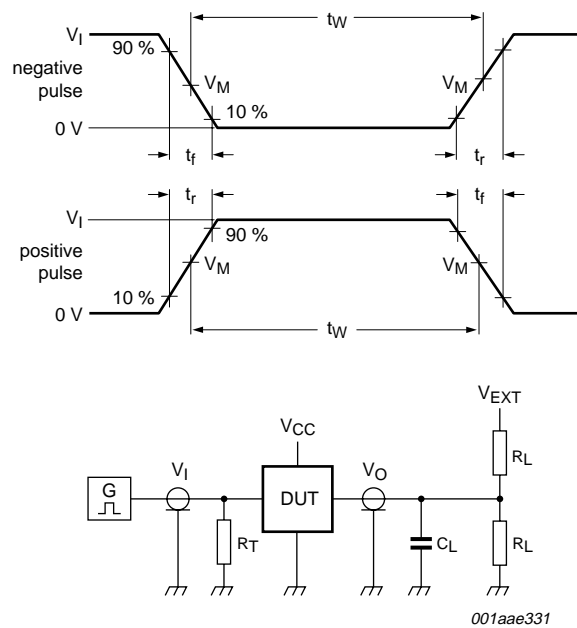
**Fig 10. Enable and disable times**



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 11. The data set-up and hold times for Dn input to LE input**



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 12. Test circuitry for switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	$2V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

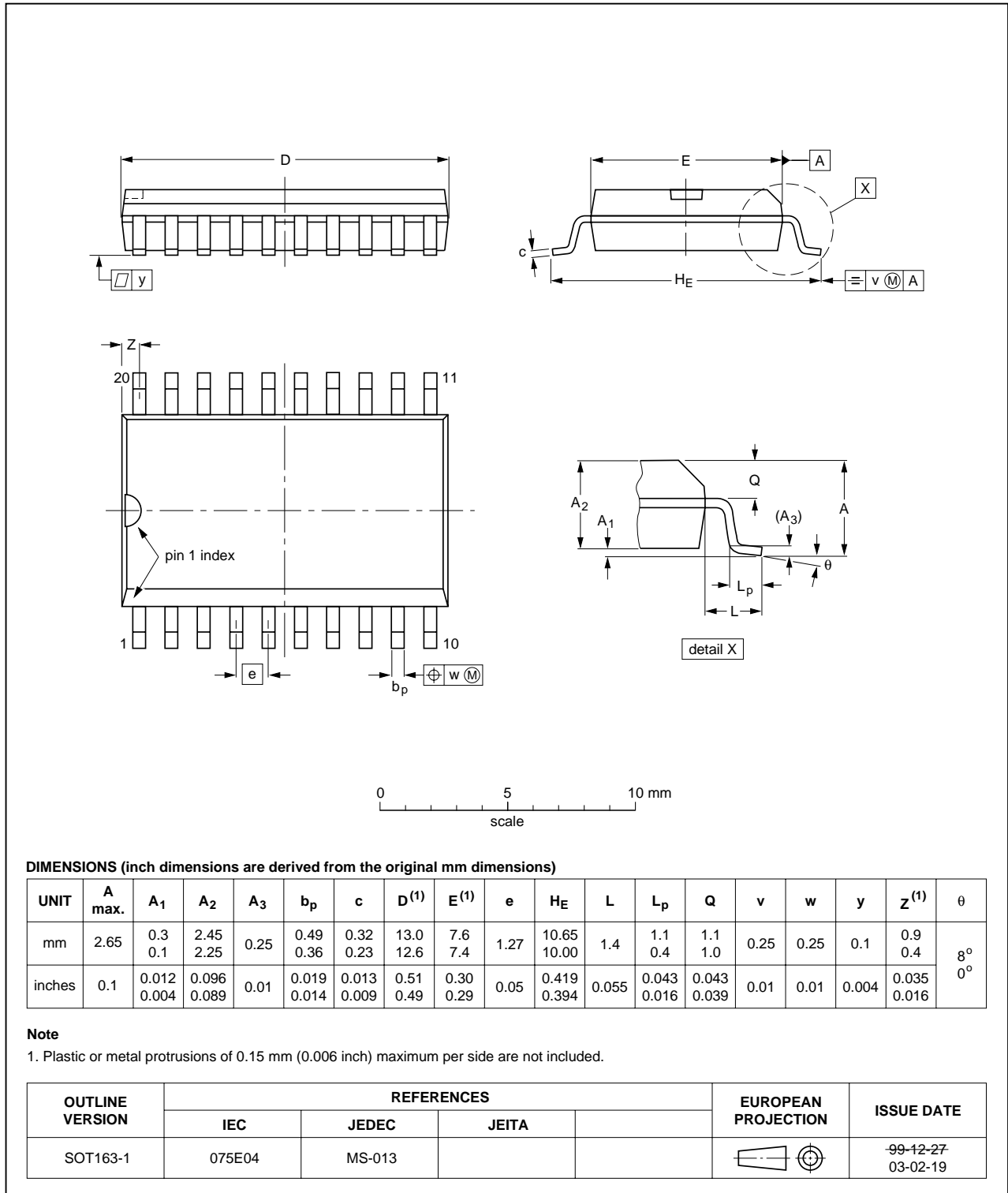


Fig 13. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

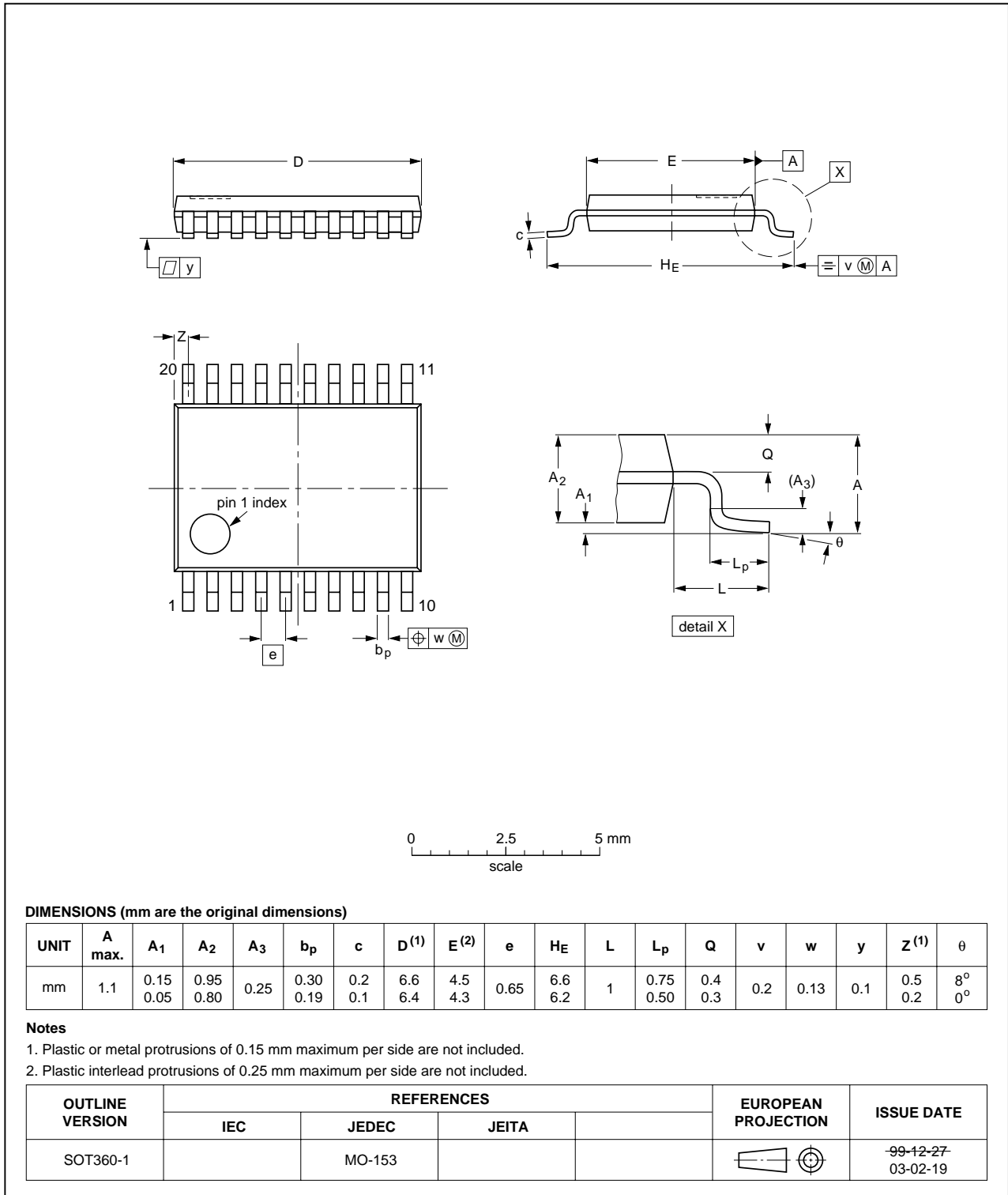


Fig 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

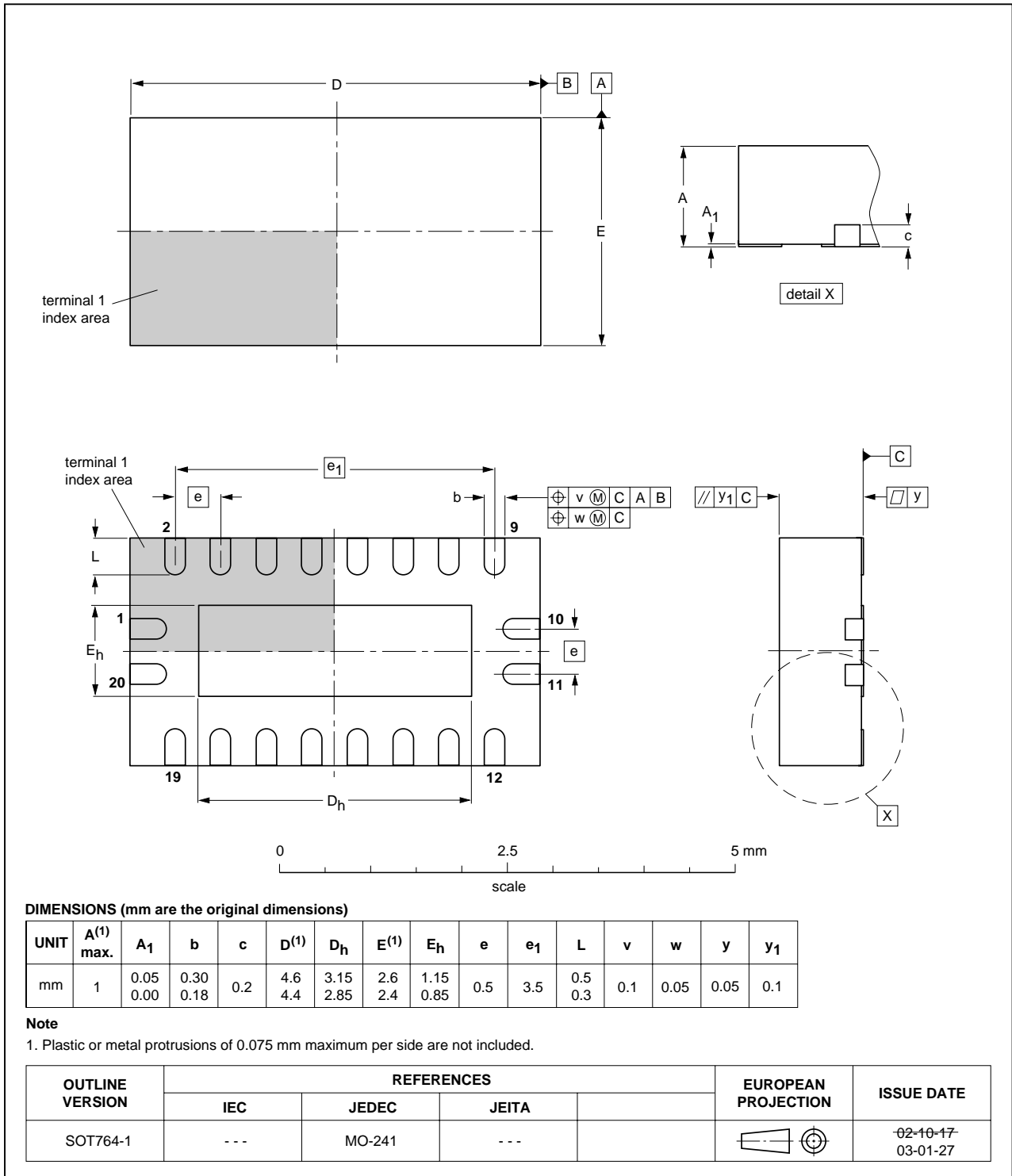


Fig 15. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC573_3	20071026	Product data sheet	-	74ALVC573_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN20 package added.</li> <li><a href="#">Section 8</a>: derating values added for DHVQFN20 package.</li> <li><a href="#">Section 12</a>: outline drawing added for DHVQFN20 package.</li> </ul>			
74ALVC573_2	20030625	Product specification	-	74ALVC573_1
74ALVC573_1	20020301	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — Nexperia products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia accepts no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Nexperia. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For additional information, please visit: <http://www.nexperia.com>

For sales office addresses, send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)



## 17. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>7</b>
<b>11</b>	<b>Waveforms</b> .....	<b>9</b>
<b>12</b>	<b>Package outline</b> .....	<b>12</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>15</b>
<b>14</b>	<b>Revision history</b> .....	<b>15</b>
<b>15</b>	<b>Legal information</b> .....	<b>16</b>
15.1	Data sheet status .....	16
15.2	Definitions .....	16
15.3	Disclaimers .....	16
15.4	Trademarks .....	16
<b>16</b>	<b>Contact information</b> .....	<b>16</b>
<b>17</b>	<b>Contents</b> .....	<b>17</b>



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.