LX1752

Dual Interleaving PWM Controller

PRODUCTION DATA SHEET

GENERAL DESCRIPTION

The LX1752 is a dual output synchronous buck controller using voltage mode PWM architecture.

The single input voltage supply feature simplifies the design and offers a wide range of operation from 4.5 to 22 volts. Each PWM has a Soft-Start pin for programming the output sequencing and serves as the shutdown control.

Current limit threshold is set with a single external resistor and protects the high-side and low-side MOSFETs by sensing the voltage drop generated from R_{DSON}.

Each PWM channel has its own external feedback compensation for performance optimization.

Internal gate drive circuitry provides 5V for the external upper and lower N channel MOSFETS.

Output voltages as low as 700mV, load currents up to 15A per phase and efficiency of 93% can be achieved with the flexible controller.

Operating alone or with other LX1752's on a bus, three multi-phase interleaving options are available: two PWM channels with 180° separation; three PWM channels at 120° or four PWM channels at 90°. This phasing is set by the tri-state input pin PSET. This architecture minimizes the input capacitor requirements.

The entire power supply design occupies a small footprint with the LX1752's low profile 28 pin, MLP package of 4x5x1mm (JEDEC MO-220).

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

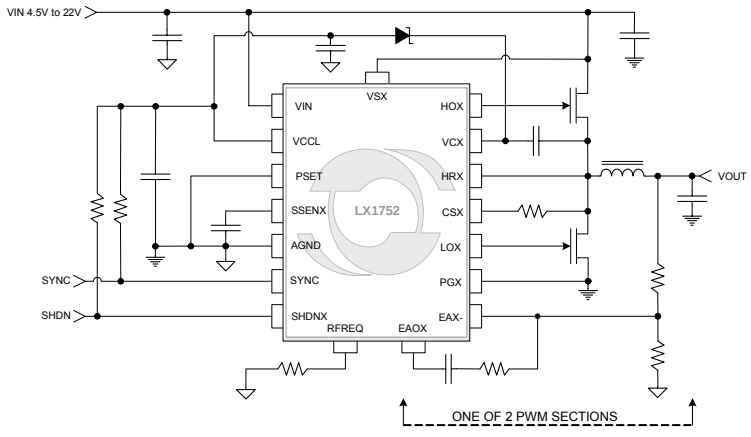
KEY FEATURES

- Dual PWM Controller, Synchronous Operation
- Voltage Mode PWM with External Compensation
- Single Input Supply, wide range 4.5V to 22V
- Precision Reference
- Outputs as low as 700mV
- Selectable PWM Frequency up to 1.5Mhz
- Synchronization Pin for PWM Frequency
- Independent and Programmable Soft Start/Enable for Power Sequencing
- Integrated High Current MOSFET Drivers
- Programmable Current Limit
- Lossless Current Sensing for Current Limit and Short Circuit Protection
- Pb-free, RoHS Compliant

APPLICATIONS

- Multi-Output Power Supplies
- Video Card Power Supplies
- PC Peripherals
- Set Top Boxes
- Point of Load DC-DC Converters

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	LQ Plastic MLPQ 28 pin RoHS Compliant / Pb-free
0 to 85	LX1752CLQ

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1752CLQ-TR)

Rev. 1.0, 2008-07-31

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ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage(VIN) ..... -0.3V to 22V
Supply Voltage (VCCL) ..... -0.3V to 6.0V
Topside Driver Supply Input Voltage (VC_X) ..... -0.3V to 28V
Topside Current Sense Input (VSx) ..... -0.3V to 28V
Current Sense Input (CS_X) ..... -0.3V(-2.0V for ≤ 50ns), to 28V
Topside Driver Return Input Voltage (VHR_X).... -0.3V(-2.0V for ≤ 50ns), to 28V
Error Amplifier Inputs (EAX-) ..... -0.3V to 5.5V
Logic Inputs (SYNC, PSET, SHDNX) .....-0.3 to VCCL
Differential Voltage: V_{HOX}-V_{HRX} (High Side Return)..... -0.3V to 6V
Soft Start Input (SSENX).....-0.3V to V_{REF}
Maximum LDO Output Current (VCCL) 100mA
Maximum Operating Junction Temperature ..... 150°C
Operating Temperature .....-20°C to 85°C
Storage Temperature Range.....-65°C to 150°C
Peak Package Solder Reflow Temp (40 seconds max exposure).... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.
x denotes respective pin designator (1 or 2).

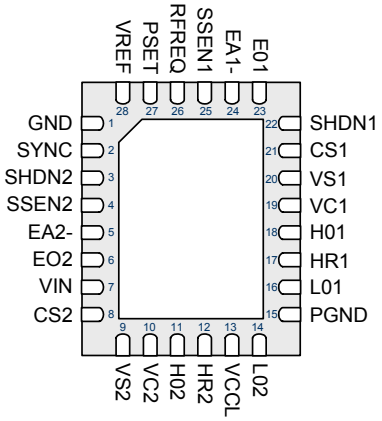
THERMAL DATA

LQ **Plastic MLPQ 28-Pin**

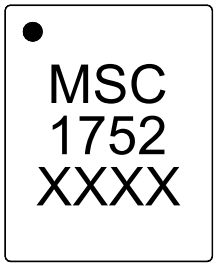
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	27°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)



LQ PACKAGE MARKINGS
"xxxx" Denote Date Code and Lot Identification

RoHS / Pb-free 100% matte Tin Pin Finish

FUNCTIONAL PIN DESCRIPTION

Name	Pin	Description
GND	1	Analog Ground. Connect this pin to a local analog ground plane. All low level signals are referenced to this ground and should return to this pin.
SYNC	2	SYNC Control Line used on the multi-channel bus. Wire OR'd negative going pulse with a common pull-up resistor.
$SHDN_X$	3, 22	The Shutdown pin is an I/O pin which connects to an internal open drain transistor and an external pull up resistor. During a fault, this pin will be low during the discharge portion of hiccup mode, and high during the recovery (soft start) portion of hiccup mode.. Used primarily for test purposes. May be used as a system level fault monitor. Each SHDN pin requires a pull-up resistor of 500Ω to 4.7K tied to VCCL.
$SSEN_X$	4, 25	Soft Start Enable input. Connect a capacitor from SSENx to GND to set the soft-start time, the rise time of the output voltage during start up. If grounded the PWM is disabled.
EA_X -	5, 24	Error Amplifier Inverting Input for the corresponding PWM channel denoted by "X". Connect to the output via external network to regulate the output voltage.
EO_X	6, 23	Error Amplifier Output – Connect to external loop compensation network for the corresponding PWM channel denoted by "X" to provide an error signal to the internal PWM comparator for duty cycle control.
VIN	7	Controller Supply Voltage. This is the input to the internal 5V LDO.

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FUNCTIONAL PIN DESCRIPTION

CS_X	8, 21	Over-Current Limit Set – connecting a resistor between CS_X pin and the junction of the drain of the low-side NMOSFET and the Source of the high-side MOSFET sets the current limit threshold for the corresponding PWM channel denoted by "X". A minimum of 200 ohms must be in series with this input. Whenever the current limit threshold is reached for 4 consecutive clock cycles the shutdown latch is set and the Soft Start capacitor is discharged through an internal resistor initiating Shutdown and then a Soft Start to generate a hiccup mode current limit.
VS_X	9, 20	Voltage reference for high side current sense. "X" denotes corresponding phase. Connect this pin directly to the high-side MOSFET's drain.
VC_X	10, 19	PWM channel High-Side MOSFET Gate Driver Supply. Connect to the flying capacitor bootstrap supply to ensure proper high-side gate driver supply voltage. "X" denotes the corresponding PWM channel.
HO_X	11, 18	High Side MOSFET Gate Driver – "X" denotes corresponding PWM channel.
HR_X	12, 17	High Side driver return, connect this pin to the High Side MOSFET source. "X" denotes the corresponding PWM channel.
VCCL	13	Output of the +5V LDO regulator. Supplies the internal circuit and the external MOSFETs gate drivers. For 4.5V < VIN < 5.5V, this pin is connected externally to VIN. For VIN > 6V this pin supplies +5V to the internal circuit and the external MOSFETs gate drivers Connect a minimum of 4.7µF ceramic capacitor from this pin to GND.
LO_X	14, 16	Low Side MOSFET Gate Driver – "X" denotes corresponding PWM channel.
PGND	15	Power ground pin for the low-side MOSFET drivers. Connect low-side MOSFETs' source directly to this pin, which connects to power ground plane
RFREQ	26	The resistor value from this pin to GND sets the PWM frequency.
PSET	27	A Tri-State logic level input that selects the phase position of the two PWM channels from the SYNC pulse. A logic low, GND, will set the PWM phases at 0 and 180 degrees. An open pin, Tri-State, will set the PWM phases at 90 and 270 degrees. A logic high, VCCL, will set the PWM phases at 120 and 240 degrees.
VREF	28	An internally generated voltage reference of 0.8V that is buffered and brought out on this pin. If used, connect a 470pF ceramic capacitor to GND.

Note: X Denotes the PWM Channel: 1 or 2

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{IN} = 12V, V_{CX} = 17V, HOX = 1000pF load to HRX, LOX =1000pF load to GND, V_{HRX} = 12V, (f = 800kHz).

Parameter	Symbol	Test Conditions	LX1752 Min	LX1752 Typ	LX1752 Max	Units
IC ELECTRICAL CHARACTERISTICS						
Input Voltage	VIN		6.0		22	V
		Connect VCCL to VIN externally	4.5		5.5	
Operation Current	I_{VIN}	No Switching		6		mA
Feedback Voltage	EAx-	Initial Accuracy; T_A = 25°C	0.691	0.700	0.709	V
		4.5V ≤ VIN ≤ 22V	0.689		0.711	
High Side Minimum Pulse Width (NOTE 3, NOTE 5)	PW_{MIN}	Switching Frequency = 800kHz to1.5Mhz Measured between 1.5V rise to 1.5V fall of HOX – HRX.			80	ns
Maximum Duty Cycle	PWM_{DC}	Measured between HOX-HRX 1.5V rise to HOX-HRX 1.5V fall.	88	92		%
Buffered Reference Voltage	V_{REF}	0mA ≤ I_{VREF} ≤ 1.0mA	0.784	0.800	0.816	V
ERROR AMPLIFIER						
DC Open Loop Gain,				70		dB
Unity gain bandwidth (NOTE 2)	AV_{UGBW}			10		MHz
High Output Voltage	V_{OH}	I Source = 2mA	3.5			V
Low Output Voltage	V_{OL}	I Sink = 100µA			100	mV
Input Common Mode Range			0.2		1.0	V
Input Bias Current	I_{IN}				30	nA
CURRENT SENSE						
CS Bias Current (Source)	I_{SET}	V_{CSx} to V_{HRX} = 0.2V; V_{PGND} = 0V, Vcx to Vhrx = 5.0V	44	50	57	µA
CS Trip Threshold Offset	V_{TRIP}	Referenced to V_{CSX}, V_{PGND} = 0V	-20	0	20	mV
CS Delay (Blanking)	T_{CSD}	(NOTE 5)		150		ns
OUTPUT DRIVERS – N Channel MOSFETS						
Drive Rise and Fall Time	$T_{R/F}$	C_L = 1000pF			40	ns
Dead Time – High Side to Low Side or Low Side to High Side	T_{DEAD}	measured between 1.5V crossings of HOX-HRX and LOX.		40		ns
High Side Driver RDS_{ON} Drive High	HO_X_RDS_{ON}	I_{HOX} = 100mA (NOTE 5)			4.8	Ohm
Drive Low		I_{HOX} = -100mA			3.3	
Low Side Driver RDS_{ON} Drive High	LO_X_RDS_{ON}	I_{LOX} = 100mA			4.4	Ohm
Drive Low		I_{LOX} = -100mA			3.3	
SYNC-FREQUENCY GENERATOR						
Maximum Clock Frequency	F_{MAX}	R_{FREQ} = 19.1kΩ	1.4	1.5	1.6	MHz
Minimum Clock Frequency	F_{MIN}	R_{FREQ} = 178kΩ	180	200	220	kHz
Ramp Amplitude	V_{RAMP}			1.2		VPP
Frequency Stability		4.5V ≤ VIN ≤22V		±5		%

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{IN} = 12V, V_{CX} = 17V, HOX = 1000pF load to HRX, LOX =1000pF load to GND, V_{HRX} = 12V, (f = 800kHz).

Parameter	Symbol	Test Conditions	LX1752			Units
			Min	Typ	Max	
UVLO AND SOFT-START (SS)						
Start-Up Threshold (VCCL)		VCCL Rising	3.75		4.35	V
Hysteresis (NOTE 2)			0.2	0.30		V
SS Input Resistance	R_{SS}			20		kΩ
SS Shutdown Threshold	V_{SHDN}		85		130	mV
Soft Start Time		C_{SS} = 0.1uF; V_{OUT} rise time from 0V to 90% of output voltage set by feedback (NOTE 2)		4.30		ms
Hiccup Mode Duty Cycle		C_{SS} = 0.1µF; 100% * On time/Off time + On time		4		%
INTERNAL LDO REGULATOR						
Regulated Output	VCCL	Internal + External Load: 0mA < I_{VCCL} < 100mA; 6V < VIN<22V.	4.5		5.5	V
PSET TRI-STATE INPUT						
Logic Level Low Threshold	PSET	Percentage of VCCL (NOTE 4)			22	%
Logic Level Open Threshold		Percentage of VCCL (NOTE 4)	40	50	60	%
Logic Level High Threshold		Percentage of VCCL (NOTE 4)	84			%
LOGIC INPUT / OUTPUT – OPEN DRAIN EXTERNAL PULL UP RESISTOR						
Sync Bus	SYNC	Threshold Logic Low External Pull-up Resistance = 500 ohms to VCCL	1.0	1.5		V
		Input Pulse Width measured at 50% of VCCL; Fall time < 5ns, Rise time < 20ns	30	100		ns
Shutdown	SHDN	Threshold Logic Low; Falling Edge	0.8	1.5		V
SWITCHING REGULATORS						
Phase to Phase Position		PSET = VCCL; Measured HO1 to HO2	80	102	120	Degrees
		PSET = Open; Measured HO1 to HO2	140	165	190	Degrees
		PSET = GND; Measured HO1 to HO2	160	180	210	Degrees
Thermal Shutdown						
Die Temperature	TSD	Rising temperature; Hiccup Mode Operation at Limit		165		°C
Die Temperature Hysteresis	TSD	Rising temperature; Hiccup Mode Operation at Limit		10		°C

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SYSTEM CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{IN} = 12V; f = 800kHz; tested using the application circuit referenced in Figure 2.

Parameter	Symbol	Test Conditions	LX1752			Units
			Min	Typ	Max	
SWITCHING REGULATORS SYSTEM CHARACTERISTICS						
Line Regulation		VIN = 6V to 22V	0.5		0.5	%
Load Regulation		0 to 5 Amps Output Load	-0.2		0.2	%

Note 1: X denotes the PWM Channel: 1 or 2.
Note 2: Assured by design and characterization. Not ATE tested.
Note 3: For switching frequencies less than 800kHz, minimum pulse width is defined by the formula PW_{MIN} = 0.064 X 1/Fsw
Note 4: PSET Logic Threshold specifications are dependent on VCCL voltage level. The following formulas apply:
PSET Logic High min. threshold = 0.81 X VCCL + 0.140 (rising)
PSET Logic Low max. threshold = 0.19 X VCCL + 0.028 (rising)
Note 5: Guaranteed by design. Not ATE tested.

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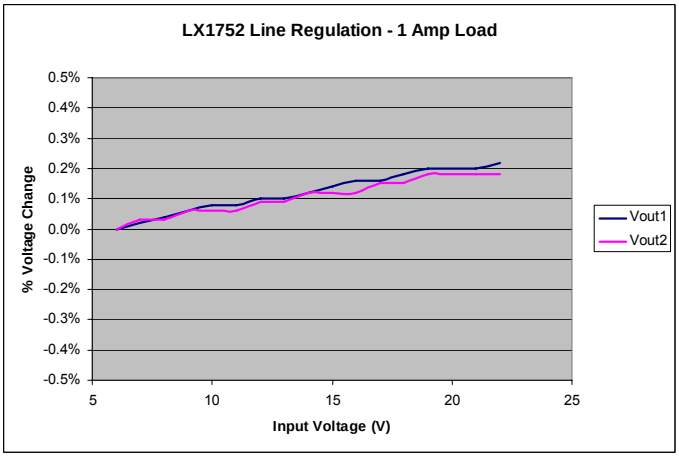
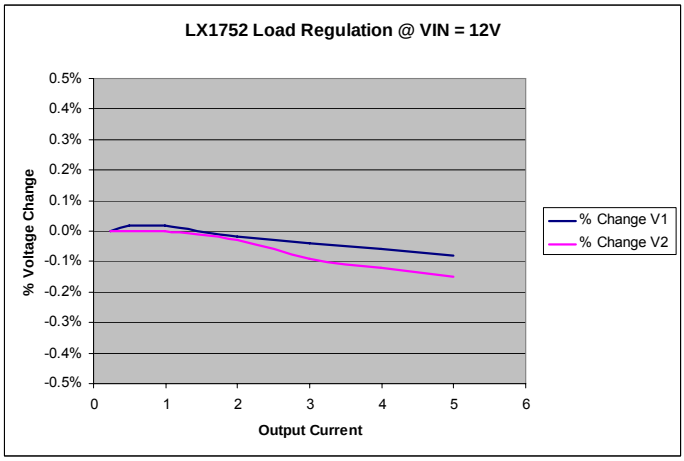
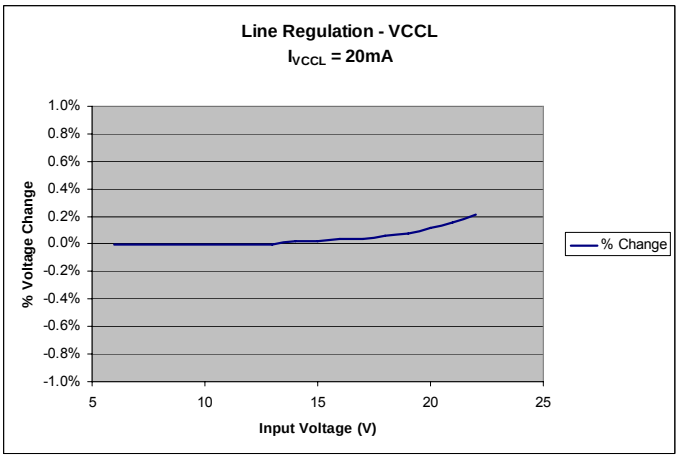
TYPICAL CHARACTERISTICS @ 25°C (REFER TO FIGURE 2)



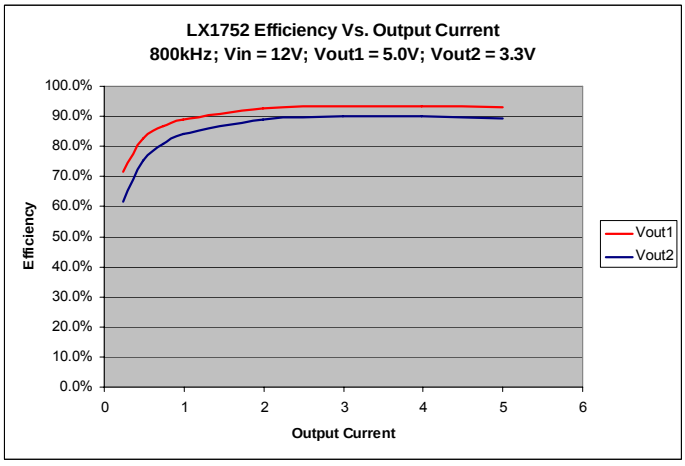
Line Regulation



Load Regulation



VCCL Line Regulation



Efficiency Vs. Output Current

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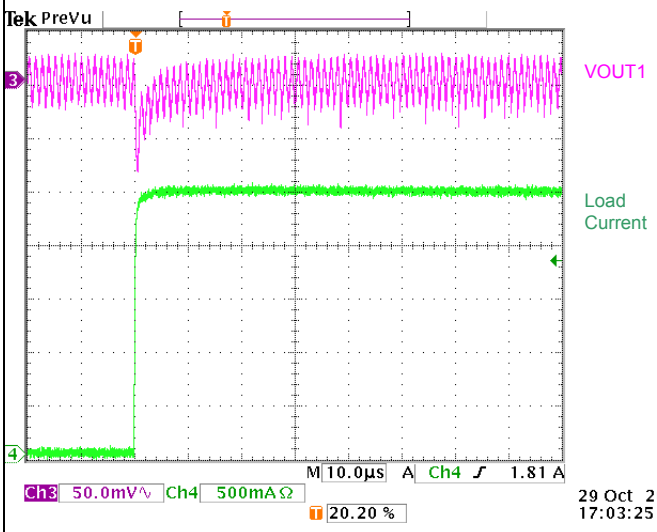
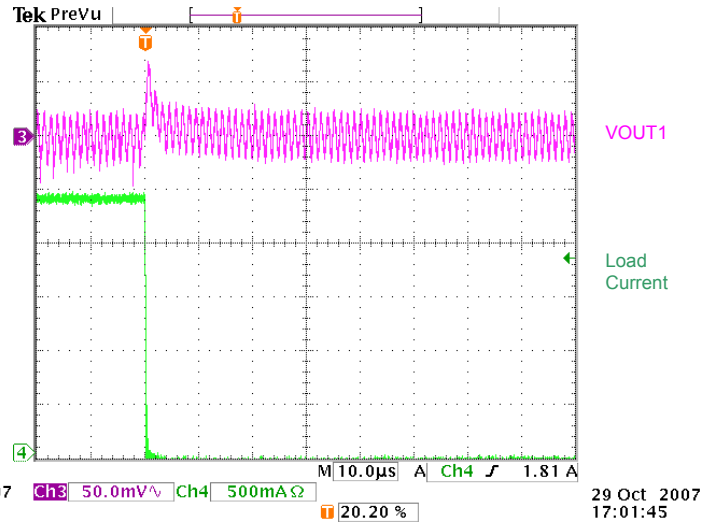
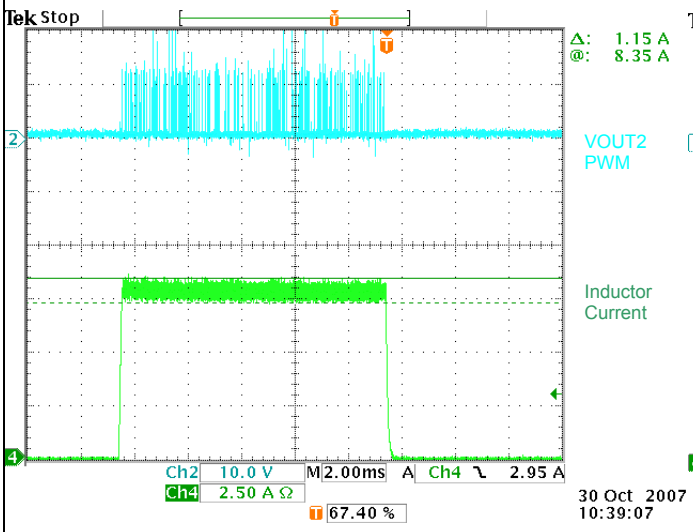
TYPICAL CHARACTERISTICS @ 25°C (REFER TO FIGURE 2)



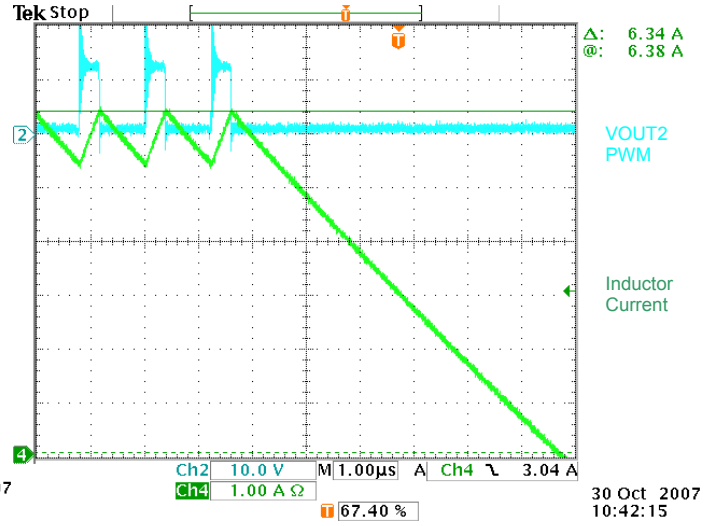
Output Load Step Response



Output Load Release Response



Short Circuit Current Limit During Hiccup Mode



Overcurrent Protection Limit - I limit set for 6.5A

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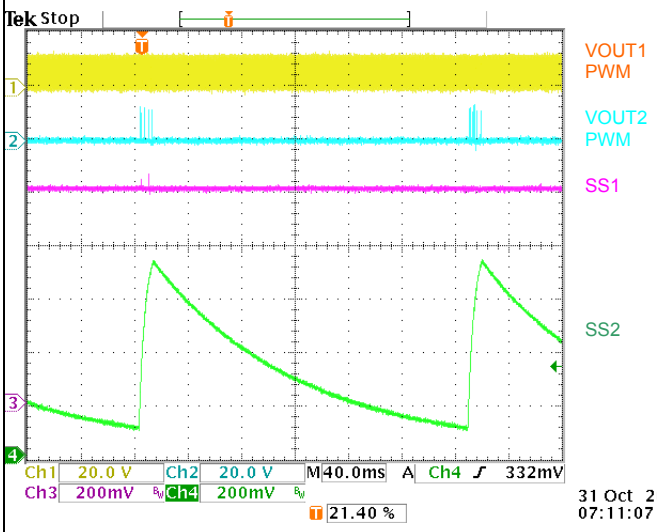
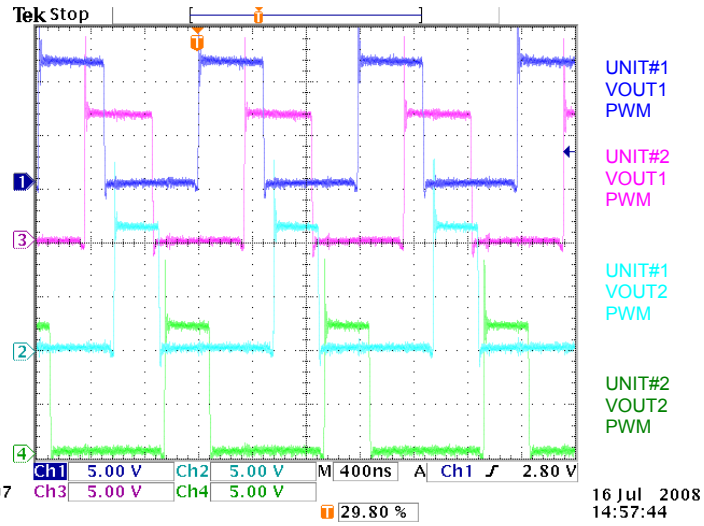
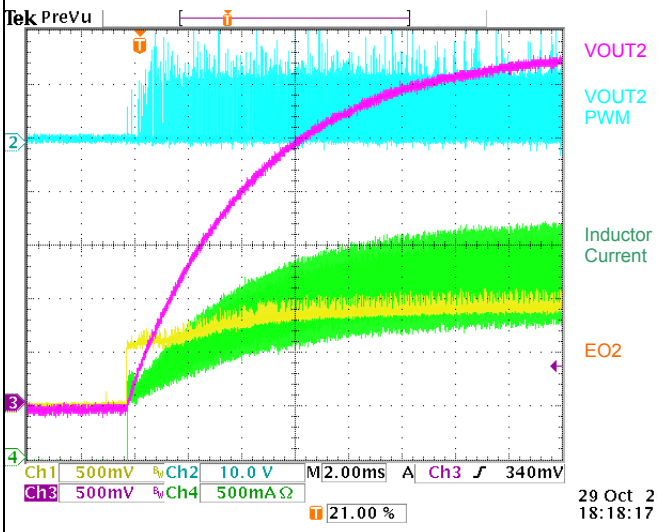
TYPICAL CHARACTERISTICS @ 25°C (REFER TO FIGURE 2)



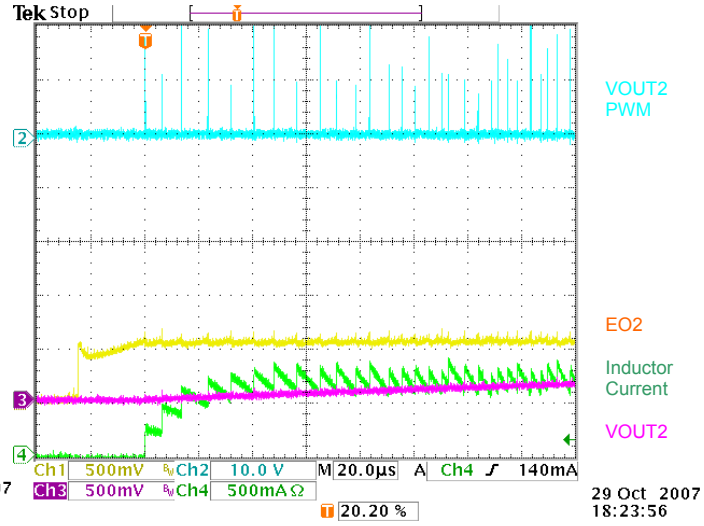
Fault Hiccup Mode – VOUT2 Shorted



Dual 1752s Synchronized and Interleaved at 90° Intervals



Soft Start at Power-up



Zoom In Soft Start at Power-up

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SIMPLIFIED BLOCK DIAGRAM

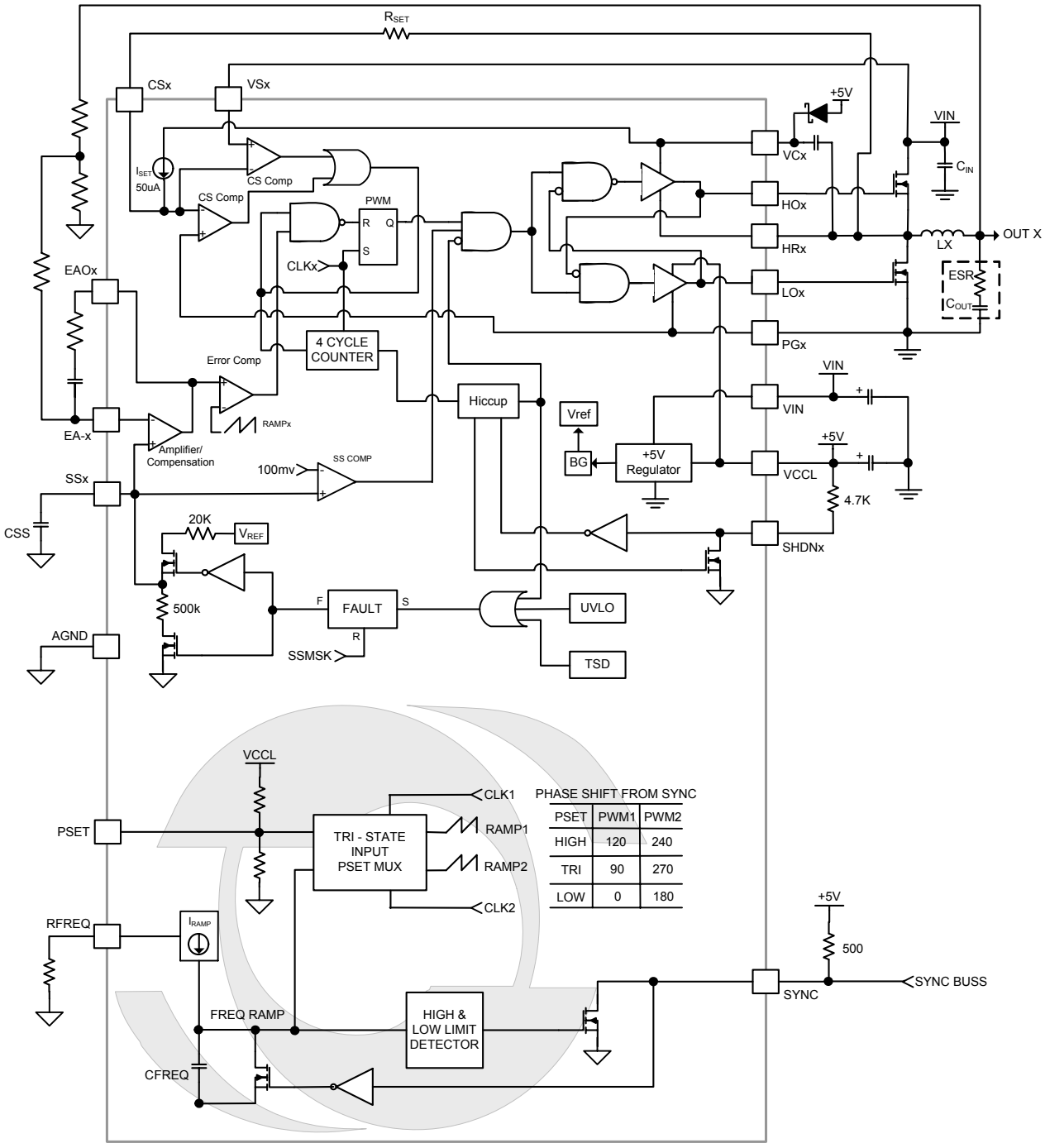

Figure 1 – Simplified Block Diagram

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APPLICATION CIRCUIT

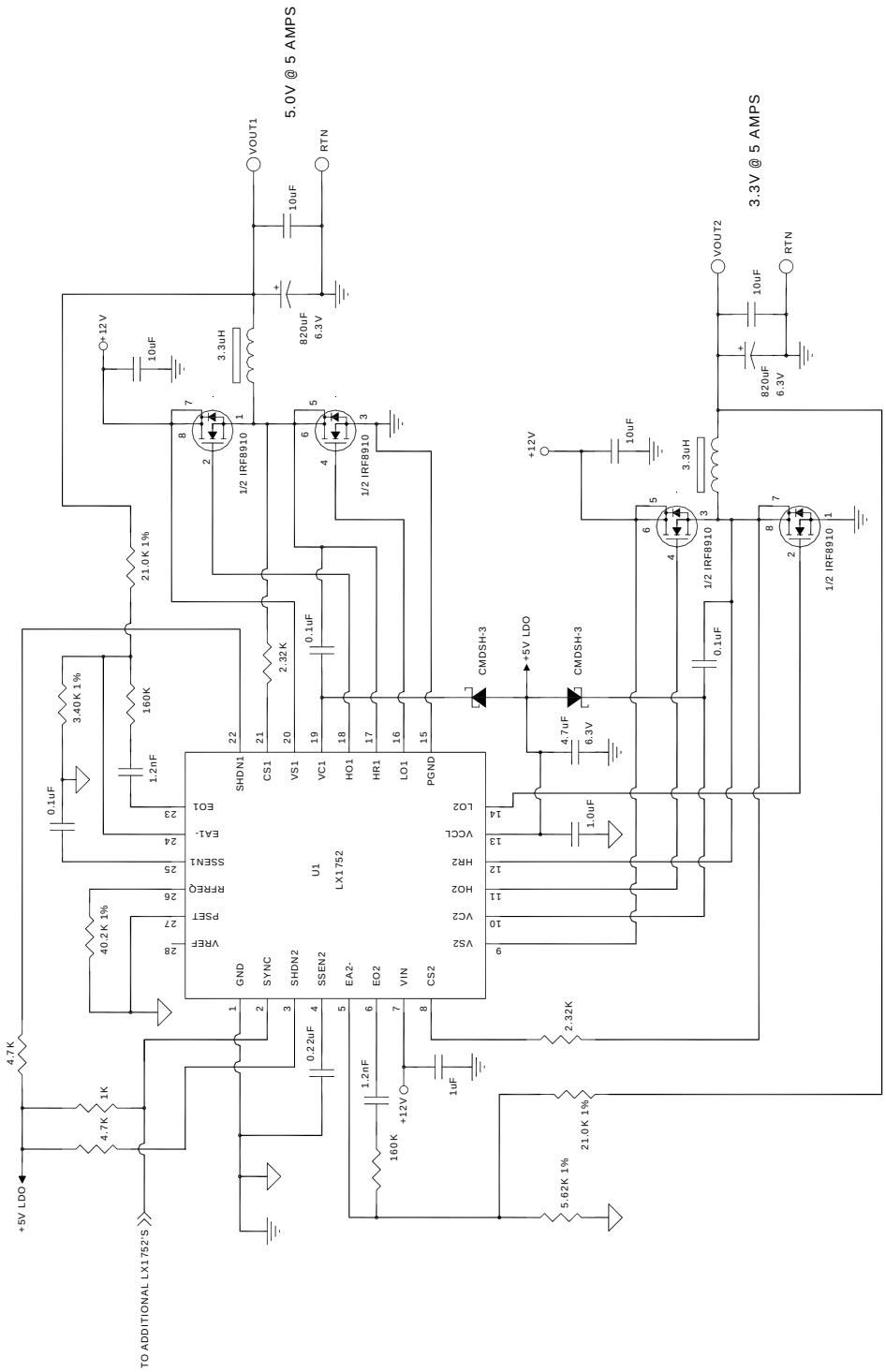

Figure 2 – LX1752 Application Schematic

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THEORY OF OPERATION

DETAIL DESCRIPTION

The LX1752 is an independent dual-output, voltage-mode, Synchronous Buck controller integrated circuit. Output current sensing is through RDS_{ON} measurement of the external power MOSFETs, and is set by a single user-programmable resistor for each output. The internal PWM clock frequency is user programmable from 200kHz to 1.5MHz, via a single programming resistor. Synchronizing of the internal PWM clock is possible for multiple LX1752 ICs using either an internally generated sync pulse, or a sync signal from an external source. Synchronized LX1752 IC's PWM outputs can be phase positioned relative to each other via a single pin configuration, allowing 90°, 120°, or 180° phase separation between outputs. Each of the two LX1752 outputs has external feedback compensation, for flexibility of output filter component selection.

OSCILLATOR FREQUENCY

The LX1752 IC's internal PWM oscillator is user-programmable from 200kHz to 1.5MHz. Programming is provided by a single resistor, R_{FREQ}, connected between the RFREQ and GND pins. The value of this resistor is based on the following formula:

$$R_{FREQ}(K\Omega) = \frac{1}{27.56E^{-9} \times F_{OSC}} - 5.156$$

EXTERNAL CLOCK SYNCHRONIZATION

The LX1752 provides external clock synchronization of the PWM clock, for multiple LX1752 ICs. This feature is implemented via a common buss connected to the LX1752 IC's SYNC pin. The SYNC pin is an I/O pin, with an open drain switch to ground providing the internally-generated output sync pulse. This allows each LX1752 SYNC pin to connect to a common buss in a wired-OR configuration. For proper operation, a pull-up resistor between the LX1752 IC's VCCL and SYNC pins must be provided. The total parallel pull-up resistance must be greater than 500 Ohms for all ICs connected to the common buss. The total pull-up resistance on the SYNC pins is sized such that the sync pulse rise time is (at maximum) less than ½ the PWM clock period. Under synchronized operation, each LX1752 is synchronized to the falling edge of the sync pulse. Multiple LX1752 ICs will synchronize to the controller with the highest PWM clock frequency. For proper operation, it is advised to set one controller's PWM frequency 15% higher than the others to insure it will always provide the master clock frequency.

An externally generated clock pulse may be used to synchronize multiple LX1752 ICs. The LX1752 synchronizes to an external signal by resetting the PWM ramp on the falling edge of the signal input at the SYNC pin. When using an external clock for synchronizing, the external clock should be provided through an open drain or open collector connection, with an external pull-up resistor between the SYNC and VCCL pins. . For proper operation, the external clock frequency must be at least 15% higher than the LX1752 internal PWM frequency set by R_{FREQ}, and external clock widths should be less than ½ the nominal period set by R_{FREQ}. Figure 3 and 4 are an example of an external sync circuit and the resultant waveforms at the moment of sync clock capture.

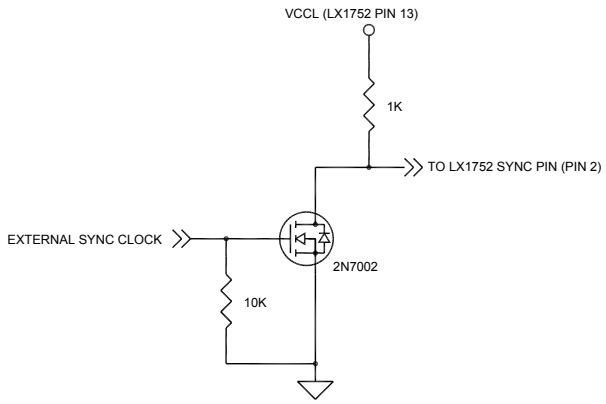

Figure 3. External Sync Circuit

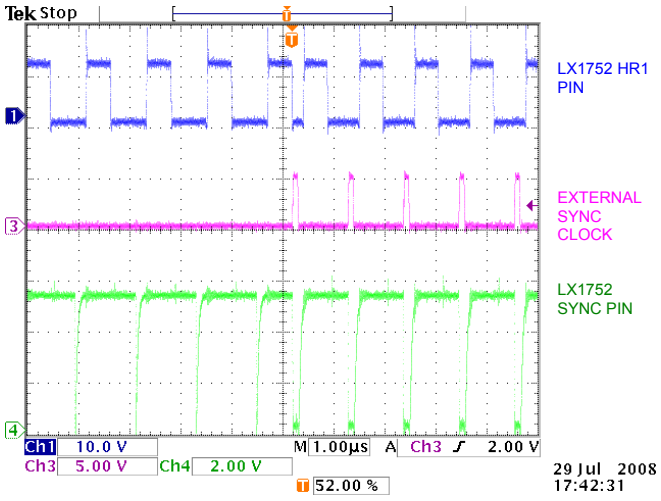

Figure 4. LX1752 External Sync Waveforms

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OUTPUT PHASE POSITIONING

The LX1752 offers phase positioning of the output PWMs. Using two synchronized LX1752 controllers, up to four PWM outputs may be interleaved at 90° intervals or 3 PWM outputs at 120° intervals. Output phase positioning relative to the SYNC pin signal can be configured via the LX1752's PSET pin. The PSET pin is a tri-mode input pin, whose state determines the PWM output's phase relationship.

PSET PIN SETTINGS		
PSET Connection	PWM 1 Position (Relative to SYNC pin signal)	PWM 2 Position (Relative to SYNC pin signal)
VCCL	120°	240°
OPEN	90°	270°
GND	0°	180°

OVER-CURRENT PROTECTION AND HICCUP MODE

The LX1752 senses the $R_{DS(ON)}$ of both the upper (Control) and the lower (Synchronous) MOSFET for current limit detection. RDS_{ON} Sensing is done via three pins: CS_X, VS_X, and PGND. The upper (Control) FET RDS_{ON} is sensed via the CS_X and VS_X pins. The lower (Synchronous) FET RDS_{ON} is sensed via the CS_X and PGND pins. Current limit is set by the resistor on the CS_X pin, and is based on the following calculation:

$$R_{CS} = \frac{I_{LIM} \times RDS_{ON}(max)}{I_{cs}(min)}$$

Where I_{CS} (min) = minimum CS pin programming current

The upper and lower MOSFET current sense contain an internal blanking circuit which delays current sensing for 150ns after their respective MOSFET is switched on. This reduces possible false current limit detection due to ringing. R_{CS} values should be chosen such that delays created by the CS_X resistor and any PCB capacitance on the CS_X pin are less than 100ns; this is to insure the CS_X pin voltage rises faster than the current sense blanking time.

For best operation of the LX1752 current sense circuit, the VS_X pin and CS_X resistor must be Kelvin-connected to their respective output MOSFET Drain and Source pins. When an over current limit is detected, a signal to reset the PWM latch is generated, and the output PWM is truncated on a cycle by cycle basis. After 4 continuous PWM cycles of current limit detection, hiccup mode is started. At the initial start of hiccup mode, the HO_X output MOSFET for that phase is held off, and the soft-start capacitor (C_{SS}) is discharged at a rate 1/25 of the soft-start rate. When the SS pin voltage decreases to the 0.1V PWM enable threshold, the hiccup mode cycle "off time" finishes, the output PWM is switched on, and the circuit soft-starts again. During the soft start period, Hiccup mode is disabled, however, cycle by cycle current limit is functional, insuring output current is kept at the current limit setting. Once $SSEN_X$ reaches 720 mV (90% of the 800mV $SSEN_X$ pin reference voltage), if an over current condition still exists, hiccup mode will again be initiated, the SS capacitor will discharge, and the PWM output will be switched off until the SS voltage decreases to 0.1V. The low duty cycle of hiccup mode, in combination with cycle by cycle current limiting, reduces the power dissipation of the output MOSFETs during a fault condition, thus providing a very reliable and robust overload and short circuit protection

INTERNAL LDO REGULATOR

The LX1752 contains a +5V LDO regulator for providing power to internal circuits, external flying bootstrap capacitors, MOSFET gate drives, and pull-up resistors for the SYNC and SHDN pins. The +5V LDO output is available at the VCCL pin. For proper operation, a minimum 4.7uF capacitor is required between the VCCL and GND pins. Total continuous LDO current should be limited to 100mA.

UNDER VOLTAGE LOCKOUT (UVLO)

At power up, the LX1752 monitors the internal LDO voltage at the VCCL pin. The VIN supply voltage has to be sufficient to produce a voltage greater than the UVLO threshold at the VCCL pin before the controller will come out of the under-voltage lock-out state. At VCCL voltages below the UVLO threshold, Both soft-start (SS) pins are held low, the internal PWM oscillator is disabled, and all MOSFETs are held off.

SOFT-START

Once the VCCL output is above the UVLO threshold, a capacitor connected between the SS_X and GND pins begins charging by a 20kΩ internal resistor connected to an 800mV reference. The capacitor voltage at the SS pin rises as a simple RC circuit. The voltage at the SS pin controls its respective output voltage through the error amplifier's non-inverting input. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor. Due to the exponential rise of the SSX pin voltage, the fastest output voltage rate of rise occurs during the first time constant of the SSX capacitor, and the internal 20KΩ resistor. During this period, the feedback reference voltage will reach 63% of its nominal setting. This rate of rise can be

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used to calculate the average startup current seen by the inductor:

$$I_{STARTUP} = C_{OUT} \frac{.63 \times V_{OUT}}{20E^3 \times C_{SS}} + I_{LOAD}$$

For lowest in-rush currents, soft start capacitors should be sized such that the output voltage rise is slower than the input voltage (VIN) rise during power-up.

EXTERNAL PWM ENABLE

The LX1752's PWM outputs can be disabled externally by holding the SS_X pin below 0.1V with an open drain transistor connected to ground. At SS_X pin $\leq$ 0.1V, both output MOSFETS are held off. Using this method, PWM enable and soft start can be controlled through an external signal. This method is useful for controlled power-up sequencing.

BUFFERED VREF OUTPUT

The LX1752 provides a buffered output of the internal 800mV reference. This output may be used as a reference for an external LDO or any application where an 800mV reference is required. Current is limited to a maximum of 1mA from this output.

EXTERNAL FEEDBACK AND COMPENSATION COMPONENTS

The LX1752 has pin access to each output's respective error amplifier inverting and output signals. This topology offers full freedom for output filter component selection and control loop optimization for stable high bandwidth operation. See compensation section below.

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OUTPUT INDUCTOR SELECTION

The Output Inductor value is selected based on the desired ripple current. Inductor Ripple current should be in the range of 20% to 40% of the maximum output current. Higher inductance values result in lower peak to peak ripple current, at the expense of slower transient response. Lower inductor values provide a higher current slew rate in response to a step change in load current, however peak to peak ripple current increases, requiring an output filter capacitor with a smaller ESR specification to meet output ripple voltage requirements. The Inductor value can be calculated by:

$$L = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE}} \times \frac{D}{F_{SW}}$$

Where D = Operating Duty Cycle
F_{SW} = PWM Switching Frequency
I_{RIPPLE} = Desired Peak to Peak Ripple Current

OUTPUT CAPACITOR SELECTION

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage rating requirements, which affect overall stability, output ripple voltage, and step load transient response.

The output ripple has three components: variation in the charge stored in the output capacitor, the voltage drop across the ESR, and the voltage drop across the ESL, caused by the current into and out of the capacitor. The following equations estimate the worst-case output ripple voltage:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

Where:

$$V_{RIPPLE(ESR)} = I_{RIPPLE} \times ESR$$

$$V_{RIPPLE(C)} = \frac{I_{RIPPLE}}{8 \times C \times F_{SW}}$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L + ESL}$$

High output current may require paralleling multiple capacitors to meet output ripple requirement, as it reduces ESR and ESL, which are the major contributors to output ripple voltage.

For step load conditions, capacitor ESR will be the dominant factor determining the size of the initial output voltage excursion. Capacitor ESR should be selected such that:

$$ESR \times (I_{RIPPLE} + \Delta I) < V_{TRANSIENT}$$

Where I_{RIPPLE} = peak to peak inductor ripple current
ΔI is the maximum load current step change
$V_{TRANSIENT}$ is the maximum allowed output voltage excursion during a load step change

A second consideration when determining the output capacitor is the minimum capacitance value required to limit voltage overshoot during a large load release, such as a transient from full load to no load. In this case, the output capacitor must be large enough to absorb the excess energy present in the inductor. Minimum output capacitance is based on the desired maximum overshoot and output inductor value, and is calculated by the following formula:

$$C_{MIN} = \frac{(I_{TRAN})^2 \times L}{(V_{OUT} + V_{OVERSHOOT})^2 - V_{OUT}^2}$$

Where I_{TRAN} = specified maximum load transient (full load to no load)
L = output inductor value
$V_{OVERSHOOT}$ = maximum allowable voltage overshoot

INPUT CAPACITOR SELECTION

RMS ripple current is the primary factor when selecting the input capacitor. Input RMS ripple current is based on operating duty cycle (D), and is at a maximum at D = 50%.

The following formula is used for calculating the input RMS current for each output:

$$I_{INRMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

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Input capacitance is largely dependent on the source impedance of the power source; however, for most cases the general rule of thumb is to use a total minimum capacitance of 10uF for every ampere of input ripple current. This is best achieved through a combination of ceramic capacitors placed as close to the output FETS as possible, and an electrolytic capacitor placed in close proximity to the LX1752 and it's associated circuit components.

FEEDBACK AND COMPENSATION COMPONENT SELECTION

The LX1752 is a voltage mode controller that uses external feedback components to establish output DC voltage and closed-loop bandwidth. This control scheme consists of an error amplifier, whose output controls a PWM modulator, which in turn drives an LC filter to produce the DC output (See Figure 5). A simple way to analyze the closed loop system is to break the loop and separate the elements into two sections: first, the combined PWM modulator and output LC filter, called the Control To Output section, and second, the Error Amplifier section (See Figure 6). Once separated, the total gain through the two sections is analyzed.

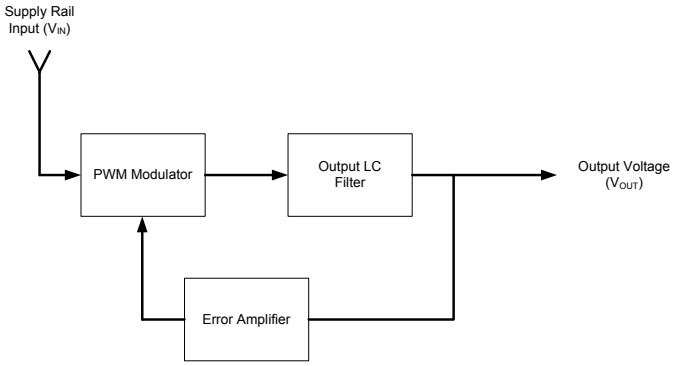

Figure 5. Voltage Mode Control Scheme

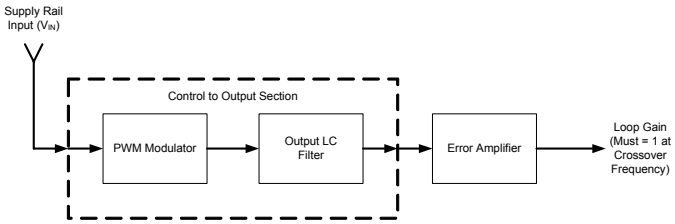

Figure 6. Separating the Loop Components

To achieve a proper closed loop system, first the crossover frequency is determined, after which the Control To Output Section is analyzed for it's gain and rolloff response at that frequency. Once the response at the crossover frequency is known, the error amplifier compensation components are chosen such that the overall gain of the two sections is equal to 1 (or 0dB) at the crossover frequency:

$$G_{FC} = G_{CTO} \times G_{EAXO} = 1$$

Where G_{FC} = loop gain at crossover frequency

G_{CTO} = Control To Output Section Gain at crossover frequency

G_{EAXO} = Error Amplifier Section Gain at crossover frequency

The LC filter creates a complex pole (-2 Slope) in the Control To Output Section's response, along with a zero created by the output capacitor ESR. So, in addition to the Gain of 1 at the crossover frequency, the phase response of the Error Amplifier Section must be designed such that the response of the Control To Output Section is compensated to achieve a first order response (-1 slope) at the crossover frequency (See Figure 7). This will insure that the phase margin at the crossover frequency is greater than 45°. This is accomplished by designing the Error Amplifier's response to counteract the pole and zero created by the output LC filter.

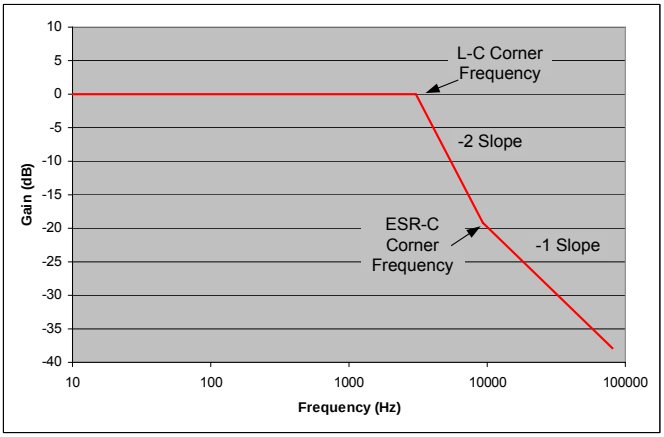

Figure 7. Output Filter Gain Vs. Frequency

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When selecting feedback and compensation components, the following steps are required:

1) Determine the input resistor value.
2) Determine the output voltage setting resistor.
3) Determine the Control-To-Output gain at the desired crossover frequency.
4) Determine the Error Amplifier gain at the desired crossover frequency.
5) Decide if Type Two or Type Three compensation is used
6) Calculate the feedback components for the desired compensation type.

1. DETERMINE THE INPUT RESISTOR VALUE:

The input resistor is sized based on the error amplifier input bias current specification. High bias currents can create output voltage errors in large-value input resistors due to the IR drop created by this current. The LX1752 has a specified input bias current of 30nA (max.). This will generate a 30uV (max.) output voltage error for every 1k Ω of input resistance. This error is small enough to neglect in most cases. For this example, use 21kΩ (See Figure 8).

2. DETERMINE THE OUTPUT VOLTAGE SETTING RESISTOR:

The voltage setting resistor is the resistor connected between the error amplifier's inverting input and ground. This resistor, in conjunction with the input resistor, forms a DC voltage divider that determines the output voltage level (see Figure 8). Because the voltage divider is connected to the input of the error amplifier, the control loop will force the DC output voltage such that the voltage developed across the setting resistor will equal the feedback voltage reference, V_{FB}. V_{FB} for the LX1752 is specified at a nominal 0.7V at room temperature. The following equation determines the voltage setting resistor:

(Equation 1) $$R_{SET} = \frac{R_{INPUT} \times 0.7}{V_{OUT} - 0.7}$$

For our example, If R_{INPUT} = 21kΩ, and desired V_{OUT} = 5V, then R_{SET} = 3.42kΩ.

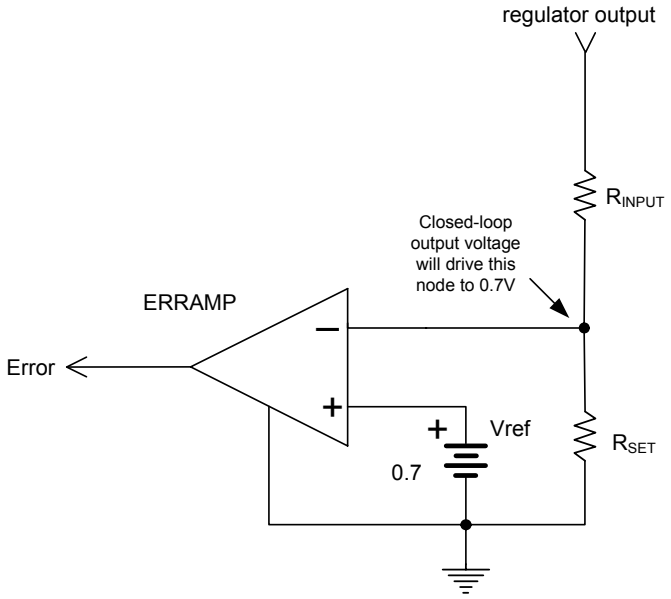

Figure 8. Output DC Setting Resistors

3. DETERMINE THE CONTROL TO OUTPUT GAIN AT THE DESIRED CROSSOVER FREQUENCY:

The first step in determining the control to output gain is to decide on the closed-loop bandwidth, or crossover frequency of the system. Bandwidths that are too wide (high crossover frequency) can amplify switching noise. Bandwidths that are too low will have poor transient response times.

The general rule-of-thumb is that the crossover frequency (F_C) should be no greater than $1/5^{th}$ the switching frequency, or :

(Equation 2) $$F_C \leq \frac{F_{SW}}{5}$$

The error amplifier gain will limit the maximum crossover frequency. The total bandwidth capable will be based on the output filter components, the DC input voltage, and the error amplifier gain. A good rule of thumb would be to limit the bandwidth to 100kHz or less.

Once the crossover frequency has been determined, the next step is to determine the total input to output gain of the Control to Output Section at the crossover frequency. The input to output gain expression for the Control to Output Section is:

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(Equation 3) $$G_{CTO} = V_{IN} \times G_{PWM} \times G_{LC}$$

Where V_{IN} = DC input voltage to the output Mosfets
G_{PWM} = PWM Modulator Gain
G_{LC} = Output LC filter Gain

The PWM Modulator Gain is based on the peak to peak PWM ramp voltage, and is simply:

(Equation 4) $$G_{PWM} = \frac{1}{V_{RAMP}}$$

Where V_{RAMP} = the peak to peak ramp amplitude

The LX1752 has a nominal ramp amplitude = 1.2V

The output LC filter creates two frequency corners in the output response: First, a complex pole with -2 slope (40dB/Decade) rolloff and 180° phase shift is created at the LC resonance frequency. Second, a zero, is created at the output capacitor and its respective Equivalent Series Resistance (ESR) corner frequency.

These two frequency corners are found by the following equations:

(Equation 5) $$F_P = \frac{1}{2\pi\sqrt{LC}}$$

And

(Equation 6) $$F_Z = \frac{1}{2\pi(RC)}$$

Where L = Output Filter Inductor
C = Output Filter Capacitor
R = Output Filter Capacitor ESR

At the crossover frequency, the LC filter's response can be found using the calculated pole and zero. This method of calculating the response will depend on the relationship of the output capacitor-ESR zero corner frequency to the chosen crossover frequency:

(Equation 7) $$G_{LC} = \frac{F_P^{\,2}}{(F_Z \times F_C)};F_Z \le F_C$$

Or

(Equation 8) $$G_{LC} = \left(\frac{F_P}{F_C}\right)^2;F_Z > F_C$$

Example Calculations:

Using the application circuit:
V_{IN} = 12V
L = 3.3uH
C= 820uF
ESR = 21mΩ
Ramp Amplitude = 1.2V
Crossover Frequency = 80kHz
Using equations 5 and 6, find the pole and zero frequency corners:

$$F_P = \frac{1}{2\pi\sqrt{3.3E^{-6} \times 820E^{-6}}} = 3.06kHz$$

$$F_Z = \frac{1}{2\pi \times 21E^{-3} \times 820E^{-6}} = 9.25kHz$$

The ESR-capacitor zero frequency of our example is less than the crossover frequency. Use equation 7 to determine the LC filter gain at the crossover frequency:

$$G_{LC} = \frac{3.06kHz^2}{9.25kHz \times 80kHz} = 12.65E^{-3}$$

The PWM Modulator gain is found using equation 4:

$$G_{PWM} = \frac{1}{1.2} = 833E^{-3}$$

Using Equation 3, the total Control to Output Section gain at the crossover can be determined:

$$G_{CTO} = 12 \times 833E^{-3} \times 12.65E^{-3} = 126.45E^{-3}$$

4. DETERMINE THE ERROR AMPLIFIER GAIN AT THE DESIRED CROSSOVER FREQUENCY:

Our example Control to Output Section gain is 0.12645 at the crossover frequency. The error amplifier gain required for unity gain at the crossover frequency will be:

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(Equation 9) $$G_{EAXO} = \frac{1}{G_{CTO}} = \frac{1}{126.45E^{-3}} = 7.908$$

Once the required Error Amplifier gain is determined, the Error Amplifier open loop gain should be examined to assure the Error Amplifier has enough open-loop gain at the crossover frequency to satisfy the above gain requirement:

(Equation 10) $$G_{EAXO} \le \frac{G_{EAOL}}{\left(\frac{G_{EAOL} \times 2\pi \cdot F_C}{2\pi \cdot F_{EAOL}}\right) + 1}$$

Where G_{EAOL} = Error Amplifier Open Loop Gain

F_{EAOL} = Error Amplifier Open Loop Bandwidth

Using the LX1752 Error Amplifier as an example:

G_{EAOL} = 70dB, gain magnitude = 3162

F_{EAOL} = 10MHz

$$\frac{3162}{\left(\frac{3162 \times 2\pi \times 80\text{kHz}}{2\pi \times 10\text{MHz}}\right) + 1} = 120.24$$

The above equation shows there is ample Error Amplifier open-loop gain available at the crossover frequency.

5. DECIDE IF TYPE TWO OR TYPE THREE COMPENSATION IS USED.

At this point, the compensation type can be decided. The two standard methods for compensating a Voltage Mode Buck converter are Type Two and Type Three compensation (the name references the number of compensating slopes in the response; Type Two has two, Type Three has three). See Figures 9 & 10. Both Type Two and Type Three compensation are identical in that they are designed to offset the complex pole and ESR zero of the output LC filter. Where they differ is in the number of compensating poles and zeros provided. Type Two compensation is known as a "single pole-zero" compensation, in that it supplies a single compensating zero, and a single compensating pole in the Error Amplifier's response. The Type Three compensation is known as "pole-zero pair" compensation, in that it supplies two compensating poles and two compensating zeros. The deciding factor for which of the two methods of compensating the loop can be used is based on the amount of available phase margin present in the Control to Output Section at the crossover frequency. Because Type Two compensation does not provide an extra phase boost after the complex LC pole, the phase boost provided by the output capacitor – ESR combination is critical when using Type Two compensation. Therefore, the relationship of the complex LC pole, F_P, to the ESR-capacitor zero, $F_{Z,}$ becomes important: if Fz/Fp is 5 or less, then Type Two Compensation may be used. Type Three compensation should be used otherwise.

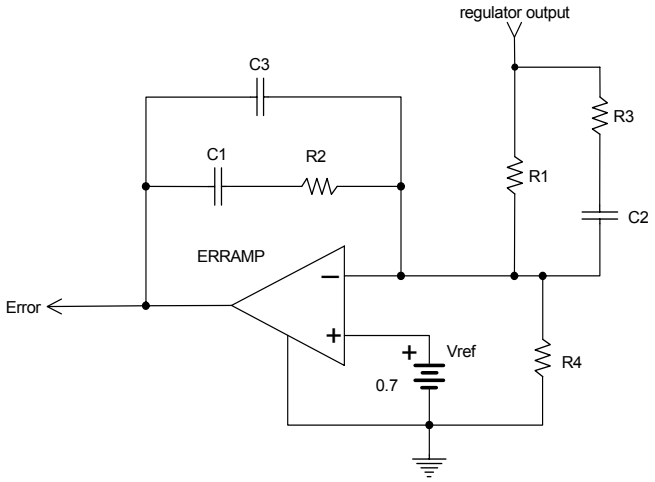

Figure 9. Type 3 Compensation

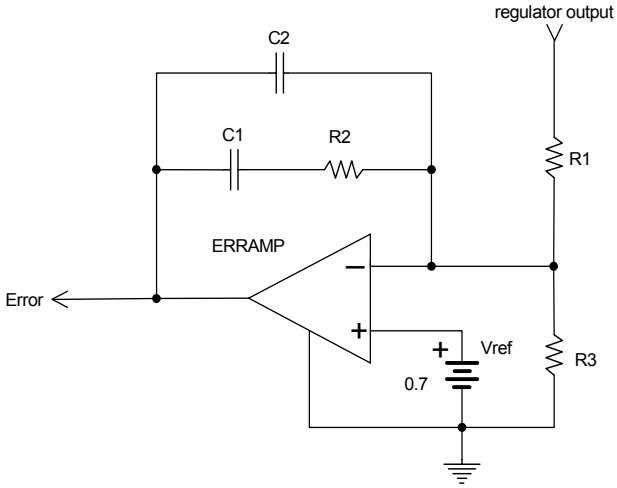

Figure 10. Type 2 Compensation

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TYPE THREE COMPENSATION COMPONENT SELECTION.

Type Three compensation contains 2 poles and 2 zeros in the feedback loop to counteract the complex pole created by the L-C output filter, and the zero created by the ESR - output capacitor. Type 3 compensation should be used when the desired crossover frequency is lower than the ESR zero frequency, or when it is higher than the ESR zero frequency and the ESR zero frequency is higher than 4 to 5 times the output LC filter corner frequency. Typical feedback response is shown in Figure 11.

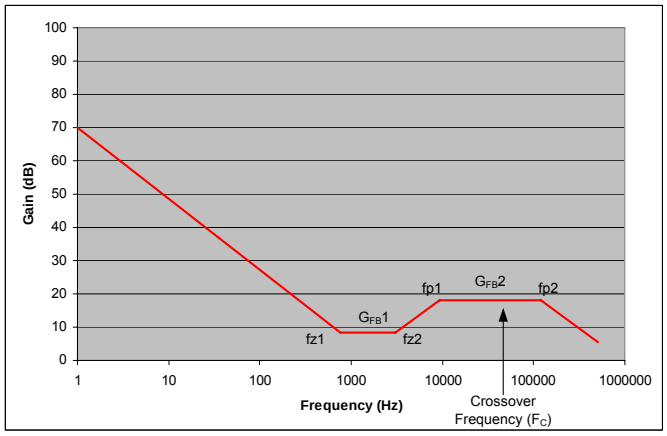

Figure 11. Typical Type 3 Feedback Response

To calculate the values, first the two compensation zeros and two compensation poles must be set.

The two compensation zeros are set to counteract the complex L-C pole at two locations, both multiples of the complex L-C pole:

1. Set the first compensation zero frequency (fz1) to the L-C pole/4:

(Equation 11) $$f_Z1 = \frac{F_P}{4}$$

2. Set the second compensation zero frequency (f_Z2) equal to the L-C pole frequency:

(Equation 12) $$f_Z2 = F_P$$

3. Next, the first compensation pole (f_P1) is set equal to the ESR - capacitor zero frequency:

(Equation 13) $$f_P1 = F_Z$$

4. Finally, the last compensation pole (f_P2) is set equal to 1/2 the switching frequency:

(Equation 14) $$f_P2 = \frac{F_{SW}}{2}$$

In order for the feedback response to be correct, the feedback loop must be set to two gain levels, $G_{FB}1$, and $G_{FB}2$

$G_{FB}2$ is the highest gain value of the two levels, and is the gain required to boost the control to output gain to 1 at the crossover frequency. $G_{FB}2$ is established after the first compensation pole frequency (f_P1), and is the complement of the total control to output gain (G_{CTO}) at the selected crossover frequency:

(Equation 15) $$G_{FB}2 = \frac{1}{G_{CTO}}$$

$G_{FB}1$ is the gain level established after the first compensation zero frequency (fz1). $G_{FB}1$ gain is derived from the crossover frequency gain ($G_{FB}2$). The method for calculating $G_{FB}1$ is dependent on whether the output capacitor – ESR zero corner frequency is greater or less than the crossover frequency.

Condition 1; $F_Z \le F_C$

(Equation 16) $$G_{FB}1 = G_{FB}2 \times \left(\frac{f_Z2}{f_P1}\right)$$

Condition 2; $F_C \le F_Z$

This condition occurs when the capacitor-ESR zero frequency corner is greater than the chosen cutoff frequency. This is a common condition with ceramic output capacitors. For this condition, $G_{FB}1$ is found by:

(Equation 17) $$G_{FB}1 = G_{FB}2 \times \left(\frac{f_Z2}{F_C}\right)$$

To calculate the compensation component values (Reference Figure 9):

First, select resistor R1. This topic is covered under "Determine the Input Resistor Value" on page 17. Resistor R4 may be selected at this time; however it is for setting the output DC level only, and is not used in the compensation calculations. R4 is covered under "Determine the Output Voltage Setting Resistor" on page 17.

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Next, calculate the value of R2; R1 & R2 will set the gain for $G_{FB}1$:

(Equation 18) $$R2 = R1 \times G_{FB}1$$

Calculate the value for C1; C1 & R2 set the first zero frequency:

(Equation 19) $$C1 = \frac{1}{2\pi(f_Z1)R2}$$

The next value is for R3; R3||R1 & R2 set the gain for $G_{FB}2$:

(Equation 20) $$R3 = \frac{R1 \times R2}{(R1 \times G_{FB}2) - R2}$$

Calculate C2; C2 & R1 + R3 set the second zero frequency:

(Equation 21) $$C2 = \frac{1}{2\pi(f_Z2)(R1 + R3)}$$

Finally, the value for C3 + C1 & R2 sets the second pole frequency:

(Equation 22) $$C3 = \frac{C1}{(2\pi(f_P2) \cdot C1 \cdot R2) - 1}$$

The first pole frequency, f_P1, will be correct with the values chosen. To verify:

(Equation 23) $$f_P1 = \frac{1}{2\pi(R3C2)}$$

Example Calculations:

Assume the following design parameters and component values:

- V_{IN} = 3.4V
- V_{OUT} = 1.24V
- V_{RAMP} = 1.2V
- PWM frequency = 800kHz
- Error Amplifier Gain = 3162 (70dB)
- Error Amplifier Bandwidth = 10MHz
- Output Inductor (L) = 2.2uH
- Output Capacitor (C) = 3000uF (2 X 1500uF capacitors in parallel)
- Capacitor ESR = 5.5mΩ (2 capacitor ESR values of 11mΩ in parallel)
- Crossover Frequency = 80kHz

Referencing Figure 7:

Step 1 – Determine the input resistor (R1) value:

Keep the input resistor value as low as practical to reduce input bias errors. For this example, choose 10.7kΩ 1% (1% part for DC output voltage accuracy).

Step 2 – Determine the DC output "setting" resistor (R4):

Using Equation 1, and the values chosen for R_{INPUT} and V_{OUT}:

R_{SET} (R4) = 13.6kΩ. Use 13.7kΩ 1% (1% part for DC output voltage accuracy).

Step 3 – Determine the Control to Output Section Gain:

Using Equation 5, and the values chosen for L and C:

F_P = 1.96kHz

Using Equation 6, and the values chosen for ESR and C:

F_Z = 9.65kHz

The ESR – Capacitor zero frequency is less than the chosen crossover frequency. Use Equation 7 to calculate the gain of the LC filter section:

G_{LC} = 4.974E-3

Using Equation 4, PWM modulator gain is:

G_{PWM} = 0.833

Finally, using Equation 3 and the chosen VIN value of 3.4V:

G_{CTO} = 14.086E-3

Step 4 - Determine required Error Amplifier Gain:

Using Equation 9, the required Error Amplifier Gain:

G_{EAXO} = 71

Use Equation 10 to determine the Error Amplifier open-loop gain at the crossover frequency:

$G_{EAXO} \leq 120.2$

Based on equation 10, there is enough gain available.

Step 5 – Determine Type Two or Type Three compensation:

For this example, F_Z/F_P is greater than 4. We will use Type Three Compensation.

Step 6 – Select Type Three components (reference Figure 9):

Using Equations 11 through 14, determine the compensation frequency components:

fz1 = 490Hz

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fz2 = 1.96kHz
fp1 = 9.65kHz
fp2 = 400kHz

Calculate the highest of the two feedback gains using Equation 15:

$G_{FB}2 = 71$

The ESR – Capacitor zero frequency is less than the chosen crossover frequency. Use Equation 16 to calculate the lower of the two feedback gains:

$G_{FB}1 = 14.4$

Using Equations 18 through 22, calculate the values for the compensation components:

R2 = 154kΩ; use 150kΩ 5%
R3 = 2.72kΩ; use 2.7kΩ 5%
C1 = 2.11nF; use 2.2nF
C2 = 6.05nF; use 5.6nF
C3 = 2.6pF; too small; omit this capacitor.

In this example, C3 value of 2.6pF is far too small to be of practical use. In this case it may be omitted without any consequence. If the additional roll off provided by C3 is still desired, the value of R_{INPUT} (R1) may be set lower, and the feedback components recalculated. This will raise the value of C3. As an alternative, set F_P2 to a lower frequency, however do not set lower than 1.5 X the crossover frequency (F_C). Figure 12 is the schematic of the example feedback compensation.

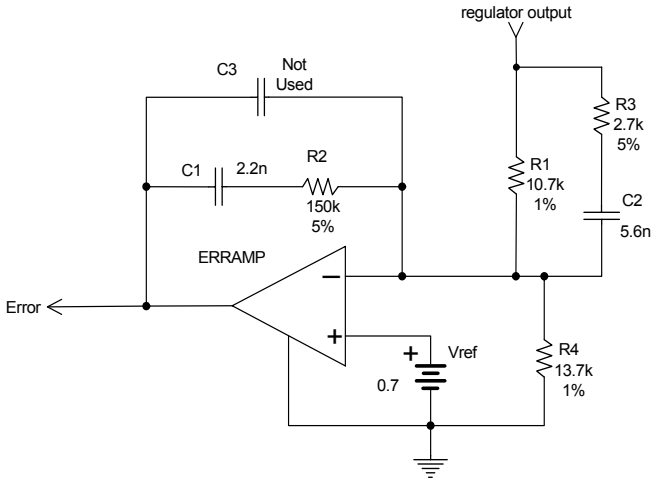

Figure 12. Example Circuit Feedback and Compensation

Figure 13 is the Bode Plot of the closed loop response of our example.

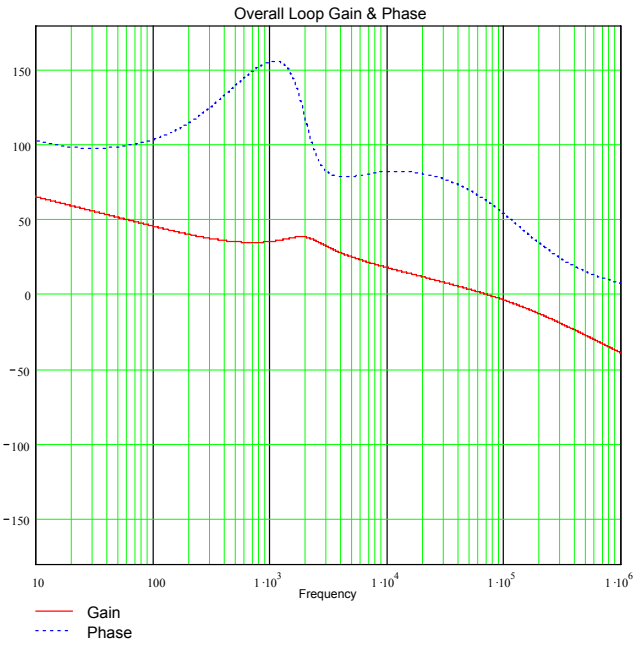

Figure 13. Bode Plot of Example Circuit

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TYPE TWO COMPENSATION COMPONENT SELECTION.

Type Two compensation contains a single zero and pole in the feedback loop to counteract the complex pole created by the L-C output filter. This type of compensation does not provide an extra phase boost after the complex LC pole frequency, which is provided by Type 3 compensation. This type of compensation is used when the phase margin of the Control to Output section is greater than the minimum closed loop phase margin desired at the crossover frequency. Typical frequency response is shown in Figure 14.

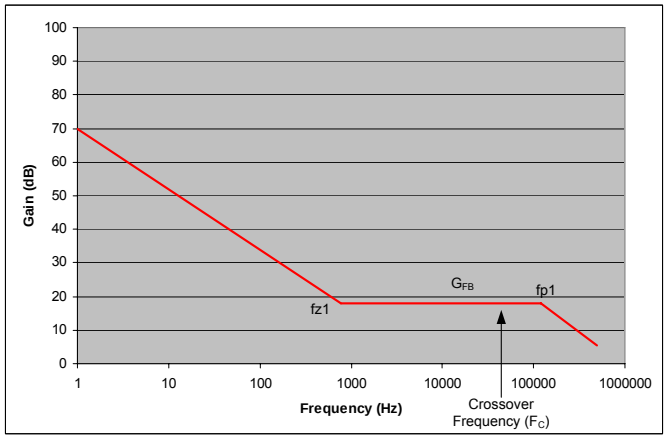

Figure 14. Typical Type 2 Feedback Response

The component values for Type 2 compensation are found using identical equations and methods as in Type 3. The main differences are that Type 2 has only one gain level, one compensating zero, and one compensating pole to calculate.

As in Type 3 Compensation, establish the frequency corners:

1. Set the first compensation zero frequency (fz1) to the L-C pole/4:

(Equation 24) $$f_Z1 = \frac{F_P}{4}$$

2. Set the compensation pole (f_P1) equal to 1/2 the switching frequency:

(Equation 25) $$f_P1 = \frac{F_{SW}}{2}$$

Type Two compensation has only one gain level to be concerned with. This is the gain required to boost the control to output gain to 1 at the crossover frequency:

(Equation 26) $$G_{FB} = \frac{1}{G_{CTO}}$$

To calculate the compensation component values (Reference Figure 8):

First, select resistor R1. This topic is covered under "Determine the Input Resistor Value" on page 15. Resistor R3 may be selected at this time; however it is for setting the output DC level only, and is not used in the compensation calculations. R3 is covered under "Determine the Output Voltage Setting Resistor" on page 16.

Next, calculate the value of R2; R1 & R2 will set the gain for G_{FB}:

(Equation 27) $$R2 = R1 \times G_{FB}$$

Calculate the value for C1; C1 & R2 set the compensating zero frequency:

(Equation 28) $$C1 = \frac{1}{2\pi(f_Z1)R2}$$

Finally, the value for C2 + C1 & R2 sets the compensating pole frequency:

(Equation 29) $$C2 = \frac{C1}{(2\pi(f_P1)\cdot C1\cdot R2) - 1}$$

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OUTPUT MOSFET SELECTION

When selecting output MOSFETs, There are five important parameters to be concerned with: Maximum V_{DS} rating, Maximum Drain Current rating, RDS_{ON}, Total Gate Charge, and Maximum Power Dissipation.

The upper and lower MOSFET positions, in many cases, can be satisfied with the same part value FET, making the use of dual MOSFET packages attractive. However, in cases where output current and switching frequency are high, the MOSFET chosen for the upper (Control) FET may differ from the lower (Synchronous) FET.

For example, in a high frequency switcher application, the power dissipated in the Control FET may be more dependent on switching losses, in which case a FET with a lower total gate charge (Qg) should be considered. The opposite is true for the Synchronous FET, where conduction losses may be the dominating factor in the total power dissipation. In this case a FET with a lower RDS_{ON} would be considered.

The maximum V_{DS} rating of the MOSFET should exceed by at least 10% the maximum DC input voltage, plus any voltage transients that might be present on the DC line, over all operating temperatures.

The maximum drain current rating of the MOSFET should be chosen to cover all operating current conditions, at all operating temperatures. Overcurrent limits, and current spikes should all be considered before selecting a MOSFET.

RDS_{ON} and total gate charge should always be as small as possible. RDS_{ON} and total gate charge (Qg) will vary inversely with each other; ie. lower gate charges typically are at the expense of higher RDS_{ON} ratings.

MOSFETs must be chosen such that their maximum power dissipation is not exceeded at any time in the application, and that the junction temperature for the device does not exceed the maximum rating for the part under all conditions. The power dissipation of the MOSFET will depend largely on two principle factors affecting loss: conduction losses, and switching losses.

At lower frequency switching, conduction losses make up the bulk of the total power dissipation in the MOSFETs. Two factors determine conduction losses: channel conduction losses (for both Control and Synchronous FETs), and body diode conduction losses (Synchronous FET only).

For conduction losses in the Control (Upper) FET, channel loss is the only concern (under normal operation the body diode does not conduct). Channel loss is due to the IR drop across the MOSFET's RDS_{ON}. When calculating channel loss, RDS_{ON} should be specified at the maximum junction temperature of the FET. Most datasheets specify RDS_{ON} at 25°C, and provide a graph for estimating the RDS_{ON} at a specific junction temperature. Channel loss for the upper FET ($PD_{RDS(CONTROL)}$) can be calculated with the following formula:

(Equation 30)

$$PD_{RDS(CONTROL)}(W) = \frac{(I_{LOAD})^2 \times RDS_{0N} \times V_{OUT}}{V_{IN}}$$

Note: specify RDS_{ON} at maximum junction temperature.

For conduction losses in the Synchronous (Lower) FET, both channel and body diode losses must be considered. As in the Control FET calculations, channel loss is a function of RDS_{ON}, and should be evaluated using the specified RDS_{ON} at the part's specified maximum junction temperature:

(Equation 31)

$$PD_{RDS(SYNC)}(W) = (I_{LOAD})^2 \times RDS_{0N} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Note: specify RDS_{ON} at maximum junction temperature.

In addition to channel loss, body diode conduction loss must be considered. Body diode conduction loss (PD_{BD}) is found using the following equation:

(Equation 32)

$$PD_{BD(SYNC)}(W) = 2 \times I_{LOAD} \times V_F \times T_{DT} \times F_{SW}$$

Where V_F = Body Diode Forward Voltage

T_{DT} = PWM output dead time

F_{SW} = PWM output switching frequency

Switching losses for the Synchronous FET are limited to the gate input losses due to the input capacitance (C_{ISS}). PD_{CISS} is found by:

(Equation 33)

$$PD_{CISS(SYNC)}(W) = 0.5 \times C_{ISS} \times (V_{GS})^2 \times F_{SW}$$

Where V_{GS} = peak gate drive voltage

Most datasheets specify C_{ISS} in a graph of capacitance vs. V_{DS}. Due to the zero voltage switching of the Synchronous FET, C_{ISS} should be chosen at $V_{DS} = 0$ for this calculation.

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Total power loss in the Synchronous FET will be the sum of the conduction and the switching losses:

(Equation 34)

$$PD_{(SYNC)}(W) = PD_{RDS(SYNC)} + PD_{BD(SYNC)} + PD_{CISS(SYNC)}$$

Switching losses in the Control FET are due to overlap switching loss, gate input loss, losses due to MOSFET capacitances, and Synchronous FET body diode reverse recovery charge.

To calculate overlap switching loss, first the average gate current must be calculated. This is found through by the average of the upper and lower drive RDS_{ON}, added to the MOSFET internal gate resistance, which is specified on most datasheets. If not specified, 2.0 Ohms may be substituted. In the LX1752, the average drive on-resistance is 3.0Ω. Average gate current can now be found by:

(Equation 35) $$I_G = 0.5 \times \frac{V_{GS}}{R_{DRIVE} + R_{GATE}}$$

Where R_{DRIVE} = average controller gate drive On resistance

R_{GATE} = MOSFET gate resistance

Once average gate current is known, the next step is to calculate the average gate switching time:

(Equation 36) $$T_S = \frac{Q_{GS2} + Q_{GD}}{I_G}$$

Where Q_{GS2} is the portion of gate to source gate charge after the gate reaches Vth to the plateau of the gate charge curve, and Q_{GD} is MOSFET gate-drain charge. Refer to the MOSFET datasheet for more detail.

With switching time (T_S), load current, PWM frequency, and maximum V_{IN} known, overlap switching loss can be calculated by:

(Equation 37) $$PD_{OLS} = I_{OUT} \times T_S \times V_{IN} \times F_{SW}$$

Gate input loss (PD_{GATE}) is found by:

(Equation 38)

$$PD_{GATE} = Q_G \times V_{GS} \times F_{SW} \times \frac{R_{GATE}}{R_{DRIVE} + R_{GATE}}$$

Where:

F_{SW} = PWM switching frequency

R_{GATE} = gate input resistance

Where Q_G = total gate charge (datasheet value)

V_{GS} = peak gate drive voltage

R_{DRIVE} = high side driver on resistance

Losses due to Synchronous FET reverse body diode recovery are based on Q_{RR}, a parameter not clearly defined in most datasheets. A good rule of thumb would be to increase the total power dissipation due to switching loss by 20% to account for losses due to Q_{RR} and MOSFET capacitances. The total Control FET switching loss would be the sum of the losses, increased by 20%:

(Equation 39)

$$PD_{SW(CONTROL)} = (PD_{OLS} + PD_{GATE}) \times 1.2$$

Total power dissipation in the Control FET can now be calculated:

(Equation 40)

$$PD_{CONTROL}(W) = PD_{SW(CONTROL)} + PD_{RDS(CONTROL)}$$

Once the power dissipations of both MOSFETS are known, the operating junction temperatures can be calculated using thermal resistance specifications contained in the MOSFET datasheet.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Careful attention to PCB layout is necessary to insure proper operation with minimal noise generation. When laying out the PCB, these guidelines should be followed:

1) Keep the input capacitor, output capacitor, output inductor and output MOSFETs (upper and lower), close together, and tie all high current output returns directly to a suitable power ground plane.
2) Keep the high current ground return paths separate from the signal return paths. It is recommended that a separate signal ground plane be used, with a common tie point between the power ground plane and the signal ground plane established at the IC signal ground pin.
3) Place the input decoupling capacitor has close to the upper and lower MOSFETs as practical. Connections between this capacitor and the upper and lower MOSFET's Drain and Source connections should be as

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short as practical.

4) The LDO filter capacitor should be placed as close to the VCCL pin as practical.
5) PGND connection to the Source pin of the Lower MOSFET should be as short as practical, and should be established with a direct connection (using no vias) if possible.
6) VS_X Pin connections should be Kelvin connected directly at the Upper MOSFET's drain pin(s).
7) HR_X connection to the Upper MOSFET's Source pin should be as short as practical, and should be established with a direct connection (using no vias) if possible.
8) LO_X and HO_X should be connected to their respective MOSFET gate pins with as short a trace as practical, and should be established with a direct connection (using no vias) if possible.
9) Stray capacitance to ground on CSx pins should be minimized. If possible, remove ground and power planes in the area directly below CS_X pins, and place each respective CS_X resistor as close to the LX1752 as practical; preferably on the same PCB side as the LX1752.
10) Place all compensation and feedback components as close to their respective error amplifier pins as practical. Keep the error amplifier input connections (EA_X-) as short as possible.
11) Place the frequency programming resistor, R_{FREQ} as close to the RFREQ and GND pins as practical.
12) Refer to the Evaluation Board for an example of the PCB layout.

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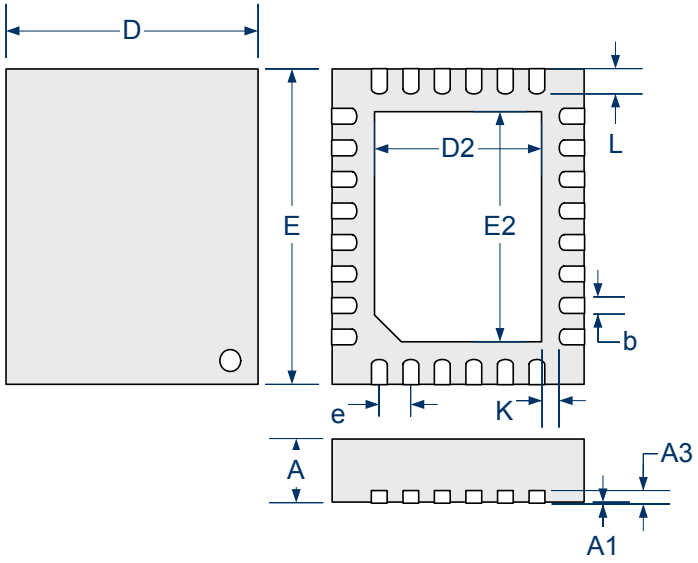
PACKAGE DIMENSIONS

LQ 28-Pin 4x5mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.02	0	0.008
A3	0.20 REF		0.008 REF	
K	0.20 REF		0.008 REF	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	2.50	2.75	0.098	0.108
E2	3.50	3.75	0.138	0.148
D	4.00 BSC		0.158 BSC	
E	5.00 BSC		0.197 BSC	

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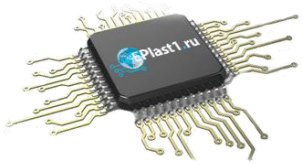
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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