

NVMFD5877NL

Power MOSFET

60 V, 39 mΩ, 17 A, Dual N-Channel, Logic Level, Dual SO8FL

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- 175°C Operating Temperature
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^{\circ}\text{C}$	I_D	17	A
		$T_{mb} = 100^{\circ}\text{C}$		12	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		$T_{mb} = 25^{\circ}\text{C}$	P_D	23	W
		$T_{mb} = 100^{\circ}\text{C}$		12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	6	A
		$T_A = 100^{\circ}\text{C}$		5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25^{\circ}\text{C}$	P_D	3.2	W
		$T_A = 100^{\circ}\text{C}$		1.6	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	74	A
Operating Junction and Storage Temperature			T_J , T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	19	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^{\circ}\text{C}$, $V_{DD} = 24\text{ V}$, $V_{GS} = 10\text{ V}$, $R_G = 25\text{ }\Omega$)	$(I_{L(pk)} = 14.5\text{ A}$, $L = 0.1\text{ mH})$		E_{AS}	10.5	mJ
	$(I_{L(pk)} = 6.3\text{ A}$, $L = 2\text{ mH})$			40	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Note 2, 3)	$R_{\Psi J-mb}$	6.5	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

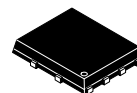
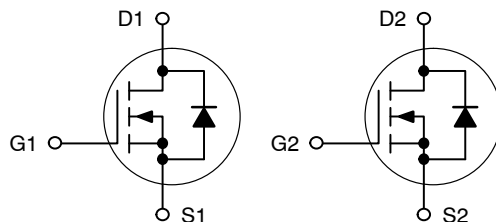


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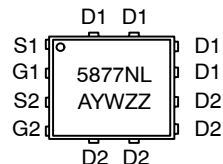
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	39 mΩ @ 10 V	17 A
	60 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



5877NL = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5877NLT1G	DFN8 (Pb-Free)	1500/Tape & Reel
NVMFD5877NLT3G	DFN8 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFD5877NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			53		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			3.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		31	39	mΩ
		V _{GS} = 4.5 V, I _D = 7.5 A		42	60	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 5.0 A		7.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		540		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			36		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 5.0 A		5.9		nC
Threshold Gate Charge	Q _{G(TH)}			0.62		
Gate-to-Source Charge	Q _{GS}			1.64		
Gate-to-Drain Charge	Q _{GD}			2.80		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48V, I _D = 5.0A		11	20	nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 5.0 A, R _G = 2.5 Ω		8.1		ns
Rise Time	t _r			15.8		
Turn-Off Delay Time	t _{d(off)}			11.8		
Fall Time	t _f			3.9		
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 5.0 A, R _G = 2.5 Ω		4.9		ns
Rise Time	t _r			6.4		
Turn-Off Delay Time	t _{d(off)}			14.5		
Fall Time	t _f			2.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5.0 A	T _J = 25°C	0.8	1.2	V
			T _J = 125°C	0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 5.0 A		14.5		ns
Charge Time	t _a			11.5		
Discharge Time	t _b			3.1		
Reverse Recovery Charge	Q _{RR}			11		nC

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		0.93		nH
Drain Inductance	L _D			0.005		
Gate Inductance	L _G			1.84		
Gate Resistance	R _G			1.5		Ω

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

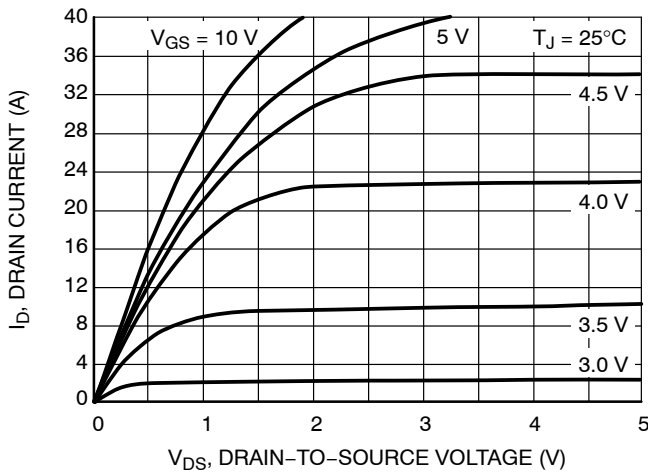


Figure 1. On-Region Characteristics

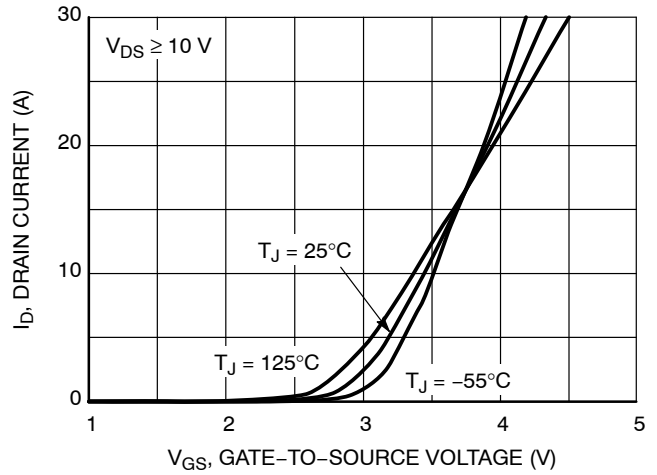


Figure 2. Transfer Characteristics

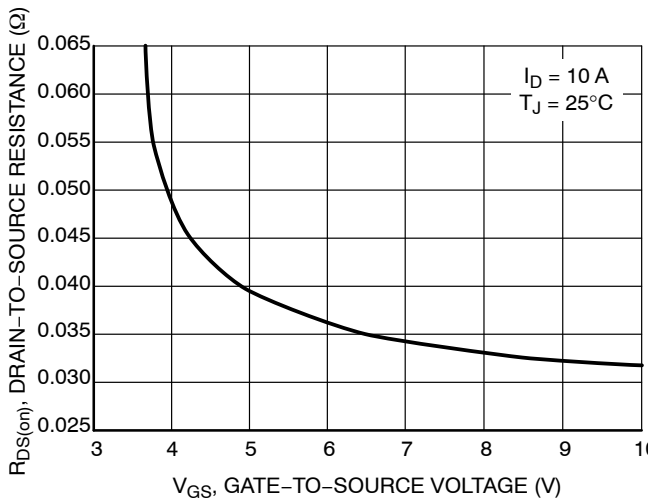


Figure 3. On-Resistance vs. Gate-to-Source Voltage

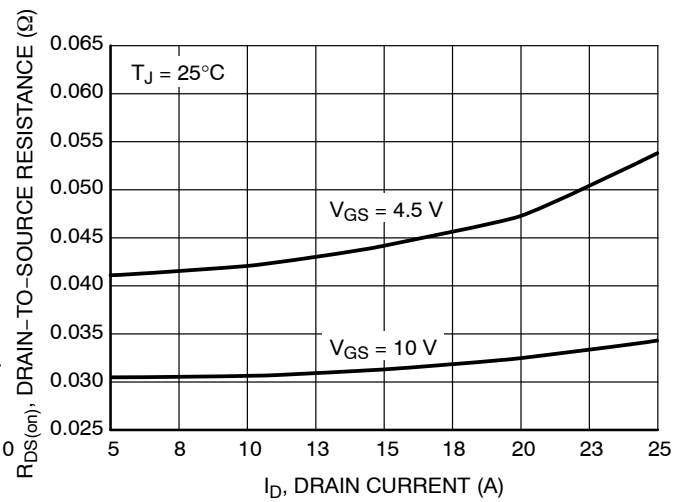


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

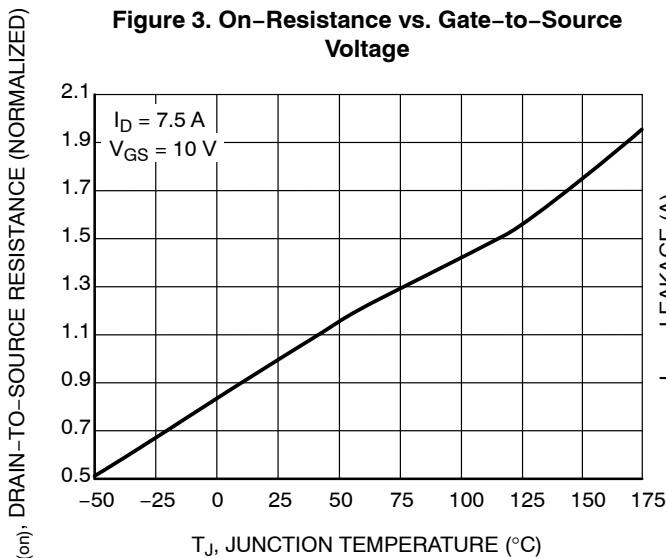


Figure 5. On-Resistance Variation with Temperature

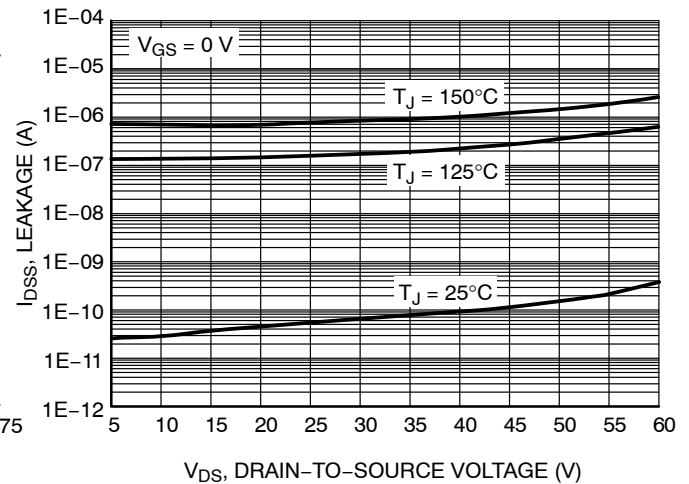


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

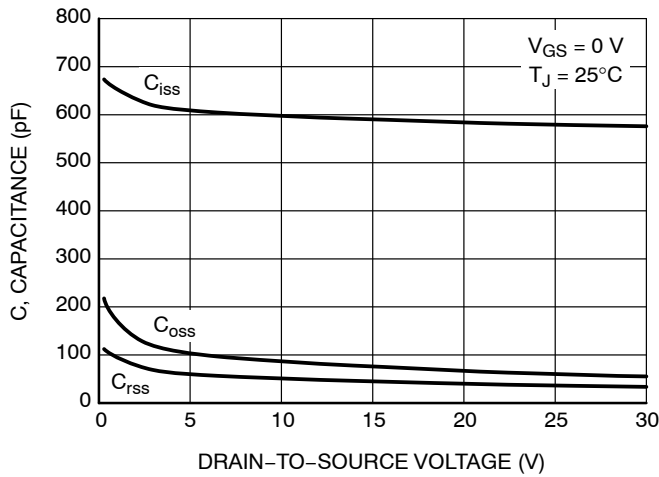


Figure 7. Capacitance Variation

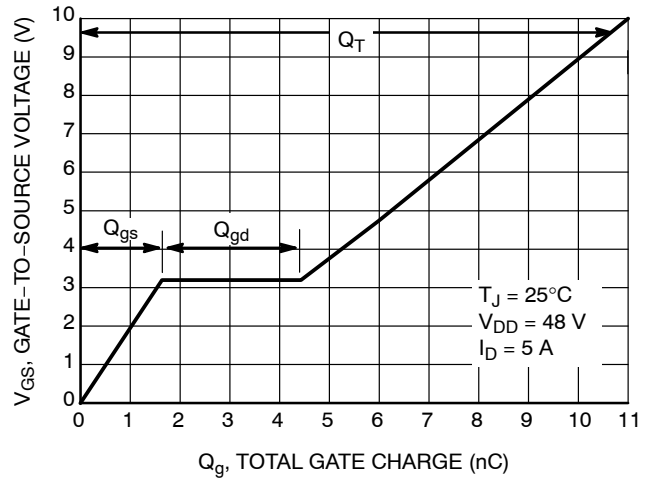


Figure 8. Gate-to-Source vs. Gate Charge

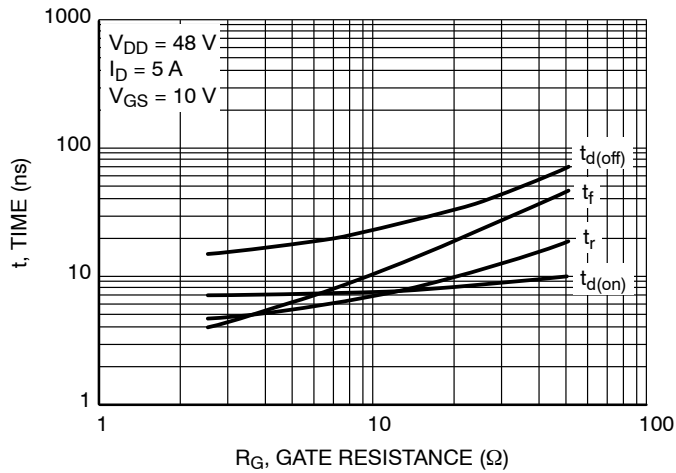


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

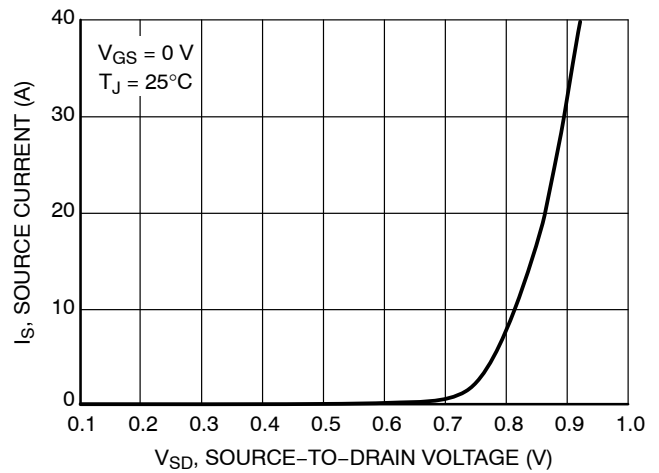


Figure 10. Diode Forward Voltage

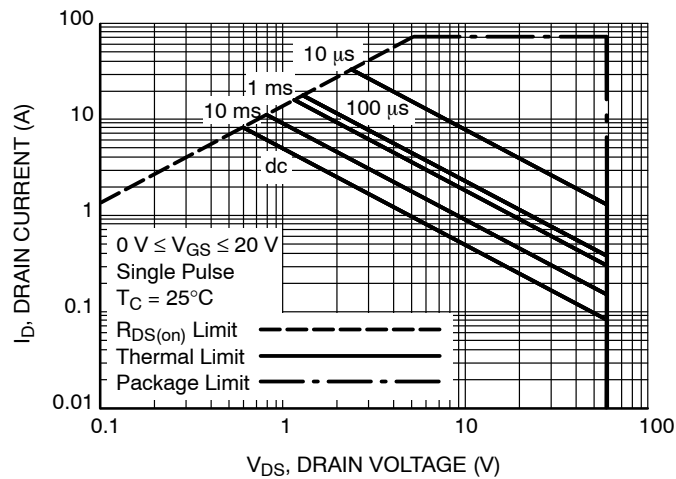


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

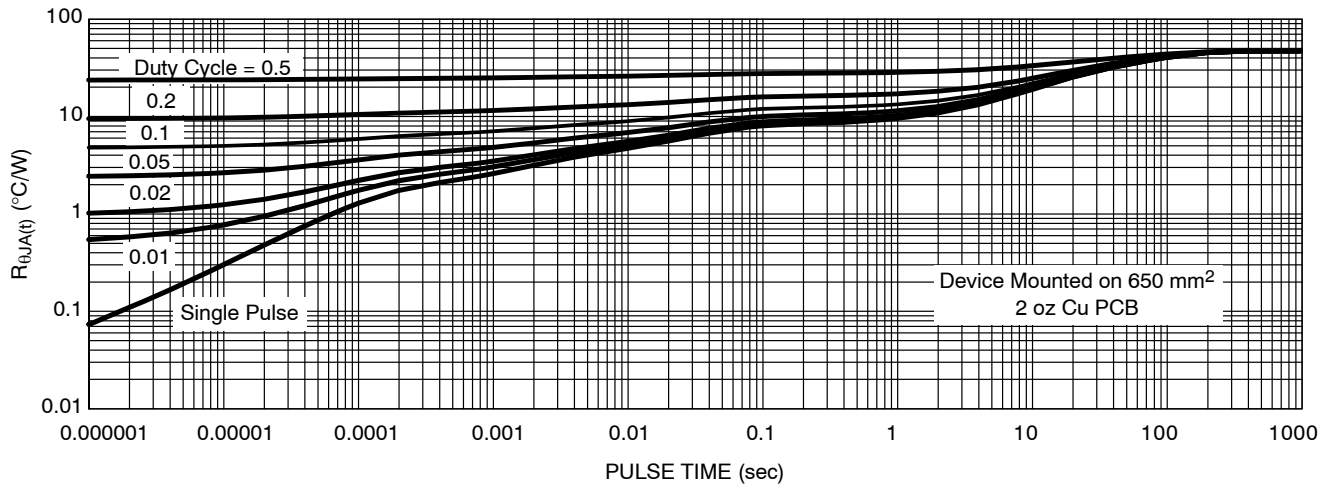
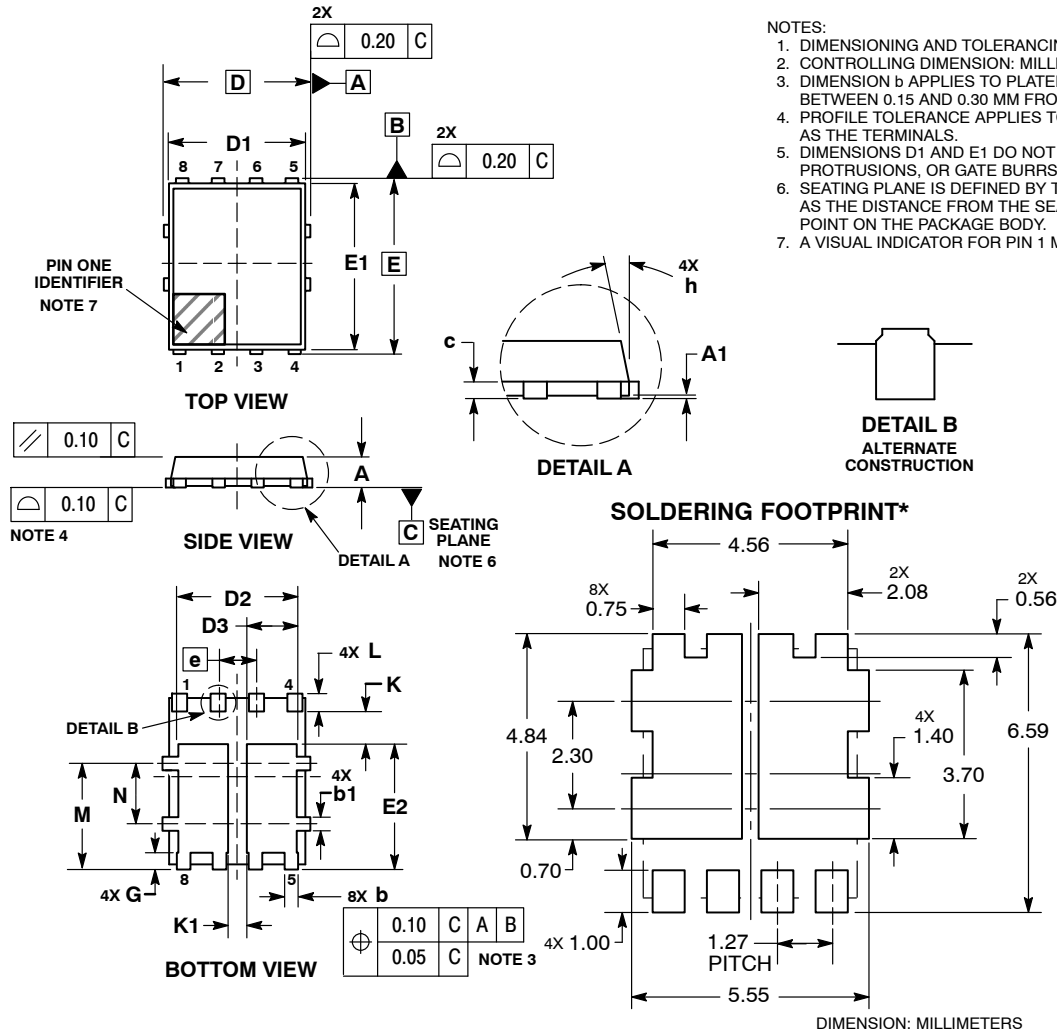


Figure 12. Thermal Response

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)
CASE 506BT
ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

MILLIMETERS			
DIM	MIN	MAX	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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