

# Sound Processor with Built-in 3-band Equalizer

## BD37532FV

### General Description

BD37532FV is a sound processor with built-in 3-band equalizer for car audio. A stereo input selector is available that functions to switch single end input and ground isolation input, input-gain control, main volume, loudness, 5ch fader volume and LPF for subwoofer. Moreover, "Advanced switch circuit", which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). Also, "Advanced switch" makes control of microcomputer easier, and constructs a high quality car audio system.

### Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, middle, treble, loudness by using advanced switch circuit
- Built-in differential input selector that can make various combination of single-ended / differential input.
- Built-in ground isolation amplifier inputs, which is ideal for external stereo input.
- Built-in input gain controller reduces volume switching noise for portable audio input.
- Decreased number of external components due to built-in 3-band equalizer filter, LPF for subwoofer and loudness filter. It is possible to freely control Q, Gv, fo of 3-band equalizer and fc of LPF, Gv of loudness by I<sup>2</sup>C BUS control.
- A gain adjustment quantity of ±20dB with a 1 dB step gain adjustment is possible for bass, middle and treble.
- Equipped with terminals for subwoofer outputs. Also, the audio signal outputs of the front, rear and subwoofer can be chosen using the I<sup>2</sup>C BUS control.
- Energy-saving design resulting in low current consumption is achieved utilizing the BiCMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Input pins and output pins are organized and separately laid out in such a way that it simplifies the pattern layout of the PCB and decreases the board dimensions.
- It is possible to control I<sup>2</sup>C BUS with 3.3V / 5V.

### Applications

It is optimal for car audio systems. It can also be used for audio equipments like mini Compo, micro Compo, TV etc.

### Key Specifications

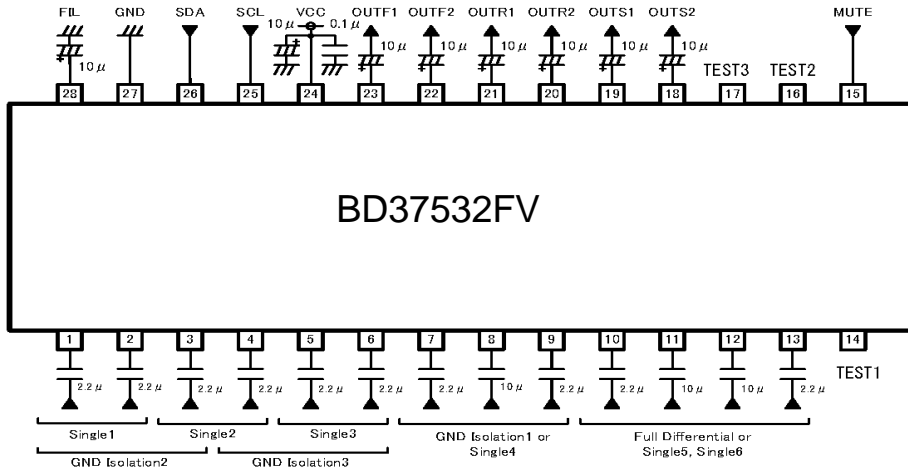
■ Power Supply Voltage Range:	7.0V to 9.5V
■ Circuit Current (No Signal):	38mA(Typ)
■ Total Harmonic Distortion 1: (FRONT,REAR)	0.001%(Typ)
■ Total Harmonic Distortion 2: (SUBWOOFER)	0.002%(Typ)
■ Maximum Input Voltage:	2.3Vrms(Typ)
■ Crosstalk Between Selectors:	-100dB(Typ)
■ Volume Control Range:	+15dB to -79dB
■ Output Noise Voltage 1: (FRONT,REAR)	3.8μVrms(Typ)
■ Output Noise Voltage 2: (SUBWOOFER)	4.8μVrms(Typ)
■ Residual Output Noise Voltage:	1.8μVrms(Typ)
■ Operating Temperature Range:	-40°C to +85°C

### Package

W(Typ) x D(Typ) x H(Max)



Typical Application Circuit

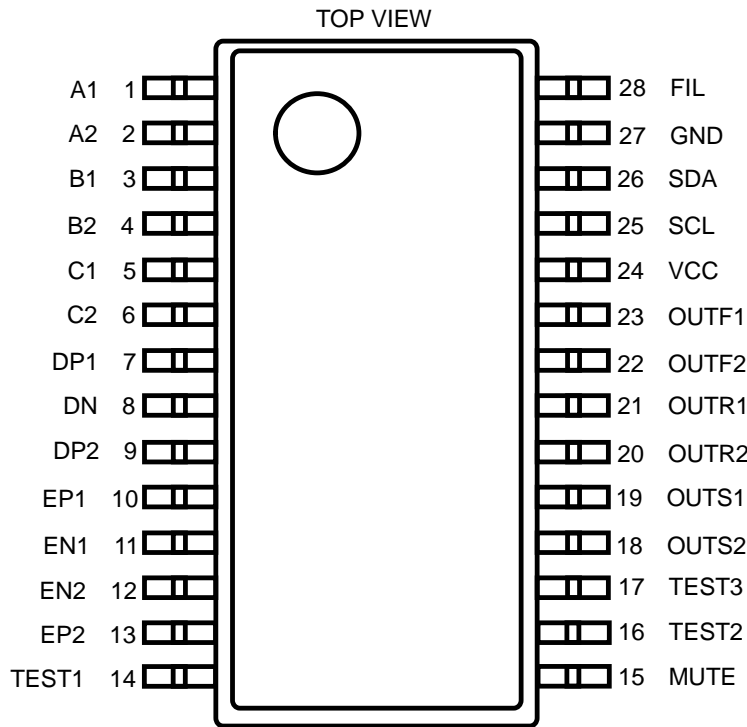


About single input 1 to 3, it is possible to change from single input to GND Isolation input 2,3.

About GND Isolation1 and Full Differential, it is possible to change from differential input to single input 4 to 6.

Unit  
R : [Ω]  
C : [F]

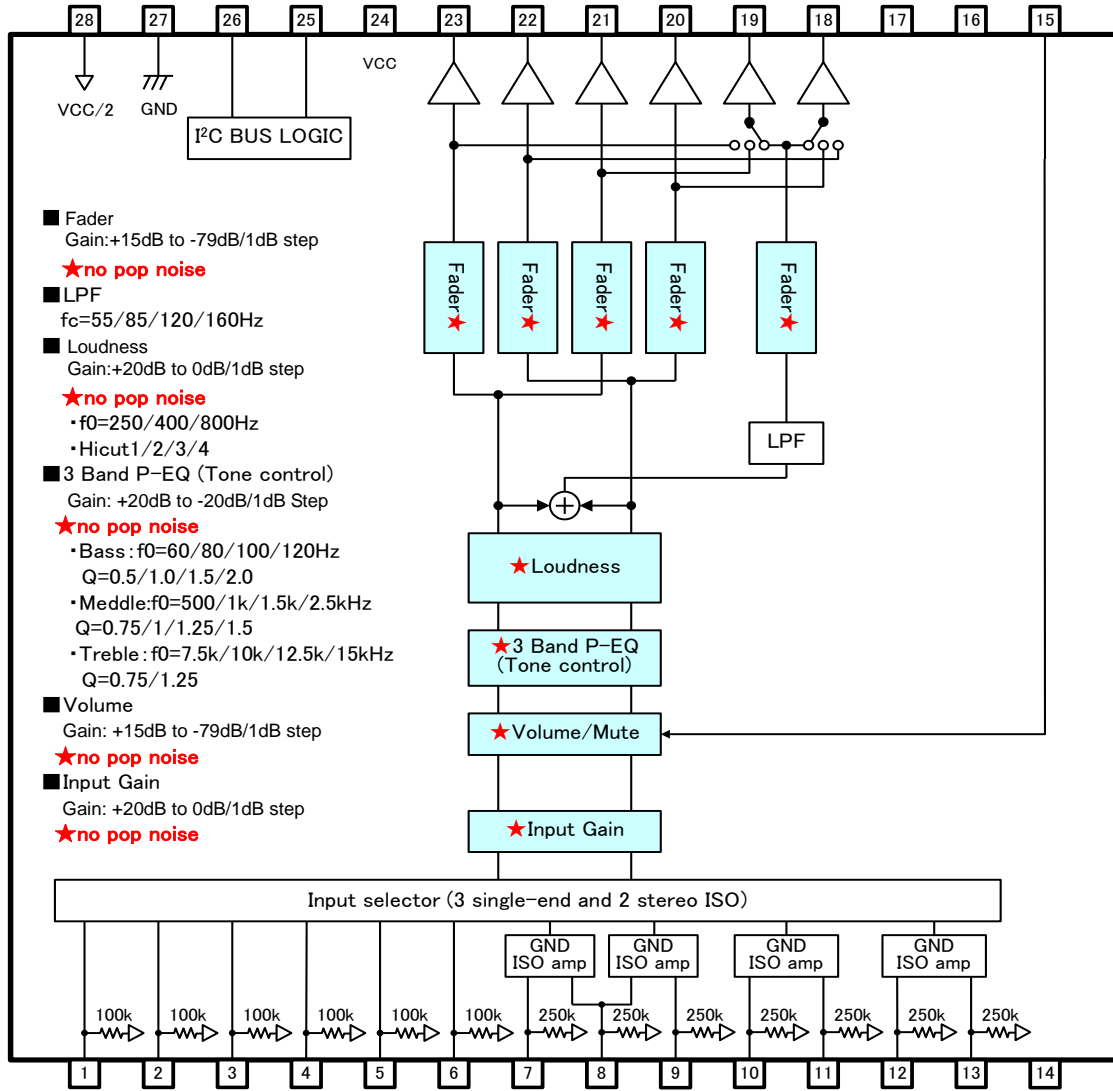
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	15	MUTE	External compulsory mute terminal
2	A2	A input terminal of 2ch	16	TEST2	Test pin
3	B1	B input terminal of 1ch	17	TEST3	Test pin
4	B2	B input terminal of 2ch	18	OUTS2	Subwoofer output terminal of 2ch
5	C1	C input terminal of 1ch	19	OUTS1	Subwoofer output terminal of 1ch
6	C2	C input terminal of 2ch	20	OUTR2	Rear output terminal of 2ch
7	DP1	D positive input terminal of 1ch	21	OUTR1	Rear output terminal of 1ch
8	DN	D negative input terminal	22	OUTF2	Front output terminal of 2ch
9	DP2	D positive input terminal of 2ch	23	OUTF1	Front output terminal of 1ch
10	EP1	E positive input terminal of 1ch	24	VCC	Power supply terminal
11	EN1	E negative input terminal of 1ch	25	SCL	I <sup>2</sup> C Communication clock terminal
12	EN2	E negative input terminal of 2ch	26	SDA	I <sup>2</sup> C Communication data terminal
13	EP2	E positive input terminal of 2ch	27	GND	GND terminal
14	TEST1	Test pin	28	FIL	VCC/2 terminal

Block Diagram



**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Rating	Unit
Power supply Voltage	V <sub>CC</sub>	10.0	V
Input voltage	V <sub>IN</sub>	V <sub>CC</sub> +0.3 to GND-0.3	V
Power Dissipation	P <sub>d</sub>	1.06 (Note 1)	W
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

(Note 1) When mounted on ROHM Standard board(70x70x1.6 (mm<sup>3</sup>), derate by 8.5mW/°C for Ta=25°C or more.  
Thermal resistance θ<sub>ja</sub> = 117.6(°C/W)

Material : A FR4 glass epoxy board(3% or less of copper foil area)

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommended Operating Conditions**

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V <sub>CC</sub>	7.0 to 9.5	V
Temperature	T <sub>opr</sub>	-40 to +85	°C

**Electrical Characteristics**

(Unless otherwise noted, Ta=25°C, V<sub>CC</sub>=8.5V, f=1kHz, V<sub>IN</sub>=1Vrms, R<sub>g</sub>=600Ω, R<sub>L</sub>=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF, Fader 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current	I <sub>Q</sub>	-	38	48	mA	No signal
	Voltage Gain	G <sub>V</sub>	-1.5	0	+1.5	dB	G <sub>V</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Channel Balance	CB	-1.5	0	+1.5	dB	CB = G <sub>V1</sub> -G <sub>V2</sub>
	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V <sub>OUT</sub> =1Vrms BW=400Hz-30KHz
	Total Harmonic Distortion 2 (SUBWOOFER)	THD+N2	-	0.002	0.05	%	V <sub>OUT</sub> =1Vrms BW=400Hz-30KHz
	Output Noise Voltage 1 (FRONT,REAR) *	V <sub>NO1</sub>	-	3.8	15	μVrms	R <sub>g</sub> = 0Ω BW = IHF-A
	Output Noise Voltage 2 (SUBWOOFER) *	V <sub>NO2</sub>	-	4.8	15	μVrms	R <sub>g</sub> = 0Ω BW = IHF-A
	Residual Output Noise Voltage *	V <sub>NOR</sub>	-	1.8	10	μVrms	Fader = -∞dB R <sub>g</sub> = 0Ω BW = IHF-A
	Crosstalk Between Channels*	CTC	-	-100	-90	dB	R <sub>g</sub> = 0Ω CTC=20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
Ripple Rejection	RR	-	-70	-40	dB	f=1kHz V <sub>RR</sub> =100mVrms RR=20log(V <sub>CC</sub> IN/V <sub>OUT</sub> )	
INPUT SELECTOR	Input Impedance (A, B, C)	R <sub>IN_S</sub>	70	100	130	kΩ	
	Input Impedance (D, E)	R <sub>IN_D</sub>	175	250	325	kΩ	
	Maximum Input Voltage	V <sub>IM</sub>	2.1	2.3	-	Vrms	V <sub>IM</sub> at THD+N(V <sub>OUT</sub> )=1 % BW=400Hz-30KHz
	Crosstalk Between Selectors *	CTS	-	-100	-90	dB	R <sub>g</sub> = 0Ω CTS=20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
Common Mode Rejection Ratio * (D, E)	CMRR	50	65	-	dB	XP1 and XN input XP2 and XN input CMRR=20log(V <sub>IN</sub> /V <sub>OUT</sub> ) BW = IHF-A,[*X · · · D,E]	

Electrical Characteristics – continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
INPUT GAIN	Minimum Input Gain	G <sub>IN_MIN</sub>	-2	0	+2	dB	Input gain 0dB V <sub>IN</sub> =100mVrms G <sub>IN</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Input Gain	G <sub>IN_MAX</sub>	+18	+20	+22	dB	Input Gain +20dB V <sub>IN</sub> =100mVrms G <sub>IN</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Gain Set Error	G <sub>IN_ERR</sub>	-2	0	+2	dB	Gain=+20dB to +1dB
MUTE	Mute Attenuation *	G <sub>MUTE</sub>	-	-105	-85	dB	Mute ON G <sub>MUTE</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
VOLUME	Maximum Gain	G <sub>V_MAX</sub>	13	15	17	dB	Volume = 15dB V <sub>IN</sub> =100mVrms G <sub>V</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Attenuation *	G <sub>V_MIN</sub>	-	-100	-85	dB	Volume = -∞dB G <sub>V</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
	Attenuation Set Error 1	G <sub>V_ERR1</sub>	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB
	Attenuation Set Error 2	G <sub>V_ERR2</sub>	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G <sub>V_ERR3</sub>	-4	0	+4	dB	ATT=-48dB to -79dB
BASS	Maximum Boost Gain	G <sub>B_BST</sub>	18	20	22	dB	Gain=+20dB f=100Hz V <sub>IN</sub> =100mVrms G <sub>B</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Cut Gain	G <sub>B_CUT</sub>	-22	-20	-18	dB	Gain=-20dB f=100Hz V <sub>IN</sub> =2Vrms G <sub>B</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Gain Set Error	G <sub>B_ERR</sub>	-2	0	+2	dB	Gain=+20dB to -20dB f=100Hz
MIDDLE	Maximum Boost Gain	G <sub>M_BST</sub>	18	20	22	dB	Gain=+20dB f=1KHz V <sub>IN</sub> =100mVrms G <sub>M</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Cut Gain	G <sub>M_CUT</sub>	-22	-20	-18	dB	Gain=-20dB f=1kHz V <sub>IN</sub> =2Vrms G <sub>M</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Gain Set Error	G <sub>M_ERR</sub>	-2	0	+2	dB	Gain=+20dB to -20dB f=1kHz
TREBLE	Maximum Boost Gain	G <sub>T_BST</sub>	18	20	22	dB	Gain=+20dB f=10kHz V <sub>IN</sub> =100mVrms G <sub>T</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Cut Gain	G <sub>T_CUT</sub>	-22	-20	-18	dB	Gain=-20dB f=10kHz V <sub>IN</sub> =2Vrms G <sub>T</sub> =20log (V <sub>OUT</sub> /V <sub>IN</sub> )
	Gain Set Error	G <sub>T_ERR</sub>	-2	0	+2	dB	Gain=+20dB to -20dB f=10kHz
FADER / SUBWOOFER	Maximum Boost Gain	G <sub>F_BST</sub>	13	15	17	dB	Fader=15dB V <sub>IN</sub> =100mVrms G <sub>F</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Maximum Attenuation *	G <sub>F_MIN</sub>	-	-100	-90	dB	Fader = -∞dB G <sub>F</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> ) BW = IHF-A
	Gain Set Error	G <sub>F_ERR</sub>	-2	0	+2	dB	Gain=+15dB to +1dB
	Attenuation Set Error 1	G <sub>F_ERR1</sub>	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	G <sub>F_ERR2</sub>	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G <sub>F_ERR3</sub>	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	R <sub>OUT</sub>	-	-	50	Ω	V <sub>IN</sub> =100mVrms
Maximum Output Voltage	V <sub>OM</sub>	2	2.2	-	Vrms	THD+N=1% BW=400Hz-30KHz	
LOUDNESS	Maximum Gain	G <sub>L_MAX</sub>	17	20	23	dB	Gain 20dB V <sub>IN</sub> =100mVrms G <sub>L</sub> =20log(V <sub>OUT</sub> /V <sub>IN</sub> )
	Gain Set Error	G <sub>L_ERR</sub>	-2	0	+2	dB	GAIN=+20dB to +1dB

VP-9690A (Average value detection, effective value display) filter by Matsushita Communication is used for \* measurement.  
Phase between input / output is same.

Typical Performance Curves

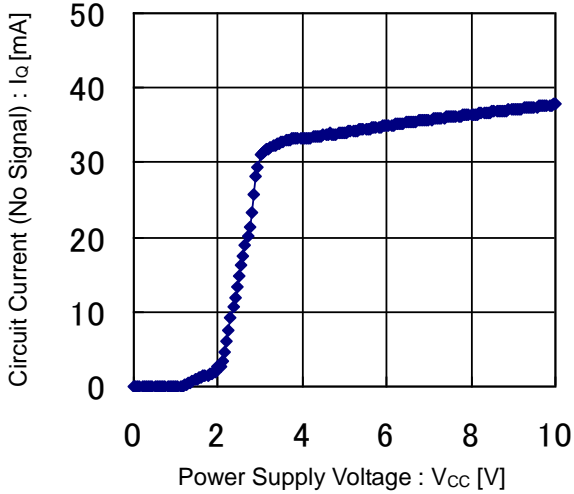


Figure 1. Circuit Current (No Signal) vs Power Supply Voltage

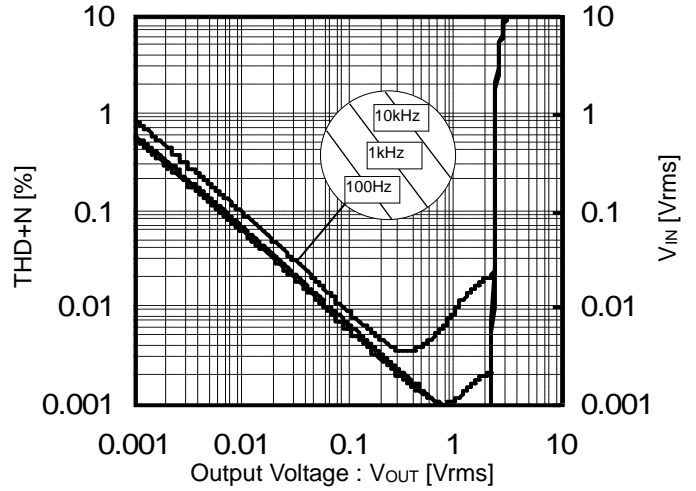


Figure 2. Total Harmonic Distortion vs Output Voltage

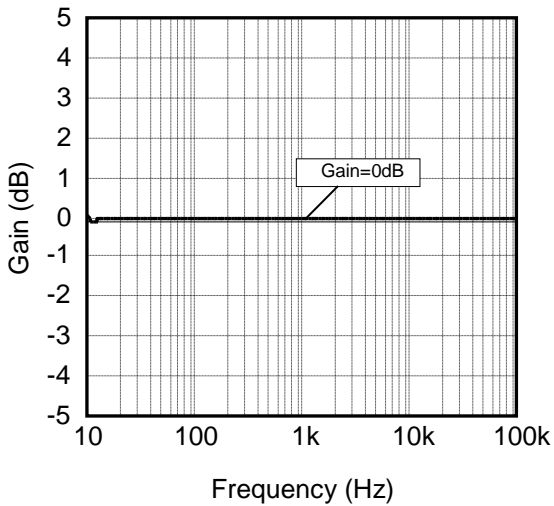


Figure 3. Gain vs Frequency

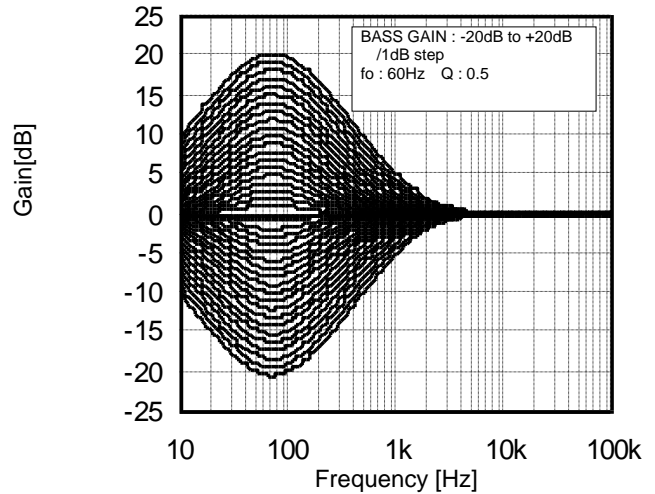


Figure 4. Bass Gain vs Frequency

Typical Performance Curves – continued

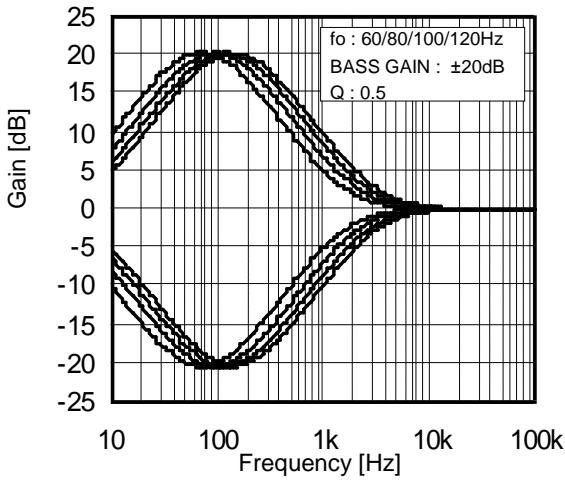


Figure 5. Bass fo vs Frequency

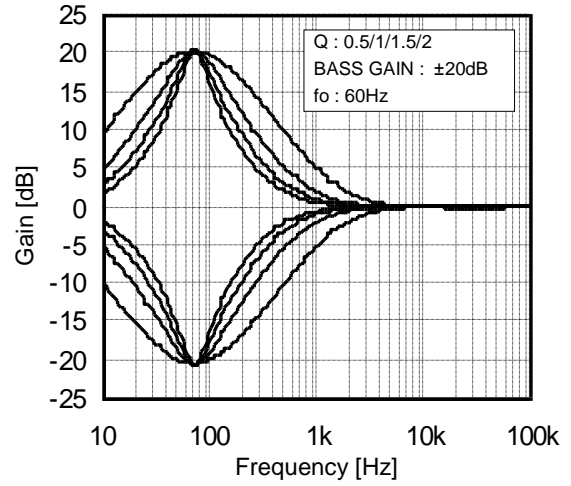


Figure 6. Bass Q vs Frequency

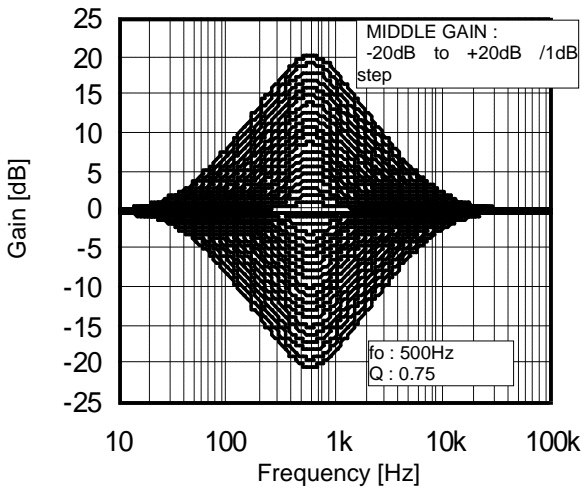


Figure 7. Middle Gain vs Frequency

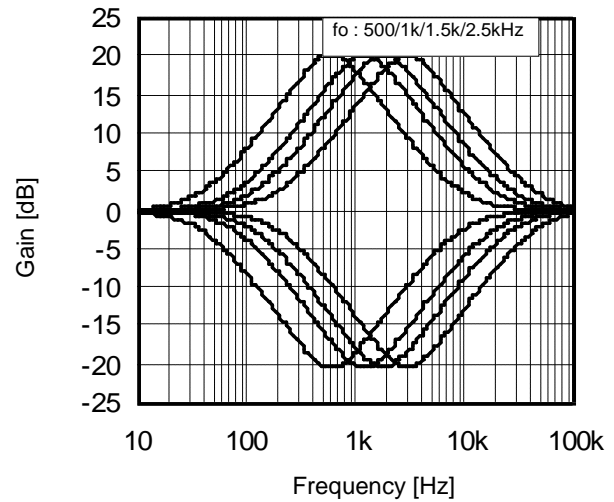


Figure 8. Middle fo vs Frequency

Typical Performance Curves – continued

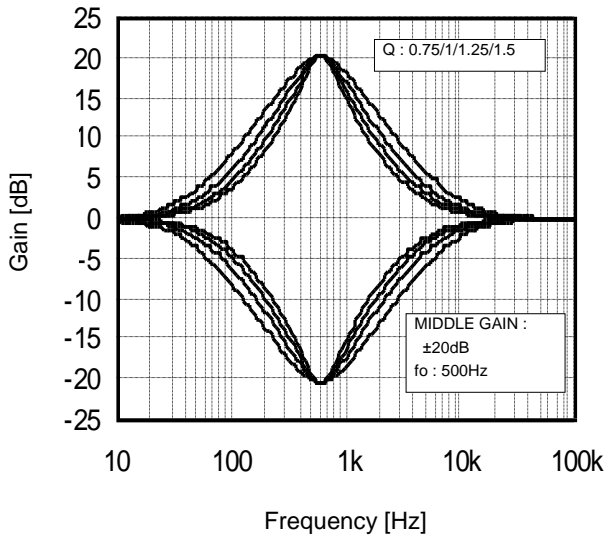


Figure 9. Middle Q vs Frequency

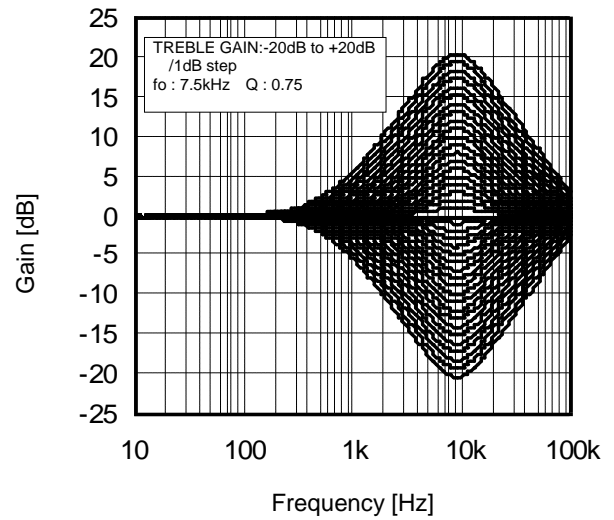


Figure 10. Treble Gain vs Frequency

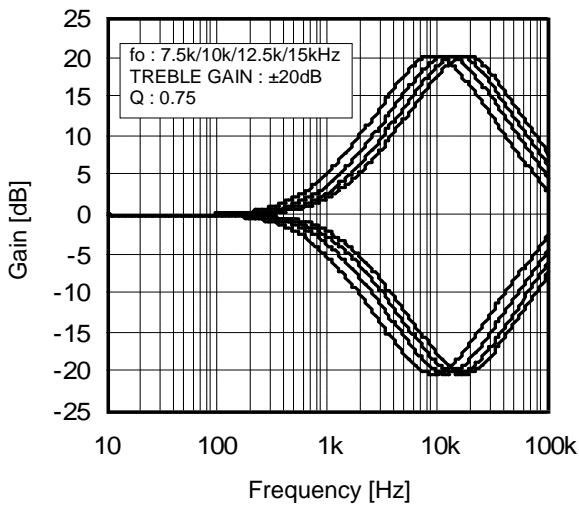


Figure 11. Treble fo vs Frequency

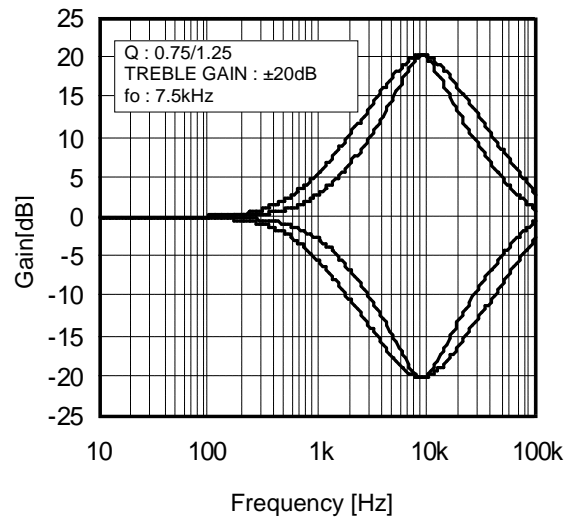


Figure 12. Treble Q vs Frequency



Typical Performance Curves – continued

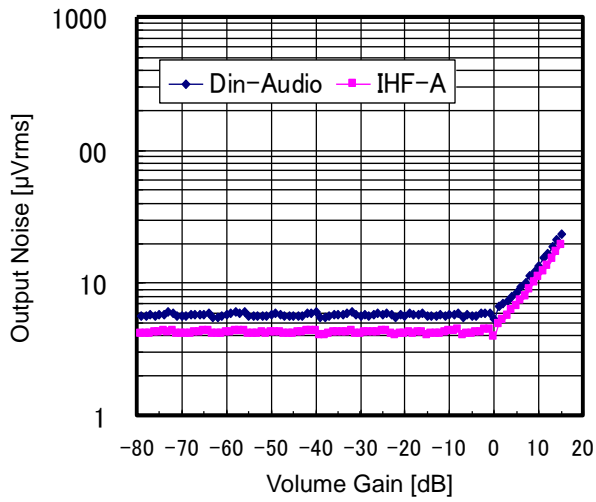


Figure 13. Output Noise vs Volume Gain

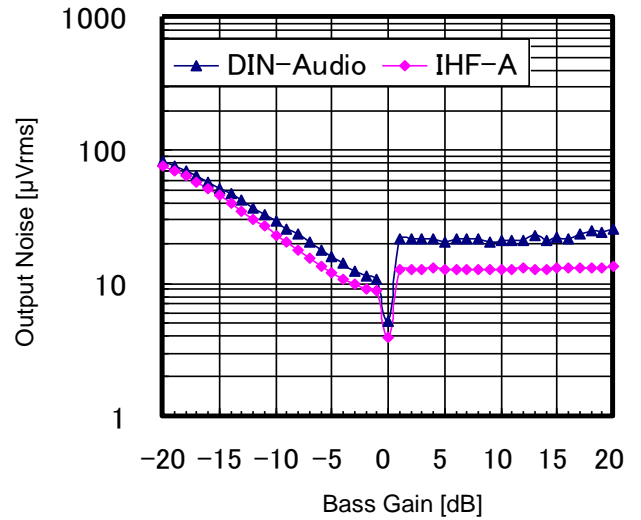


Figure 14. Output Noise vs Bass Gain

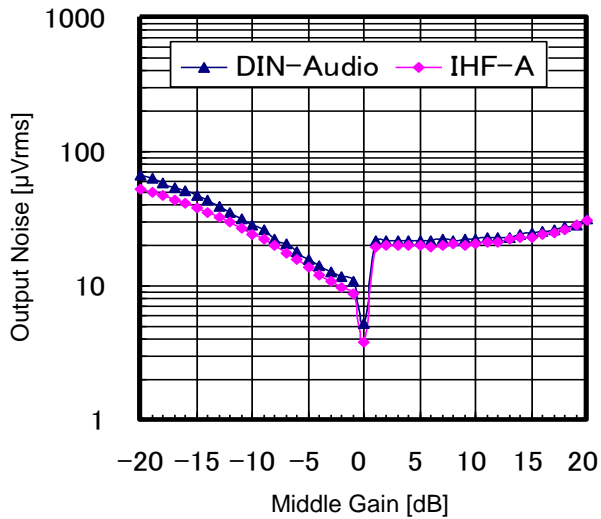


Figure 15. Output Noise vs Middle Gain

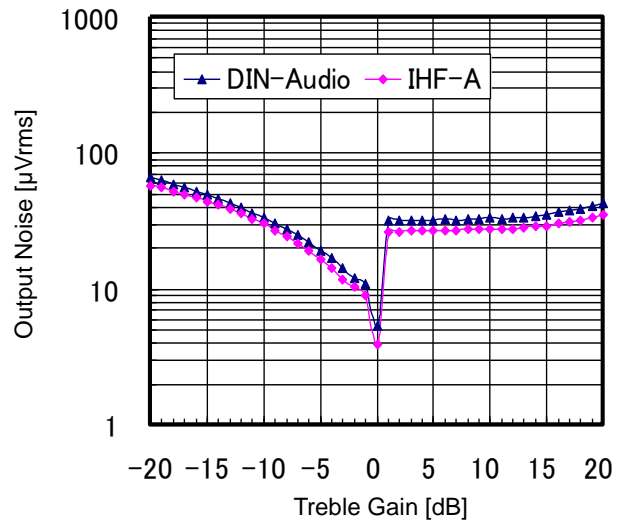


Figure 16. Output Noise vs Treble Gain

Typical Performance Curves – continued

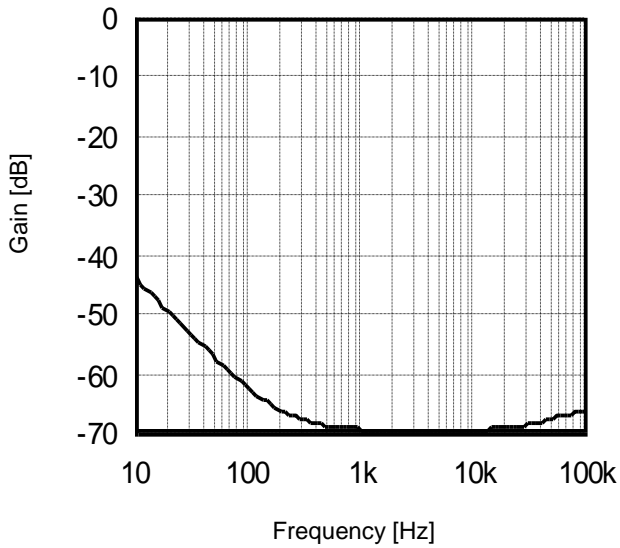


Figure 17. CMRR vs Frequency

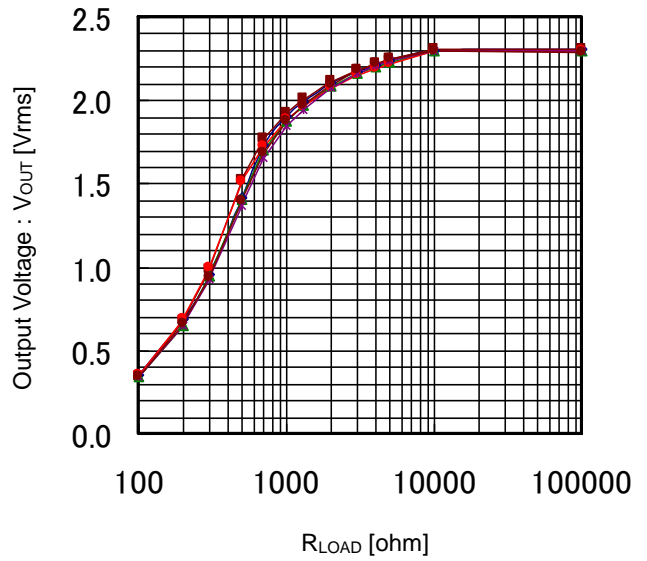


Figure 18. Output Voltage vs R<sub>LOAD</sub>

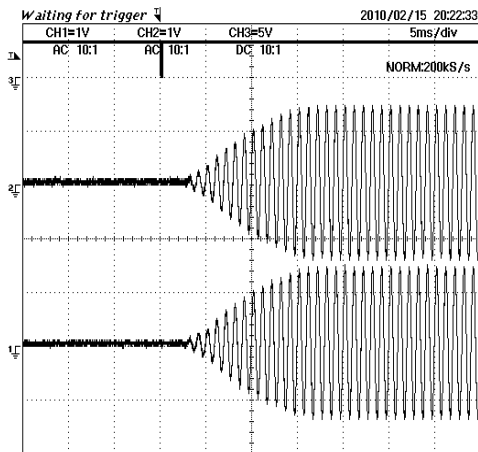


Figure 19. Advanced Switch 1

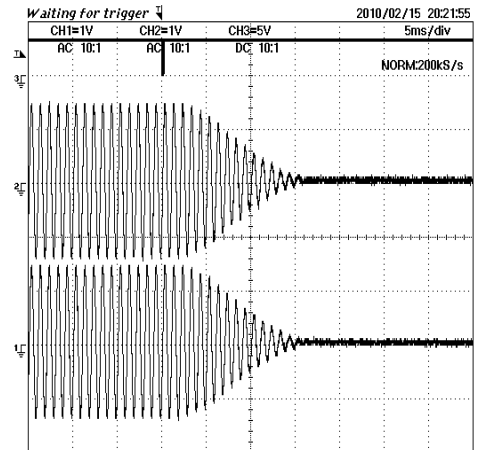


Figure 20. Advanced Switch 2

Timing Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

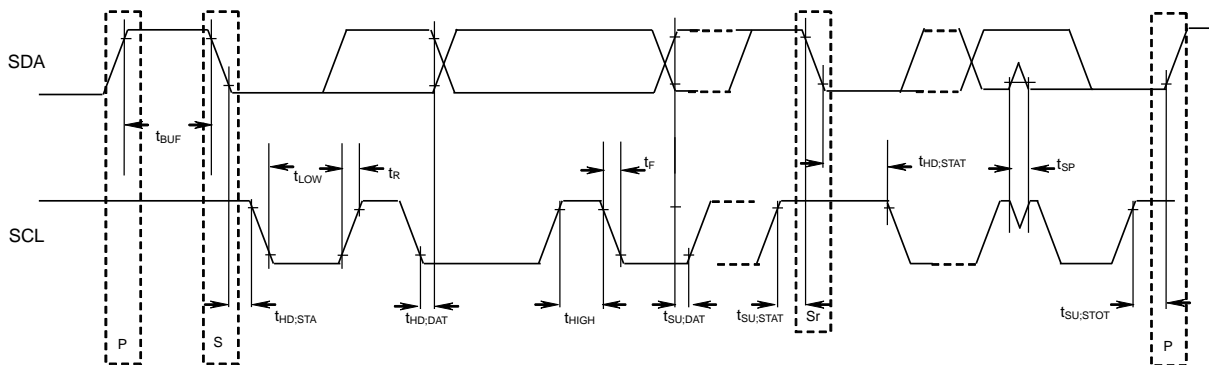


Figure 21. Definition of Timing on the I<sup>2</sup>C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I<sup>2</sup>C-bus devices  
(Unless specified particularly, Ta=25°C, Vcc=8.5V)

Parameter	Symbol	Fast-mode I <sup>2</sup> C-bus		Unit
		Min	Max	
1 SCL clock frequency	f <sub>SCL</sub>	0	400	kHz
2 Bus free time between a STOP and START condition	t <sub>BUF</sub>	1.3	-	μS
3 Hold time (repeated) START condition. After this period, the first clock pulse is generated	t <sub>HD:STA</sub>	0.6	-	μS
4 LOW period of the SCL clock	t <sub>LOW</sub>	1.3	-	μS
5 HIGH period of the SCL clock	t <sub>HIGH</sub>	0.6	-	μS
6 Set-up time for a repeated START condition	t <sub>SU:STA</sub>	0.6	-	μS
7 Data hold time:	t <sub>HD:DAT</sub>	0.06 <sup>(Note)</sup>	-	μS
8 Data set-up time	t <sub>SU:DAT</sub>	120	-	ns
9 Set-up time for STOP condition	t <sub>SU:STO</sub>	0.6	-	μS

All values referred to VIH Min and VIL Max Levels (see Table 2).

(Note) The device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

About 7 (t<sub>HD:DAT</sub>), 8(t<sub>SU:DAT</sub>), make the setup in which the margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I<sup>2</sup>C-bus devices

Parameter	Symbol	Fast-mode devices		Unit
		Min	Max	
10 LOW level input voltage:	V <sub>IL</sub>	-0.3	+1	V
11 HIGH level input voltage:	V <sub>IH</sub>	2.3	5	V
12 Pulse width of spikes which must be suppressed by the input filter.	t <sub>SP</sub>	0	50	ns
13 LOW level output voltage: at 3mA sink current	V <sub>OL1</sub>	0	0.4	V
14 Input current each I/O pin with an input voltage between 0.4V and 4.5V.	I <sub>I</sub>	-10	+10	μA

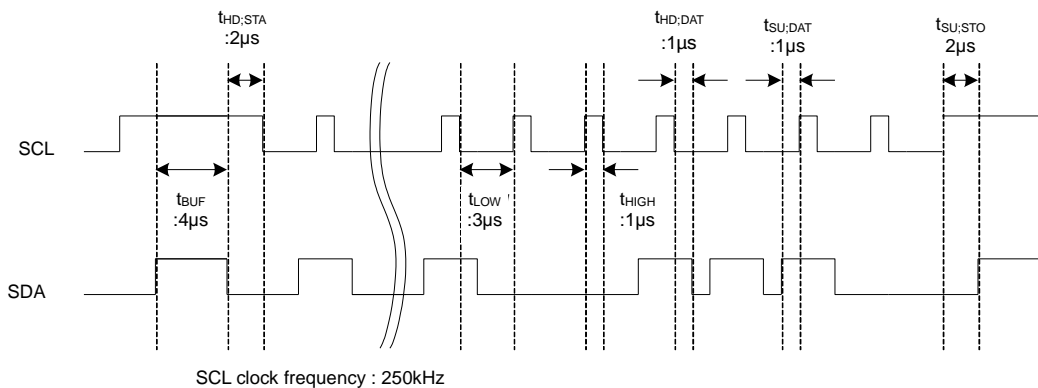
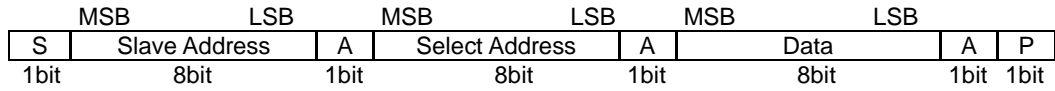


Figure 22. A Command Timing Example in the I<sup>2</sup>C Data Transmission

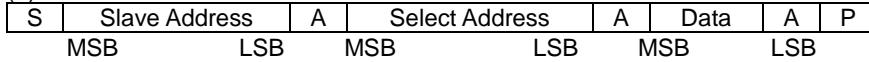
(2) I<sup>2</sup>C BUS FORMAT



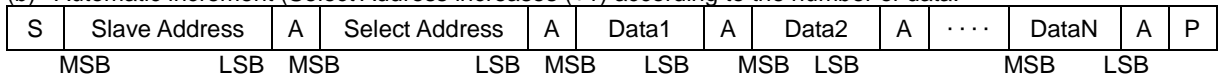
- S = Start conditions (Recognition of start bit)
- Slave Address = Recognition of slave address. 7 bits in upper order are voluntary.  
The least significant bit is "L" for write mode.
- A = ACKNOWLEDGE bit (Recognition of acknowledgement)
- Select Address = Select address for volume, bass and treble.
- Data = Data on every volume and tone.
- P = Stop condition (Recognition of stop bit)

(3) I<sup>2</sup>C BUS Interface Protocol

(a) Basic form

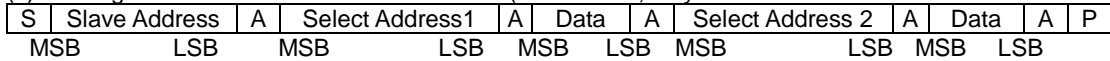


(b) Automatic increment (Select Address increases (+1) according to the number of data.)



- (Example) ①Data1 shall be set as data of address specified by Select Address.  
 ②Data2 shall be set as data of address specified by Select Address +1.  
 ③DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration unavailable for transmission (In this case, only Select Address1 is set.)



(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

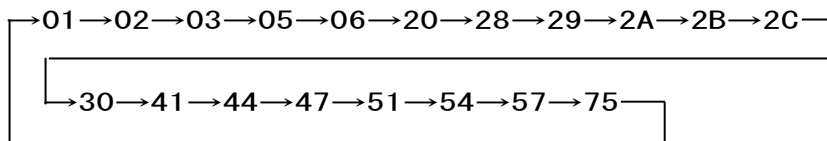
(5) Select Address & Data

Items	Select Address (hex)	Data							
		MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Loudness		0	1	Advanced switch time of Mute	
Initial setup 2	02	LPF Phase	0	Subwoofer Output Select		0	Subwoofer LPF fc		
Initial setup 3	03	0	0	0	Loudness fo		0	0	1
Input Selector	05	Full-diff Type	0	0	Input selector				
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Volume Gain / Attenuation							
Fader 1ch Front	28	Fader Gain / Attenuation							
Fader 2ch Front	29	Fader Gain / Attenuation							
Fader 1ch Rear	2A	Fader Gain / Attenuation							
Fader 2ch Rear	2B	Fader Gain / Attenuation							
Fader Subwoofer	2C	Fader Gain / Attenuation							
Test Mode	30	1	1	1	1	1	1	1	1
Bass setup	41	0	0	Bass fo		0	0	Bass Q	
Middle setup	44	0	0	Middle fo		0	0	Middle Q	
Treble setup	47	0	0	Treble fo		0	0	0	Treble Q
Bass gain	51	Bass Boost/Cut	0	0	Bass Gain				
Middle gain	54	Middle Boost/Cut	0	0	Middle Gain				
Treble gain	57	Treble Boost/Cut	0	0	Treble Gain				
Loudness Gain	75	0	Loudness Hicut		Loudness Gain				
System Reset	FE	1	0	0	0	0	0	0	1

 Advanced switch

Note

1. The Advanced Switch works in the latch part while changing from one function to another..
2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.



3. Advanced Switch is not used for the functions of input selector and subwoofer output select etc. Please turn on MUTE when changing the settings of this side of the set.
4. When using Mute function of this IC at the time of changing input selector, please switch mute ON/OFF while waiting for advanced-mute time.

Select address 01 (hex)

Time	MSB Advanced switch time of Mute							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	1	0	0	
1.0msec							0	1	
1.4msec							1	0	
3.2msec							1	1	

Time	MSB Advanced switch time of Input gain/Volume/Tone/Fader/Loudness							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	1	Advanced switch Time of Mute		
7.1 msec			0	1					
11.2 msec			1	0					
14.4 msec			1	1					

Mode	MSB Advanced switch ON/OFF							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
OFF	0	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	1	Advanced switch Time of Mute		
ON	1								

Select address 02(hex)


fc	MSB Subwoofer LPF fc							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
OFF	LPF Phase	0	Subwoofer Output Select		0	0	0	0	
55Hz						0	0	1	
85Hz						0	1	0	
120Hz						0	1	1	
160Hz						1	0	0	
Prohibition						Other setting			

Mode	MSB Subwoofer Output Select							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
LPF	LPF Phase	0	0	0	0	Subwoofer LPF fc			
Front			0	1					
Rear			1	0					
Prohibition			1	1					

Phase	MSB LPF Phase							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
0°	0	0	Subwoofer output select		0	Subwoofer LPF fc			
180°	1								

Select address 03(hex)

f0	MSB Loudness fo							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
250Hz	0	0	0	0	0	0	0	1	
400Hz				0	1				
800Hz				1	0				
Prohibition				1	1				


 : Initial condition

Select address 05(hex)

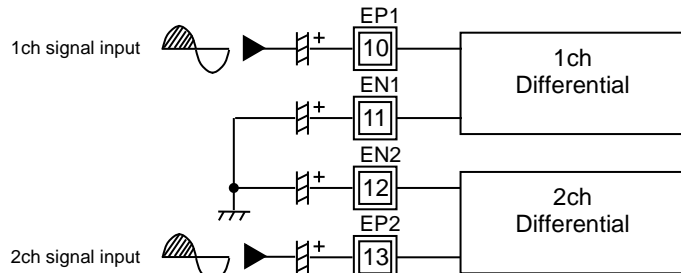
Mode			Input Selector								
	OUTF1	OUTF2	D7	D6	D5	D4	D3	D2	D1	D0	
A	A1	A2	Full-diff bias type select	0	0	0	0	0	0	0	
B	B1	B2				0	0	0	0	1	1
C	C1	C2				0	0	0	1	0	0
D single	DP1	DP2				0	0	0	1	1	1
E1 single	EP1	EN1				0	1	0	1	1	0
E2 single	EN2	EP2				0	1	0	1	1	1
A diff	A1	B1				0	1	1	1	1	1
C diff	B2	C2				1	0	0	0	0	0
D diff	DP1	DP2				0	0	1	1	1	0
E full diff	EP1	EP2				0	1	0	0	0	0
Input SHORT Prohibition						Other setting					

Input SHORT : The input impedance of each input terminal is lowered from 100kΩ(Typ) to 6 kΩ(Typ).  
(For quick charge of coupling capacitor)

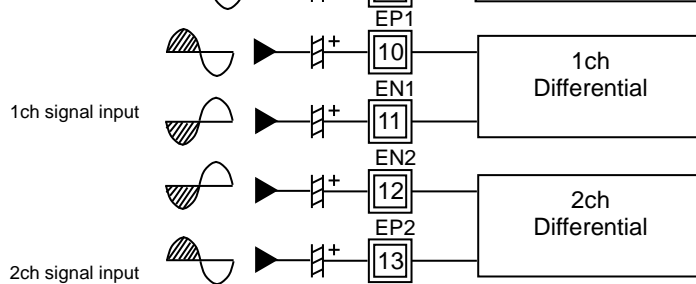
Mode	Full-diff Bias Type Select								LSB
	D7	D6	D5	D4	D3	D2	D1	D0	
Negative Input	0	0	0	Input Selector					
Bias	1								

 : Initial condition

Negative input type  
For Ground –isolation type)




Bias type  
For differential amplifier type



Select address 06 (hex)

Gain	MSB			Input Gain				LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
0dB	Mute ON/OFF	0	0	0	0	0	0	0	
1dB				0	0	0	0	1	
2dB				0	0	0	1	0	
3dB				0	0	0	1	1	
4dB				0	0	1	0	0	
5dB				0	0	1	0	1	
6dB				0	0	1	1	0	
7dB				0	0	1	1	1	
8dB				0	1	0	0	0	
9dB				0	1	0	0	1	
10dB				0	1	0	1	0	
11dB				0	1	0	1	1	
12dB				0	1	1	0	0	
13dB				0	1	1	0	1	
14dB				0	1	1	1	0	
15dB				0	1	1	1	1	
16dB				1	0	0	0	0	
17dB				1	0	0	0	1	
18dB				1	0	0	1	0	
19dB				1	0	0	1	1	
20dB	1	0	1	0	0				
Prohibition				1	1	0	1	1	
				:	:	:	:	:	
				1	1	1	1	1	

Mode	MSB			Mute ON/OFF				LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
OFF	0	0	0	Input Gain					
ON	1								

 : Initial condition



Select address 20, 28, 29, 2A, 2B, 2C (hex)

Gain & ATT	MSB Vol, Fader Gain / Attenuation							LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
Prohibition	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	1	
	:	:	:	:	:	:	:	:	
	0	1	1	1	0	0	0	0	
15dB	0	1	1	1	0	0	0	1	
14dB	0	1	1	1	0	0	1	0	
13dB	0	1	1	1	0	0	1	1	
:	:	:	:	:	:	:	:	:	
-77dB	1	1	0	0	1	1	0	1	
-78dB	1	1	0	0	1	1	1	0	
-79dB	1	1	0	0	1	1	1	1	
Prohibition	1	1	0	1	0	0	0	0	
	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	0	
-∞dB	1	1	1	1	1	1	1	1	

Select address 41(hex)

Q factor	MSB Bass				Q factor		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
0.5	0	0	Bass fo		0	0	0	0
1.0							0	1
1.5							1	0
2.0							1	1

fo	MSB Bass				fo		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
60Hz	0	0	0	0	0	0	Bass Q factor	
80Hz			0	1				
100Hz			1	0				
120Hz			1	1				

Select address 44(hex)

Q factor	MSB Middle				Q factor		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Middle fo		0	0	0	0
1.0							0	1
1.25							1	0
1.5							1	1

fo	MSB Middle				fo		LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
500Hz	0	0	0	0	0	0	Middle Q factor	
1kHz			0	1				
1.5kHz			1	0				
2.5kHz			1	1				

 : Initial condition

Select address 47 (hex)

Q factor	MSB		Treble				Q factor		LSB
	D7	D6	D5	D4	D3	D2	D1	D0	
0.75	0	0	Treble fo		0	0	0	0	
1.25	0	0	Treble fo		0	0	0	1	

fo	MSB		Treble				fo		LSB
	D7	D6	D5	D4	D3	D2	D1	D0	
7.5kHz	0	0	0	0	0	0	0	Treble Q factor	
10kHz			0	1					
12.5kHz			1	0					
15kHz			1	1					

Select address 51, 54, 57 (hex)

Gain	MSB		Bass/Middle/Treble Gain					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Middle/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB	1	0	1	0	0			
Prohibition	1	0	1	0	1	0	1	
	:	:	:	:	:	:	:	
	1	1	1	1	1	1	0	
	1	1	1	1	1	1	1	


Mode	MSB		Bass/Middle/Treble Boost/Cut					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Middle/Treble Gain				
Cut	1							

 : Initial condition

Select address 75 (hex)

Mode	MSB			Loudness Hicut				LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
Hicut1	0	0	0	Loudness Gain					
Hicut2		0	1						
Hicut3		1	0						
Hicut4		1	1						

Gain	MSB			Loudness Gain				LSB	
	D7	D6	D5	D4	D3	D2	D1	D0	
0dB	0	Loudness Hicut	0	0	0	0	0	0	
1dB			0	0	0	0	0	1	
2dB			0	0	0	1	0	0	
3dB			0	0	0	1	1	1	
4dB			0	0	1	0	0	0	
5dB			0	0	1	0	1	1	
6dB			0	0	1	1	1	0	
7dB			0	0	1	1	1	1	
8dB			0	1	0	0	0	0	
9dB			0	1	0	0	0	1	
10dB			0	1	0	1	1	0	
11dB			0	1	0	1	1	1	
12dB			0	1	1	0	0	0	
13dB			0	1	1	0	1	1	
14dB			0	1	1	1	1	0	
15dB			0	1	1	1	1	1	
16dB			1	0	0	0	0	0	
17dB			1	0	0	0	0	1	
18dB			1	0	0	1	1	0	
19dB			1	0	0	1	1	1	
20dB	1	0	1	0	0	0			
Prohibition				:	:	:	:	:	
				1	1	1	1	1	

 : Initial Condition

(6) About Power ON Reset

Built-in IC initialization is made during power ON of the supply voltage. Please send initial data to all addresses at supply voltage on. Also, please turn ON MUTE at the set side until initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t <sub>RISE</sub>	33	-	-	μsec	V <sub>CC</sub> rise time from 0V to 5V
VCC Voltage of Release Power ON Reset	V <sub>POR</sub>	-	4.1	-	V	

(7) About External Compulsory Mute Terminal

It is possible to forcibly set Mute from the outside by setting input voltage at the MUTE terminal.

Mute Voltage Condition	Mode
GND to 1.0V	MUTE ON
2.3V to V <sub>CC</sub>	MUTE OFF

Establish the voltage of MUTE in the condition to be defined.


Application Information

1. Function and Specifications

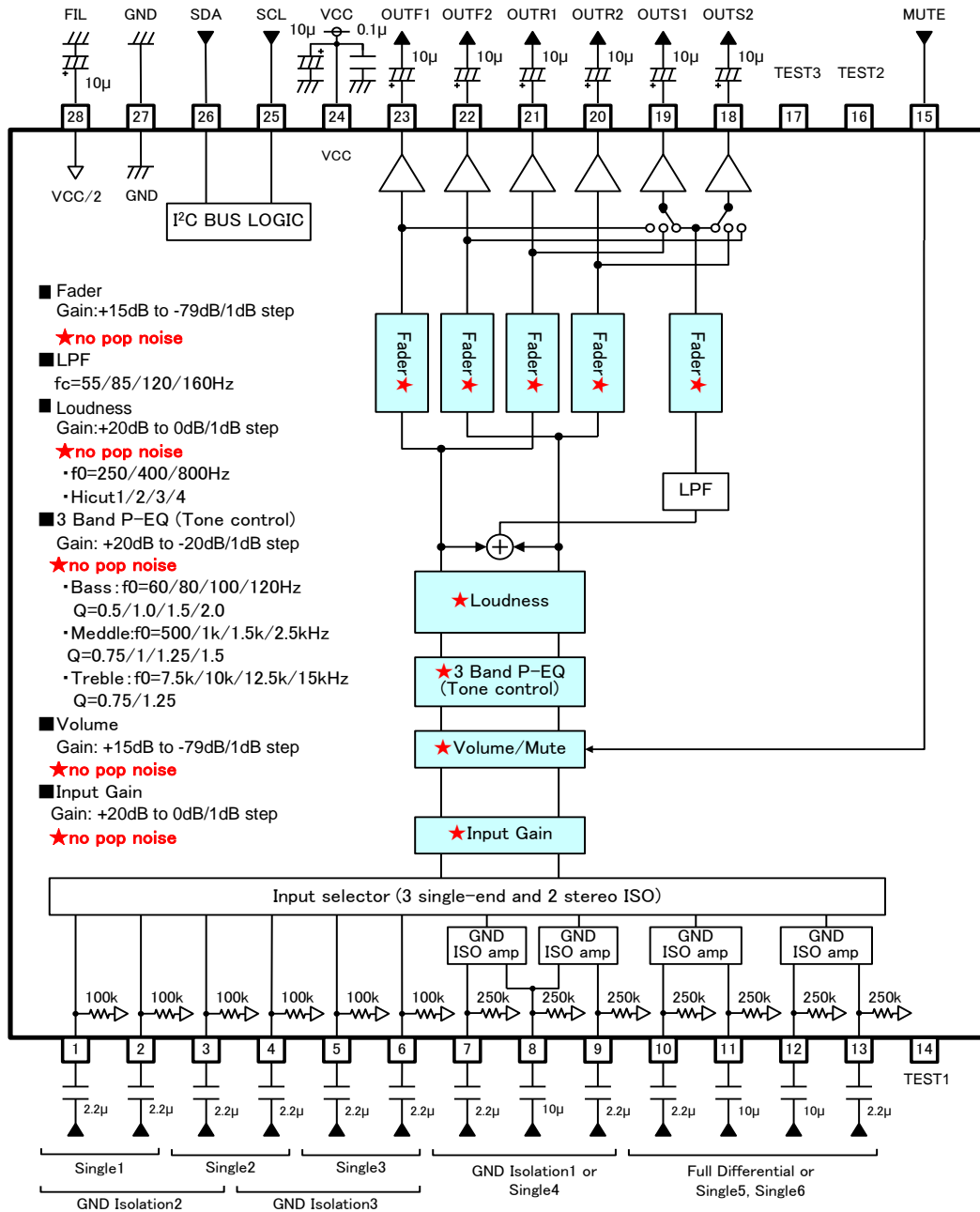
Function	Specifications																												
Input selector	<ul style="list-style-type: none"> <li>· (Stereo input)</li> <li>· Single-End/Diff/Full-Diff</li> </ul> (Possible to set the number of single-end/diff/full-diff as follows )																												
	<table border="1"> <thead> <tr> <th></th> <th>Single-End</th> <th>Differential</th> <th>Full-Differential</th> </tr> </thead> <tbody> <tr> <td>Mode 1</td> <td>0</td> <td>3</td> <td>1</td> </tr> <tr> <td>Mode 2</td> <td>1</td> <td>2</td> <td>1</td> </tr> <tr> <td>Mode 3</td> <td>3</td> <td>1</td> <td>1</td> </tr> <tr> <td>Mode 4</td> <td>4</td> <td>0</td> <td>1</td> </tr> <tr> <td>Mode 5</td> <td>5</td> <td>1</td> <td>0</td> </tr> <tr> <td>Mode 6</td> <td>6</td> <td>0</td> <td>0</td> </tr> </tbody> </table>		Single-End	Differential	Full-Differential	Mode 1	0	3	1	Mode 2	1	2	1	Mode 3	3	1	1	Mode 4	4	0	1	Mode 5	5	1	0	Mode 6	6	0	0
		Single-End	Differential	Full-Differential																									
	Mode 1	0	3	1																									
	Mode 2	1	2	1																									
	Mode 3	3	1	1																									
	Mode 4	4	0	1																									
Mode 5	5	1	0																										
Mode 6	6	0	0																										
Table.1 Combination of input selector																													
Input gain	<ul style="list-style-type: none"> <li>· +20dB to 0dB (1dB step)</li> <li>· Possible to use “Advanced switch” for prevention of switching noise.</li> </ul>																												
Mute	<ul style="list-style-type: none"> <li>· Possible to use “Advanced switch” for prevention of switching noise.</li> </ul>																												
Volume	<ul style="list-style-type: none"> <li>· +15dB to -79dB (1dB step), -∞dB</li> <li>· Possible to use “Advanced switch” for prevention of switching noise.</li> </ul>																												
Bass	<ul style="list-style-type: none"> <li>· +20dB to -20dB (1dB step)</li> <li>· Q=0.5, 1, 1.5, 2</li> <li>· fo=60, 80, 100, 120Hz</li> <li>· Possible to use “Advanced switch” when changing gain</li> </ul>																												
Middle	<ul style="list-style-type: none"> <li>· +20dB to -20dB (1dB step)</li> <li>· Q=0.75, 1, 1.25, 1.5</li> <li>· fo=500, 1k, 1.5k 2.5kHz</li> <li>· Possible to use “Advanced switch” when changing gain</li> </ul>																												
Treble	<ul style="list-style-type: none"> <li>· +20dB to -20dB (1dB step)</li> <li>· Q=0.75, 1.25</li> <li>· fo=7.5k, 10k, 12.5k, 15kHz</li> <li>· Possible to use “Advanced switch” when changing gain</li> </ul>																												
Fader	<ul style="list-style-type: none"> <li>· +15dB to -79dB(1dB step), -∞dB</li> <li>· Possible to use “Advanced switch” for prevention of switching noise.</li> </ul>																												
Loudness	<ul style="list-style-type: none"> <li>· +20dB to 0dB(1dB step)</li> <li>· fo=250/400/800Hz</li> <li>· Possible to use “Advanced switch” for prevention of switching noise.</li> </ul>																												
LPF	<ul style="list-style-type: none"> <li>· fc=55/85/120/160Hz, pass</li> <li>· Phase shift (0°/180°)</li> </ul>																												

2. Volume / Fader Volume Attenuation Data

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1	-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0	-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1	-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0	-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1	-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0	-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1	-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0	-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1	-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0	-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1	-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0	-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1	-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0	-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1	-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0	-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1	-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0	-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1	-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0	-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1	-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0	-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1	-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0	-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1	-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0	-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1	-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0	-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1	-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0	-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1	-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0	-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1	-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0	-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1	-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0	-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1	-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0	-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1	-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0	-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1	-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0	-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1	-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0	-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1	-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0	-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1	-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0	-∞	1	1	1	1	1	1	1	1

 : Initial condition

3. Application Circuit



Unit  
R : [Ω]  
C : [F]

(Note) About single input 1 to 3, it is possible to change from single input to GND Isolation input 2,3.

(Note) About GND Isolation1 and Full Differential, it is possible to change from differential input to single input 4 to 6.

Notes on wiring

- ① Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
- ② GND lines should be one-point connected.
- ③ Wiring pattern of Digital shall be away from that of analog unit and crosstalk should not be acceptable.
- ④ If possible, SCL and SDA lines of I<sup>2</sup>C BUS should not be in parallel.  
The lines should be shielded, if they are adjacent to each other.
- ⑤ If possible, analog input lines should not be in parallel. The lines should be shielded, if they are adjacent to each other.
- ⑥ TEST pins (Pin 14,15,16) should be OPEN.

Power Dissipation

About the thermal design of the IC

Characteristics of an IC are greatly affected by the temperature at which it is used. Exceeding absolute maximum ratings may degrade and destroy the device. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

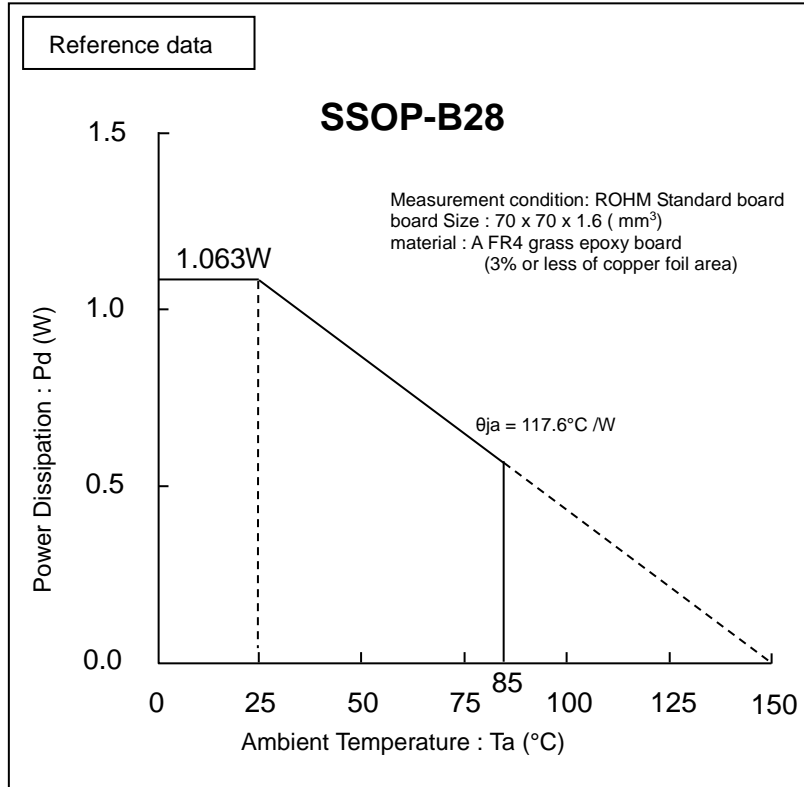
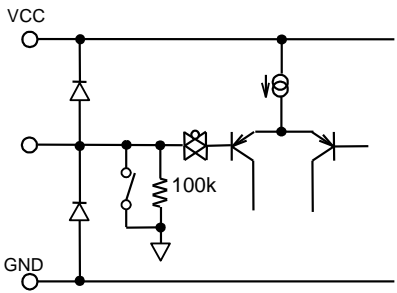
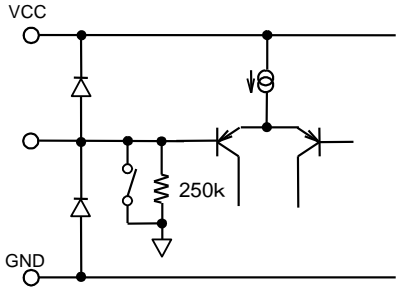
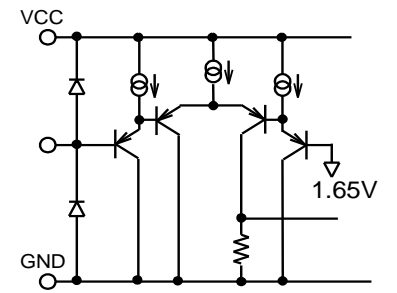
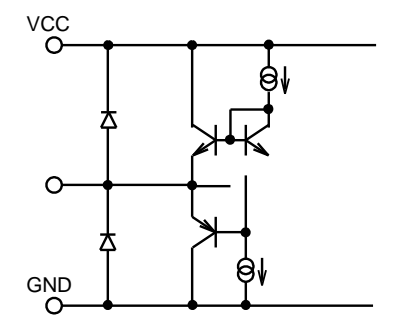


Figure 23. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ (Typ).
7 8 9 10 11 12 13	DP1 DN DP2 EP1 EN1 EN2 EP2	4.25		Input terminal available to single/Differential mode. The input impedance is 250kΩ (Typ).
15	MUTE	-		A terminal for external compulsory mute. If terminal voltage is High level, the mute is OFF. And if the terminal voltage is Low level, the mute is ON.
18 19 20 21 22 23	OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader and Subwoofer output.

Values in the pin explanation and input/output equivalent circuit are for reference purposes only. It is not a guaranteed value.



I/O Equivalent Circuits - continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
24	VCC	8.5		Power supply terminal.
25	SCL	-		A terminal for clock input of I <sup>2</sup> C BUS communication.
26	SDA	-		A terminal for data input of I <sup>2</sup> C BUS communication.
27	GND	0		Ground terminal.
28	FIL	4.25		Voltage for reference bias of analog signal system. The simple pre-charge circuit and simple discharge circuit for an external capacitor are built in.
14 16 17	TEST	-		TEST terminal

Values in the pin explanation and input/output equivalent circuit are for reference purposes only. It is not a guaranteed value.

**Operational Notes****1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

**2. Power Supply Lines**

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

**3. Ground Voltage**

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

**4. Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

**5. Thermal Consideration**

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

**6. Recommended Operating Conditions**

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

**7. Inrush Current**

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

**8. Operation Under Strong Electromagnetic Field**

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

**9. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

**10. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.  
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

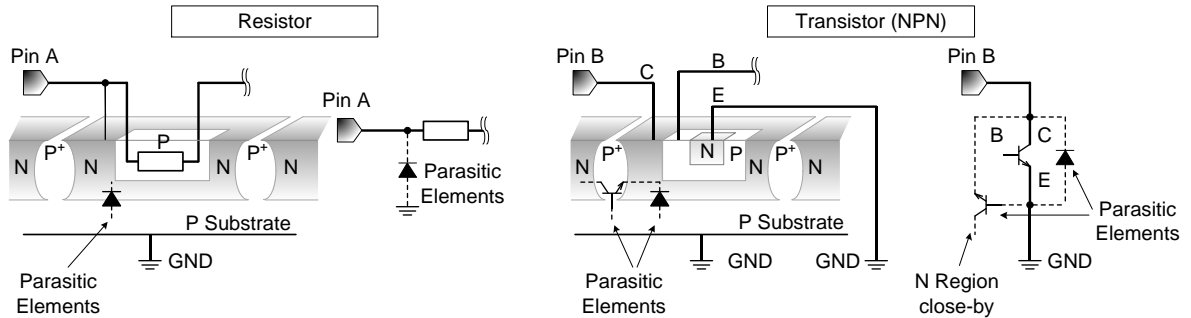
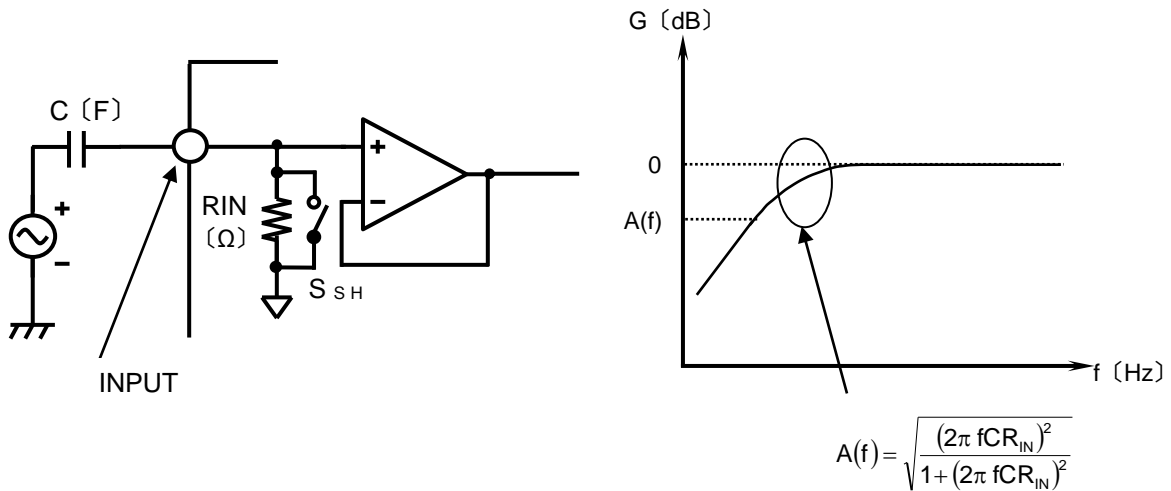


Figure 24. Example of monolithic IC structure

13. About a Signal Input Part

(a) About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance  $R_{IN}(\Omega)$  at the input signal terminal of the IC that would be sufficient to form an RC characterized HPF.



(b) About the Input Selector SHORT

SHORT mode is the command which makes switch  $S_{SH} = ON$  of input selector part so that the input impedance  $R_{IN}$  of all terminals becomes small. Switch  $S_{SH}$  is OFF when SHORT command is not selected. The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of  $S_{SH}$  and makes it low impedance, please use it at no signal condition.

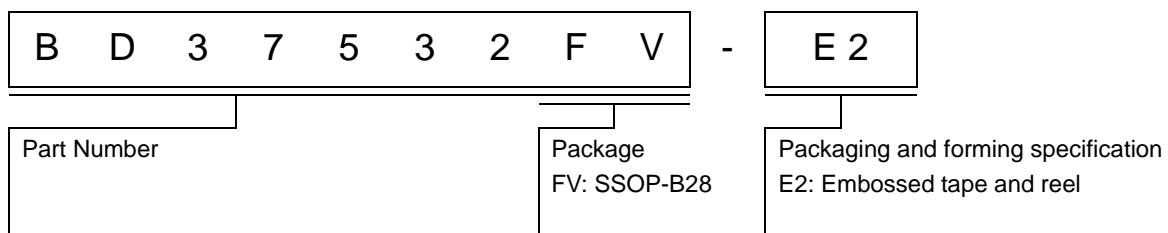
14. About Mute Terminal (Pin 15) when Power Supply is OFF

There should be no applied voltage to Mute terminal (Pin 15) when power-supply is OFF. If in case voltage is supplied to Mute terminal, please insert a series resistor (about 2.2kΩ) to Mute terminal. (Please refer to Application Circuit Diagram.)

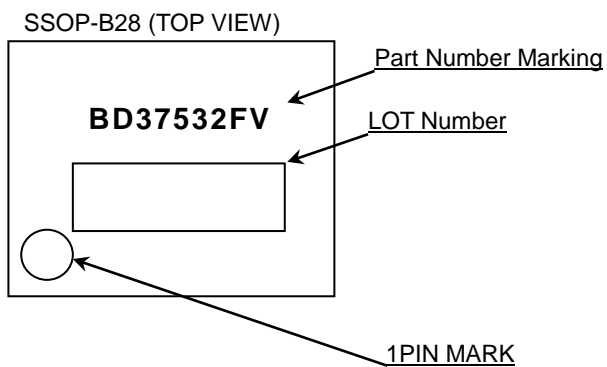
15. About TEST Pin

TEST Pin should be OPEN.  
 Pin 14, 16, 17 are TEST Pins

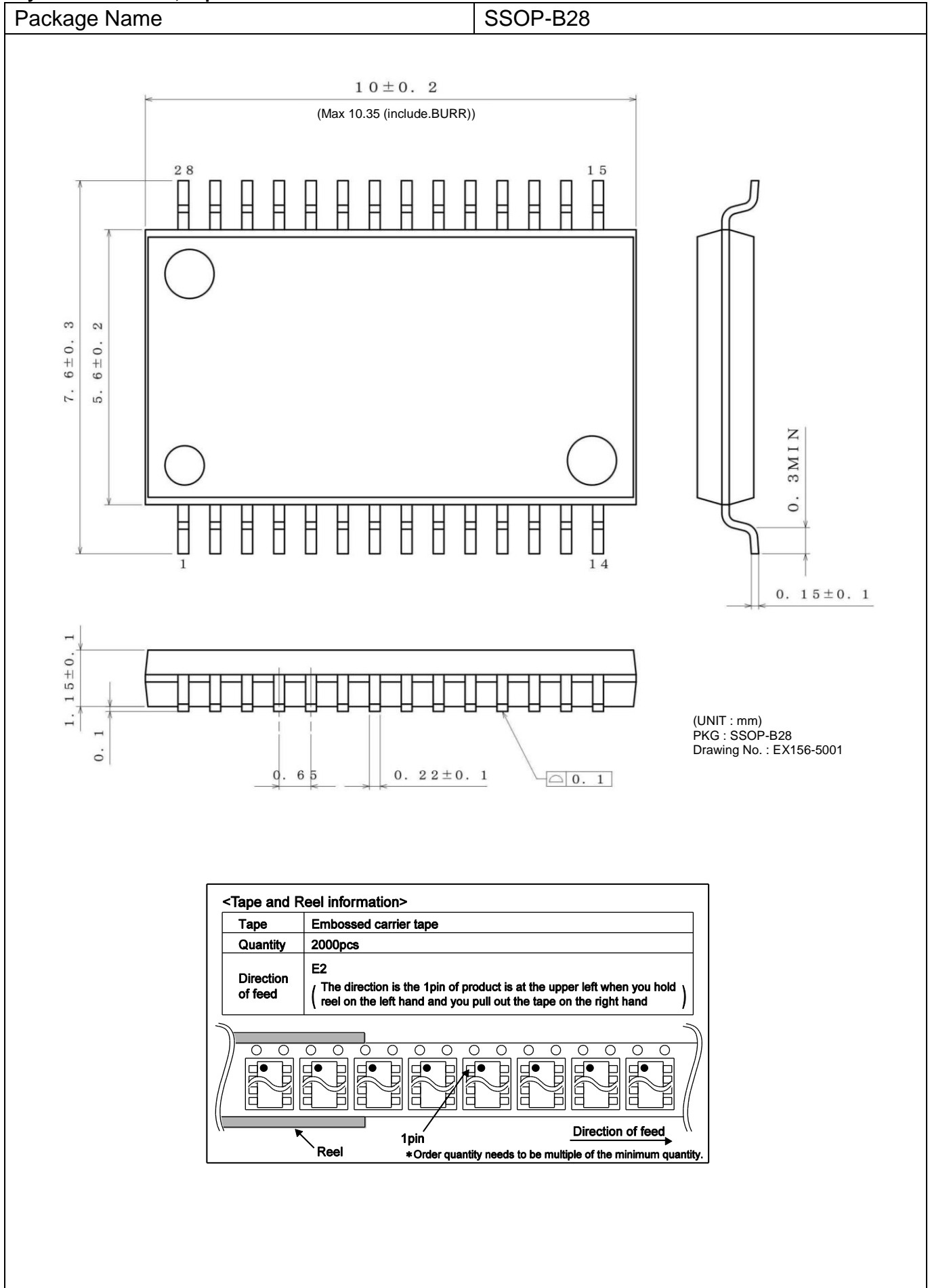
Ordering Information



Marking Diagram



Physical Dimension, Tape and Reel Information



## Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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CLASS IV		CLASS III	

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  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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  - Use of the Products in places subject to dew condensation
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
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  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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