74AUP1T97

Low-power configurable gate with voltage-level translator

Rev. 6 — 28 March 2017 Product data sheet

1 General description

The 74AUP1T97 provides low-power, low-voltage configurable logic gate functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter and buffer. All inputs can be connected to V_{CC} or GND.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V.

The 74AUP1T97 is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 V or 3.3 V supply voltage.

The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 V to 2.3 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

2 Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5 000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1 000 V
- Low static power consumption; I_{CC} = 1.5 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

nexperia

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1T97GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74AUP1T97GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm	SOT886
74AUP1T97GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74AUP1T97GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74AUP1T97GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74AUP1T97GX	-40 °C to +125 °C	X2SON6	plastic thermal extremely thin small outline package; no leads; 6 terminals; body 1 x 0.8 x 0.35 mm	SOT1255
74AUP1T97UK	-40 °C to +125 °C	WLCSP6	wafer level chip-scale package; 6 bumps; 0.65 x 0.44 x 0.27 mm	SOT1454-1

4 Marking

Table 2. Marking

Type number	Marking code[1]
74AUP1T97GW	59
74AUP1T97GM	59
74AUP1T97GF	59
74AUP1T97GN	59
74AUP1T97GS	59
74AUP1T97GX	59
74AUP1T97UK	9

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Pinning information

5.1 Pinning

Table 3. Pinning

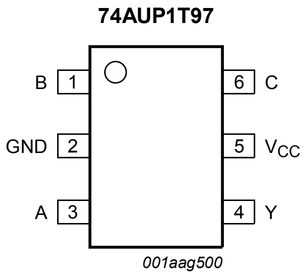
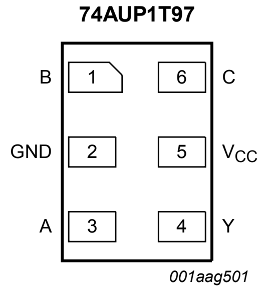
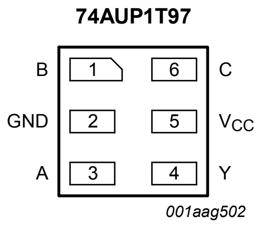


Figure 1. Pin configuration SOT363 (SC-88)



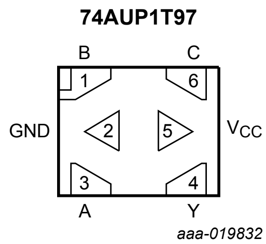
Transparent top view

Figure 2. Pin configuration SOT886 (XSON6)



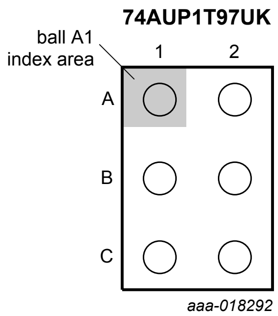
Transparent top view

Figure 3. Pin configuration SOT891, SOT1115 and SOT1202 (XSON6)



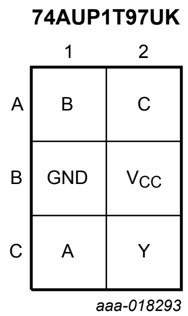
Transparent top view

Figure 4. Pin configuration SOT1255 (X2SON6)



Transparent top view

Figure 5. Pin configuration SOT1454-1 (WLCSP6)



Transparent top view

Figure 6. Ball mapping for SOT1454-1 (WLCSP6)

5.2 Pin description

Table 4. Pin description

Symbol	Pin		Description
	SC88, XSON6 and X2SON6	WLCSP6	
B	1	A1	data input
GND	2	B1	ground (0 V)
A	3	C1	data input
Y	4	C2	data output
V_{CC}	5	B2	supply voltage
C	6	A2	data input

6 Functional description

Table 5. Function table [1]

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7 Functional diagram

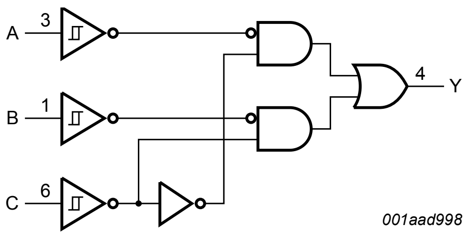


Figure 7. Logic symbol

8 Logic configurations

Table 6. Function selection table

Logic function	Figure
2-input MUX	see Figure 8
2-input AND	see Figure 9
2-input OR with one input inverted	see Figure 10
2-input NAND with one input inverted	see Figure 10
2-input AND with one input inverted	see Figure 11
2-input NOR with one input inverted	see Figure 11
2-input OR	see Figure 12
Inverter	see Figure 13
Buffer	see Figure 14

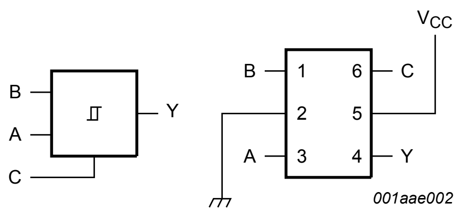


Figure 8. 2-input MUX

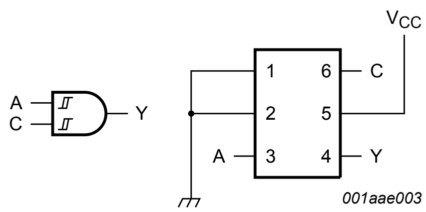


Figure 9. 2-input AND gate

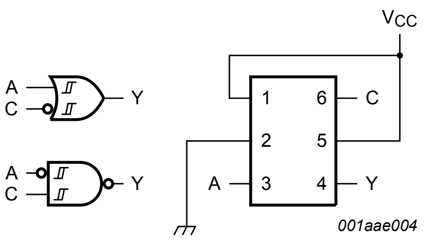


Figure 10. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted

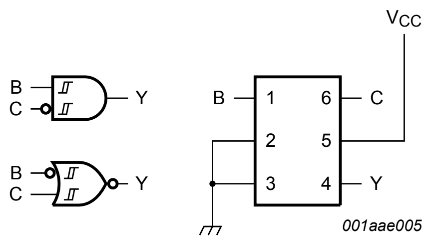


Figure 11. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted

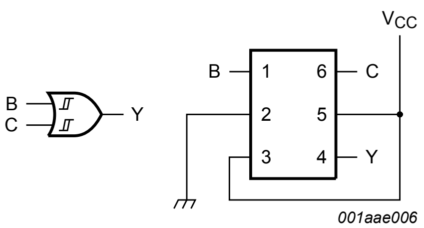


Figure 12. 2-input OR gate

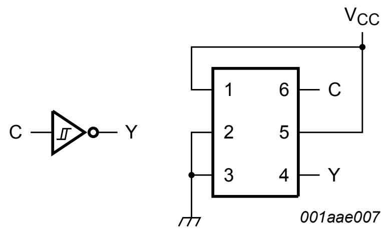


Figure 13. Inverter

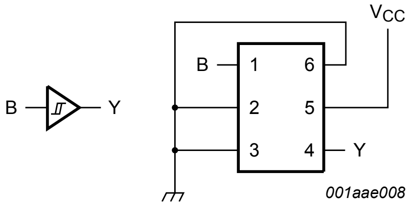


Figure 14. Buffer

9 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SC-88 package: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For X2SON6 and XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.
For WLCSP6 package: above 102.5 °C the value of P_{tot} derates linearly with 5.3 mW/K.

10 Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C

11 Static characteristics

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{T+}	positive-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V_{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V_{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V_H	hysteresis voltage	($V_H = V_{T+} - V_{T-}$)				
		V_{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V_{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = -20 μA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 μA; V_{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.1	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	-	1.2	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.8	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.7	-	pF
T_{amb} = -40 °C to +85 °C						
V_{T+}	positive-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V_{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T-}	negative-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V_{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V_H	hysteresis voltage	($V_H = V_{T+} - V_{T-}$)				
		V_{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V_{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = -20 μA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 μA; V_{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.5	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	-	1.5	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 2.7 V; I_O = 0 A [1]	-	-	4	μA
		V_{CC} = 3.0 V to 3.6 V; I_O = 0 A [2]	-	-	12	μA
T_{amb} = -40 °C to +125 °C						
V_{T+}	positive-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V_{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
		V_{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V_H	hysteresis voltage	($V_H = V_{T+} - V_{T-}$)				
		V_{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V_{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = -20 μA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.11	-	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		I_O = -2.3 mA; V_{CC} = 2.3 V		1.77	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V		1.67	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V		2.40	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V		2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}					
		I_O = 20 μA; V_{CC} = 2.3 V to 3.6 V		-	-	0.11	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.75	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V		-	-	3.5	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 2.7 V; I_O = 0 A	[1]	-	-	7	μA
		V_{CC} = 3.0 V to 3.6 V; I_O = 0 A	[2]	-	-	22	μA

[1] One input at 0.3 V or 1.1 V, other input at V_{CC} or GND.
[2] One input at 0.45 V or 1.2 V, other input at V_{CC} or GND.

12 Dynamic characteristics

Table 10. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 16.

Symbol	Parameter	Conditions		25 °C			-40 °C to +125 °C			Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
V_{CC} = 2.3 V to 2.7 V; V_I = 1.65 V to 1.95 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							
		C_L = 5 pF		2.2	3.5	5.5	0.5	6.8	7.5	ns
		C_L = 10 pF		2.6	4.1	6.3	1.0	7.9	8.7	ns
		C_L = 15 pF		2.9	4.6	6.9	1.0	8.7	9.6	ns
		C_L = 30 pF		3.7	5.8	8.4	1.5	10.8	11.9	ns
V_{CC} = 2.3 V to 2.7 V; V_I = 2.3 V to 2.7 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							
		C_L = 5 pF		1.8	3.4	5.5	0.5	6.0	6.6	ns
		C_L = 10 pF		2.2	4.0	6.2	1.0	7.1	7.9	ns
		C_L = 15 pF		2.5	4.4	6.8	1.0	7.9	8.7	ns
		C_L = 30 pF		3.2	5.6	8.3	1.5	10.0	11.0	ns
V_{CC} = 2.3 V to 2.7 V; V_I = 3.0 V to 3.6 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							
		C_L = 5 pF		1.4	3.1	5.0	0.5	5.5	6.1	ns
		C_L = 10 pF		1.8	3.7	5.7	1.0	6.5	7.2	ns
		C_L = 15 pF		2.2	4.2	6.3	1.0	7.4	8.2	ns
		C_L = 30 pF		2.9	5.3	7.9	1.5	9.5	10.5	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 1.65 V to 1.95 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							
		C_L = 5 pF		2.1	2.9	3.9	0.5	8.0	8.8	ns
		C_L = 10 pF		2.5	3.4	4.6	1.0	8.5	9.4	ns
		C_L = 15 pF		2.9	3.9	5.2	1.0	9.1	10.1	ns
		C_L = 30 pF		3.6	5.0	6.7	1.5	9.8	10.8	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 2.3 V to 2.7 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							
		C_L = 5 pF		1.7	2.8	4.2	0.5	5.3	5.9	ns
		C_L = 10 pF		2.1	3.4	5.0	1.0	6.1	6.8	ns
		C_L = 15 pF		2.4	3.8	5.6	1.0	6.8	7.5	ns
		C_L = 30 pF		3.2	5.0	7.1	1.5	8.5	9.4	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 3.0 V to 3.6 V										
t_{pd}	propagation delay	A, B, C to Y; see Figure 15	[2]							

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
		C_L = 5 pF	1.4	2.7	4.2	0.5	4.7	5.2	ns
		C_L = 10 pF	1.8	3.3	5.0	1.0	5.7	6.3	ns
		C_L = 15 pF	2.1	3.8	5.6	1.0	6.2	6.9	ns
		C_L = 30 pF	2.9	4.9	7.1	1.5	7.8	8.6	ns
T_{amb} = 25 °C									
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]							
		V_{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	4.3	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

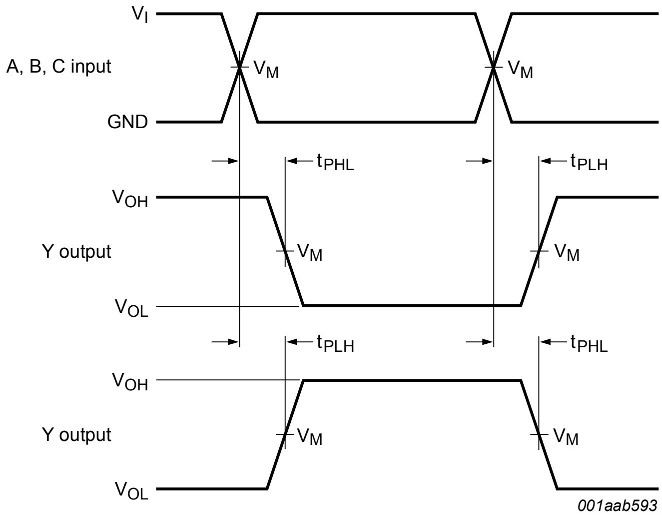
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12.1 Waveforms and test circuit



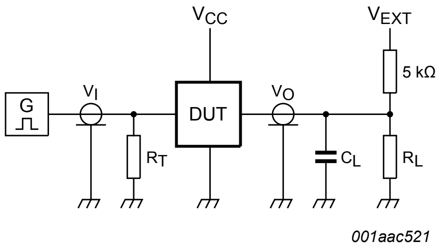
Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 15. Input A, B and C to output Y propagation delay times

Table 11. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
2.3 V to 3.6 V	$0.5V_{CC}$	$0.5V_I$	1.65 V to 3.6 V	≤ 3.0 ns



Test data is given in Table 12.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Figure 16. Test circuit for measuring switching times

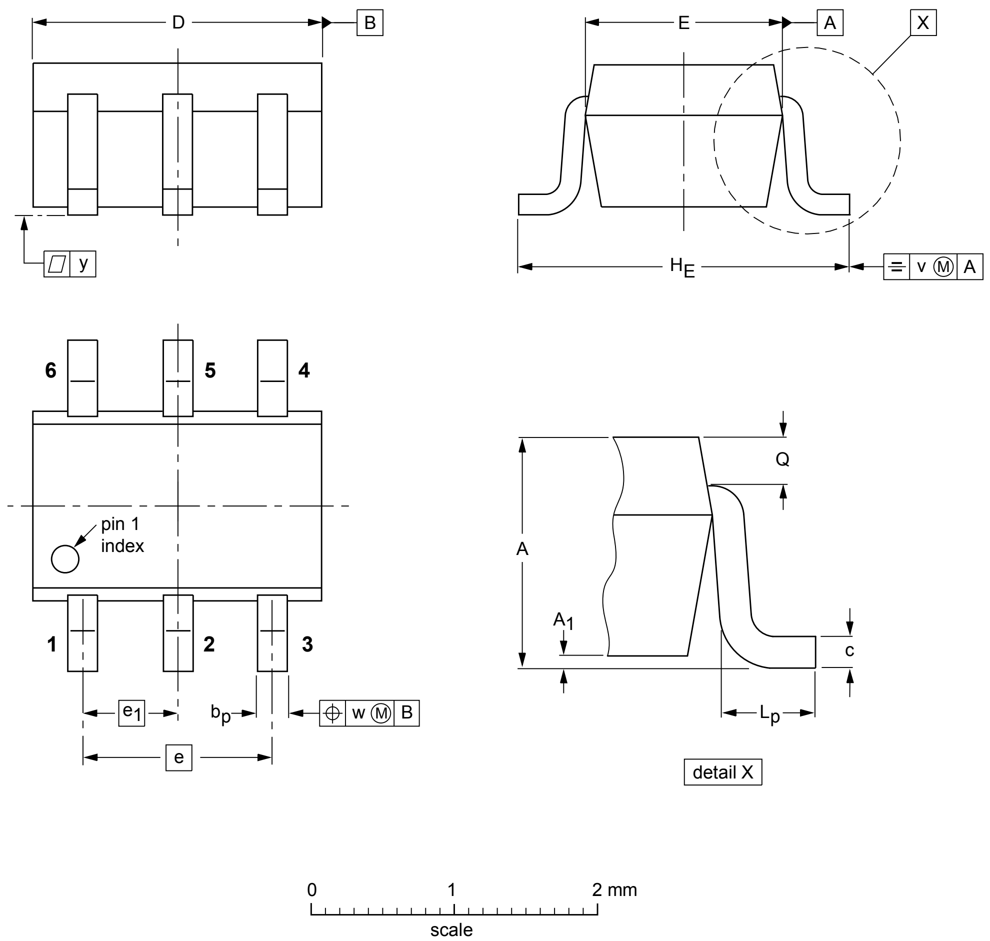
Table 12. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times R_L = 5 kΩ, for measuring propagation delays, setup and hold times and pulse width R_L = 1 MΩ.

13 Package outline

Plastic surface-mounted package; 6 leads **SOT363**



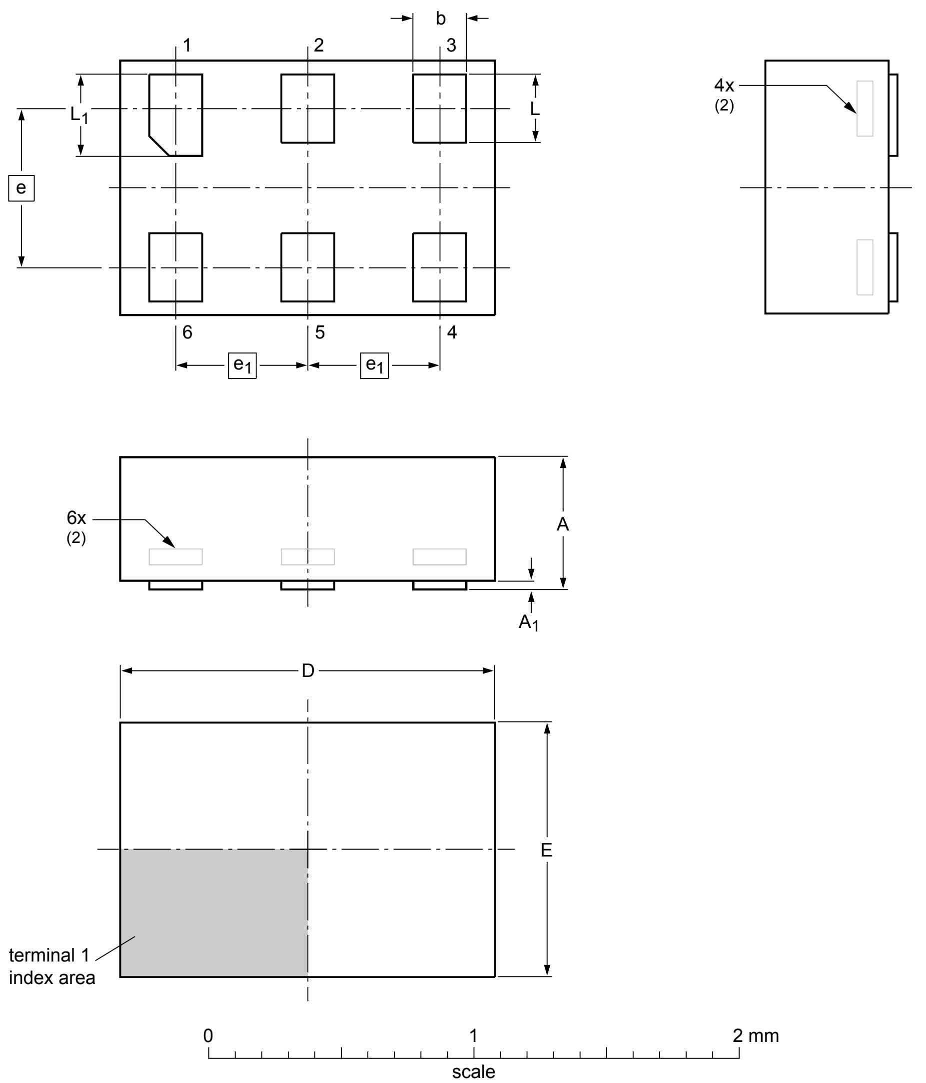
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Figure 17. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm — SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
mm	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

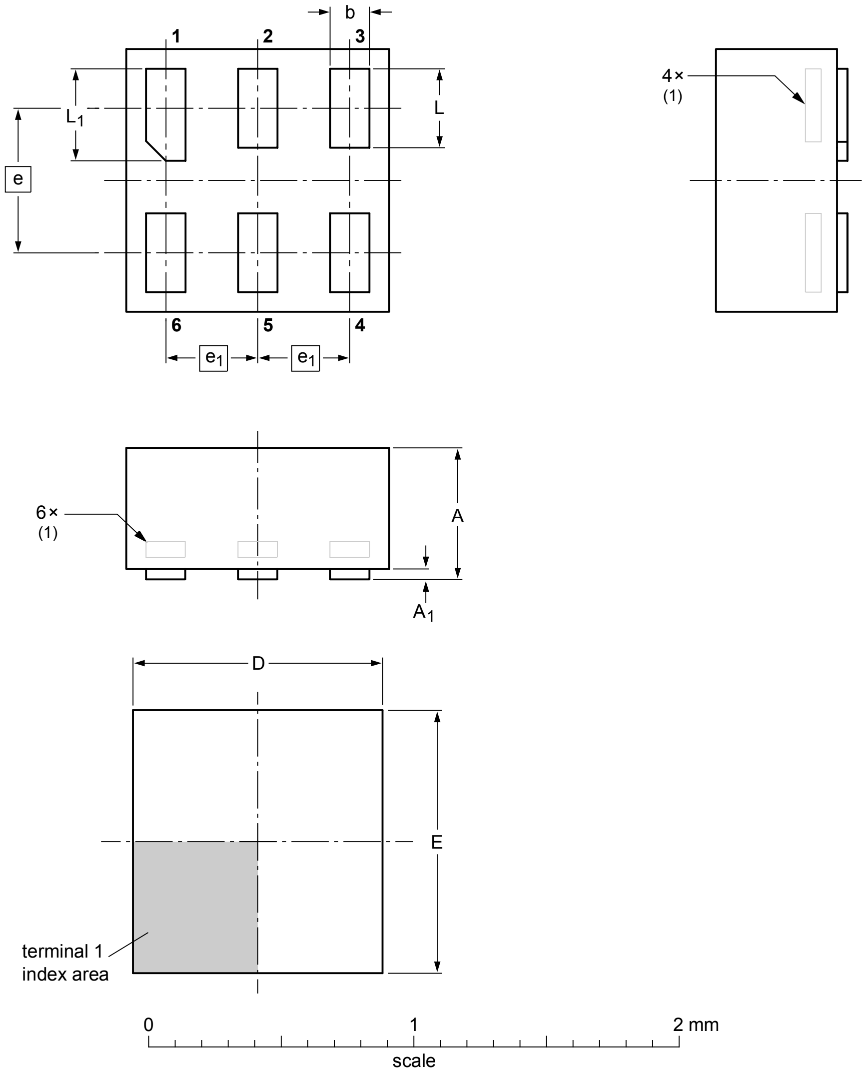
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Figure 18. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

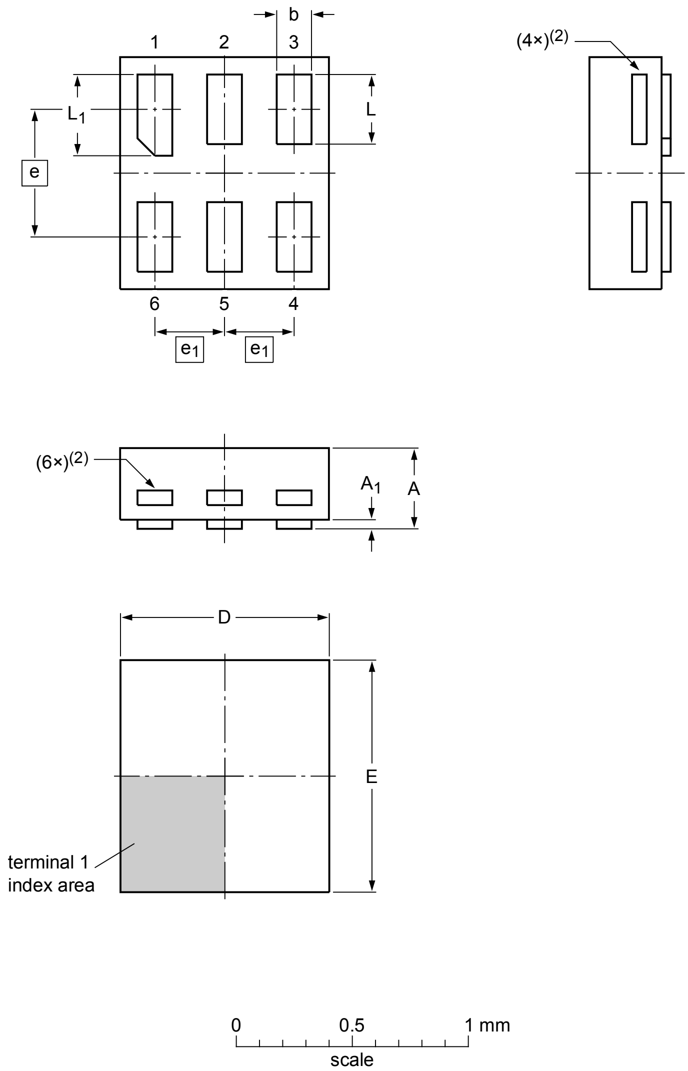
Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Figure 19. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

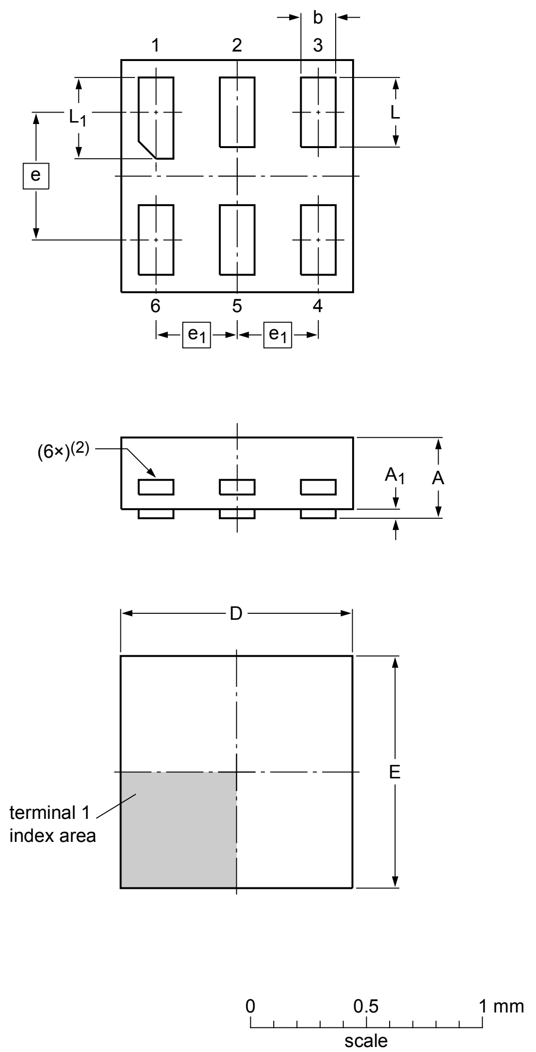
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Figure 20. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

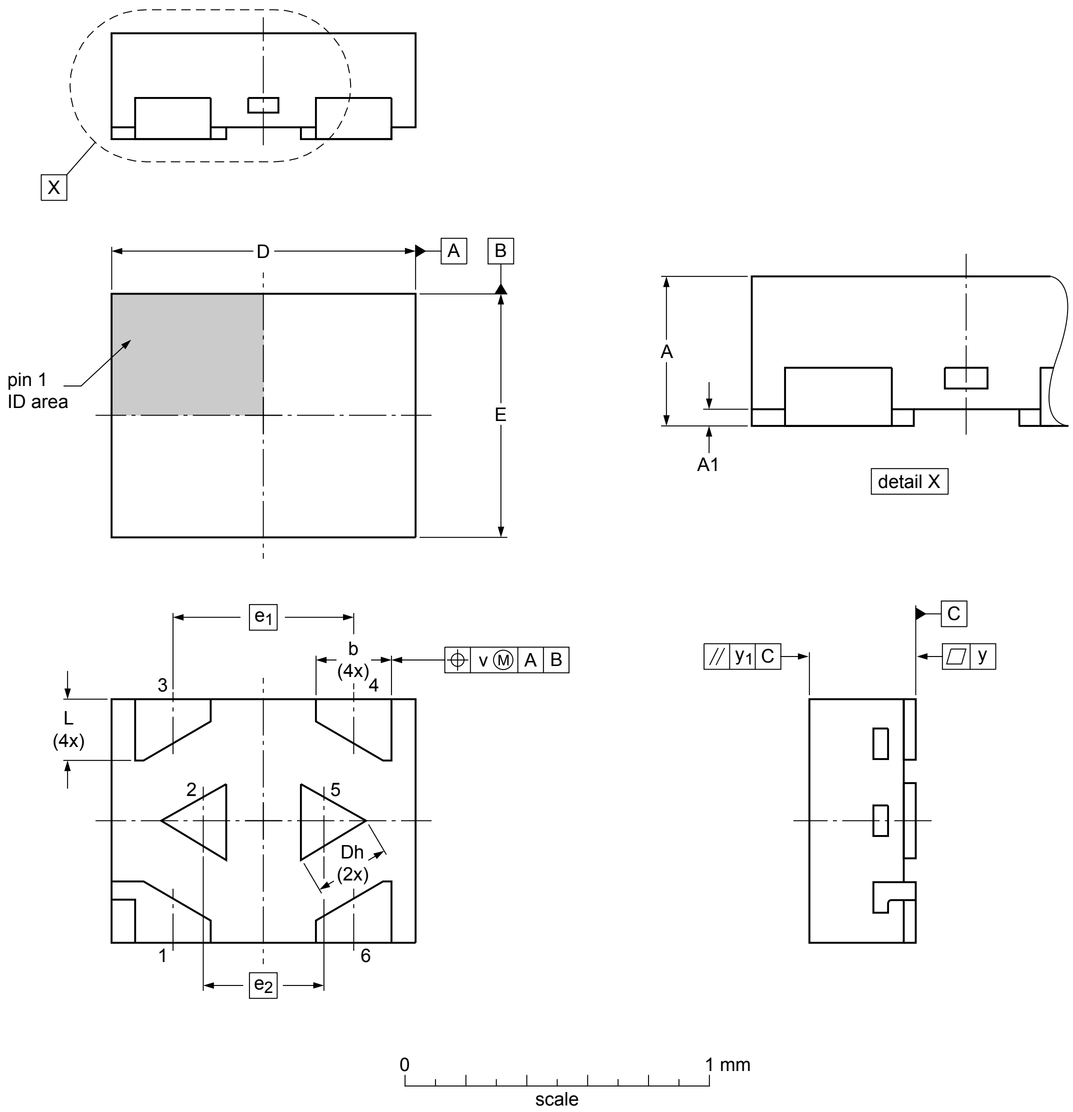
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Figure 21. Package outline SOT1202 (XSON6)

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 x 0.8 x 0.35 mm **SOT1255**



Dimensions (mm are the original dimensions)

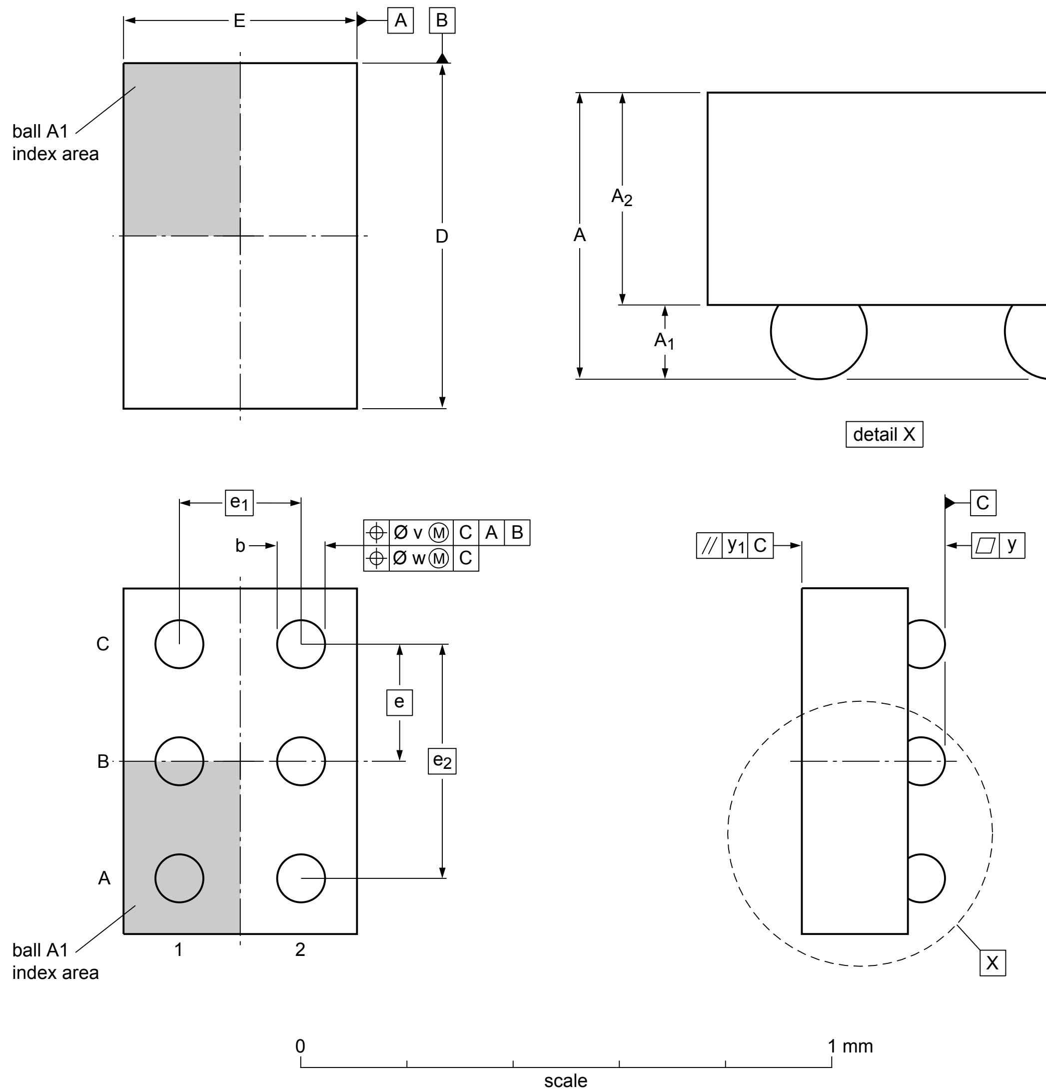
Unit		A	A_1	D	D_h	E	e_1	e_2	b	L	v	y	y_1
	max	0.35	0.04	1.05	0.30	0.85			0.30	0.25			
mm	nom	0.32	0.02	1.00	0.25	0.80	0.60	0.40	0.25	0.20	0.10	0.05	0.05
	min	0.30	0.00	0.95	0.22	0.75			0.22	0.17			

sot1255_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1255						~~15-07-20~~ 15-07-22

Figure 22. Package outline SOT1255 (X2SON6)

WLCSP6: wafer level chip-scale package, 6 bumps; 0.65 x 0.44 x 0.27 mm **SOT1454-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	0.30	0.085	0.22	0.100	0.68	0.47							
	nom	0.27	0.070	0.20	0.085	0.65	0.44	0.22	0.23	0.44	0.15	0.05	0.05	0.1
	min	0.24	0.055	0.18	0.070	0.62	0.41							

sot1454-1_po

Outline version	References IEC	References JEDEC	References JEITA		European projection	Issue date
SOT1454-1		- - -				~~15-11-16~~ 14-12-16

Figure 23. Package outline SOT1454-1 (WLCSP6)

14 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T97 v.6	20170328	Product data sheet	-	74AUP1T97 v.5
Modifications:	• Added type number 74AUP1T97UK (WLCSP6).			
74AUP1T97 v.5	20150917	Product data sheet	-	74AUP1T97 v.4
Modifications:	• Added type number 74AUP1T97GX (SOT1255/X2SON6).			
74AUP1T97 v.4	20120815	Product data sheet	-	74AUP1T97 v.3
Modifications:	• Package outline drawing of SOT886 (Figure 18) modified.			
74AUP1T97 v.3	20111130	Product data sheet	-	74AUP1T97 v.2
74AUP1T97 v.2	20101018	Product data sheet	-	74AUP1T97 v.1
74AUP1T97 v.1	20071025	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 28 March 2017
Document identifier: 74AUP1T97

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