

Large Current External FET Controller Type Switching Regulators



Dual-output Step-up, Negative Voltage, Step-down Switching Regulators (Controller type) BA9743AFV, BA9744FV, BA9741F, BA9741FS

Description

The BA9743AFV, BA9744FV, and BA9741F/FS are a 2-channel ICs, incorporating a switching regulator controller that uses a pulse width modulation. Both channels can be used for DC/DC converter operations including step up, step down, and inverting. Furthermore, since these ICs have significantly compact design, they are best suited for use as a power supply in miniature portable equipment.

Features

- 1) Built-in timer-latch type short prevention circuit
- 2) Built-in malfunction prevention circuit during low input voltage
- 3)Built-in high-accuracy reference voltage output pinBA9743AFV2.505V±1%BA9744FV1.222V±1%BA9741F/FS2.5V±4%
- 4) Rest period adjustable over the whole range of duty ratio
- 5) A wide input range provided

BA9741F	VCC=3.6 to 35V
BA9741FS	VCC=3.6 to 35V
BA9743AFV	VCC=3.6 to 35V
BA9744FV	VCC=2.5 to 35V

Aplications

DC/DC converter in LCD, PC, AV, printer, DVD, projector, TV, Fax machine, Copying machine, Measuring equipment, etc

Product lineup

	BA9743AFV	BA9744FV	BA9741F/FS
Power supply voltage	3.6V~35V	3.6V~35V	3.6V~35V
Output pin current	100mA	30mA	100mA
Output pin voltage	Max. 35V	Max. 35V	Max. 35V
Error amplifier input voltage	0.3V~1.6V	0.3V~1.5V	0.3V~1.6V
iming capacitance	100p~15000pF	100p~15000pF	100p~15000pF
iming resistance	5.1k~50kΩ	3k~15kΩ	5.1k~50kΩ
Oscillation frequency	10k~800kHz	10k~800kHz	10k~800kHz
Operating temperature	–40°C~+85°C	-40°C~+85°C	–40°C~+85°C
Package	SSOP-B16	SSOP-B16	SOP16/SSOP-A16

Absolute maximum ratings

	Ourseland		Linit			
Item	Symbol	BA9743AFV	BA9744FV	BA9741F	BA9741FS	Unit
Power supply voltage	VCC	36	36 36 36		V	
Power dissipation	Pd	450 ^{*3}	450 ^{*3}	500 ^{*1}	650 ^{*2}	mW
Operating temperature	Topr	-40~+85	-40~+85	-40-	~+85	°c
Storage temperature	Tstg	-55~+125	-55~+125	-55~+125		°c
Output pin current	lo	120 ^{*4}	60 ^{*4}	120 ^{*4}		mA
Output pin voltage	Vo	36	36	3	6	V

*1 Reduce by 4.5 mW/ °C over 25°C. (when mounted on a PCB of 50mm×50mm×1.6 mm)

*2 Reduce by 5.0 mW/ $^\circ C$ over 25 $^\circ C.$

(when mounted on a PCB of 70mm×70mm×1.6 mm)

*3 Reduce by 6.5 mW/ °C over 25°C. (when mounted on a PCB of 70mm×70mm×1.6 mm)

*4 Should not exceed Pd- or ASO-value.

Electrical characteristics

O BA9743AFV

Electrical characteristics (Unless otherwise specified, Ta=25 $^\circ\text{C}$ and Vcc=6V)

			1.5			
Item	Symbol	Min.	Limits Typ.	Max.	Unit	Conditions
[Reference voltage section]						
Output voltage	VREF	2.48	2.505	2.53	٧	IREF=1mA
Input stability	VDLI	-	1	10	mV	VCC=3.6~35V
Load stability	VDLO	-	1	10	mV	IREF=0~5mA
[Triangular wave oscillator section	ייייייייייייייייייייייייייייייייייייי					•
Oscillation frequency	Fosc	320	400	480	KHz	RRT=10kΩ,CCT=220pF
Frequency variation	FDV	_	1	_	%	VCC=3.6~35V
[Protection circuit section]						
Threshold voltage	VIT	1.48	1.64	1.80	V	
Standby voltage	VSTB	_	50	100	mV	No pull-up
Latch voltage	VLT	_	30	100	mV	No pull-up
Source current	I SCP	1.5	2.5	3.5	μA	
Comparator threshold voltage	VCT	0.95	1.05	1.15	V	5pin, 12pin
[Rest period adjustment circuit se						
Input threshold voltage	Vto	1.87	1.97	2.07	v	Duty cycle = 0%
(fosc=10kHz)	Vt100	1.38	1.48	1.58	v	Duty cycle = 100%
ON duty cycle	Don	45	55	65	%	VREF is divided by $13k\Omega$ and $27k\Omega$ resistors.
Input bias current	BDT	-	0.1	1	μA	DTC=2.0V
Latch mode source current	I DT	200	560	_	μA	DTC=OV
Latch input voltage	Vdt	2.28	2.48	_	V	IDT=40 μ A
[Low-input-voltage malfunction pre	evention circuit	section]				
Threshold voltage	Vut	2.23	2.53	2.83	٧	
			•			•
[Error amplifier section]						
[Error amplifier section] Input offset voltage	VIO	_	-	6	mV	
	V10	_	-	6 30	mV nA	
Input offset voltage			- - 15			
Input offset voltage Input offset current	110		 15 85	30	nA	
Input offset voltage Input offset current Input bias current Open loop gain	l IO I IB	- - 70 0.3		30	nA nA	VCC=3.6~35V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage	l I O I IB AV		85	30 100 —	nA nA dB	VCC=3.6~35V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio	IIO IIB AV VCM	0.3	85 —	30 100 - 1.6	nA nA dB V	VCC=3.6~35V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage	IIO IIB AV VCM CMRR	0.3 60	85 — 80	30 100 - 1.6	nA nA dB V dB	VCC=3.6~35V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output current	IIO IIB AV VCM CMRR VOM	0.3 60 2.3	85 — 80 2.5	30 100 1.6 	nA nA dB V dB V	VCC=3.6~35V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output current Output sink current	IIO IIB AV VCM CMRR VOM VOL	0.3 60 2.3 -	85 80 2.5 0.7	30 100 1.6 	nA nA dB V dB V V V mA	FB=1.25V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output current	II0 IIB AV VCM CMRR VOM VOL IOI	0.3 60 2.3 - 3	85 80 2.5 0.7 20	30 100 1.6 	nA nA dB V dB V V V	
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output voltage Minimum output current Output sink current Output source current [PWM comparator section]	II0 IIB AV VCM CMRR VOM VOL IOI	0.3 60 2.3 - 3	85 80 2.5 0.7 20	30 100 1.6 	nA nA dB V dB V V V mA	FB=1.25V FB=1.25V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode rejection ratio Maximum output voltage Minimum output current Output sink current Output source current	110 11B AV VCM CMRR VOM VOL 101 100	0.3 60 2.3 - 3 45	85 80 2.5 0.7 20 75	30 100 - 1.6 - 0.9 - -	nA nA dB V dB V V mA μA	FB=1.25V FB=1.25V Duty cycle = 0%
Input offset voltage Input offset current Input bias current Open loop gain Common-mode rejection ratio Maximum output voltage Minimum output current Output sink current Output source current [PWM comparator section] Input threshold voltage	110 11B AV VCM CMRR VOM VOL 101 100 VtO	0.3 60 2.3 - 3 45 1.87	85 80 2.5 0.7 20 75 1.97	30 100 - 1.6 - 0.9 - - 2.07	nA nA dB V dB V V mA μ A	FB=1.25V FB=1.25V
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output voltage Minimum output current Output sink current Output source current [PWM comparator section] Input threshold voltage (fosc=10kHz) [Output section]	110 11B AV VCM CMRR VOM VOL 101 100 VtO	0.3 60 2.3 - 3 45 1.87	85 80 2.5 0.7 20 75 1.97	30 100 - 1.6 - 0.9 - - 2.07	nA nA dB V dB V V mA μ A	FB=1.25V FB=1.25V Duty cycle = 0%
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output voltage Minimum output current Output sink current Output source current [PWM comparator section] Input threshold voltage (fosc=10kHz)	110 11B AV VCM CMRR VOM VOL 101 100 Vt0 Vt0	0.3 60 2.3 - 3 45 1.87	85 80 2.5 0.7 20 75 1.97 1.48	30 100 - 1.6 - 0.9 - - 2.07 1.58	nA nA dB V dB V V mA μ A V V V	FB=1.25V FB=1.25V Duty cycle = 0% Duty cycle = 100%
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output voltage Minimum output current Output sink current Output source current [PWM comparator section] Input threshold voltage (fosc=10kHz) [Output section] Saturation voltage Leak current	110 11B AV VCM CMRR V00 101 100 Vt0 Vt0 Vt0 Vt0	0.3 60 2.3 - 3 45 1.87 1.38	85 80 2.5 0.7 20 75 1.97 1.48	30 100 - 1.6 - 0.9 - - 2.07 1.58 1.2	nA nA dB V dB V mA μA V V V V V V V V V V V V V	FB=1.25V FB=1.25V Duty cycle = 0% Duty cycle = 100%
Input offset voltage Input offset current Input bias current Open loop gain Common-mode input voltage Common-mode rejection ratio Maximum output voltage Minimum output voltage Minimum output current Output sink current Output source current [PWM comparator section] Input threshold voltage (fosc=10kHz) [Output section] Saturation voltage	110 11B AV VCM CMRR V00 101 100 Vt0 Vt0 Vt0 Vt0	0.3 60 2.3 - 3 45 1.87 1.38	85 80 2.5 0.7 20 75 1.97 1.48	30 100 - 1.6 - 0.9 - - 2.07 1.58 1.2	nA nA dB V dB V mA μA V V V V V V V V V V V V V	FB=1.25V FB=1.25V Duty cycle = 0% Duty cycle = 100%

 \bigodot This IC is not designed to be radiation-resistant.

OBA9744FV

Electrical characteristics (Unless otherwise specified, Ta=25 $^\circ\text{C}$ and Vcc=3V)

Item	Symbol		Limits		Linit	Conditions
Item	Symbol	Min.	Тур.	Max.	Unit	Conditions
Reference voltage section]						
Dutput voltage	VREF	1.210	1.222	1.234	V	IREF=1mA
nput stability	VDLI	-	3	10	mV	VCC=2.5~35V
oad stability	VDLO	-	1	10	mV	IREF=0~5mA
Triangular wave oscillator section	1]					
Dscillation frequency	Fosc	320	400	480	KHz	RRT=5.1k,CCT=220pF
Frequency variation	FDV	-	1	-	%	Vcc=2.5~35V
Protection circuit section]						
hreshold voltage	Vit	0.98	1.18	1.38	V	
Standby voltage	VSTB	-	50	100	mV	No pull-up
atch voltage	VLT	_	23	100	mV	No pull-up
Source current	I SCP	1.0	2.0	3.0	μA	
Comparator threshold voltage	Vст	0.15	0.25	0.35	V	5pin, 12pin
Rest period adjustment circuit se	ction]					
nput threshold voltage	Vto	0.96	1.01	1.06	V	Duty cycle=0%
fosc=10kHz)	Vt100	0.46	0.49	0.52	V	Duty cycle=100%
ON duty cycle	Don	45	55	65	%	
nput bias current	BDT	-	0.1	1	μA	DTC=2V
atch mode source current	IDT	390	780	-	μA	DTC=0V
atch input voltage	Vdt	Vcc-0.5	Vcc-0.4	-	V	IDT=40 μ A
ow-input-voltage malfunction pre	evention circuit	section]				
hreshold voltage	Vut	1.6	1.9	2.2	V	
Error amplifier section]						
nput offset voltage	VIO	-	0	6	mV	
nput offset current	110	-	0	30	nA	
nput bias current	ЦВ	-	15	100	nA	
Dpen loop gain	AV	65	85	-	dB	
Common-mode input voltage	VCM	0.3	-	1.5	V	VCC=2.5~35V
Common-mode rejection ratio	CMRR	60	80	_	dB	
Aaximum output voltage	Vom	1.5	2.0	_	V	
/inimum output current	Vol	-	0.1	0.3	V	
Dutput sink current	101	1	2.1	_	mA	FB=0.75V
Dutput source current	100	50	70	90	μA	FB=0.75V
PWM comparator section]						
nput threshold voltage	Vt0	0.96	1.01	1.06	V	Duty cycle=0%
(fosc=10kHz)	Vt100	0.46	0.49	0.52	V	Duty cycle=100%
Output section]						
Saturation voltage 1	VSAT	-	0.06	0.3	V	lo=10mA
Saturation voltage 2	VSAT	-	0.15	0.4	V	Io=30mA
eak current	LEAK	-	0	5	μA	Vo=35V
Total device]						
Total device] Standby current	ICCS	_	3.6	5.0	mA	When output is OFF

 \bigodot This IC is not designed to be radiation-resistant.

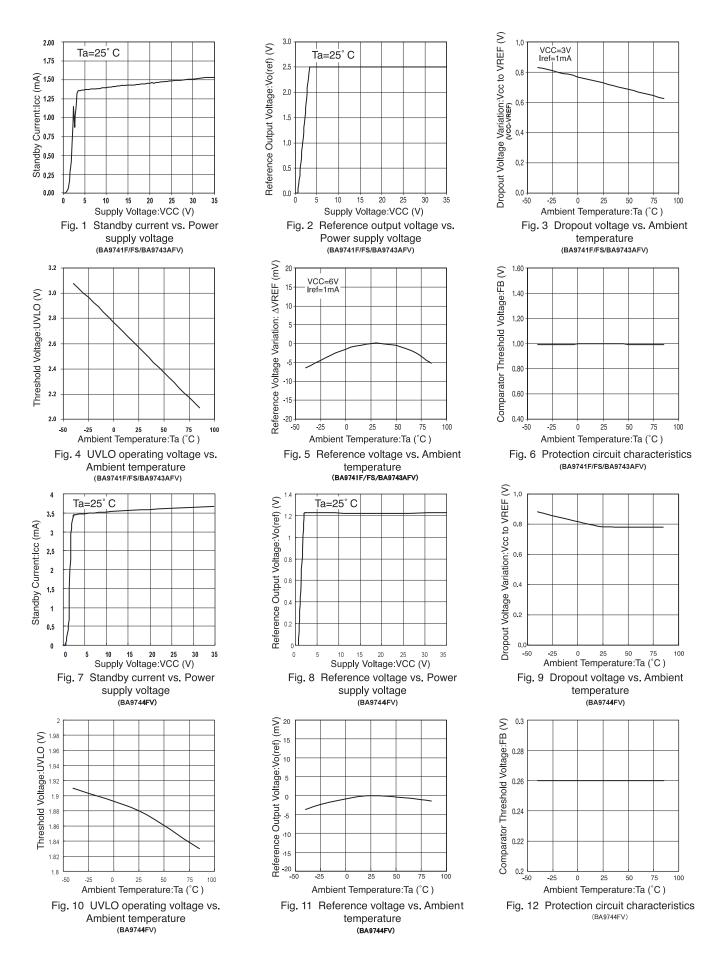
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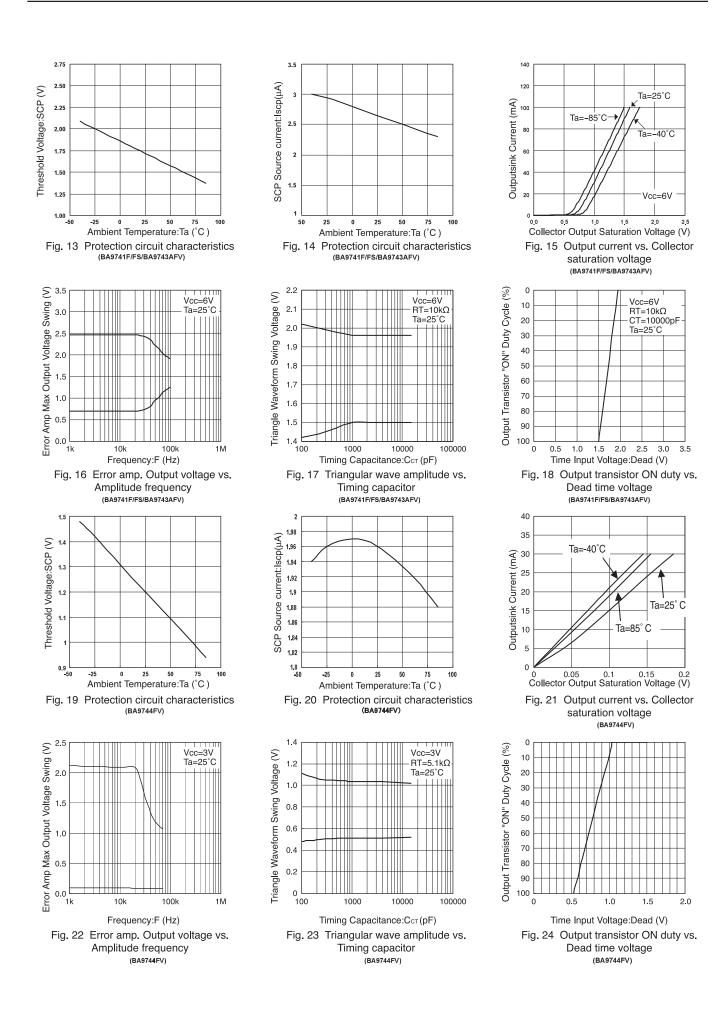
Electrical characteristics (Unless otherwise specified, Ta=25 $^{\circ}\text{C}$ and Vcc=3V)

Itom	Symbol		Limits		Linit	Conditions
Item	Symbol	Min.	Тур.	Max.	Unit	Conditions
[Reference voltage section]						
Output voltage	VREF	2.4	2.5	2.6	V	IREF=1mA
Input stability	VDLI	-	1	10	mV	VCC=3.6~35V
Load stability	VDLO	-	1	10	mV	IREF=0~5mA
[Triangular wave oscillator sectio	n]					
Oscillation frequency	Fosc	320	400	480	KHz	RRT=10kΩ,CCT=220pF
Frequency variation	FDV	-	1	-	%	VCC=3.6~35V
[Protection circuit section]						
Threshold voltage	VIT	1.48	1.64	1.80	V	
Standby voltage	VSTB	-	50	100	mV	No pu li- up
Latch voltage	VLT	-	30	100	mV	No pu l- up
Source current	ISCP	1.5	2.5	3.5	μA	
Comparator threshold voltage	VCT	0.9	1.05	1.2	V	5pin, 12pin
[Rest period adjustment circuit se	ection]					
Input threshold voltage	Vto	1.79	1.97	2.15	V	Duty cycle=0%
(fosc=10kHz)	Vt100	1.32	1.48	1.64	V	Duty cycle=100%
ON duty cycle	Don	45	55	65	%	VREF is divided by $13k\Omega$ and $27k\Omega$ resistors
Input bias current	BDT	_	0.1	1	μA	DTC=2.0V
Latch mode source current	I DT	200	560	_	μΑ	DTC=0V
Latch input voltage	VDT	2.28	2.48	-	V	IDT=40 μ A
[Low-input-voltage malfunction p	revention circuit	section]				
Threshold voltage	VUT	_	2.53	-	V	
[Error amplifier section]						
Input offset voltage	VIO	-	-	6	mV	
Input offset current	110	-	_	30	nA	
Input bias current	ЦВ	-	15	100	nA	
Open loop gain	AV	70	85	_	dB	
Common-mode input voltage	VCM	0.3	_	1.6	v	VCC=3.6~35V
Common-mode rejection ratio	CMRR	60	80	-	dB	100 0.0 001
Maximum output voltage	Vom	2.3	2.5	_	V	
Minimum output current	Vol	_	0.7	0.9	V	
Output sink current	101	3	20	_	mA	FB=1.25V
Output source current	100	45	75		μΑ	FB=1.25V
[PWM comparator section]	100				port	1.5 11201
	Vt0	1.79	1.97	2.15	V	Duty cycle=0%
Input threshold voltage (fosc=10kHz)	Vt10	1.32	1.48	1.64	v	Duty cycle=100%
[Output section]	1100	1.02	1.40	1.04		
Saturation voltage	VSAT	_	0.8	1.2	V	lo=75mA
Leak current	VSAT ILEAK		0.8	5	μΑ	Vo=35V
	ILEAK	-		5	μΑ	¥ 0=00 ¥
[Total device]	1000		1.2	1.0		When output in OEE
Standby current		_	1.3	1.8	mA	When output is OFF
Average current dissipation This IC is not designed to be rad	ICCA	-	1.6	2.3	mA	RRT=10kΩ

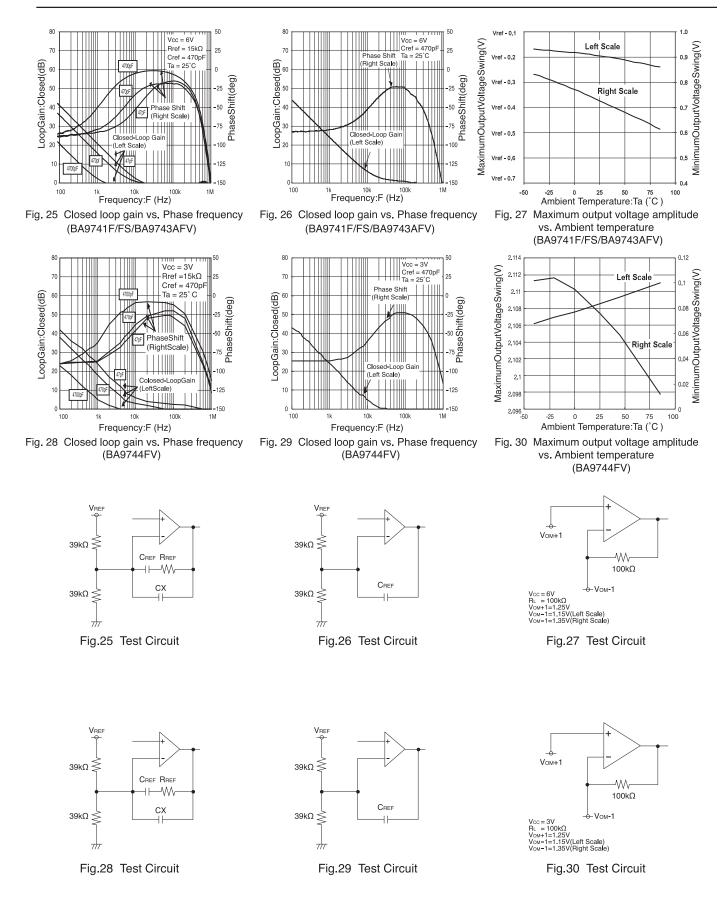
 \bigodot This IC is not designed to be radiation-resistant.

Reference data

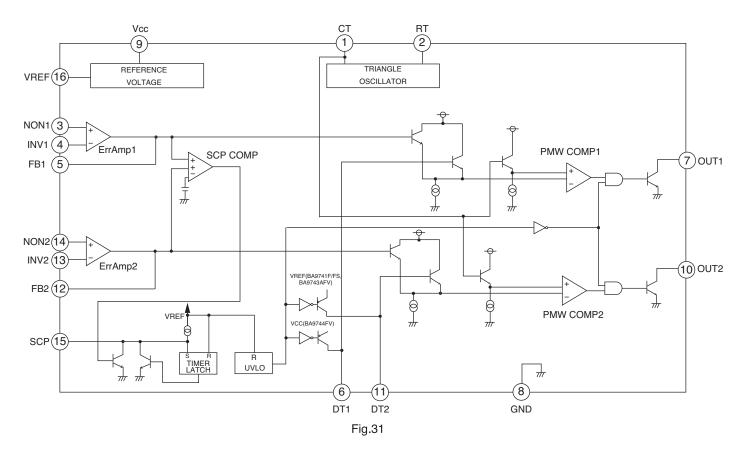


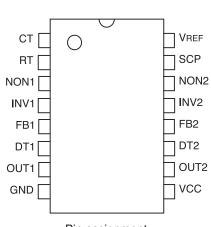


BA9743AFV, BA9744FV, BA9741F/FS



• Block diagram/Pin assignment





Pin	assignment
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PIN	Pin name	Function
No.		
1	СТ	External timing capacitance
2	RT	External timing resistance
3	NON 1	Positive input for error amplifier 1
4	I N V 1	Negative input for error amplifier 1
5	FB1	Output for error amplifier 1
6	DT1	Output 1 dead time/soft start setting
7	OUT 1	Output 1
8	GND	GROUND
9	VCC	Power supply
10	OUT 2	Output 2
11	DT2	Output 2 dead time / soft start setting
12	FB2	Output for error amplifier 2
13	I N V 2	Negative input for error amplifier 2
14	NON2	Positive input for error amplifier 2
15	SCP	Timer latch setting
16	Vref	Reference voltage output

Description of operations

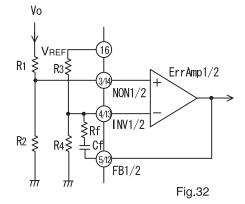
1) REFERENE VOLTAGE (Reference voltage section)

From the power supply voltage input through the VCC pin (pin 9), a reference voltage, which is stabilized at the VREF, is supplied as the operating power supply voltage for the internal circuits of the IC and, at the same time, output through the VREF pin (pin 16).

2) ErrAmp1/2 (Error amplifiers)

In the case of step up / step down application, the non-inverting input pins NON1 and NON2 are used to detect the output voltage by feeding back the voltage from the final output stage (i.e., loading side). R1 and R2, which are connected to these pins, are resistors used to control the output voltage. The voltage applied to the inverting input pins INV1 and INV2 as a reference input voltage of the error amplifiers themselves, should be the voltage obtained by dividing the reference voltage (VREF) by resistance.

$$(V_{REF} \ \frac{R4}{R3 + R4})$$



Furthermore, the resistor Rf and the capacitor Cf, connected between the FB1/2 (Pin 5/12) and INV1/2 (Pin 6/11), are used for feedback of the error amplifier, enabling settings of any desired level of loop gain.

It is recommended to provide AC feedback using the capacitor Cf and the resistor Rf as the feedback for the error amplifier. The amplifier output pins FB1 and FB2 are connected to the PWM and SCP comp., and used as the non-inverting input pins. The output voltage (Vo) setting is shown below:

$$Vo = \frac{R1 + R2}{R2} \times (VREF \frac{R4}{R3 + R4})$$

Since the input range VOM of the NON and INV pins is 0.3V to 1.6V (for BA9741F/FS / BA9743AFV) or 0.3V to 1.5V (for BA9744FV), it is recommended to set the range to approximately VREF/2, i.e., as shown below.

3) Triangle Oscillator (Triangular wave oscillator section)

Used to generate a triangular waveform to be input in the PWM comp. 1/2.

The oscillator circuit charges/discharges the timing capacitor CCT that is connected between the CT pin (pin 1) and the GND at a constant current, set with resistor RRT that is connected between the RT pin (pin 2) and the GND. The triangular waveform is obtained through detecting and resetting this charged/discharged voltage.

The oscillation frequency is given through the external CCT and RRT pins by the formula shown below (BA9741F/FS/BA9743AFV): (BA9741F/FS/BA9743AFV)

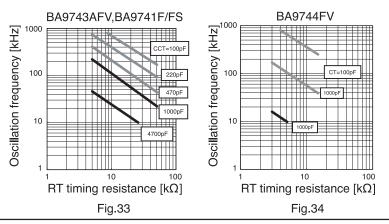
fosc ≒VRT/(2·CCT·RRT·ΔVosc)≒ 1/(CCT·RRT) VRT: RT pin voltage 1Vtyp ΔVosc: Triangular wave amplitude voltage=Vt0-Vt100=0.49Vtyp (BA9744FV) fosc ≒ VRT/(2·CCT·RRT·ΔVosc) ≒ 1/(CCT·RRT) VRT: RT pin voltage 0.6Vtyp ΔVosc: Triangular wave amplitude voltage=Vt0-Vt100=0.52Vtyp

However, at high frequencies, since delay in the internal circuit results in an error against the formula, set oscillation frequency according to the fosc- RRT graph shown below:

Furthermore, this triangular wave can be output through the CT pin (pin 1).

Range of standard external CCT and RRT pins

RRT: 5.1k Ω at minimum to 50k Ω at maximum (BA9741F/FS / BA9743AFV) or 3k Ω at minimum to 15k Ω at maximum (BA9744FV) CCT: 100pF at minimum to 15000pF at maximum



4) SCP Comp (Timer-latch type short-circuit prevention circuit)

When the output voltage malfunctions because of a short circuit, this function is used to turn OFF the output transistor forcedly, in order to protect the system. If the output voltage drops in realtion to the set voltage level, an error will be amplified through the Err Amp and the voltage at the FB1/FB2 pins will reach the low voltage side. If SCP Comp sets the voltage below the threshold level for either the FB1 or FB2, (i.e., 1.05Vtype for the BA9741F/FS / BA9743AFV or 0.25Vtype for the BA9744FV), the short prevention circuit will be activated to start the charging of the capacitor of SCP pin. When VIT=1.64Vtyp for the BA9741F/FS / BA9743AFV or VIT=1.18Vtyp for the BA9744FV is achieved, the output transistor will turn OFF.

The time is set by the capacitor (Cscp) connected to the SCP (pin 15) . The time TscP is obtained by the formula shown below:

$$SCPT = \frac{VIT + VSTB}{ISCP} \cdot CSCP$$

For example, in the case of the BA9743AFV, assuming that CSCP=0.1µF, VIT=1.64V, VSTB=0.05V and ISCP=2.5µA.

SCPT =
$$\frac{1.64 - 0.05}{2.5\mu} \times 0.1\mu$$
 = 63.6mS

In order to stop the function of the short prevention circuit, short-circuit the SCP pin to GND

5) PWM Comp 1/2 DEAD TIME (Rest period adjustment circuit / Dead time)

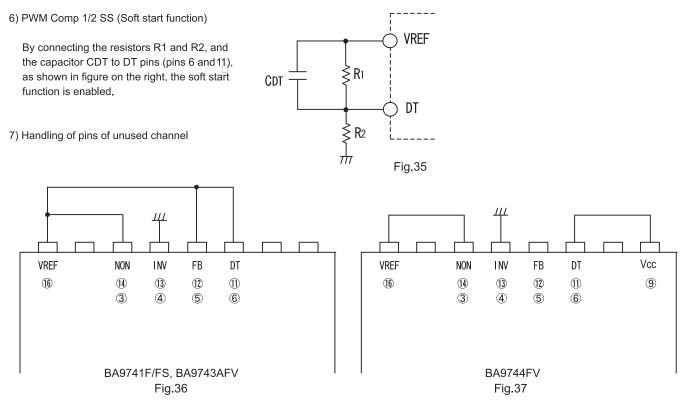
This function can be set by dividing the resistance of DT1 and DT2 pins (pins 6 and 11) between VREF and GND. With PWM Comp, comparing the dead time voltage input and the error voltage from the Err Amp with the triangular wave, the output drive transistors are turned ON/OFF.

When Dead time voltage>Error voltage, the output duty is determined by the dead time voltage. The dead time voltage VDT is obtained by the expression shown below

$$VD = V_{REF} \cdot \frac{R2}{R1 + R2}$$

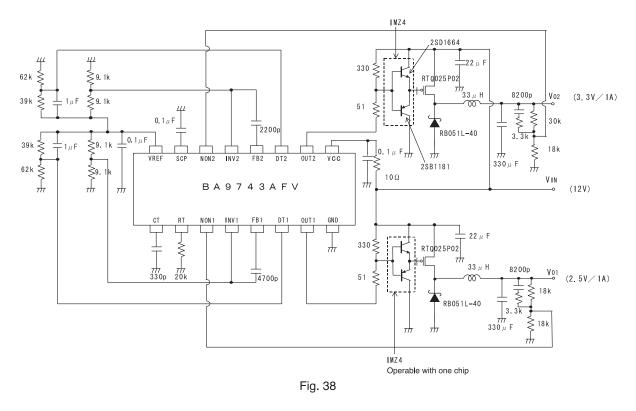
(BA9741F/FS/BA9743AFV) When VDT=1.48Vtyp: Duty 100% When VDT=1.97Vtyp: Duty 0% (Provided, howeve, that fosc=10kHz) (BA9744FV) When VDT=0.49Vtyp: Duty 100% When VDT=1.01Vtyp: Duty 0% (Provided; howeve that fosc=10kHz)

Note: If the oscillation frequency is at a high level, the upper/lower limits (Vt0/Vt100) of the triangular wave will be shifted in the direction in which the amplitude is developed.



If channel 1 is only used, the unused channel should be handled as shown above.

• Typical application circuit



1) Setting the coil (L) and capacitor (Co) of output section

The settings of the coil and capacitor with the step down application are made as shown below:.

<Setting of L value>

If the load current increases, a current will continuously flow through the coil, thus holding the relational formulas (1).

	Ts	$(VIN - Vo) \times Vo$	(1)	VIN	: Input voltage
Γ=	$\Delta IL \times$	$\frac{(VIN - VO) \times VO}{VIN}$	(1)	Ts	: 1/(Oscillation frequency)
				ΔIL	: Ripple current of coil

 Δ IL should tyically be set to 30% or less than the maximum output current (lomax). Increasing the L value decreases the ripple current (Δ IL). Generally, the larger the L value, the smaller the allowable current of coil.

Consequently, since the ripper current exceeding the allowable current results in variations in the L value, check for the appropriate current value with the coil manufacturer.

<Setting of output capacitor Co>

The output capacitor Co should be selected according to the ESR (Electric Series Resistance) characteristics of the capacitor. For the output ripple voltage (Δ Vo), the following formula is held according to the ESR of the output capacitor:

$\Delta \mathsf{Vo}\,\dot{\leftrightarrows}\,\Delta\mathsf{IL}\,{\times}\,\mathsf{ESR}$

ESR: Series resistance of the output capacitor Co

A ripple component, due to the output capacitor, is significantly small in comparison to that due to the ESR. Even though the Co value should meet the condition of $1/(3\cdot Ts) > 1/2\pi$ (L × Co)1/2, it is recommended to use a capacitor with a high enough capacitance value, to meet the ESR condition.

<Switching element>

The switching element should be determined according to the peak current. The peak current lsw (peak) flowing thought the switching element is equal to that flowing through the coil, thus holding the formula shown below:

Isw (peak) = Io + Δ IL/2

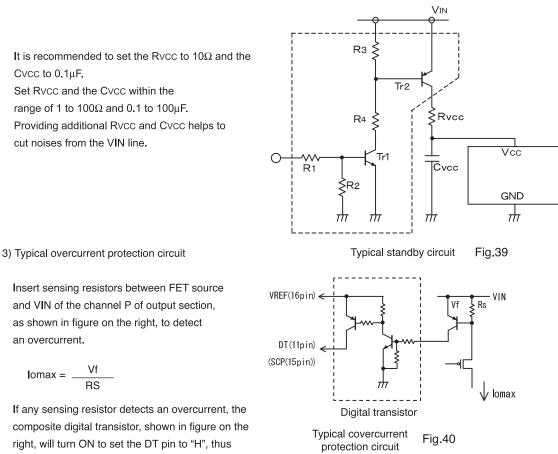
Select a switching element that has an allowable current that is twice (or more) as large as the peak current obtained by the formula shown above. Furthermore, with consideration given to overcurrent caused by output short-circuited, provide an application for overcurrent protection, wherever necessary.

2) Typical standby circuit

The typical standby circuit is shown in the dotted frame below.

An additional switch is typically mounted between the power supply (VIN) and the IC power supply pin (Vcc).

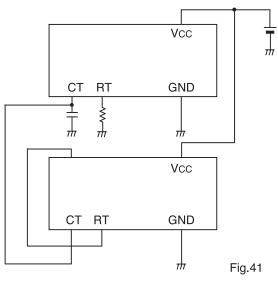
Controlling the switch so that Tr1 and Tr2 will turn OFF when the standby circuit is activated, reduces current flow in standby mode.



turning OFF the output.

Once the DT pin has been set to "H", soft start (restart) mode is enabled through an external capacitor.Furthermore, if an overcurrent flows through the circuit, latching will be enabled through connecting the digital transistor PNP collector to the SCP pin (pin 15).

4) Typical application of Master/Slave operation circuit

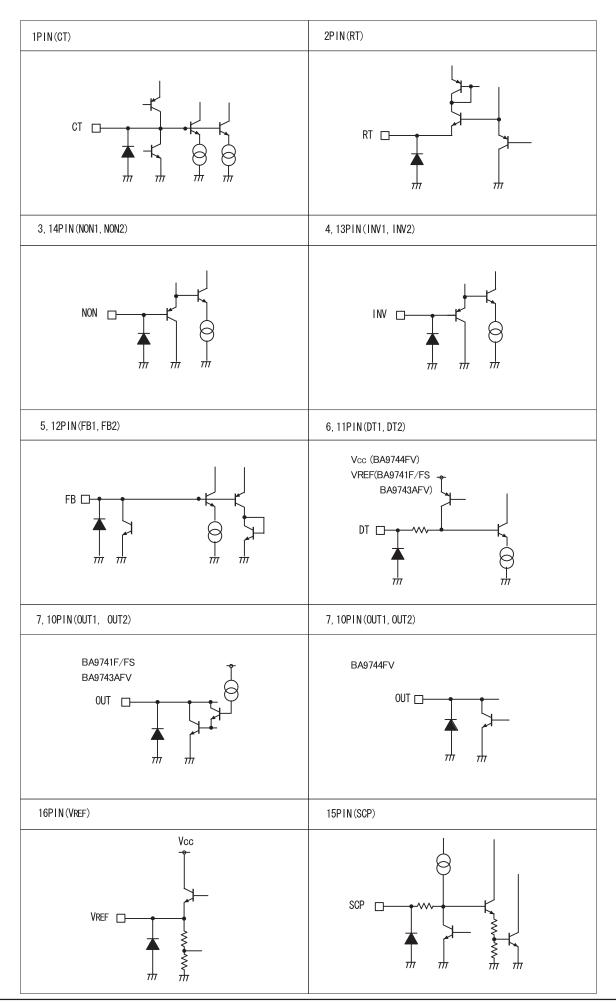


Caution:

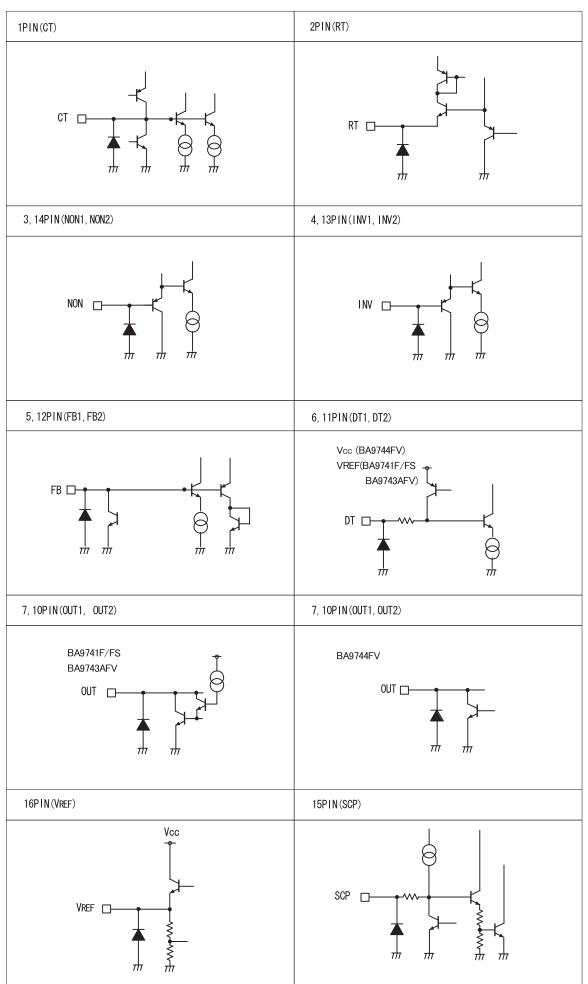
The oscillation frequency should be determined according to capacitors and resistors connected to the CT pin (pin 1) and RT pin (pin 2) on the master IC.

However, increasing the number of slave ICs, increases the parasitic capacitance of these ICs in contact with the CT pin, resulting in a drift of oscillation frequency.

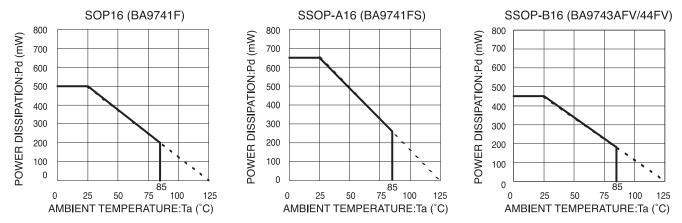
Equivalent circuit



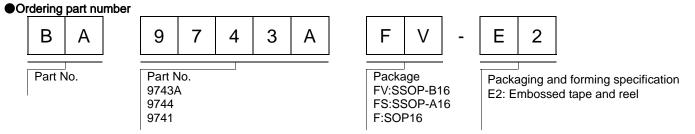
Equivalent circuit



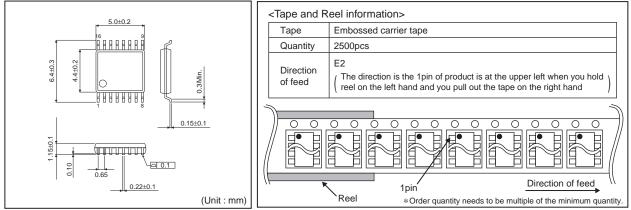
•Heat dissipation characteristics



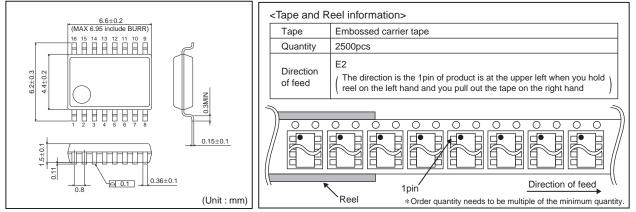
Note: When mounted on a printed circuit board of 70.0×70.0×1.6 mm (SOP16 and SSOP-A16) When mounted on a printed circuit board of 50.0×50.0×1.6 mm (SSOP-B16)



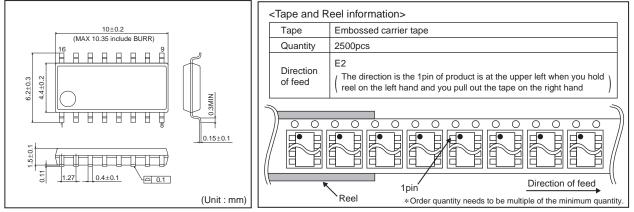
SSOP-B16



SSOP-A16







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 - [h] Use of the Products in places subject to dew condensation
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For details, please refer to ROHM Mounting specification

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 - [d] the Products are exposed to high Electrostatic
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- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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