**Product data sheet** 

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high bidirectional blocking voltage and high current surge capability with high thermal cycling performance.

## 2. Features and benefits

- · High bidirectional blocking voltage capability
- · High current surge capability
- · High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Capacitive Discharge Ignition (CDI)
- · Crowbar protection
- · Inrush protection
- Motor control
- Voltage regulation

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{RRM}$	repetitive peak reverse voltage			-	-	650	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>h</sub> ≤ 69 °C		-	-	7.5	Α
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_h \le 69 ^{\circ}\text{C}$ ; $\overline{\text{Fig. 1}}$ ; $\overline{\text{Fig. 2}}$ ; $\overline{\text{Fig. 3}}$		-	-	12	Α
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5		-	-	120	Α
		half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms		-	-	132	Α
Tj	junction temperature			-	-	125	°C
Static characteristics							
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 7$		-	2	15	mA
Dynamic characteristics							

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 436 V; $T_j$ = 125 °C; $R_{GK}$ = 100 Ω; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; Fig. 12	200	1000	-	V/µs
		$V_{DM}$ = 436 V; $T_j$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit; Fig. 12	50	130	-	V/µs

# 5. Pinning information

### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	mb	A <del>- [                                  </del>
2	Α	anode		G sym037
3	G	gate		Symosi
mb	n.c.	mounting base; isolated		
			1 2 3	
			TO-220F (SOT186A)	

# 6. Ordering information

### **Table 3. Ordering information**

Type number	Package					
	Name	Description	Version			
BT151X-650R	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A			

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# 7. Limiting values

### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	650	V
$V_{RRM}$	repetitive peak reverse voltage		-	650	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>h</sub> ≤ 69 °C	-	7.5	Α
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_h \le 69 ^{\circ}\text{C}$ ; Fig. 1; Fig. 2; Fig. 3	-	12	Α
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5	-	120	А
		half sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 8.3 ms	-	132	Α
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	72	A²s
dl <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 30 mA	-	50	A/µs
I <sub>GM</sub>	peak gate current		-	2	Α
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
T <sub>j</sub>	junction temperature		-	125	°C

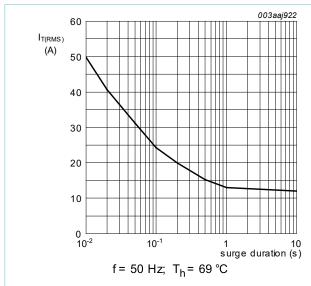


Fig. 1. RMS on-state current as a function of surge duration; maximum values

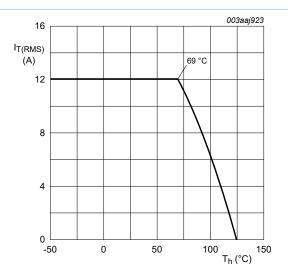


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

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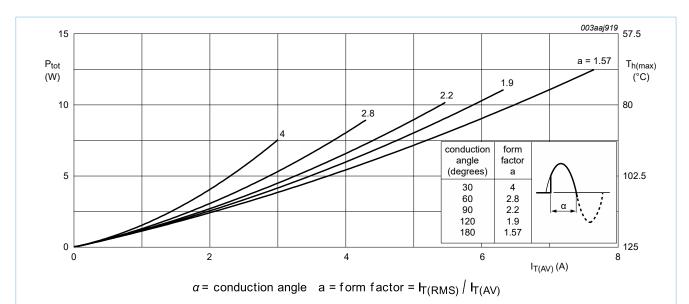


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

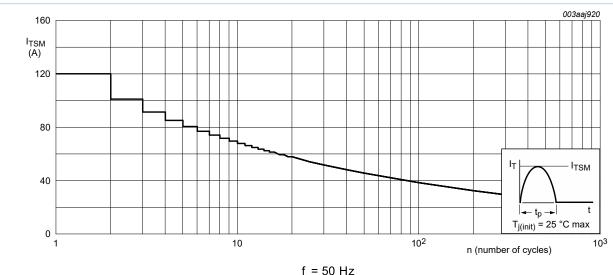
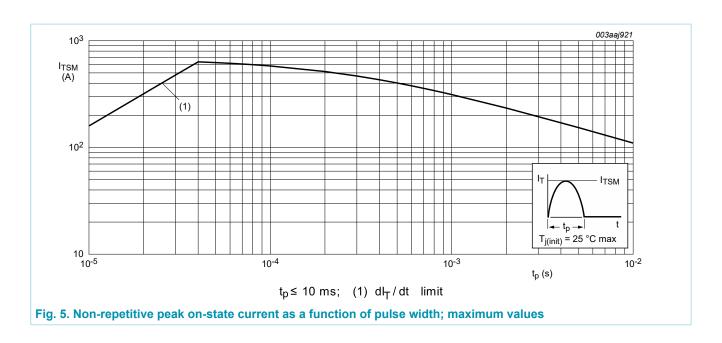


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

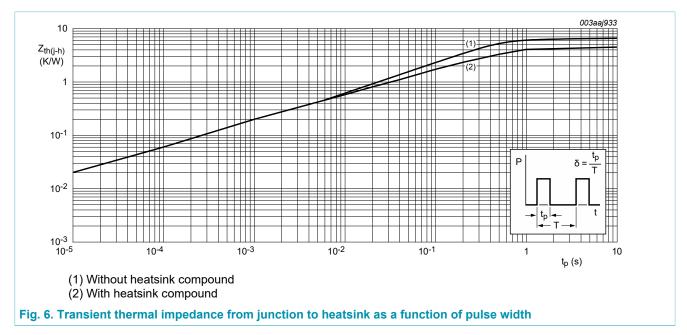
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## 8. Thermal characteristics

**Table 5. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-h)</sub>	thermal resistance	with heatsink compound; Fig. 6	-	-	4.5	K/W
	from junction to heatsink	without heatsink compound; Fig. 6	-	-	6.5	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



## 9. Isolation characteristics

**Table 6. Isolation characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>isol(RMS)</sub>	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz $\leq$ f $\leq$ 60 Hz; RH $\leq$ 65 %; T <sub>h</sub> = 25 °C	-	-	2500	V
C <sub>isol</sub>	isolation capacitance	from anode to external heatsink; f = 1 MHz; T <sub>h</sub> = 25 °C	-	10	-	pF

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## 10. Characteristics

**Table 7. Characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C}; Fig. 7$	-	2	15	mA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T_j = 25 \text{ °C}; Fig. 8$	-	10	40	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	7	20	mA
$V_{T}$	on-state voltage	I <sub>T</sub> = 23 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.75	V
$V_{GT}$	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.6	1	V
		$V_D$ = 650 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11	0.25	0.4	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 650 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
I <sub>R</sub>	reverse current	V <sub>R</sub> = 650 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
Dynamic ch	naracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 436 V; $T_j$ = 125 °C; $R_{GK}$ = 100 Ω; $(V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; Fig. 12	200	1000	-	V/µs
		$V_{DM}$ = 436 V; $T_j$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit; Fig. 12	50	130	-	V/µs
t <sub>gt</sub>	gate-controlled turn-on time	$I_{TM}$ = 40 A; $V_D$ = 650 V; $I_G$ = 100 mA; $dI_G/dt$ = 5 A/ $\mu$ s; $T_j$ = 25 °C	-	2	-	μs
t <sub>q</sub>	commutated turn-off time	$V_{DM} = 436 \text{ V}; T_j = 125 \text{ °C}; I_{TM} = 20 \text{ A}; V_R = 25 \text{ V}; (dI_T/dt)_M = 30 \text{ A/µs}; dV_D/dt = 50 \text{ V/µs}; R_{GK(ext)} = 100 \Omega; (V_{DM} = 67\% \text{ of V}_{DRM})$	-	70	-	μs

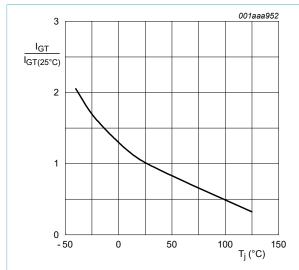


Fig. 7. Normalized gate trigger current as a function of junction temperature

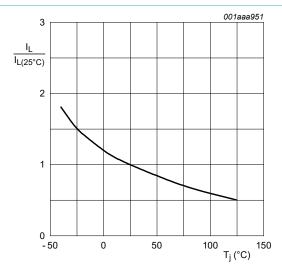


Fig. 8. Normalized latching current as a function of junction temperature

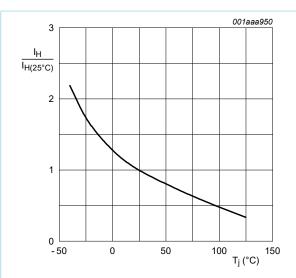
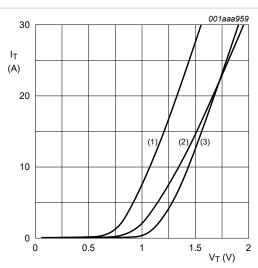


Fig. 9. Normalized holding current as a function of junction temperature



 $V_o$  = 1.06 V;  $R_s$  = 0.0304  $\Omega$ 

(1)  $T_j = 125$  °C; typical values (2)  $T_j = 125$  °C; maximum values

(3) T<sub>i</sub> = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

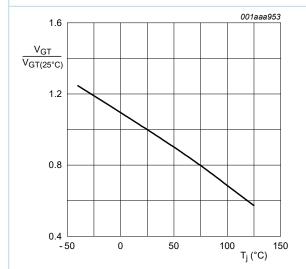
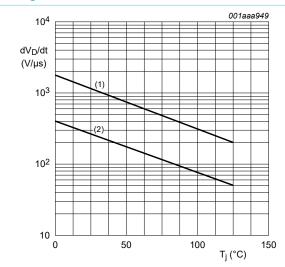


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

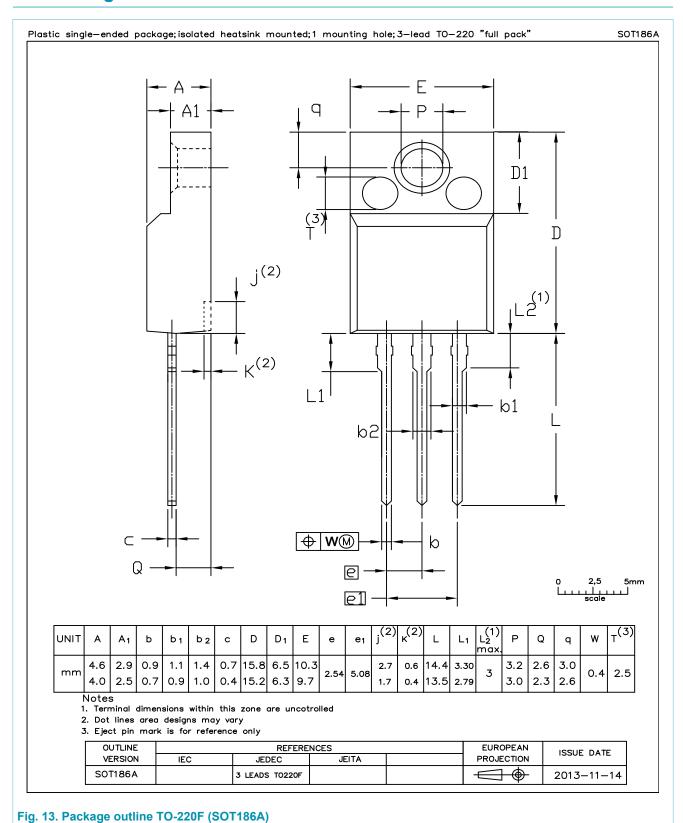


(1)  $R_{GK} = 100 \Omega$ ;

(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

# 11. Package outline



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# 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.ween-semi.com
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