Digital Controller for Isolated Power Supply Applications

ADP1043A

FEATURES

- **Integrates all typical controller functions**
  - **Digital control loop**
  - **Remote and local voltage sense**
  - **Primary and secondary side current sense**
  - **PWM control**
  - **Synchronous rectifier control**
  - **Current sharing**
  - **Integrated programmable loop filter**
- **I²C interface**
- **Extensive fault detection and protection**
- **Extensive programming**
- **Fast calibration**
- **EEPROM**
- **Standalone or microcontroller control**

APPLICATIONS

- **AC-to-DC power supplies**
- **Isolated dc-to-dc power supplies**
- **Redundant power supplies**
- **Parallel power supplies**
- **Server, storage, network, and communications infrastructure**

GENERAL DESCRIPTION

The ADP1043A is a secondary side power supply controller IC designed to provide all the functions that are typically needed in an ac-to-dc or isolated dc-to-dc control application.

The ADP1043A is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, pulse-width modulation (PWM) generation, and hot-swap sense and control. The control loop is digital with an integrated programmable digital filter. Protection features include current limiting, ac sense, undervoltage lockout (UVLO), and overvoltage protection (OVP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and redundancy of critical circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard I²C bus provides access to the many monitoring and system test functions.

The ADP1043A is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

TYPICAL APPLICATION CIRCUIT

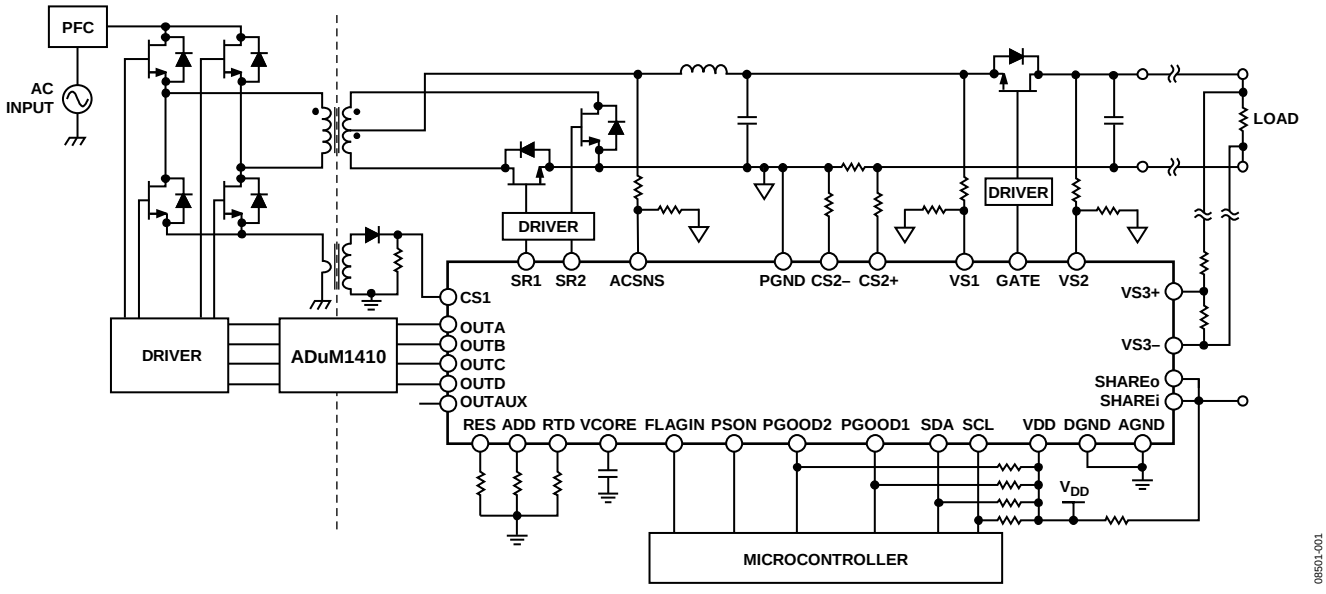


Figure 1.

Rev. 0

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REVISION HISTORY

10/09—Revision 0: Initial Version

The ADP1043A is a secondary side controller for switch mode power supplies (SMPS). It is designed for use in isolated redundant applications. The ADP1043A integrates the typical functions that are needed to control a power supply. These include

- Output voltage sense and feedback
- Digital loop filter compensation
- PWM generation
- Current sharing
- Current, voltage, and temperature sense
- OrFET control
- Housekeeping and I²C interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block. The feedback ADCs use a multipath approach (patent pending). The ADP1043A combines a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. Loop compensation is implemented using the digital filter. This PID (proportional, integral, derivative) filter is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs.

The PWM block generates up to seven programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and unique switching topologies to be realized.

A current share bus interface provides for parallel power supplies. The part also has hot-swap OrFET sense and control for N + 1 redundant power supplies.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary and secondary side current sense, are included. An extensive set of protections is offered, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), ground continuity monitoring, and ac sense.

All these features are programmable through the I²C bus interface. This bus interface is also used to calibrate the power supply. Other information, such as input current, output current, and fault flags, is also available through the I²C bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1043A. For more information about the GUI, contact Analog Devices, Inc., for the latest software and a user guide.

The ADP1043A operates from a single 3.3 V supply and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

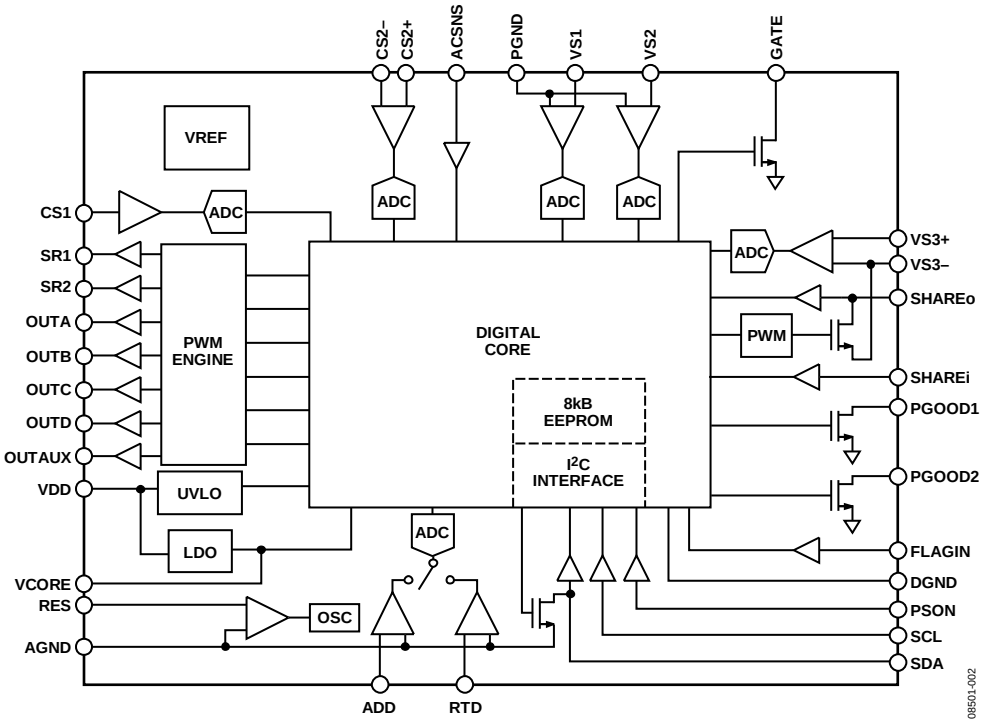


Figure 2.

SPECIFICATIONS

V_{DD} = 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	V_{DD}		3.1	3.3	3.6	V
I_{DD}	I_{DD}	Normal operation (PSON is high)		20		mA
		Power supply off (PSON is low)		15		mA
		During EEPROM programming (40 ms)		I_{DD} + 8		mA
POWER-ON RESET						
Power-On Reset		V_{DD} rising	3.05			V
UVLO		V_{DD} falling	2.75	2.85	2.95	V
UVLO Hysteresis				35		mV
OVLO			3.7	3.9	4.1	V
VCORE PIN						
Output Voltage		T_A = 25°C	2.3	2.5	2.7	V
OSCILLATOR AND PLL						
PLL Frequency		RES = 49.9 kΩ	190	200	210	MHz
OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2 PINS						
Output Low Voltage	V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage	V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
AC SENSE		PWM and resonant mode				
Input Voltage Threshold			0.3	0.45	0.65	V
Propagation Delay		From ACSNS threshold to SR start; resonant mode only		160		ns
VS1, VS2, VS3 LOW SPEED ADC						
Input Voltage Range	V_{IN}	Differential voltage from VS1, VS2 to PGND, and from VS3+ to VS3−	0	1	1.55	V
Sampling Frequency	f_{SAMP}			100		Hz
Voltage Sense Measurement Accuracy		From 0% to 100% of input voltage range	−10		+10	% FSR
			−155		+155	mV
		From 10% to 90% of input voltage range	−2.5		+2.5	% FSR
			−38.75		+38.75	mV
		From 900 mV to 1.1 V	−1.5		+1.5	% FSR
			−23.25		+23.25	mV
Voltage Sense Measurement Resolution				12		Bits
Voltage Differential from VS3− to PGND			−200		+200	mV
VS1 OVP Comparator Speed		Register 0x2C[2] = 0		300		µs
VS1 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS1		2.5		%
VS2 and VS3 OVP Comparator Speed		Register 0x2C[2] = 0		300		µs
VS2 and VS3 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS2 and VS3		2.5		%
VS1 HIGH SPEED ADC						
Sampling Frequency	f_{SAMP}			400		kHz
Resolution				6		Bits
Dynamic Range				±18		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE 1 (CS1 PIN)						
Input Voltage Range	V_{IN}		0	1	1.38	V
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 10% to 90% of input voltage range	−3.0		+3.0	% FSR
			−41.4		+41.4	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
			−138		+138	mV
Current Sense Measurement Resolution				12		Bits
CS1 Fast OCP Threshold			1.1	1.2	1.3	V
CS1 Fast OCP Speed				80	100	ns
CS1 Accurate OCP DC Accuracy		From 10% to 90% of input voltage range	−3.0		+3.0	% FSR
			−41.4		+41.4	mV
CS1 Accurate OCP Speed				10		ms
Leakage Current				4.0		µA
CURRENT SENSE 2 (CS2+, CS2− PINS)						
Input Voltage Range	V_{IN}	Differential voltage from CS2+ to CS2−	−100		+225	mV
ADC Input Voltage Range		LSB = 61.04 µV	0		225	mV
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 0 mV to 200 mV	−4		+4	mV
		From 200 mV to 225 mV	−15		+15	mV
			−7.5		+7.5	% FSR
Current Sense Measurement Resolution				12		Bits
CS2 Accurate OCP Accuracy		From 0 mV to 200 mV	−4		+4	mV
		From 200 mV to 225 mV	−15		+15	mV
			−7.5		+7.5	% FSR
CS2 Accurate OCP Speed				10		ms
Current Sink (High Side)				100		µA
Current Source (Low Side)				100		µA
Common-Mode Voltage at the CS2+ and CS2− Pins		To achieve CS2 measurement accuracy	0.8	1	1.3	V
GATE PIN (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
OrFET PROTECTION (CS2+, CS2−)		Low-side current sensing only				
Accurate OrFET Threshold Accuracy			−1.2	0	+1	mV
Accurate OrFET Speed				10		ms
Fast OrFET Accuracy		−25 mV setting	−40	−25	−10	mV
		−50 mV setting	−70	−50	−30	mV
		−75 mV setting	−100	−75	−50	mV
		−100 mV setting	−125	−100	−75	mV
Fast OrFET Speed		Debounce = 40 ns		110	150	ns
RTD PIN						
Input Voltage Range	V_{IN}		0	1	1.55	V
Current Source		RTD resistor = 100 kΩ	9.5	10.8	12	µA
RTD ADC Measurement Accuracy		From 2% to 20% of input voltage range	−1		+1	% FSR
		From 32 mV to 320 mV	−15.5		+15.5	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
		From 0 V to 1.55 V	−155		+155	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OTP Threshold Accuracy		When RTD = 10 kΩ	−0.5		+0.5	% FSR
			−7.75		+7.75	mV
		When RTD = 100 kΩ	−5		+5	% FSR
			−77.5		+77.5	mV
OTP Speed				10		ms
OTP Threshold Hysteresis		When RTD = 10 kΩ		16		mV
PGOOD1, PGOOD2, SHAREo PINS (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
PSON, FLAGIN, SHAREi PINS (DIGITAL INPUTS)						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS		V_{DD} = 3.3 V				
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Output Low Voltage	V_{OL}				0.4	V
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						
Clock Frequency				100	400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus-Free Time	t_{BUF}		4.7			µs
Start Setup Time	$t_{SU;STA}$		4.7			µs
Start Hold Time	$t_{HD;STA}$		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_R				1000	ns
SCL, SDA Fall Time	t_F				300	ns
Data Setup Time	$t_{SU;DAT}$		250			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
EEPROM RELIABILITY						
Endurance[1]			10,000			Cycles
Data Retention[2]		T_J = 85°C	20			Years

[1] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) VDD	4.2 V
Digital Pins	−0.3 V to V_{DD} + 0.3 V
VS3− to PGND, AGND, DGND	−0.3 V to +0.3 V
RTD, VS1 to AGND	2.5 V
VS2, VS3+, ADD to AGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.5 kV
ESD Human Body Model	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	44.4	6.4	°C/W

SOLDERING

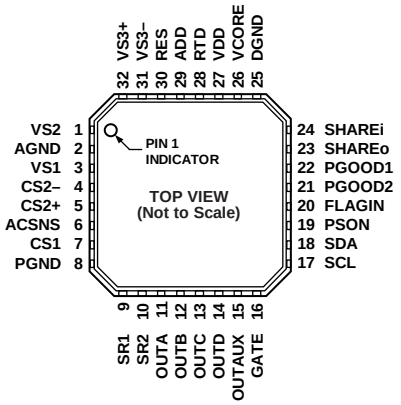
It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1043A and when soldering the part onto the PCB. The AN-772 Application Note discusses this topic in detail (see www.analog.com).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE ADP1043A HAS AN EXPOSED THERMAL PAD ON THE UNDERSIDE OF THE PACKAGE. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE PCB GROUND PLANE.

08501-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS2	Power Supply Output Sense Input. This signal is referred to PGND. Input to a low frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
2	AGND	Analog Ground. This pin is the ground for the analog circuitry of the ADP1043A. Star connect to DGND.
3	VS1	Local Voltage Sense Input. This signal is referred to PGND. Input to a high frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
4	CS2–	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sensing in a 12 V application, place a 110 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 10 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula $R = (V_{COMMONMODE} - 1)/100\ \mu A$. A 0.1% resistor must be used to connect this circuit.
5	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sensing in a 12 V application, place a 110 kΩ resistor between the sense resistor and this pin. When using low-side current sensing, place a 10 kΩ resistor between the sense resistor and this pin. When using high-side current sensing, use the formula $R = (V_{COMMONMODE} - 1)/100\ \mu A$. A 0.1% resistor must be used to connect this circuit.
6	ACSNS	AC Sense Input. This input is connected upstream of the main inductor through a resistor divider network. The nominal voltage for this circuit is 0.45 V. This signal is referred to PGND.
7	CS1	Primary Side Current Sense Input. This pin is the current transformer input to measure and control the primary side current. This signal is referred to PGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming.
8	PGND	Power Ground. This pin is the ground connection for the main power rail of the power supply. Star connect to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
15	OUTAUX	Auxiliary PWM Output. This pin can be disabled when not in use. This signal is referred to AGND.
16	GATE	OrFET Gate Drive Output (Open Drain). This signal is referred to AGND.
17	SCL	I^2C Serial Clock Input. This signal is referred to AGND.
18	SDA	I^2C Serial Data Input and Output (Open Drain). This signal is referred to AGND.

Pin No.	Mnemonic	Description
19	PSON	Power Supply On Input. This signal is referred to DGND. This is the hardware PSON control signal. It is recommended that a 1 nF capacitor be included from the PSON pin to DGND for noise debounce and decoupling.
20	FLAGIN	Flag Input. An external signal can be input at this pin to generate a flag condition.
21	PGOOD2	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD2 flag. This pin is set if any flag is set.
22	PGOOD1	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD1 flag. This pin is set if any of the following are out of range: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, or load OVP.
23	SHAREo	Share Bus Output Voltage Pin. Connect this pin to 3.3 V through a 2.2 kΩ resistor. When configured as a digital share bus, this pin is a digital output. This signal is referred to AGND.
24	SHAREi	Share Bus Feedback Pin. Connect this pin to the SHAREo pin. This signal is referred to AGND.
25	DGND	Digital Ground. This pin is the ground for the digital circuitry of the ADP1043A. Star connect to AGND.
26	VCORE	Output of 2.5 V Regulator. Connect a 100 nF capacitor from this pin to DGND.
27	VDD	Positive Supply Input. Range is from 3.1 V to 3.6 V. This signal is referred to AGND.
28	RTD	Thermistor Input. A 100 kΩ thermistor is placed from this pin to AGND. This signal is referred to AGND.
29	ADD	Address Select Input. Connect a resistor from ADD to AGND. This signal is referred to AGND.
30	RES	Resistor Input. This pin sets up the internal voltage reference for the ADP1043A. Connect a 49.9 kΩ resistor (±0.1%) from RES to AGND. This signal is referred to AGND.
31	VS3−	Inverting Remote Voltage Sense Input. There should be a low ohmic connection to AGND. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
32	VS3+	Noninverting Remote Voltage Sense Input. This signal is referred to VS3−. Use 0.1% resistors as the resistor divider to connect this circuit. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming.
Exposed Pad	EP	The ADP1043A has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the PCB ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

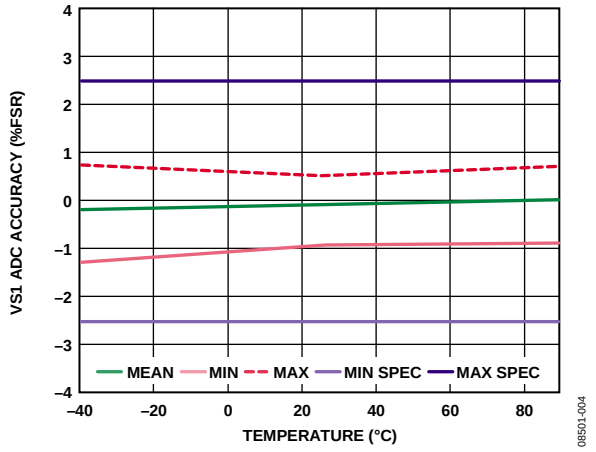


Figure 4. VS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

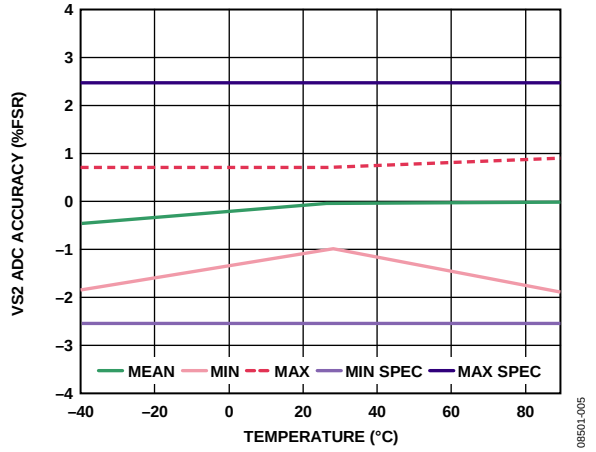


Figure 5. VS2 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

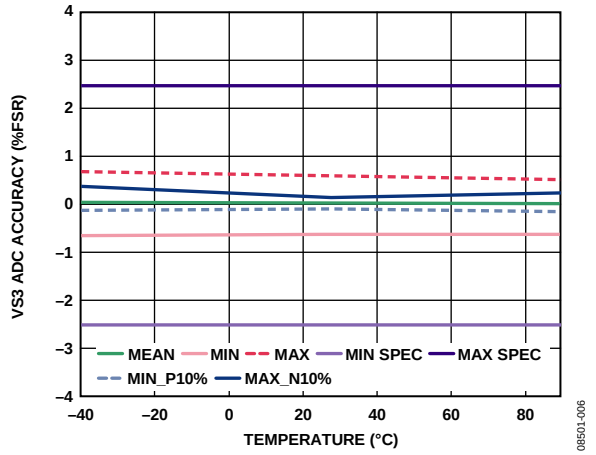


Figure 6. VS3 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

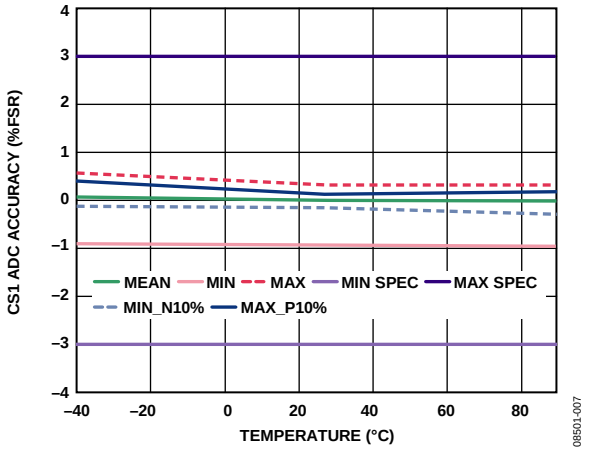


Figure 7. CS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

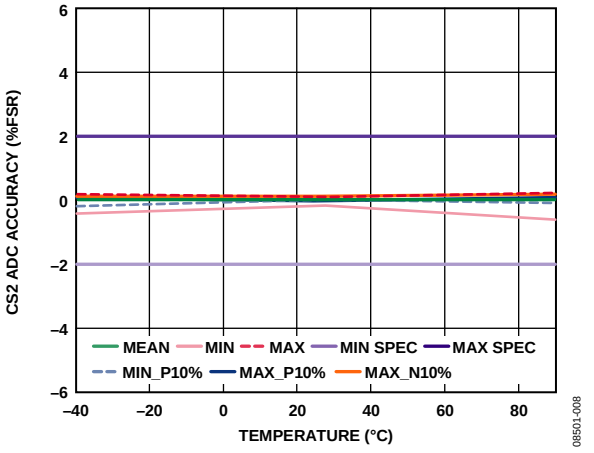


Figure 8. CS2 ADC Accuracy vs. Temperature (from 0 mV to 200 mV)

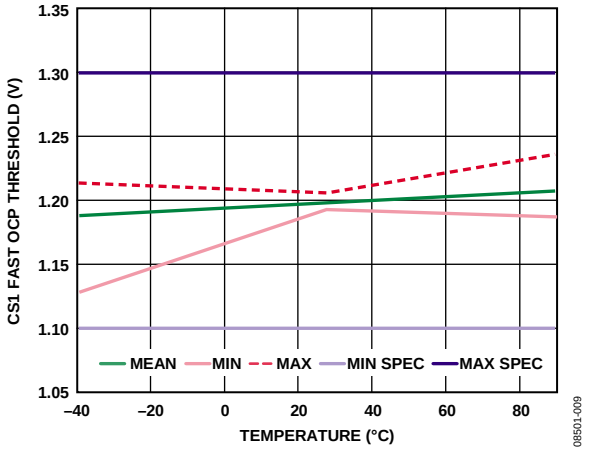


Figure 9. CS1 Fast OCP Threshold vs. Temperature

THEORY OF OPERATION

CURRENT SENSE

The ADP1043A has two individual current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the output current and the share bus information. They can be calibrated to remove any errors due to external components.

CS1 Operation (CS1)

CS1 is typically used for the monitoring and protection of the primary side current. This is commonly known as the current transformer (CT) method of current sensing. The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.38 V. The input signal is also fed into a comparator for fast OCP protection. The typical configuration for the current sense is shown in Figure 10.

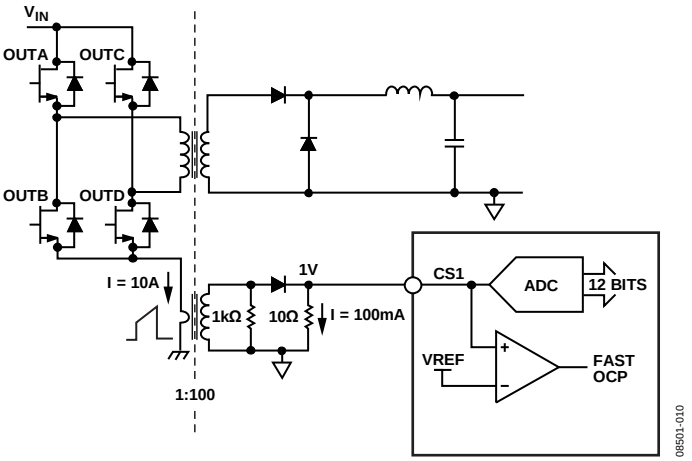


Figure 10. Current Sense 1 (CS1) Operation

The comparator effectively measures peak current, and the ADC effectively measures the average current information. This information is available through the I²C interface. Various thresholds and limits can be set for CS1, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

CS2 Operation (CS2+, CS2–)

CS2± is used for the monitoring and protection of the secondary side current. The full-scale range of the CS2 ADC is 225 mV. The nominal full load voltage drop can be configured for 37.5 mV, 75 mV, or 150 mV. The differential inputs are fed into an ADC through a pair of external resistors. When using low-side current sensing, a 10 kΩ resistor is required. When using high-side current sensing, a 110 kΩ resistor is required (for a 12 V application).

Low-side current sensing is recommended because it provides improved performance compared with high-side current sensing. High-side current sensing is not supported for applications where the output voltage is above 20 V common mode. (There is not enough offset trim range above 20 V common mode.)

Typical configurations are shown in Figure 11 and Figure 12. Various thresholds and limits can be set for CS2, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

When not in use, both CS2 inputs should be connected through 10 kΩ resistors to PGND.

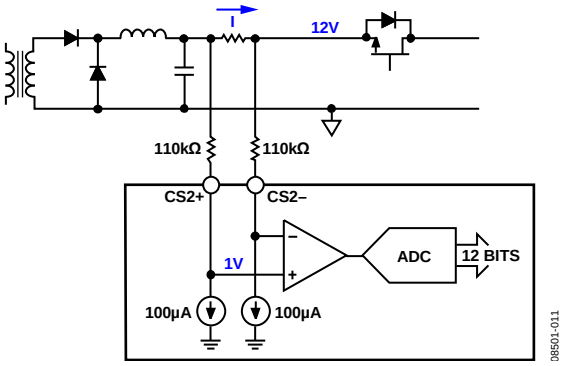


Figure 11. High-Side Resistive Current Sense

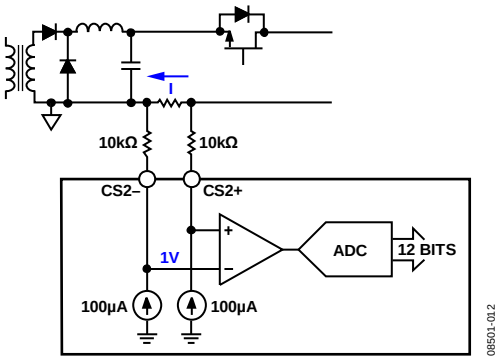


Figure 12. Low-Side Resistive Current Sense (Recommended)

VOLTAGE SENSE AND CONTROL LOOP

Multiple voltage sense inputs on the ADP1043A are used for the monitoring, control, and protection of the power supply output. The voltage information is available through the I²C interface. All voltage sense points can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1043A (see the Power Supply Calibration and Trim section for more information).

The update rate of the ADC from a control loop standpoint is set to the switching frequency. Therefore, if the switching frequency is set to 100 kHz, the ADC outputs a signal every 100 kHz to the control loop. Because the Σ-Δ modulators of the ADC sample at 1.6 MHz, the output of the ADC is the average of the 16 readings taken during the 1.6 MHz time frame.

For voltage monitoring, the VS1, VS2, and VS3 voltage value registers are updated every 10 ms. The ADP1043A stores every ADC sample for 10 ms and then outputs the average value at the end of the 10 ms period. Therefore, if these registers are read at least every 10 ms, a true average value is read. The same applies to the CS1 and CS2 current readings.

For the control loop, the high speed signal always comes from the VS1 high speed ADC. The low speed signal normally comes from the VS3 low speed ADC. However, during soft start or in response to a load OVP or other fault condition, the ADP1043A can switch its low speed regulating point from VS3 to VS1.

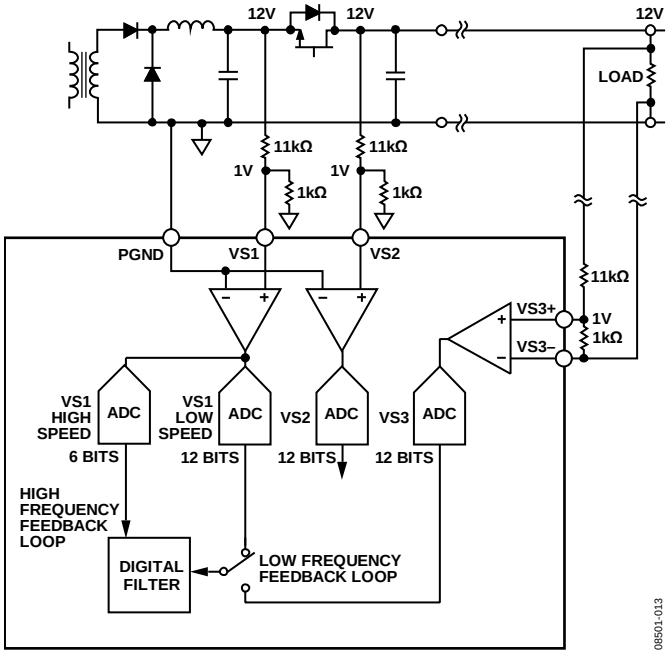


Figure 13. Voltage Sense Configuration

VS1 Operation (VS1)

VS1 is used for the monitoring and protection of the power supply voltage at the output of the LC stage, upstream of the OrFET. This is also the high frequency feedback loop for the power supply. The VS1 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS1 pin (see Figure 13). The resistor divider is necessary because the ADP1043A VS1 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into a high speed and a low speed Σ-Δ ADC. The output of the VS1 ADCs goes to the digital filter.

The high speed ADC has a 2 MHz bandwidth and is run from a 25 MHz clock. It has a range of ±18 mV. When the sampling rate is 200 kHz, there is 0.6 mV (two LSBs) of quantization noise. Increasing the sampling rate to 400 kHz increases the quantization noise to 1.2 mV.

In the event of a load overvoltage condition, the power supply is regulated from the VS1 sense point, rather than from the VS3 sense point.

VS2 Operation (VS2)

VS2 is typically used for the monitoring and protection of the output of the power supply, downstream of the OrFET. It is used with VS1 to control the OrFET gate drive turn-on. The VS2 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS2 pin (see Figure 13). The resistor divider is necessary because the ADP1043A VS2 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into an ADC. The output of the VS2 ADC goes to the VS2 voltage value register (Register 0x16).

VS3 Operation (VS3+, VS3–)

VS3± is used for the monitoring and protection of the remote load voltage. It is a fully differential input. This is the main feedback sense point for the power supply control loop. The VS3 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS3± pins (see Figure 13). The resistor divider is necessary because the ADP1043A VS3 ADC input range is 0 V to 1.55 V. This divided-down signal is internally fed into an ADC. The output of the VS3 ADC goes to the digital filter.

ADCs

The ADP1043A includes several ADCs. The high speed ADC is described in the VS1 Operation (VS1) section. The other ADCs are low speed, high resolution. They have a 1 kHz bandwidth and 12-bit resolution. Each ADC has its own voltage reference for added protection from potential failure. The digital output of each ADC is readable through the appropriate value register.

DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). It is recommended that the Analog Devices software GUI be used to program the filter. The software GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$H(z)=\left(\frac{d}{202.24\times m}\times\frac{z}{z-1}\right)+\left(\frac{c}{7.68}\times\frac{z-b}{z-a}\right) \quad (1)$$

where:
a = filter_pole_register_value/256.
b = filter_zero_register_value/256.
c = high_frequency_gain_register_value.
d = low_frequency_gain_register_value.
m = 1 when 48.8 kHz ≤ f_{SW} < 97.7 kHz.
m = 2 when 97.7 kHz ≤ f_{SW} < 195.3 kHz.
m = 4 when 195.3 kHz ≤ f_{SW} < 390.6 kHz.
m = 8 when 390.6 kHz ≤ f_{SW}.

To go from z-domain to s-domain, plug the following equation into the H(z) equation:

$$z(s)=\frac{2f_{SW}+s}{2f_{SW}-s}$$

where f_{SW} is the switching frequency.

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). Therefore, the extra phase delay for phase margin, Φ, introduced by the filter block is

$$\Phi = 180\times(f_C/f_{SW})$$

where:
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one tenth of the switching frequency, the phase delay is 18°. The GUI incorporates this phase delay into its calculations.

Two sets of registers allow for two distinct filter responses. The main filter, called the normal mode filter, is controlled by programming Register 0x60 to Register 0x63. The other filter, called the light load mode filter, is controlled by programming Register 0x64 to Register 0x67. The ADP1043A uses the light load mode filter only when the modulation is below the load current threshold (programmed through Register 0x3B).

The Analog Devices software GUI allows the user to program the light load mode filter in the same manner as the normal mode filter. It is recommended that the GUI be used for this purpose.

In addition, during the soft start process, a different set of digital filters is used. The soft start filter value for a, b, and c in Equation 1 is 0, and the d value is programmed through the soft start filter gain setting (Register 0x5F[1:0]).

PWM AND SYNC RECT OUTPUTS (OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2)

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. These outputs can be used for several control topologies, including full-bridge, phase-shifted ZVS, and interleaved two switch forward converter configurations. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoot-through and cross-conduction. It is recommended that the Analog Devices software GUI be used to program these outputs. Figure 14 shows an example configuration to drive a full-bridge, phase shift topology with synchronous rectification.

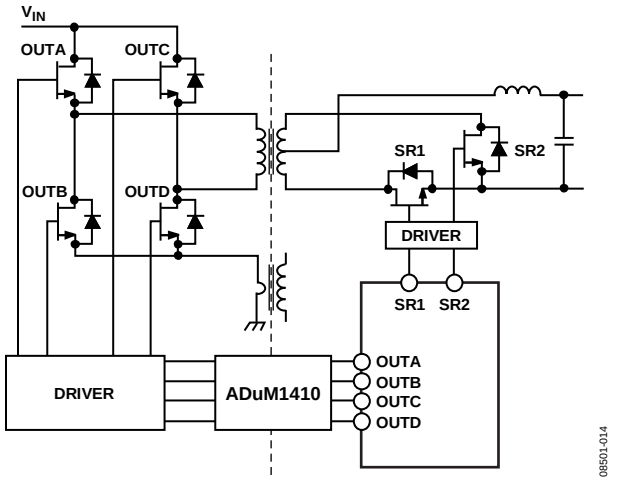


Figure 14. PWM Pin Assignment

The PWM and SR outputs all work together. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers, and then latch the information into the ADP1043A at one time. During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1043A to ensure that new timing information is programmed simultaneously. This is done by setting Register 0x5D[0] to 1. It is recommended that PWM outputs be disabled when not in use.

OUTAUX is an additional PWM output pin; OUTAUX allows an extra PWM signal to be generated at a different frequency from the other six PWM outputs. This signal can be used to drive an extra power converter stage, such as a buck controller located in front of a full-bridge converter. OUTAUX can also be used as a clock reference signal.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when using synchronous rectification. These PWM signals can be set up similarly to the other PWM outputs. The turn-on of these signals can be programmed in two ways. They can either be turned on to their full PWM value immediately, or they can be turned on in a soft start fashion. When turned on in a soft start, the signals ramp up from zero duty cycle to the desired duty cycle. The advantage of ramping the SR signals is to minimize a voltage step that would occur by turning the SR FETs on completely. The advantage of turning the SR signals completely on immediately is that they can help to minimize the voltage transient caused by a load step.

Using Register 0x54[1], the SR soft start can be programmed to occur just once, the first time that the SR signals are enabled, or every time that the SR signals are enabled.

When programming the ADP1043A to use SR soft start, ensure correct operation of this function by setting the falling edge of SR1 (t_{10}) to a lower value than the rising edge of SR1 (t_9) and by setting the falling edge of SR2 (t_{12}) to a lower value than the rising edge of SR2 (t_{11}).

The speed of the SR enable is approximately 200 µs. This ensures that in case of a load step, the SR signals (and any other PWM outputs that are temporarily disabled) can be turned on quickly enough to prevent damage to the FETs that they are controlling.

ADAPTIVE DEAD TIME CONTROL

A set of registers called the adaptive dead time (ADT) registers (Register 0x68 to Register 0x6F) allows the dead time between PWM edges to be adapted on-the-fly. The ADP1043A uses the ADT only when the modulation is below the dead time (load current) threshold (programmed in Register 0x68). The Analog Devices software GUI allows the user to easily program the dead time values, and it is recommended that the software be used for that purpose.

Each individual PWM rising and falling edge (t_1 to t_{14}) can then be programmed to have a specific dead time offset. This offset can be positive or negative. The offset is relative to the nominal edge position. For example, if t_1 has a nominal rising edge of 100 ns and the ADT setting for t_1 is −15 ns, t_1 moves to 85 ns when it falls below the adaptive dead time threshold. The dead times are programmed using Register 0x69 to Register 0x6F.

LIGHT LOAD MODE

Register 0x3B allows the ADP1043A to shut down PWM outputs under light load conditions. The light load current threshold can be programmed. Below this current threshold, the SR outputs are disabled. The user can also program any of the other PWM outputs to shut down below this current threshold. This allows the ADP1043A to be used with an interleaved two transistor forward topology, incorporating phase shedding at light load. The light load mode digital filter is also used during light load mode.

MODULATION LIMIT

Using the modulation limit register (Register 0x2E), it is possible to apply a maximum modulation limit and a minimum modulation limit to any PWM signal, thus limiting the modulation range of any PWM. These limits are a percentage of the switching period. If the modulation required is lower than the minimum setting, pulse skipping can be enabled.

Following is an example of how to use the modulation limit settings. In this example, the switching cycle period is 4 µs and modulation on the t_2 edge (falling edge) is enabled. The nominal position of t_2 is set to 1.6 µs, which is 40% of the 4 µs period. The modulation high limit is set to (nominal + 50%). Therefore, the modulation high limit is (40% + 50%) = 90% of the switching cycle period; 90% of 4 µs = 3.6 µs. The modulation low limit is set to (nominal − 35%). Therefore, the modulation low limit is (40% − 35%) = 5% of the switching cycle period; 5% of 4 µs = 0.2 µs.

The GUI provided with the ADP1043A is recommended for evaluating this feature of the ADP1043A (see Figure 15).

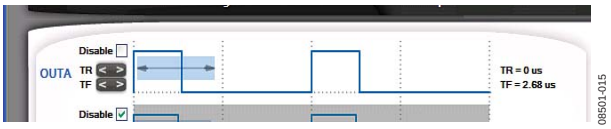


Figure 15. Setting Modulation Limits (Modulation Range Shown by Arrows)

OrFET CONTROL (GATE)

The GATE control signal drives an external OrFET. The OrFET gate control is used to protect against power flow into the power supply from another supply. This ensures that power flows only out of the power supply and that the unit can be hot-swapped. The OrFET circuit can be used only when the ADP1043A is connected to a sense resistor on the low side. The OrFET circuit is not guaranteed for operation with high-side current sensing.

The GATE pin is an open-drain, N-channel MOSFET. An external 2.2 kΩ pull-up resistor is recommended. Its output is normally high to keep the OrFET turned off. When the start-up criteria have been achieved, the GATE output is pulled low, allowing the OrFET to turn on. The OrFET turn-on and turn-off thresholds can be individually programmed. The GATE outputs are CMOS levels (0 V to 3.3 V). An external driver is required to turn the OrFET on or off.

The OrFET can be turned off by three methods:

- Fault flag (any fault flag can be programmed to turn off the OrFET)
- Fast OrFET control circuit
- Accurate OrFET control circuit

Fast OrFET control looks at the reverse voltage across CS2+ and CS2− and is implemented using an analog comparator (see Figure 16). If the voltage difference between CS2+ and CS2− is greater than the fast OrFET threshold programmed in Register 0x30, the OrFET is turned off.

Accurate OrFET control also uses the reverse voltage across the CS2+ and CS2− pins to disable the OrFET (see Figure 16). If the voltage difference between CS2+ and CS2− is greater than 0 mV, the OrFET is disabled. The accurate OrFET circuit is more accurate, but it is slower than the fast OrFET circuit.

The OrFET turn-on circuit looks at the voltage difference between VS1 and VS2 (see Figure 16). When the forward voltage drop from VS1 to VS2 is greater than the programmable OrFET enable threshold (Register 0x30[5:4]), the OrFET is enabled. The OrFET enable threshold can be set to −0.5%, 0%, 1%, or 2% of the nominal output voltage (12 V).

Recommended Setup

In a 12 V application, while in normal operating mode

- When 12 V < V_{OUT} < OVP, use the accurate OrFET control circuit to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In a 12 V application, while in light load mode

- When 12 V < V_{OUT} < OVP, use ACSNS to turn off the OrFET.
- When V_{OUT} > OVP, use load OVP to turn off the OrFET.

In a 12 V application, when an internal short circuit occurs, follow this procedure:

1. Use fast OrFET to turn off the OrFET.
2. Use CS1 OCP or VS1 UVP to shut down the unit and restart it.

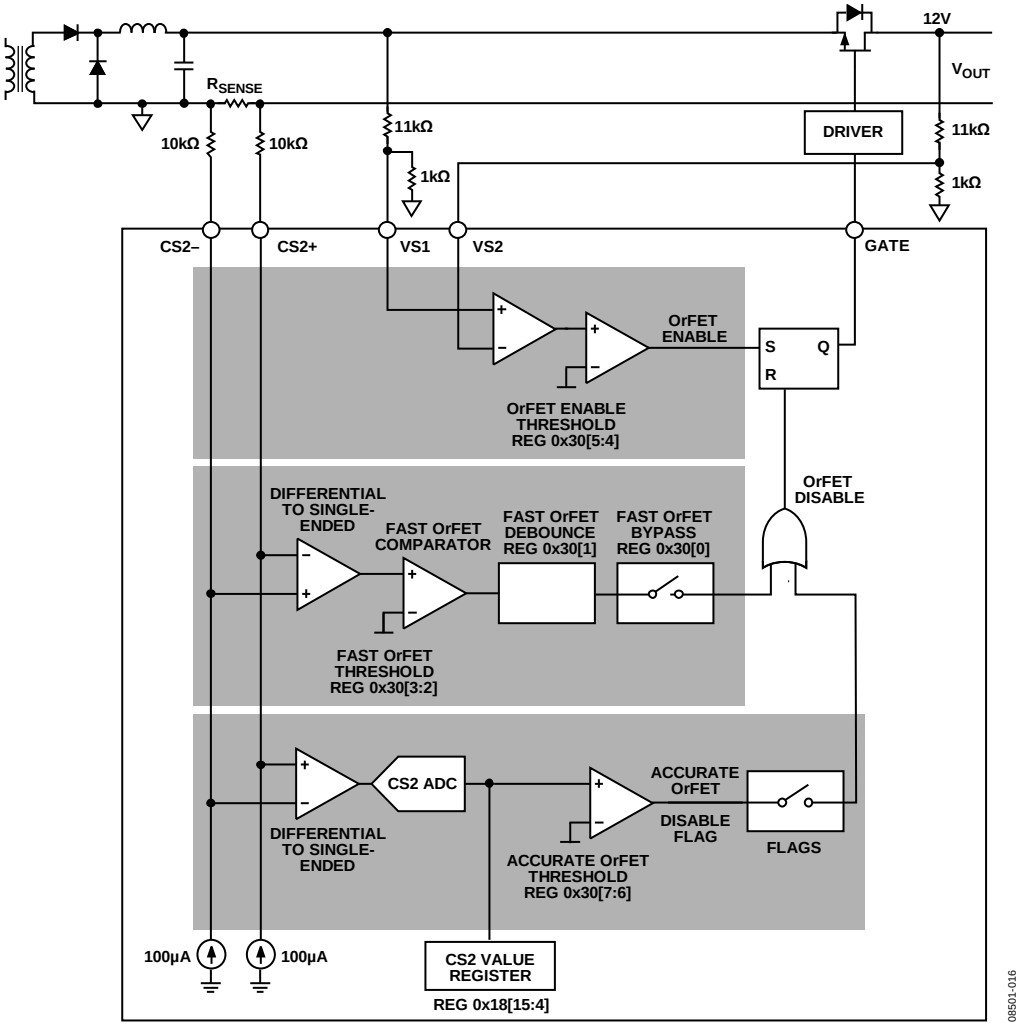


Figure 16. OrFET Control Circuit Internal Detailed Diagram

OrFET Operation Examples

Hot Plug into a Live Bus

A new PSU is plugged into a live 12 V bus (yellow). The internal voltage VS1 (red) is ramped up before the OrFET is turned on. After the OrFET is turned on (green), current in the new PSU begins to flow to the load (blue). The turn-on voltage threshold between the new PSU and the bus is programmable.

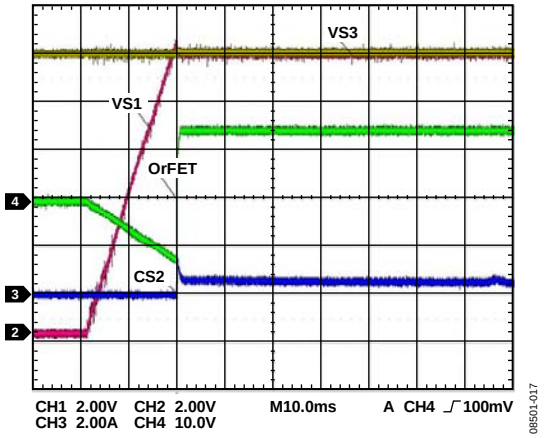


Figure 17. Hot Plug into a Live Bus (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Runaway Master

A rogue PSU on the bus (yellow) has a fault condition, and the result is that the bus voltage increases above the OVP threshold. The good PSU turns off the OrFET (green) and regulates its internal voltage VS1 (red). When the rogue power supply fault condition is removed, the bus voltage decreases. The OrFET of the good PSU is immediately turned on and the good PSU resumes regulating from VS3.

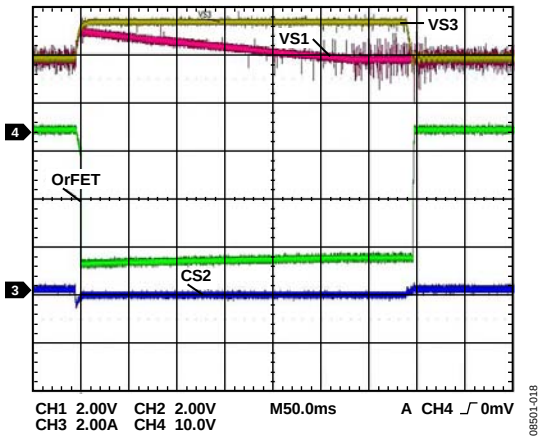


Figure 18. Runaway Master (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Short Circuit

When one of the output rectifiers fails, the bus voltage can collapse if the OrFET is not promptly turned off. The fast OrFET comparator is used to protect the system from this fault event. Figure 19 shows a short circuit applied to the output capacitors, before the OrFET. After the fast OrFET threshold for CS2 (blue) is triggered, the OrFET (green) is turned off. In this case, the gate driver is not very fast and takes about 500 ns. (A larger buffer to drive the OrFET would turn it off quicker.) Figure 19 also shows the operation when the short circuit is removed. The internal regulation point, VS1 (red), returns to 12 V, and the OrFET (green) is reenabled. The PSU again begins to contribute current to the load (blue).

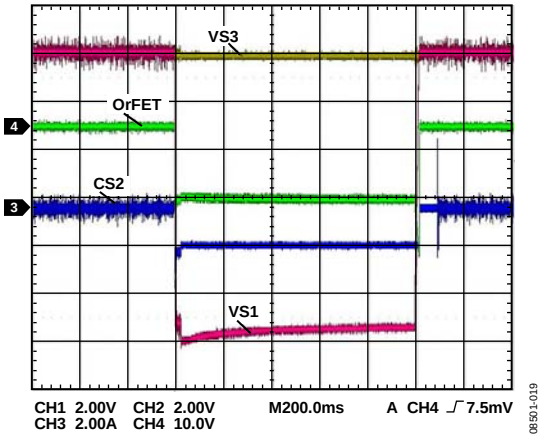


Figure 19. Internal Short Circuit (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

Light Load Mode Operation

PSU 1 increases its voltage at light load from 12 V to 12.1 V (yellow). Both PSU 1 and PSU 2 are CCM, so PSU 1 sources current and PSU 2 sinks current (blue). In PSU 2, after 10 ms the accurate OrFET control turns off the OrFET to prevent reverse current from flowing. Note that the OrFET voltage (green) is solid during this transition because PSU 1 and PSU 2 are in CCM mode.

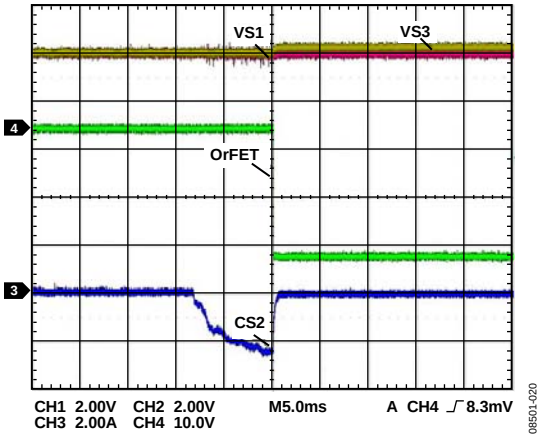


Figure 20. Light Load Mode (Yellow Is Bus Voltage; Red Is VS1 Voltage; Green Is OrFET Control Signal; Blue Is Load Current)

VDD

When VDD is applied, a certain time elapses before the part is capable of regulating the power supply. When the VDD rises above the power-on reset and UVLO levels, it takes approximately 20 µs for VCORE to reach its operational point of 2.5 V. The EEPROM contents are then downloaded to the registers. The download takes an additional 25 µs (approximately). After the EEPROM download, the ADP1043A is ready for operation. If the ADP1043A is programmed to power up at this time, the soft start ramp begins.

VDD/VCORE OVLO

The ADP1043A has built-in overvoltage protection (OVP) on its supply rails. When the VDD or VCORE voltage rises above the OVLO threshold, the response can be programmed. This circuit can be set to be ignored, but it is recommended that the user not program the OVP circuit to be ignored.

POWER GOOD

The ADP1043A has two power-good pins. The PGOOD1 pin and fault flag are set when any of the following conditions are out of range: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, or load OVP.

The PGOOD2 pin and fault flag are set when any flag is set: power supply, OrFET, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, voltage continuity, UVP, accurate OrFET disable, ACSNS, external flag (FLAGIN), VCORE OV, VDD OV, local OVP, load OVP, OTP, CRC fault, and EEPROM unlocked.

If Register 0x2D[3] is set, PGOOD2 looks only at the flags that are not programmed to be ignored.

The PGOOD2 pin can also be used as an interrupt pin to notify a host controller that a flag has been set. The polarity of the PGOOD1 and PGOOD2 pins is configured as active low.

SOFT START

A dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, and the voltage loop digital filter is used.

Fault Condition During Soft Start

If a CS1 fast OCP fault condition occurs during soft start, the entire soft start routine is reset, and the ADP1043A begins another soft start routine. All other fault flags are ignored during soft start.

Soft Start Routine

When the user turns on the power supply (enables PSON), the following soft start procedure occurs:

1. The PSON signal is enabled at Time t_0. The ADP1043A checks that initial flags are OK. These flags include VDD OK and GND OK.
2. The ADP1043A waits for Time t_1 before it begins soft start. The length of t_1 is set in Register 0x2C, Bits[4:3].
3. The soft start begins to ramp up the power supply voltage at the start of Time t_2.
4. The ADP1043A keeps the OrFET gate signal turned off. The voltage differential across the OrFET increases (VS1 − VS2) due to the diode conduction of the OrFET. When the voltage differential reaches the OrFET enable threshold (Register 0x30, Bits[5:4]), the OrFET gate signal is enabled at Time t_3. The ADP1043A begins to regulate voltage from VS3 instead of VS1.
5. After the power supply voltage increases above the VS1 UVP undervoltage limit (Register 0x34, Bits[6:0]), at the end of Time t_4, the UVP flag is reset.
6. After the UVP flag is reset and if all other PGOOD1 fault conditions are OK, the PGOOD1 signal waits for Time t_5 before it is enabled. The length of t_5 is programmable in Register 0x2D, Bits[7:4].

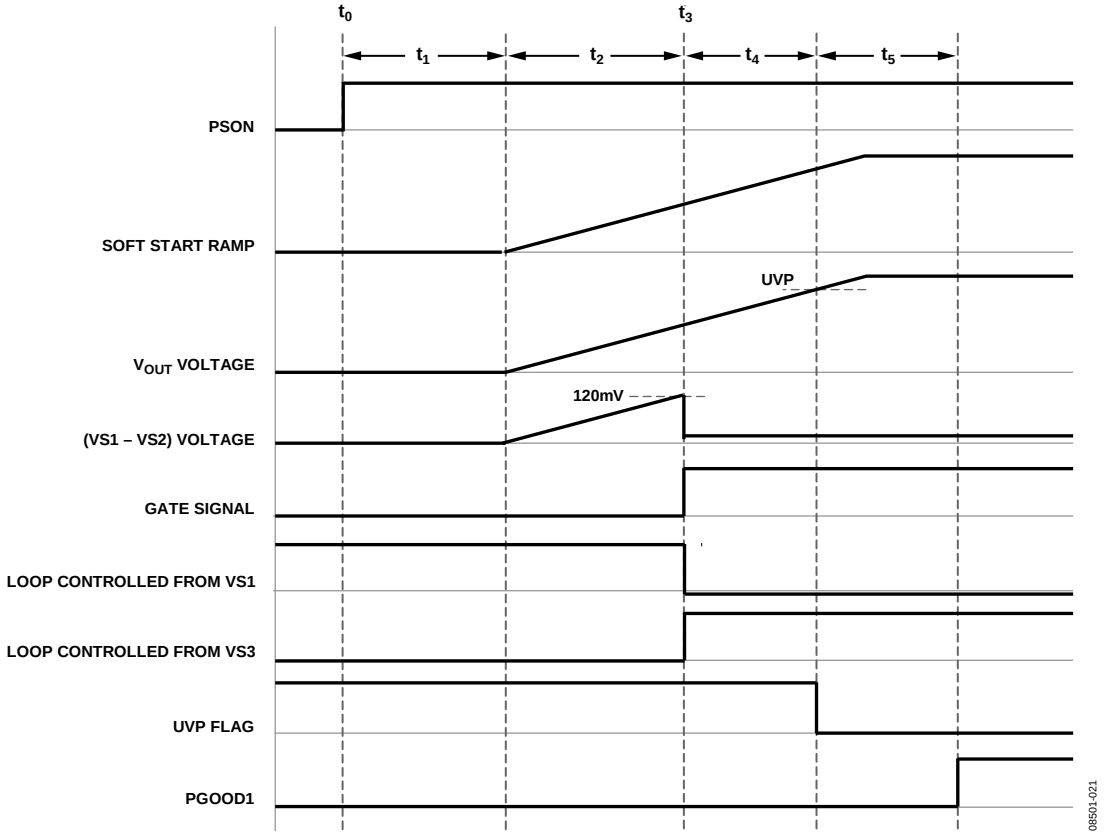


Figure 21. Soft Start Timing Diagram

CURRENT SHARING (SHARE)

The ADP1043A supports both analog current sharing and digital current sharing. It is recommended that analog current sharing be used because it offers improved performance over digital current sharing. Digital current sharing requires a load line of >15 mΩ to prevent oscillation between units. The analog current sharing scheme has no such issues.

Using Register 0x29, Bit 3, it is possible to program the ADP1043A to use the CS1 current information or the CS2 current information for current sharing.

Analog Current Sharing

The ADP1043A supports analog current sharing. The current reading from CS1 or CS2 can be output to the SHAREo pin in the form of a digital bit stream, which is the output of the current sense ADC (see Figure 23). The bit stream is proportional to the current being delivered by this unit to the load. By filtering this digital bit stream using an external RC filter, the current information is turned into an analog voltage. This means that there is now an analog voltage that is proportional to the current being delivered by this unit to the load. This voltage can be compared to the share bus. If the unit is not supplying enough current, an error signal can be applied to the VS3 feedback point. This signal causes the unit to increase its output voltage and, therefore, its current contribution to the load.

For more information about the analog current share functionality, including schematics and measurements in different fault and setup conditions, see the product page for the ADP1043A.

Digital Share Bus

The digital share bus scheme is similar in principle to the traditional analog share bus scheme. The difference is that instead of using a voltage on the share bus to represent current, a digital word is used.

The ADP1043A outputs a digital word onto the share bus. The digital word is a function of the current that the power supply is providing (the higher the current, the larger the digital word).

The power supply with the highest current controls the bus (master). A power supply that is putting out less current (slave) sees that another supply is providing more power to the load than it is. During the next cycle, the slave increases its current output contribution by increasing its output voltage. This cycle continues until the slave outputs the same current as the master, within a programmable tolerance range. Figure 22 shows the configuration of the digital share bus.

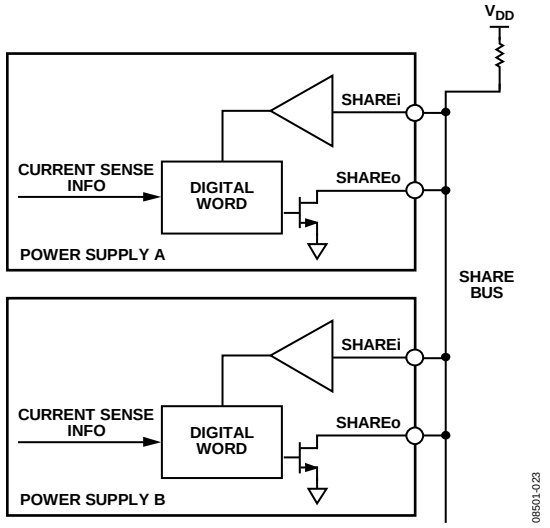


Figure 22. Digital Current Share Configuration

The digital share bus is based on a single-wire communication bus principle; that is, the clock and data signals are contained together.

When two or more ADP1043A devices are connected, they synchronize their share bus timing. This synchronization is performed by the start bit at the beginning of a communications frame. If a new ADP1043A is hot-swapped onto an existing digital share bus, it waits to begin sharing until the next frame. The new ADP1043A monitors the share bus until it sees a stop bit, which designates the end of a share frame. It then performs synchronization with the other ADP1043A devices during the next start bit. The digital share bus frame is shown in Figure 24.

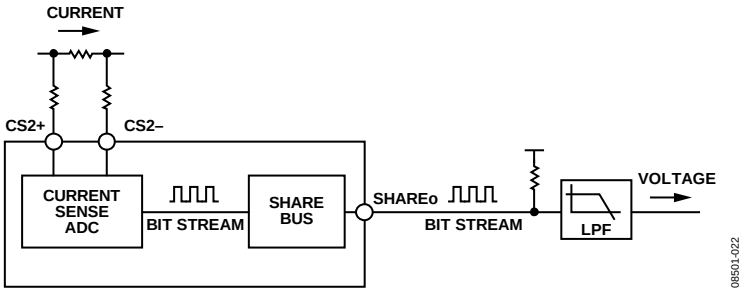


Figure 23. Analog Current Share Configuration

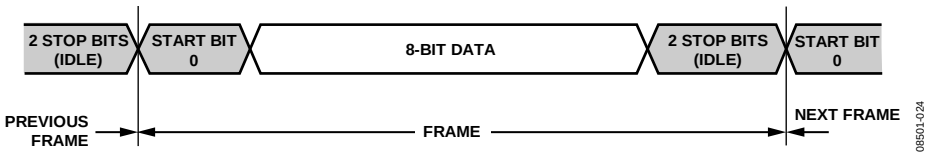


Figure 24. Digital Current Share Frame Timing Diagram

Figure 25 shows the possible signals on the share bus.

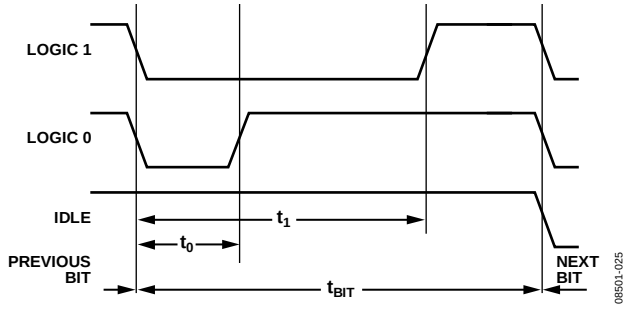


Figure 25. Share Bus High, Low, and Idle Bits

The length of a bit (t_{BIT}) is fixed at 10 µs. A Logic 1 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 75% of t_{BIT}. A Logic 0 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 25% of t_{BIT}.

The bus is idle when it is high during the whole period of t_{BIT}. All other activity on the bus is illegal. Glitches up to t_{GLITCH} (200 ns) are ignored.

The digital word that represents the current information is eight bits long. The ADP1043A takes the eight MSBs of the CS1 or CS2 reading (whichever the user chooses as the current share signal) and uses this reading as the digital word. When read, the share bus value at any given time is equal to the CS1 or CS2 current reading (see Figure 26).

Digital Share Bus Scheme

Each power supply compares the digital word that it is outputting with the digital words of all the other supplies on the bus.

Round 1

In Round 1, every supply first places its MSB on the bus. If a supply senses that its MSB is the same as the value on the bus, it continues to Round 2. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave.

When a supply becomes a slave, it stops communicating on the share bus because it knows that it is not the master. The supply then increases its output voltage in an attempt to share more current.

If two units have the same MSB, they both continue to Round 2, because either of them could be the master.

Round 2

In Round 2, all supplies that are still communicating on the bus place their second MSB on the share bus. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave and it stops communicating.

Round 3 to Round 8

The same algorithm is repeated for up to eight rounds to allow supplies to compare their digital words and, in this way, to determine whether each unit is the master or a slave.

Digital Share Bus Configuration

The digital share bus can be configured in various ways. The bandwidth of the share bus loop is programmable in Register 0x29[2:0]. The extent to which a slave tries to match the current of the master can be selected by programming Register 0x2A[3:0]. The primary side or the secondary side can be used as the current share signal by programming Register 0x29[3].

A load line may be required between PSUs when using a digital share bus. A minimum impedance of 15 mΩ is recommended between the remote voltage sense node and the load.

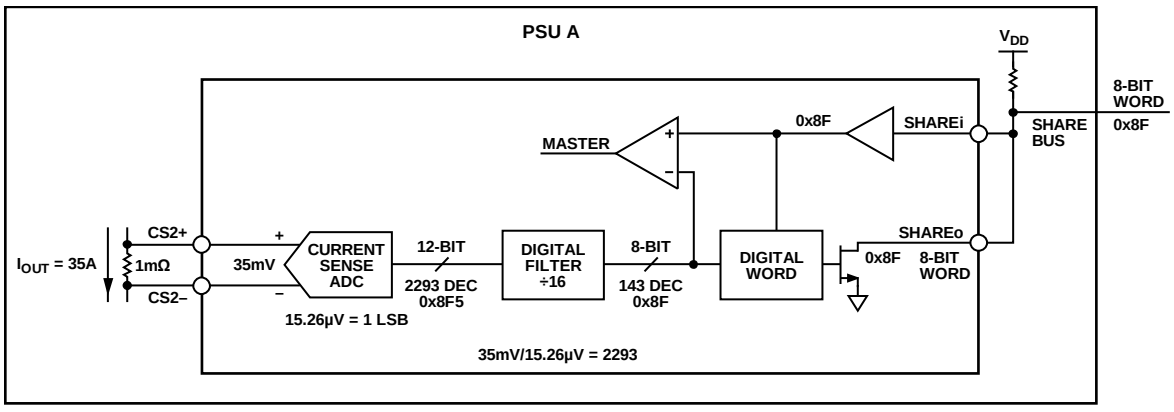


Figure 26. How the Share Bus Generates the Digital Word to Place on the Digital Share Bus

POWER SUPPLY SYSTEM AND FAULT MONITORING

The ADP1043A has extensive system and fault monitoring capabilities. The system monitoring functions include voltage, current, power, and temperature readings. The fault conditions include out-of-limit values for current, voltage, power, and temperature. The limits for the fault conditions are programmable. The ADP1043A has an extensive set of flags that are set when certain thresholds or limits are exceeded. These thresholds and limits are described in the Fault Registers section.

FLAGS

The ADP1043A has an extensive set of flags that are set when certain limits, conditions, and thresholds are exceeded. The real-time status of these flags can be read in Register 0x00 to Register 0x03. The response to these flags is individually programmable. Flags can be ignored or used to trigger tasks such as turning off certain PWM outputs or the OrFET GATE output. Flags can also be used to turn off the power supply. The ADP1043A can be programmed to respond when these flags are reset. For more information, see Register 0x08 to Register 0x0D.

The ADP1043A also has a set of latched fault registers (Register 0x04 to Register 0x07). The latched fault registers have the same flags as Register 0x00 to Register 0x03, but the flags in the latched registers remain set so that intermittent faults can be detected. Reading a latched register resets all the flags in that register.

MONITORING FUNCTIONS

The ADP1043A monitors and reports several signals, including voltages, currents, power, and temperature. All these values are stored in individual registers and can be read through the I²C interface. See the Value Registers section for more details.

VOLTAGE READINGS

The VS1, VS2, and VS3 ADCs have an input range of 1.55 V. The outputs of the ADCs are 12-bit values, which means that the LSB size is 1.55 V/4096 = 378.4 µV. The user is limited to an input range of 1.5 V, which means that the ADC output code is limited to 1.5 V/378.4 µV = 3964.

The equation to calculate the ADC code at a certain voltage (Vx) is given by the following formula:

$$ADC\ Code = Vx/378.4\ \mu V$$

For example, when there is 1 V on the input of the ADC

$$ADC\ Code = 1\ V/378.4\ \mu V$$

$$ADC\ Code = 2643$$

In a 12 V application, the 12 V reading is divided down using a resistor divider network to provide 1 V at the sense pin. Therefore, to convert the register value to a real voltage, use the following formula:

$$V_{OUT} = (VSx_Voltage_Value/2643) \times ((R1 + R2)/R2)$$

In a 12 V system, this equates to

$$V_{OUT} = (VSx_Voltage_Value/2643) \times 12\ V$$

CURRENT READINGS

CS1 Pin

DC Input Voltage

The CS1 ADC is identical in design to the VS1, VS2, and VS3 ADCs. Therefore, the description in the Voltage Readings section also applies to the CS1 ADC. When there is exactly 1 V on the CS1 pin, the value in the CS1 value register (Register 0x13) reads 2968.

CS1 has an input range of 1.38 V. The ADC performs a 12-bit reading conversion on this value, which means that the LSB size is 1.38 V/4096 = 337 µV.

The equation to calculate the ADC code at a certain CS1 input voltage (Vx) is given by the following formula:

$$ADC\ Code = Vx/337\ \mu V$$

For example, when there is 1 V on the CS1 input pin

$$ADC\ Code = 1\ V/337\ \mu V$$

$$ADC\ Code = 2968$$

AC Input Voltage

CS1 often receives a rectified ac signal through a current transformer. In this case, the ADC has a frequency response (see Figure 27).

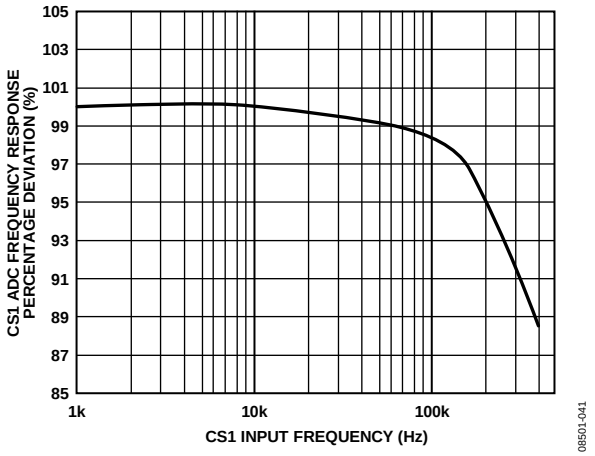


Figure 27. CS1 ADC Frequency Response

To compensate for this frequency response, the multiplication factor (M) should be used, as shown in the following equation:

$$M = (-2 \times 10^{-18} \times f_{SW}^3) + (2 \times 10^{-12} \times f_{SW}^2) + (2 \times 10^{-8} \times f_{SW}) + 0.9998$$

where f_{SW} is the switching frequency of the power supply.

Using the multiplication factor (M) results in a more accurate reading. This formula can be used by an MCU or other system monitoring device. The ADP1043A GUI has the option to use this formula.

CS2 Pin

The user sets the full-scale (FS) voltage drop—37.5 mV, 75 mV, or 150 mV—that is present across the R_{SENSE} resistor by programming Register 0x23, Bits[7:6].

The CS2 ADC has an input range of 250 mV. The resolution is 12 bits, which means that the LSB size is 250 mV/4096 = 61.04 µV. The user is limited to an input range of 215 mV.

The equation to calculate the ADC code at a certain voltage (V_X) is given by the following formula:

$$ADC\ Code = V_X/250\ mV \times 4096$$

For example, when there is 150 mV on the input of the ADC

$$ADC\ Code = 150\ mV/250\ mV \times 4096$$

$$ADC\ Code = 2457$$

Therefore, to convert the CS2 value reading to a real current, use the following formula:

$$I_{OUT} = (CS2_Value/2457) \times (FS/R_{SENSE})$$

where:
FS is the full-scale voltage drop (37.5 mV, 75 mV, or 150 mV).
R_{SENSE} is the sense resistor value.

For example, if CS2_Value = 1520, R_{SENSE} = 20 mΩ, and FS = 150 mV, the real current is calculated as follows:

$$I_{OUT} = (1520/2457) \times (150\ mV/20\ m\Omega)$$
$$I_{OUT} = 4.64\ A$$

POWER READINGS

The output power value register (Register 0x19) is the product of the VS3 voltage value and the CS2 current value. Therefore, a combination of the formulas in the Voltage Readings section and the CS2 Pin section is used to calculate the power reading in watts. This register is a 16-bit word. It multiplies two 12-bit numbers and discards the eight LSBs.

$$P_{OUT} = (V_{OUT}) \times (I_{OUT})$$

For example,

$$P_{OUT} = (12\ V) \times (4.64\ A) = 55.68\ W$$

POWER MONITORING ACCURACY

The ADP1043A power monitoring accuracy is specified relative to the full-scale range of the signal that it is measuring.

FIRST FLAG FAULT ID AND VALUE REGISTERS

When the ADP1043A registers several fault conditions, it stores the value of the first fault in a dedicated register. For example, if the overtemperature (OTP) fault is registered, followed by an OVP fault, the OTP flag is stored in the first flag ID register (Register 0x10). This register gives the user more information for fault diagnosis than a simple flag. The contents of this register are latched, meaning that they are stored until read by the user. The contents are also reset by a PSON signal.

If a flag is set to be ignored, it does not appear in the first flag register.

EXTERNAL FLAG INPUT (FLAGIN PIN)

The FLAGIN pin can be used to send an external fault signal into the ADP1043A. The reaction to this flag can be programmed in the same way as the internal flags.

TEMPERATURE READINGS (RTD PIN)

The RTD pin is set up for use with an external 100 kΩ negative temperature coefficient (NTC) thermistor. The RTD pin has an internal 10.8 µA current source. Therefore, with a 100 kΩ thermistor, the voltage on the RTD pin is 1 V at 25°C. An ADC on the ADP1043A monitors the voltage on the RTD pin.

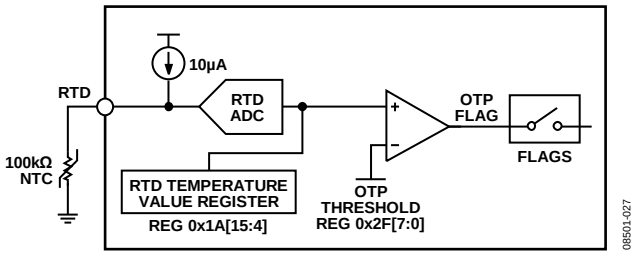


Figure 28. RTD Pin Internal Details

The output of the RTD ADC is linearly proportional to the voltage on the RTD pin. However, thermistors exhibit a nonlinear function of resistance vs. temperature. Therefore, it is necessary to perform some postprocessing on the RTD ADC reading to accurately read the temperature. This postprocessing can be in the form of a lookup table or polynomial equation to match the specific NTC being used.

OVERTEMPERATURE PROTECTION (OTP)

If the temperature sensed at the RTD pin exceeds the programmable threshold, the OTP flag is set. The hysteresis on this flag is 16 mV (see Register 0x2F in Table 43 for details). The response to the OTP flag is programmable.

The RTD trim is required to make accurate temperature readings at the lower end of the RTD ADC range. This results in a more accurate measurement for determining the OTP threshold (see the RTD/OTP Trim section).

OVERCURRENT PROTECTION (OCP)

The ADP1043A has several OCP functions. CS1 and CS2 have individual OCP circuits to provide both primary and secondary side protection.

CS1 has two protection circuits: CS1 fast OCP and CS1 accurate OCP (see Figure 29). CS1 fast OCP is an analog comparator. When the voltage at the CS1 pin exceeds the (fixed) 1.2 V threshold, the CS1 fast OCP flag is set. A blanking time can be set to ignore the current spike at the beginning of the current signal. A debounce time can be programmed to improve the noise immunity of the OCP circuit. When the CS1 fast OCP comparator is set, all PWM outputs are immediately disabled for the remainder of the switching cycle. They are reenabled at the start of the next switching cycle. This function can be bypassed if not needed.

CS1 accurate OCP is used for more precise control of overcurrent protection. With CS1 accurate OCP, the reading at the output of the CS1 ADC (Register 0x13) is compared to a programmable OCP value. The CS1 accurate OCP value can be programmed from 0 to 31 decimal using Register 0x22, Bits[4:0]. If the CS1 reading exceeds the CS1 accurate OCP value, the CS1 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

CS2 has one OCP protection circuit: CS2 accurate OCP. The reading at the output of the CS2 ADC (Register 0x18) is compared to a programmable OCP threshold. The CS2 OCP threshold can be programmed from 0 to 254 decimal using Register 0x26, Bits[7:0]. If the CS2 reading exceeds the CS2 OCP threshold, the CS2 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

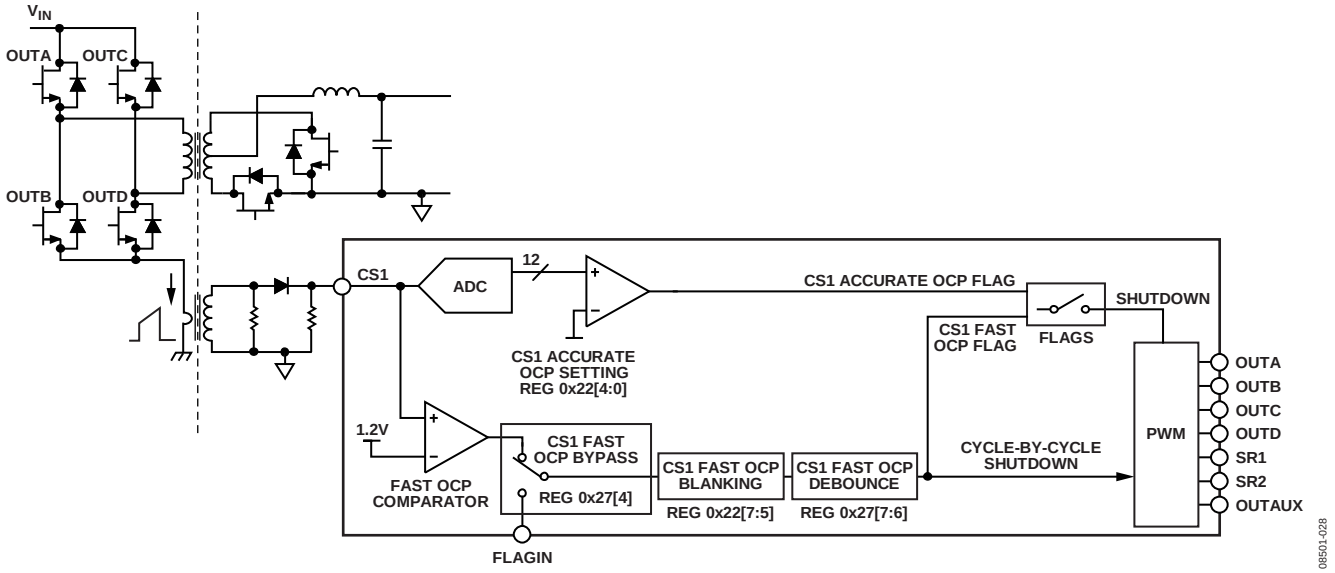


Figure 29. CS1 OCP Detailed Internal Schematic

CONSTANT CURRENT MODE

The ADP1043A can be configured to operate in constant current mode. The threshold to enter constant current mode operation is 10% current below the CS2 accurate OCP setting. Below this current, the part operates normally, using the output voltage as the feedback signal for closed-loop operation.

When the ADP1043A reaches the constant current mode threshold, a flag is set. The CS2 current reading is used instead of the output voltage as the feedback signal for closed-loop operation. The output voltage is ramped down linearly to 60% of its nominal value as the load resistance decreases to ensure that the current remains constant.

When the control loop reaches 60% of V_{OUT}, the part again uses the output voltage to close the loop, but at the reduced level (60% of nominal). If the load resistance continues to decrease, the current may rise again in this region, up to the CS2 OCP level, but the voltage is kept limited to 60% of nominal (see Figure 30). The UVP or CS2 OCP flags can be used to program a shutdown action.

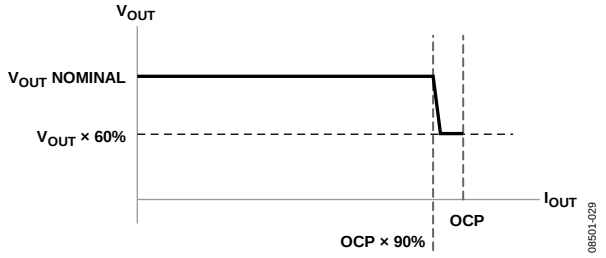


Figure 30. Constant Current Mode (V_{OUT} vs. I_{OUT})

OVERVOLTAGE PROTECTION (OVP)

The ADP1043A has two OVP circuits. If the output voltage at the VS1, VS2, or VS3 pin exceeds the programmable threshold for that pin, that OVP flag is set; the response to that flag can be programmed. VS1 has one OVP circuit. VS2 and VS3 share the other OVP circuit. The OVP circuits can be programmed for different OVP thresholds. See Register 0x32 and Register 0x33 for more information. The formula to set the OVP threshold voltage is given by

$$VSx\ OVP = [(89 + VS1_OVP_Setting)/128] \times 1.55\ V$$

For example, when the VS1 OVP setting = 10, then

$$VS1\ OVP = [(89 + 10)/128] \times 1.55\ V = 1.2\ V$$

UNDERVOLTAGE PROTECTION (UVP)

If the voltage being sensed at the VS1 pin goes below the programmable UVP threshold, the UVP flag is set. Exceptions to this rule (called undervoltage blanking) include during startup and when ACSNS is not within limits. The response to the UVP condition is programmable (see Register 0x34 in Table 48 for more information).

AC SENSE (ACSNS)

The ACSNS circuit performs multiple monitoring functions. It determines indirectly whether the primary side input voltage is present, as well as monitoring whether a switching waveform is present at the output of the synchronous rectifier stage (or rectifier diodes). The output of the synchronous rectifier stage (or rectifier diodes) is connected to this pin through an external resistor divider network.

The ACSNS circuit within the ADP1043A has a comparator that checks for a signal of 0.45 V or greater every switching cycle. For example, if the switching frequency is set to 200 kHz, the switching cycle is 5 µs. The comparator timeout is therefore set to 5 µs to match the switching cycle. If the comparator does not trip during the 5 µs interval, the ACSNS flag is set.

VOLT-SECOND BALANCE

The ADP1043A has a dedicated circuit to maintain volt-second balance in the main transformer when operating in full-bridge topology. This means that a dc blocking capacitor is not necessary.

The circuit monitors the dc current flowing in both halves of the full bridge and stores this information. It compensates the PWM drive signals to ensure equal current flow in both halves of the full bridge. The input is through the CS1 pin. Several switching cycles are required for the circuit to operate effectively. The volt-second balance places up to 80 ns of modulation on the OUTB and OUTD pins.

Note that the compensation of the PWM drive signals is performed on t_4 (OUTB) and t_8 (OUTD) only. Therefore, it is necessary to use these pins as the modulating PWM signals for the feature to operate correctly.

The SR1 and SR2 rising edges (t_9 and t_{11}) can also be independently set to modulate due to the volt-second balance circuit. The SR1 rising edge (t_9) modulates in the same direction as the OUTB falling edge (t_4); the SR2 rising edge (t_{11}) modulates in the same direction as the OUTD falling edge (t_8).

Also note that the ADP1043A assumes that the CS1 current pulse signal that it sees first in each cycle is related to OUTB, and that the second current pulse signal in each cycle is related to OUTD. If the first current pulse signal is smaller than the second, OUTB is increased and OUTD is decreased. If the first current pulse signal is greater than the second, OUTB is decreased and OUTD is increased.

LOAD LINE

The ADP1043A can optionally introduce a digital load line into the power supply. This option is programmed in the load line impedance register (Register 0x36). This feature can be used for advanced current sharing techniques. By default, the load line is disabled. The load line is introduced digitally, and its slope can be programmed. It works by taking the CS2 current reading and adjusting the output voltage accordingly. A load line of up to 51.5 mΩ can be chosen. Figure 31 shows the load line results using the ADP1043A evaluation board. The evaluation board uses a 10 mΩ R_{SENSE} resistor.

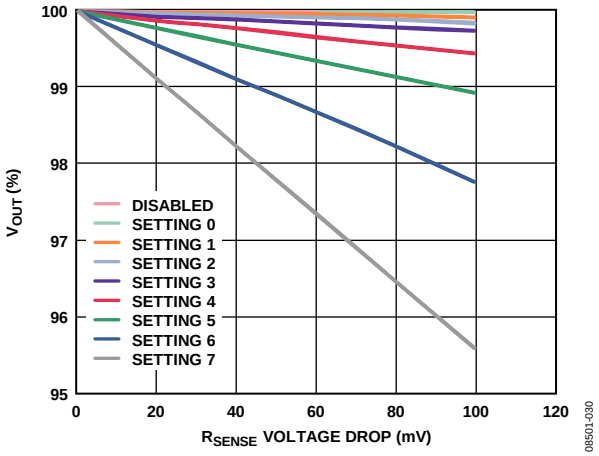


Figure 31. Load Line Settings

POWER SUPPLY CALIBRATION AND TRIM

The ADP1043A allows the entire power supply to be calibrated and trimmed digitally in the production environment. It can calibrate items such as output voltage and trim for tolerance errors introduced by sense resistors and resistor dividers, as well as its own internal circuitry. The part comes factory trimmed, but it can be retrimmed by the user to compensate for the errors introduced by external components.

The ADP1043A allows the user enough trim capability to trim for external components with a tolerance of 0.5% or better. If the ADP1043A is not trimmed in the production environment, it is recommended that components with a 0.1% tolerance be used for the inputs to CS1, CS2, VS1, VS2, VS3+, and VS3− to meet data sheet specifications.

CS1 TRIM

Using a DC Signal

A known voltage (Vx) is applied at the CS1 pin. The CS1 ADC should output a digital code equal to Vx/337 µV. The CS1 gain trim register (Register 0x21) is adjusted until the CS1 ADC value in Register 0x13 reads the correct digital code.

Using an AC Signal

A known current (Ix) is applied to the PSU input. This current passes through a current transformer, a diode rectifier, and an external resistor (R_{CS1}) to convert the current information to a voltage (Vx). This voltage is fed into the CS1 pin. The voltage (Vx) is calculated as follows:

$$Vx = Ix \times (n2/n1) \times R_{CS1}$$

where $n2/n1$ is the turns ratio of the current transformer.

The CS1 ADC should output a digital code equal to Vx/337 µV. The CS1 gain trim register (Register 0x21) is adjusted until the CS1 ADC value in Register 0x13 reads the correct digital code.

As described in the CS1 Pin section, the CS1 ADC has a frequency response. To achieve more accurate trimming, the following multiplication factor (M) should be used:

$$M = (-2 \times 10^{-18} \times f_{SW}^3) + (2 \times 10^{-12} \times f_{SW}^2) + (2 \times 10^{-8} \times f_{SW}) + 0.9998$$

where f_{SW} is the switching frequency of the power supply.

CS2 TRIM

The CS2 trim must compensate for offset and gain errors. The offset error requires both an analog trim and a digital trim. The CS2 ADC range does not begin at 0 V but instead begins at −25 mV to allow it to perform reverse current protection for the OrFET circuit. Therefore, with −25 mV at the CS2 input, the ADC code should read 0. With 0 mV at the CS2 input, the ADC code should read 100 decimal. For this reason, the analog offset trim is performed until the CS2 reading equals 100 decimal (not 0). For this reason, also, the digital trim is required.

CS2 Offset Trim

It is important to perform the CS2 offset trim as described in the following steps.

1. Set the nominal full-scale sense resistor voltage drop in Register 0x23, Bits[7:6].
2. Set high-side or low-side current sensing in Register 0x24, Bit 7.
3. Offset errors can be introduced by the external bias resistors and the internal current sources. Apply no-load current across the sense resistor. Adjust the CS2 offset trim value (Register 0x24, Bits[6:0]) until the CS2 value in Register 0x18 reads as close to 100 decimal as possible.
4. Adjust the CS2 digital trim register (Register 0x25) until the CS2 value in Register 0x18 reads 0.

The offset trim is now completed, and the ADC code reads 0 if there is no-load current across the sense resistor.

CS2 Gain Trim

After performing the offset trim, perform the gain trim to remove any mismatch that is introduced by the sense resistor tolerance. The ADP1043A can trim for sense resistors with a tolerance of 1% or better.

1. Apply a known current (I_{OUT}) across the sense resistor.
2. Adjust the CS2 gain trim value (Register 0x23, Bits[5:0]) until the CS2 value in Register 0x18 reads the value calculated by the following formula:

   $$CS2\ Value = I_{OUT} \times 2457 \times (R_{SENSE}/FS)$$

   where:
   FS is the full-scale voltage drop.
   R_{SENSE} is the sense resistor value.

   For example, if I_{OUT} = 4.64 A, R_{SENSE} = 20 mΩ, and FS = 150 mV, then

   $$CS2\ Value = (4.64\ A \times 2457) \times (20\ m\Omega/150\ mV)$$
   $$CS2\ Value = 1520 \text{ decimal}$$

The CS2 circuit is now trimmed. After the current sense trim is performed, the OCP limits and settings should be configured.

VOLTAGE CALIBRATION AND TRIM

The voltage sense inputs are optimized for sensing signals at 1 V and cannot sense a signal greater than 1.5 V. In a 12 V system, a 12:1 resistor divider is required to reduce the 12 V signal to below 1.5 V. It is recommended that the output voltage of the power supply be reduced to 1 V for best performance. The resistor divider can introduce errors, which need to be trimmed. The ADP1043A has enough trim range to trim out errors introduced by resistors with 0.5% tolerance or better. The ADCs output a digital word of 2643 decimal (0xA53) when there is exactly 1 V at their inputs.

OUTPUT VOLTAGE SETTING (VS3+, VS3− TRIM)

The VS3 input requires a gain trim. Enable the power supply with no-load current. The power supply output voltage is divided down by the VS3 resistor divider to give 1 V at the VS3+ and VS3− input pins. The VS3 trim register (Register 0x3A) is altered until the VS3 value in Register 0x17 reads 2643 decimal (0xA53). This step should be done before any other trim routines.

VS1 TRIM

The VS1 input requires a gain trim. Enable the power supply with no-load current. The VS1 voltage is divided down by the VS1 resistor divider to give 1 V at the VS1 pin. The VS1 trim register (Register 0x38) is altered until the VS1 value in Register 0x15 reads 2643 decimal (0xA53).

VS2 TRIM

The VS2 input requires a gain trim. Enable the power supply with no-load current. The VS2 voltage is divided down by the VS2 resistor divider to give 1 V at the VS2 pin. The VS2 trim register (Register 0x39) is altered until the VS2 value in Register 0x16 reads 2643 decimal (0xA53).

RTD/OTP TRIM

A 100 kΩ NTC thermistor should be used with the ADP1043A. In a PSU trim, the following procedure should be used:

1. Heat the thermistor or PSU to a known temperature that will result in an OTP threshold.
2. Adjust the temperature gain trim register (Register 0x2B) to give the correct temperature reading (Register 0x1A) at this temperature.
3. Adjust the OTP threshold register (Register 0x2F) until the OTP flag is set.

This procedure achieves the most accurate OTP, because it takes into account the part-to-part variations of the ADP1043A and the thermistor being used.

LAYOUT GUIDELINES

This section explains best practices that should be followed to ensure optimal performance of the ADP1043A. In general, all components should be placed as close to the ADP1043A as possible.

Several inputs to the ADP1043A are sensitive. Therefore, take extra care when handling and soldering the part. Along with correct cleaning of the IC after soldering, a short curing process (1 hour at 150°C) is recommended. Analog Devices also recommends encapsulating the IC in protective resin after this curing to ensure that any impurities cannot contaminate the IC.

CS2 + and CS2−

The routing of the traces from the sense resistor to the ADP1043A should be laid out in parallel to each other. The traces should also be kept close together and as far from the switch nodes as possible.

VS3+ and VS3−

The routing of the traces from the remote voltage sense point to the ADP1043A should be laid out in parallel to each other. The traces should also be kept close together and as far from the switch nodes as possible.

VDD

Place decoupling capacitors as close to the part as possible. A 100 nF capacitor from VDD to AGND is recommended.

SDA and SCL

The routing of the traces should be laid out in parallel to each other. The traces should also be kept close together and as far from the switch nodes as possible.

CS1

Run the traces from the current sense transformer to the ADP1043A in parallel to each other. The traces should also be kept close together and as far from the switch nodes as possible.

Exposed Pad

The exposed pad underneath the ADP1043A should be soldered to the PCB ground plane.

VCORE

Place the 100 nF capacitor as close to the part as possible.

RES

Place the 49.9 kΩ resistor as close to the part as possible.

RTD

Route a single trace to the ADP1043A from the thermistor. Place the thermistor close to the hottest part of the power supply.

AGND

Create an AGND ground plane and make a single point (star) connection to the power supply system ground.

COMMUNICATION

I²C INTERFACE

Control of the ADP1043A is carried out via the I²C interface. The ADP1043A is connected to the I²C bus as a slave device under the control of a master device.

I²C Address

The I²C address of the ADP1043A is set by connecting an external resistor from the ADD pin to AGND. Table 5 lists the recommended resistor values and the associated I²C addresses. Eight different addresses can be used. If an incorrect resistor value is used and the resulting I²C address is close to a threshold between two addresses, a flag is set (address flag in Register 0x03, Bit 5; see Table 11).

The recommended values in Table 5 can vary by ±2 kΩ; the ADP1043A still reports the same address. Therefore, it is recommended that 1% tolerance resistors be used on the ADD pin.

I²C Address 0x58 is the broadcast address, which allows multiple parts to be written to simultaneously. By using the broadcast address instead of a specific I²C address from Table 5, all ADP1043A devices on the I²C bus are written to. The broadcast address can be used for write commands only.

Table 5. Recommended Resistor Values for I²C Addresses

I²C Address	Resistor Value (kΩ)
0x50	9 (or connect the ADD pin directly to AGND)
0x51	27
0x52	45
0x53	63
0x54	81
0x55	98
0x56	116
0x57	134 (or connect the ADD pin directly to VDD)

General I²C Timing

The ADP1043A has a timeout feature to protect against a fault condition on the SDA line. The I²C interface monitors the SDA line and, if it stays low for time 0.65 ms < t_low < 1.3 ms, the I²C interface is reset and waits for another start condition.

The I²C specification defines specific conditions for different types of read and write operations. General I²C read and write operations are shown in the timing diagrams of Figure 32, Figure 33, and Figure 34, and are described in this section.

The general I²C protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit slave address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read).
2. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.
3. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal.
4. If the operation is a write operation, the first data byte after the slave address is a command byte that tells the slave device what to expect next. It may be an instruction, such as telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written.
5. Because data can flow in only one direction, as defined by the R/$\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before a read operation, it may be necessary to first perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.
6. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge bit. The master takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

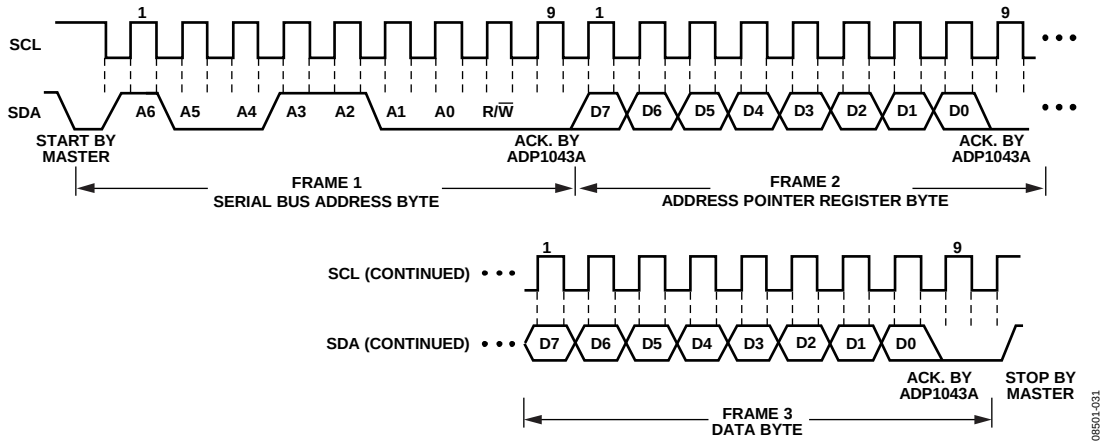


Figure 32. Writing a Register Address to the Address Pointer Register, and Then Writing Data to the Selected Register

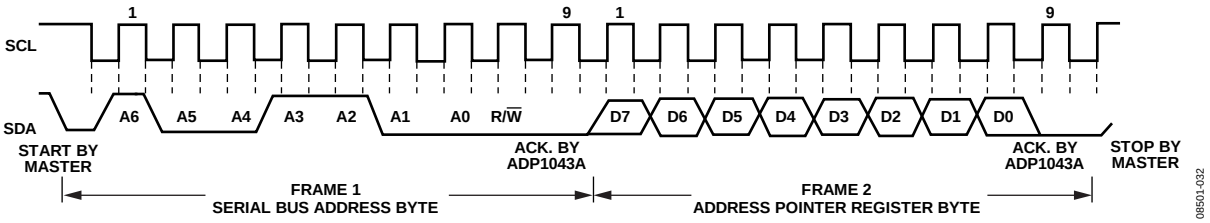


Figure 33. Writing to the Address Pointer Register Only

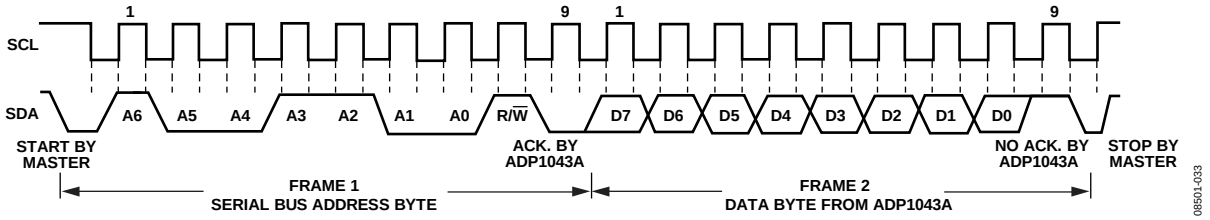


Figure 34. Reading Data from a Previously Selected Register

EEPROM

The EEPROM is partitioned into two major blocks: the factory block and the main block. The factory block contains 128 8-bit bytes, and the main block contains 8k 8-bit bytes.

Factory Block

The factory block is organized into 128 bytes. It is used to store the original Analog Devices factory calibration and register settings. The user cannot change these settings. The contents of the factory block can be downloaded to the registers at any time by writing 0x01 to Register 0x7B.

Main Block

The main block is available to store data. It is partitioned into 16 pages; each page contains 512 bytes. The data on each page is sorted into bytes organized in the form of eight rows and 64 columns (see Figure 35).

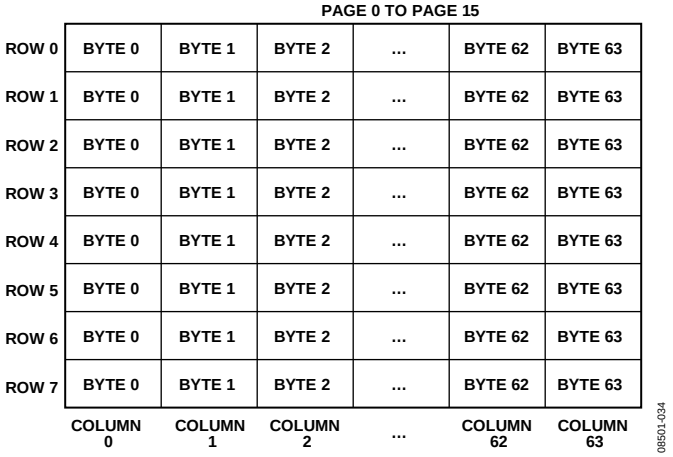


Figure 35. EEPROM Page Diagram

Main Block, Page 0 (User Settings)

The ADP1043A user register settings are stored in Page 0 of the main block. Every time that VDD is applied to the ADP1043A, the register settings are automatically downloaded from Page 0 of the EEPROM to the registers. The ADP1043A has a unique command to write new values to Page 0. This is done by writing 0x00 to Register 0x7B. Clicking the **Update EEPROM** button in the Analog Devices software GUI also performs this task.

MAIN Block, Page 1 to Page 15 (Scratchpad)

Page 1 to Page 15 of the main block can be used as a scratchpad to store other data. Register 0x7C and Register 0x7D are used to point to the page, row, and column of the byte to be accessed.

Write Example

Write data 0xAA to Page 12, Row 3, Column 30 of the ADP1043A at I²C Address 0x57.

```
Write: DevAddr=0x57 AddrPtr=0x7C Data=0x63
Write: DevAddr=0x57 AddrPtr=0x7D Data=0x1E
Write: DevAddr=0x57 AddrPtr=0x7E Data=0xAA
```

Read Example

Read data from Page 10, Row 7, Column 62 of the ADP1043A at I²C Address 0x50.

```
Read: DevAddr=0x50  AddrPtr=0x7C Data=0x57
Read: DevAddr=0x50  AddrPtr=0x7D Data=0x3E
Read: DevAddr=0x50  AddrPtr=0x7E
```

Table 6. EEPROM Registers

Address (Hex)	Register Name	Description
0x5E	Password lock	Write the password to this register twice to unlock the EEPROM or to change its password
0x7B	EEPROM restore factory default register settings	Write a command code to this register to perform one of the following EEPROM operations: 0x00: Upload registers to Page 0 of the main block (user settings) 0x01: Download factory settings (factory block) to the registers 0x02: Page erase operation
0x7C	EEPROM X address	Set XADR[6:0] of EEPROM: XADR[6:3] selects one of 16 pages of the main block XADR[2:0] selects one of eight rows per page
0x7D	EEPROM Y address	Set YADR[5:0] of EEPROM: YADR[5:0] selects one of 64 bytes in a single row
0x7E	EEPROM register	Read or write to this register to read or program a byte in EEPROM main memory

EEPROM Password Lock

The EEPROM password prevents the EEPROM contents from being changed accidentally or purposely by an unwanted source. The password ensures that critical specifications such as OVP and OCP cannot be changed.

The EEPROM is always locked. When the EEPROM downloads its contents to the registers, the password is also downloaded. If the user writes the same password to Register 0x5E twice, the EEPROM is unlocked and can be updated.

While the EEPROM is unlocked, it is possible to change the password by writing a new value to Register 0x5E. After this value is updated, the EEPROM contains the new password. The factory default password is 0x00.

To update the EEPROM password, the user must write to Register 0x7B. Writing 0x00 to this register updates the EEPROM. The user must wait at least 50 ms after this write command before attempting any further communication with the ADP1043A.

Note that the EEPROM should not be written to for the first 500 ms after VDD has been applied.

EEPROM Password Change

To change the EEPROM password, follow these steps:

1. Write the old password to Register 0x5E (password lock register).
2. Write the new password to Register 0x5E (password lock register) for the first time.
3. Write the new password to Register 0x5E (password lock register) for the second time.
4. Write the new password to Register 0x5E (password lock register) for the third time.
5. Write 0x00 to Register 0x7B.
6. Wait 50 ms.
7. To lock the EEPROM, write any value other than the password value into Register 0x5E.

Cyclic Redundancy Check (CRC)

The ADP1043A performs a check to ensure that the EEPROM contents are correctly downloaded to registers at startup. It compares the total number of 1s downloaded with the total number of 1s that were last written to the EEPROM. If there is a discrepancy, the CRC fault flag is set in Register 0x03, Bit 1. This flag is used to ensure that the correct data is downloaded from the EEPROM to the registers at startup.

SOFTWARE GUI

A free software GUI is available for programming and configuring the ADP1043A. The GUI is designed to be intuitive to power supply designers and dramatically reduces power supply design and development time. The software includes filter design and power supply PWM topology windows. The GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1043A.

For more information about the GUI, contact Analog Devices for the latest software and a user guide. Evaluation boards are also available by contacting Analog Devices.

To download the latest GUI, click on the **About** button at the top of the GUI Main screen. Click on the link to check for GUI updates.

REGISTER LISTING

Table 7. Register List

Address	Name
Fault Registers	
0x00	Fault Register 1
0x01	Fault Register 2
0x02	Fault Register 3
0x03	Fault Register 4
0x04	Latched Fault Register 1
0x05	Latched Fault Register 2
0x06	Latched Fault Register 3
0x07	Latched Fault Register 4
0x08	Fault Configuration Register 1
0x09	Fault Configuration Register 2
0x0A	Fault Configuration Register 3
0x0B	Fault Configuration Register 4
0x0C	Fault Configuration Register 5
0x0D	Fault Configuration Register 6
0x0E	Flag configuration
0x0F	Soft start blank fault flags
Value Registers	
0x10	First flag ID
0x11	Reserved
0x12	VS1/PWM value (input voltage)
0x13	CS1 value (input current)
0x14	CS1 × (VS1/PWM) value (input power)
0x15	VS1 voltage value
0x16	VS2 voltage value
0x17	VS3 voltage value (output voltage)
0x18	CS2 value (output current)
0x19	CS2 × VS3 value (output power)
0x1A	RTD temperature value
0x1D	Share bus value
0x1E	Modulation value
0x1F	Line impedance value
0x20	Reserved
Current Sense and Current Limit Registers	
0x21	CS1 gain trim
0x22	CS1 accurate OCP limit
0x23	CS2 gain trim
0x24	CS2 analog offset trim
0x25	CS2 digital trim
0x26	CS2 accurate OCP limit
0x27	CS1 fast OCP setting
0x28	Volt-second balance gain setting
0x29	Share bus bandwidth
0x2A	Share bus setting
0x2B	Temperature gain trim
0x2C	PSON/soft start setting
0x2D	Pin polarity setting
0x2E	Modulation limit
0x2F	OTP threshold
0x30	OrFET

Address	Name
Voltage Sense Registers	
0x31	VS3 voltage setting (remote voltage)
0x32	VS1 overvoltage limit (OVP)
0x33	VS2 and VS3 overvoltage limit (OVP)
0x34	VS1 undervoltage limit (UVP)
0x35	Line impedance limit
0x36	Load line impedance
0x38	VS1 trim
0x39	VS2 trim
0x3A	VS3 trim
0x3B	Light load mode disable setting
ID Registers	
0x3C	Silicon revision ID
0x3D	Manufacturer ID
0x3E	Device ID
PWM and Synchronous Rectification Timing Registers	
0x3F	OUTAUX switching frequency setting
0x40	PWM switching frequency setting
0x41	OUTA rising edge timing (OUTA pin)
0x42	OUTA rising edge setting (OUTA pin)
0x43	OUTA falling edge timing (OUTA pin)
0x44	OUTA falling edge setting (OUTA pin)
0x45	OUTB rising edge timing (OUTB pin)
0x46	OUTB rising edge setting (OUTB pin)
0x47	OUTB falling edge timing (OUTB pin)
0x48	OUTB falling edge setting (OUTB pin)
0x49	OUTC rising edge timing (OUTC pin)
0x4A	OUTC rising edge setting (OUTC pin)
0x4B	OUTC falling edge timing (OUTC pin)
0x4C	OUTC falling edge setting (OUTC pin)
0x4D	OUTD rising edge timing (OUTD pin)
0x4E	OUTD rising edge setting (OUTD pin)
0x4F	OUTD falling edge timing (OUTD pin)
0x50	OUTD falling edge setting (OUTD pin)
0x51	SR1 rising edge timing (SR1 pin)
0x52	SR1 rising edge setting (SR1 pin)
0x53	SR1 falling edge timing (SR1 pin)
0x54	SR1 falling edge setting (SR1 pin)
0x55	SR2 rising edge timing (SR2 pin)
0x56	SR2 rising edge setting (SR2 pin)
0x57	SR2 falling edge timing (SR2 pin)
0x58	SR2 falling edge setting (SR2 pin)
0x59	OUTAUX rising edge timing (OUTAUX pin)
0x5A	OUTAUX rising edge setting (OUTAUX pin)
0x5B	OUTAUX falling edge timing (OUTAUX pin)
0x5C	OUTAUX falling edge setting (OUTAUX pin)
0x5D	OUTx and SRx pin disable setting
0x5E	Password lock

Address	Name
Digital Filter Programming Registers	
0x5F	Soft start digital filter LF gain setting
0x60	Normal mode digital filter LF gain setting
0x61	Normal mode digital filter zero setting
0x62	Normal mode digital filter pole setting
0x63	Normal mode digital filter HF gain setting
0x64	Light load mode digital filter LF gain setting
0x65	Light load mode digital filter zero setting
0x66	Light load mode digital filter pole setting
0x67	Light load mode digital filter HF gain setting
Adaptive Dead Time Registers	
0x68	Dead time threshold
0x69	Dead Time 1
0x6A	Dead Time 2
0x6B	Dead Time 3
0x6C	Dead Time 4
0x6D	Dead Time 5
0x6E	Dead Time 6
0x6F	Dead Time 7
EEPROM Registers	
0x7B	EEPROM restore factory default register settings
0x7C	EEPROM X address
0x7D	EEPROM Y address
0x7E	EEPROM register

DETAILED REGISTER DESCRIPTIONS

FAULT REGISTERS

Register 0x04 to Register 0x07 are latched fault registers. In these registers, flags are not reset when the fault disappears. Flags are cleared only by a register read (provided that the fault no longer persists). Note that latched bits are clocked on a low-to-high transition only. Also note that these register bits are cleared when read via the I²C interface unless the fault is still present. It is recommended that the latched fault register be read again after the faults disappear to ensure that the register is reset.

Table 8. Register 0x00—Fault Register 1 and Register 0x04—Latched Fault Register 1 (1 = Fault, 0 = Normal Operation)

Bits	Name	R/W	Description	Register	Action
7	Power supply	R	1 = power supply is off. All PWM outputs are disabled. This bit stays high until the power supply is restarted.		None
6	OrFET	R	1 = OrFET control signal at the GATE pin (Pin 16) is off.	0x30	
5	PGOOD1 fault	R	1 = Power-Good 1 fault. At least one of the following flags has been set: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, or load OVP.		None
4	PGOOD2 fault	R	1 = Power-Good 2 fault. At least one of the following flags has been set: power supply, OrFET, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, voltage continuity, UVP, accurate OrFET disable, ACSNS, external flag (FLAGIN), VCORE OV, VDD OV, local OVP, load OVP, OTP, CRC fault, and EEPROM unlocked. (The user can choose to ignore one or more flags. See Table 41 for more information.)	0x2D	None
3	SR off	R	Sync rects are disabled. This flag is set when one of the following cases is true: SR1 and SR2 are disabled by the user. The load current has fallen below the threshold in Register 0x3B. A flag that was configured to disable the sync rects has been set.	 0x5D 0x3B 0x08 to 0x0D	None
2	CS1 fast OCP	R	CS1 current is above its fast overcurrent protection limit. This is a 1.2 V threshold on the CS1 pin. Fast OCP is a comparator.		Programmable
1	CS1 accurate OCP	R	CS1 current is above its accurate overcurrent protection limit.	0x22	Programmable
0	CS2 accurate OCP	R	CS2 current is above its accurate overcurrent protection limit.	0x26	Programmable

Table 9. Register 0x01—Fault Register 2 and Register 0x05—Latched Fault Register 2 (1 = Fault, 0 = Normal Operation)

Bits	Name	R/W	Description	Register	Action
7	Voltage continuity	R	Voltage differential between VS1 and VS2 pins or between VS2 and VS3 pins is outside limits. Either (VS1 − VS2) > 100 mV or (VS2 − VS3) > 100 mV.		Programmable
6	UVP	R	VS1 is below its undervoltage limit.	0x34	Programmable
5	Accurate OrFET disable	R	Reverse voltage across CS2 pins is above limit. This is the accurate OrFET reverse voltage.	0x30	Programmable
4	VDD UV	R	VDD is below limit.		Immediate shutdown
3	VCORE OV	R	2.5 V VCORE is above limit.		Immediate shutdown
2	VDD OV	R	VDD is above limit. The I²C interface stays functional, but a PSON toggle is required to restart the power supply.	0x0E	Programmable
1	Load OVP	R	VS2 or VS3 is above its overvoltage limit.	0x33	Programmable
0	Local OVP	R	VS1 is above its overvoltage limit.	0x32	Programmable

Table 10. Register 0x02—Fault Register 3 and Register 0x06—Latched Fault Register 3 (1 = Fault, 0 = Normal Operation)

Bits	Name	R/W	Description	Register	Action
7	OTP	R	Temperature is above OTP limit.	0x2F	Programmable
6	Reserved	R	Reserved.		
5	Share bus	R	Current share is outside regulation limit.	0x2A	Programmable
4	Constant current	R	Power supply is operating in constant current mode (constant current mode is enabled).	0x27	None
3	Reserved	R	Reserved.		
2	Line impedance	R	Line impedance between VS2 and VS3 is above limit.	0x35	None
1	Soft start filter	R	The soft start filter is in use.	0x5F	None
0	External flag	R	The external flag pin (FLAGIN) is set.		Programmable

Table 11. Register 0x03—Fault Register 4 and Register 0x07—Latched Fault Register 4 (1 = Fault, 0 = Normal Operation)

Bits	Name	R/W	Description	Register	Action
7	Reserved	R	Reserved.		
6	Modulation	R	Modulation is at its minimum or maximum limit.	0x2E	None
5	Address	R	The ADD resistor is not correct.		None
4	Light load mode	R	The system is in light load mode.	0x3B	None
3	Reserved	R	Reserved.		
2	ACSNS	R	The ac sense timing or amplitude is not correct. The ac sense comparator has not tripped for one switching cycle.		Programmable
1	CRC fault	R	The EEPROM contents downloaded are incorrect.		Immediate shutdown
0	EEPROM unlocked	R	The EEPROM is unlocked.		None

Table 12. Register 0x08 to Register 0x0D—Fault Configuration Registers

Register Name	Address	Bits	Flag	Shutdown Debounce
Fault Configuration Register 1	0x08	[7:4]	CS1 fast OCP	See Register 0x27 in Table 35
		[3:0]	CS1 accurate OCP	See Register 0x0E in Table 14
Fault Configuration Register 2	0x09	[7:4]	CS2 accurate OCP	See Register 0x0E in Table 14
		[3:0]	Load OVP (VS2 or VS3)	2 ms
Fault Configuration Register 3	0x0A	[7:4]	Local OVP (VS1)	2 ms
		[3:0]	External flag input (FLAGIN)	100 ms
Fault Configuration Register 4	0x0B	[7:4]	OTP	100 ms
		[3:0]	UVP	100 ms
Fault Configuration Register 5	0x0C	[7:4]	Accurate OrFET reverse voltage	100 ms
		[3:0]	Voltage continuity	100 ms
Fault Configuration Register 6	0x0D	[7:4]	Share bus	100 ms
		[3:0]	ACSNS	1 ms or 100 ms

Register 0x08 to Register 0x0D allow the user to program the response when each flag is set.

Table 13. Register 0x08 to Register 0x0D—Fault Configuration Register Bit Descriptions

Bits	Name	R/W	Description		
7	Timing	R/W	This bit specifies when the flag is set. 0 = after debounce. 1 = immediately.		
6	Resolve issue	R/W	This bit specifies when the part is reenabled after the fault that triggered the flag has been resolved. 0 = reenable after the power supply reenable time set in Register 0x0E[1:0]. 1 = remain disabled; power supply must be restarted to reenable.		
[5:4]	Action	R/W	These bits specify the action that the part takes in response to the flag.		
			Bit 5	**Bit 4**	**Action**
			0	0	Ignore flag completely
			0	1	Disable SR1 and SR2
			1	0	Disable OrFET
			1	1	Disable power supply (disable all PWM outputs and OrFET GATE)
3	Timing	R/W	Same as Bit 7.		
2	Resolve issue	R/W	Same as Bit 6.		
[1:0]	Action	R/W	Same as Bits[5:4].		

Table 14. Register 0x0E—Flag Configuration Register

Bits	Name	R/W	Description			
7	VDD OV/VCORE OV flags ignore	R/W	Setting this bit means that the VDD OV and VCORE OV flags are ignored.			
6	VDD OV/VCORE OV restart	R/W	Setting this bit to 1 means that if the part shuts down, it will download the EEPROM contents again before restarting. Setting this bit to 0 means that if the part shuts down, it will not download the EEPROM contents again before restarting.			
5	VDD OV/VCORE OV debounce	R/W	Setting this bit to 1 means that there is a 500 µs debounce before the part shuts down. Setting this bit to 0 means that there is a 2 µs debounce before the part shuts down.			
[4:2]	Accurate OCP off delay for CS1 and CS2	R/W	When an accurate OCP flag is set, there is a delay before the corresponding action is performed. This delay is programmed using these bits.			
			Bit 4	**Bit 3**	**Bit 2**	**Debounce**
			0	0	0	1.3 ms
			0	0	1	13 ms
			0	1	0	130 ms
			0	1	1	260 ms
			1	0	0	600 ms
			1	0	1	1.3 sec
			1	1	0	2 sec
			1	1	1	2.6 sec
[1:0]	Power supply reenable time	R/W	These bits specify the time delay before restarting the power supply after a shutdown. SR1, SR2, and OrFET are reenabled immediately.			
			Bit 1	**Bit 0**	**Time (sec)**	
			0	0	0.5	
			0	1	1	
			1	0	2	
			1	1	4	

Table 15. Register 0x0F—Soft Start Blank Fault Flags Register

Bits	Name	R/W	Description
7	Blank SR	R/W	Setting this bit means that the SR1 and SR2 PWM outputs are not enabled until the end of the soft start ramp time.
6	Blank OTP	R/W	Setting this bit means that the OTP flag is ignored until the end of the soft start ramp time.
5	Blank FLAGIN	R/W	Setting this bit means that the FLAGIN flag is ignored until the end of the soft start ramp time.
4	Blank local OVP	R/W	Setting this bit means that the local OVP flag is ignored until the end of the soft start ramp time.
3	Blank load OVP	R/W	Setting this bit means that the load OVP flag is ignored until the end of the soft start ramp time.
2	Blank CS2 accurate OCP	R/W	Setting this bit means that the CS2 accurate OCP flag is ignored until the end of the soft start ramp time.
1	Blank CS1 accurate OCP	R/W	Setting this bit means that the CS1 accurate OCP flag is ignored until the end of the soft start ramp time.
0	Blank CS1 fast OCP	R/W	Setting this bit means that the CS1 fast OCP flag is ignored until the end of the soft start ramp time.

VALUE REGISTERS

Table 16. Register 0x10—First Flag ID

Bits	Name	R/W	Description					
[7:4]	Reserved	R	Reserved.					
[3:0]	First flag ID	R	These bits record the flag that was set first. Restarting the power supply resets this register. Reading this register also resets the register.					
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Flag**	**Error**
			0	0	0	0	None	No flag
			0	0	0	1	Register 0x01, Bit 3	VCORE OV
			0	0	1	0	Register 0x01, Bit 2	VDD OV
			0	0	1	1	Register 0x03, Bit 1	EEPROM CRC
			0	1	0	0	Register 0x00, Bit 2	CS1 fast OCP
			0	1	0	1	Register 0x00, Bit 1	CS1 accurate OCP
			0	1	1	0	Register 0x00, Bit 0	CS2 accurate OCP
			0	1	1	1	Register 0x01, Bit 1	Load OVP
			1	0	0	0	Register 0x01, Bit 0	Local OVP
			1	0	0	1	Register 0x02, Bit 0	FLAGIN
			1	0	1	0	Register 0x02, Bit 7	OTP
			1	0	1	1	Register 0x01, Bit 6	UVP
			1	1	0	0	Register 0x01, Bit 5	Reverse voltage
			1	1	0	1	Register 0x01, Bit 7	Voltage continuity
			1	1	1	0	Register 0x02, Bit 5	Share bus
			1	1	1	1	Register 0x03, Bit 2	ACSNS

Table 17. Register 0x12—VS1/PWM Value (Input Voltage)

Bits	Name	R/W	Description
[15:0]	Input voltage value	R	This register contains the 16-bit input voltage information. Because the input voltage is normally on the other side of the isolation barrier from the ADP1043A, the part does not directly sense the input voltage. The input voltage is defined as the VS1 voltage divided by the PWM modulation. To read the input voltage information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the input voltage information. The eight bits of the second read return the eight LSBs of the input voltage information. To translate this reading into the real input voltage, use the following equation: $V_{INPUT} = (Input_Voltage_Value_Reading/2643) \times ((R1 + R2)/R2)$ where *R1* and *R2* are the external resistor divider values between the power supply output and the VS1 pin. This reading does not take into account an external turns ratio on the main transformer.

Table 18. Register 0x13—CS1 Value (Input Current)

Bits	Name	R/W	Description
[15:4]	Input current value	R	This register contains the 12-bit input current information. This value is derived from a voltage measurement at the CS1 input. To read the input current information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the input current information. The top four bits of the second read return the four LSBs of the input current information. The range of the CS1 input pin is from 0 V to 1.38 V. This value has 12 bits of resolution, which results in an LSB size of 337 µV. At 0 V input, the value in this register is 0 (0x000). At 1.3 V input, the value in this register is 3856 (0xF10). The nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2968 (0xB98).
[3:0]	Reserved	R	Reserved.

Table 19. Register 0x14—CS1 × (VS1/PWM) Value (Input Power)

Bits	Name	R/W	Description
[15:0]	Input power value	R	This register contains the 16-bit input power information. This value is the product of the input voltage (VS1/PWM) multiplied by the input current (CS1), that is, (VS1/PWM) × CS1. To read the input power information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the input power information. The eight bits of the second read return the eight LSBs of the input power information.

Table 20. Register 0x15—VS1 Voltage Value

Bits	Name	R/W	Description
[15:4]	VS1 voltage value	R	This register contains the 12-bit local output voltage information. This voltage is measured at the VS1 pin. To read the VS1 voltage information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the local output voltage information. The top four bits of the second read return the four LSBs of the local output voltage information. The range of the VS1 input pin is from 0 V to 1.55 V. This value has 12 bits of resolution, which results in an LSB size of 378 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3964 (0xF7C). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2643 (0xA53).
[3:0]	Reserved	R	Reserved.

Table 21. Register 0x16—VS2 Voltage Value

Bits	Name	R/W	Description
[15:4]	VS2 voltage value	R	This register contains the 12-bit load output voltage information. This voltage is measured at the VS2 pin. To read the load VS2 voltage information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the load output voltage information. The top four bits of the second read return the four LSBs of the load output voltage information. The range of the VS2 input pin is from 0 V to 1.55 V. This value has 12 bits of resolution, which results in an LSB size of 378 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3964 (0xF7C). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2643 (0xA53).
[3:0]	Reserved	R	Reserved.

Table 22. Register 0x17—VS3 Voltage Value (Output Voltage)

Bits	Name	R/W	Description
[15:4]	VS3 voltage value	R	This register contains the 12-bit remote output voltage information. This value is the differential voltage between the VS3+ and VS3− pins. To read the remote output voltage information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the remote output voltage information. The top four bits of the second read return the four LSBs of the remote output voltage information. The range of the VS3 input pin is from 0 V to 1.55 V. This value has 12 bits of resolution, which results in an LSB size of 378 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3964 (0xF7C). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2643 (0xA53).
[3:0]	Reserved	R	Reserved.

Table 23. Register 0x18—CS2 Value (Output Current)

Bits	Name	R/W	Description
[15:4]	Output current value	R	This register contains the 12-bit output current information. This information is the voltage drop across the sense resistor. The user must divide this value by the sense resistor value to obtain the current value. To read the output current information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the output current information. The top four bits of the second read return the four LSBs of the output current information. The CS2 pin has an input range of 250 mV. This value has 12 bits of resolution, which results in an LSB size of 61.04 µV. The nominal voltage setting in Bits[7:6] of Register 0x23 changes this LSB step size. If the nominal voltage range is from 75 mV to 150 mV, the LSB step size is 61.04 µV. At a 30 mV input signal on CS2, the value in this register is 30 mV/61.04 µV = 491 (0x1EB). If the nominal voltage range is from 37.5 mV to 75 mV, the LSB step size is 30.52 µV. At a 30 mV input signal on CS2, the value in this register is 30 mV/30.52 µV = 982 (0x3D6). If the nominal voltage range is from 0 mV to 37.5 mV, the LSB step size is 15.26 µV. At a 30 mV input signal on CS2, the value in this register is 30 mV/15.26 µV = 1966 (0x7AE).
[3:0]	Reserved	R	Reserved.

Table 24. Register 0x19—CS2 × VS3 Value (Output Power)

Bits	Name	R/W	Description
[15:0]	Output power value	R	This register contains the 16-bit output power information. This value is the product of the remote output voltage value (VS3) and the output current reading (CS2). To read the output power information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the output power information. The eight bits of the second read return the eight LSBs of the output power information. See the Power Readings section for the formulas needed to convert this digital reading into power information.

Table 25. Register 0x1A—RTD Temperature Value

Bits	Name	R/W	Description
[15:4]	Temperature value	R	This register contains the 12-bit output temperature information, as determined from the RTD pin. To read the temperature information, this register must be read using two consecutive read operations. The eight bits of the first read return the eight MSBs of the temperature information. The top four bits of the second read return the four LSBs of the temperature information. The range of the RTD pin is from 0 V to 1.55 V. This value has 12 bits of resolution, which results in an LSB size of 378 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3964 (0xF7C). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2643 (0xA53).
[3:0]	Reserved	R	Reserved.

Table 26. Register 0x1D—Share Bus Value

Bits	Name	R/W	Description
[7:0]	Share bus value	R	This register contains the 8-bit share bus voltage information. If the power supply is the master, this register outputs 0.

Table 27. Register 0x1E—Modulation Value

Bits	Name	R/W	Description
[7:0]	Modulation value	R	This register contains the 8-bit modulation information. It outputs the amount of modulation from 0% to 100% that is being placed on the modulating edges.

Table 28. Register 0x1F—Line Impedance Value

Bits	Name	R/W	Description
[7:0]	Line impedance value	R	This register contains the 8-bit line impedance information. This value is (VS2 – VS3)/CS2.

CURRENT SENSE AND CURRENT LIMIT REGISTERS

Table 29. Register 0x21—CS1 Gain Trim

Bits	Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS1 gain trim	R/W	This value calibrates the primary side current sense gain. See the CS1 Trim section for more information.

Table 30. Register 0x22—CS1 Accurate OCP Limit

Bits	Name	R/W	Description			
[7:5]	CS1 fast OCP blanking	R/W	These bits determine the blanking time for CS1 before fast OCP is enabled. This time is measured from the start of a switching cycle. It is synchronized with the rising edge of OUTB and OUTD. If using OUTAUX, the time is synchronized with the rising edge of OUTAUX.			
			Bit 7	**Bit 6**	**Bit 5**	**Delay (ns)**
			0	0	0	0
			0	0	1	40
			0	1	0	80
			0	1	1	120
			1	0	0	200
			1	0	1	400
			1	1	0	600
			1	1	1	800
[4:0]	CS1 accurate OCP	R/W	These bits set the CS1 accurate OCP threshold. The digital word that is output from the CS1 ADC is compared with this threshold. If the CS1 ADC reading (Register 0x13) is greater than the OCP threshold set by these bits, the CS1 accurate OCP flag is set. This value should be programmed only after the CS1 trim has been performed. The range of these bits is from 0 to 31, that is, 0 V to 1.38 V in 43.125 mV steps. The following equation gives the threshold of the CS1 OCP: *CS1_OCP_Threshold* = (*CS1_OCP_Limit*/31) × 1.38 The range is programmable from 0% to 138% of the nominal voltage on the CS1 pin. For example, if the CS1 OCP limit is 12 V, then *CS1_OCP_Threshold* = (12/31) × 1.38 V = 534 mV Setting these bits to 0 gives an OCP limit of 0% of the nominal voltage on the CS1 pin. Setting these bits to 10 gives an OCP limit of 44.5% of the nominal voltage on the CS1 pin. Setting these bits to 31 gives an OCP limit of 138% of the nominal voltage on the CS1 pin.			

Table 31. Register 0x23—CS2 Gain Trim

Bits	Name	R/W	Description			
[7:6]	CS2 nominal	R/W	These bits set the nominal full-scale voltage drop across the sense resistor. This is Step 1 in the CS2 Offset Trim section. These bits set the LSB step size of the CS2 ADC.			
			Bit 7	**Bit 6**	**Nominal Voltage Drop Across R_{SENSE} at Full Scale (mV)**	**LSB Step Size (µV)**
			0	0	37.5	15.26
			0	1	75	30.52
			1	0	150	61.04
5	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.			
[4:0]	CS2 gain trim	R/W	This register calibrates the secondary side (CS2) current sense gain. It calibrates for errors in the sense resistor. This is Step 2 in the CS2 Gain Trim section.			

Table 32. Register 0x24—CS2 Analog Offset Trim

Bits	Name	R/W	Description
7	CS2 high side	R/W	This bit is set high if high-side current sensing is used. This bit is set low if low-side current sensing is used. This is Step 2 in the CS2 Offset Trim section.
6	Offset polarity	R/W	1 = negative offset is introduced. 0 = positive offset is introduced.
[5:0]	CS2 offset trim	R/W	This register calibrates the secondary side (CS2) current sense common-mode error. It calibrates for errors in the resistor divider network. This is Step 3 in the CS2 Offset Trim section.

Table 33. Register 0x25—CS2 Digital Trim

Bits	Name	R/W	Description
[7:0]	CS2 digital trim	R/W	This register contains the CS2 digital trim level. This value is used to calibrate the CS2 value that is read in Register 0x18. This is Step 4 in the CS2 Offset Trim section.

Table 34. Register 0x26—CS2 Accurate OCP Limit

Bits	Name	R/W	Description
[7:0]	CS2 accurate OCP	R/W	This register sets the CS2 accurate OCP current level. This 8-bit number is compared to the CS2 value register (Register 0x18). When the CS2 value register is greater than the value in this register, the CS2 accurate OCP flag is set. The maximum setting of this register is 254 (0xFE). Setting this register to 255 (0xFF) is not allowed.

Table 35. Register 0x27—CS1 Fast OCP Setting

Bits	Name	R/W	Description		
[7:6]	CS1 fast OCP debounce	R/W	These bits set the CS1 fast OCP debounce value. This is the minimum time that the CS1 signal must be constantly above the fast OCP limit before the PWM outputs are shut down. When this happens, all PWM outputs are disabled for the remainder of the switching cycle.		
			Bit 7	**Bit 6**	**Debounce (ns)**
			0	0	0
			0	1	40
			1	0	80
			1	1	120
5	VS balance enable	R/W	Setting this bit enables volt-second balance for the main transformer (used for full-bridge configurations). This value introduces extra modulation on the OUTB and OUTD modulating waveforms to provide volt-second balance in both branches of the full bridge. For more information, see the Volt-Second Balance section.		
4	CS1 fast OCP bypass	R/W	Setting this bit to 1 means that the FLAGIN pin is used for CS1 fast OCP instead of the CS1 pin.		
3	Constant current mode	R/W	When this bit is set, constant current mode is enabled 10% below the CS2 accurate OCP limit. 1 = constant current mode enabled. 0 = constant current mode disabled.		
2	VS balance leading edge blanking	R/W	Setting this bit means that the current spike at the beginning of each CS1 reading is ignored by the volt-second balance circuit.		
[1:0]	CS1 fast OCP timeout	R/W	If the CS1 fast OCP comparator is set, all PWM outputs that are on during that time are immediately disabled for the remainder of the switching cycle. The PWM outputs resume normal operation at the beginning of the next switching cycle. These bits set the number of consecutive switching cycles for the comparator before the CS1 fast OCP flag is set.		
			Bit 1	**Bit 0**	**Number of Switching Cycles**
			0	0	1
			0	1	2
			1	0	4
			1	1	8

Table 36. Register 0x28—Volt-Second Balance Gain Setting

Bits	Name	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	VS balance gain setting	R/W	These bits set the gain of the volt-second balance circuit. The gain can be changed by a factor of 64. When these bits are set to 00, it takes approximately 700 ms to achieve volt-second balance. When these bits are set to 11, it takes approximately 10 ms to achieve volt-second balance.		
			Bit 1	**Bit 0**	**Volt-Second Balance Gain**
			0	0	1
			0	1	4
			1	0	16
			1	1	64

Table 37. Register 0x29—Share Bus Bandwidth

Bits	Name	R/W	Description
[7:5]	Reserved	R/W	Reserved.
4	Bit stream	R/W	1 = the current sense ADC reading is output on the SHAREo pin. This bit stream can be used for analog current sharing. 0 = the digital share bus signal is output on the SHAREo pin. This signal can be used for digital current sharing.
3	Current share select	R/W	1 = CS1 reading used for current share. 0 = CS2 reading used for current share.
[2:0]	Share bus bandwidth	R/W	These bits determine the amount of bandwidth dedicated to the share bus. The value 000 is the lowest possible bandwidth, and the value 111 is the highest possible bandwidth.

Table 38. Register 0x2A—Share Bus Setting

Bits	Name	R/W	Description
[7:4]	Number of bits dropped by master	R/W	These bits determine how much a master device reduces its output voltage to maintain current sharing.
[3:0]	Bit difference between master and slave	R/W	These bits determine how closely a slave tries to match the current of the master device. The higher the setting, the larger the distance that satisfies the current sharing criteria.

Table 39. Register 0x2B—Temperature Gain Trim

Bits	Name	R/W	Description
[7:5]	Reserved	R/W	Set these bits to 000 for normal operation.
4	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[3:0]	Gain trim	R/W	This register calibrates the RTD ADC gain. It calibrates for errors in the ADC. This value allows ±12% trim to be realized.

Table 40. Register 0x2C—PSON/Soft Start Setting

Bits	Name	R/W	Description		
[7:6]	PS_ON setting	R/W	These bits determine which signal is used by the ADP1043A as the PS_ON control.		
			Bit 7	**Bit 6**	**PS_ON Setting**
			0	0	The ADP1043A is always on.
			0	1	Hardware PSON pin is used to enable or disable the power supply.
			1	0	Software PS_ON bit (Bit 5) is used to enable or disable the power supply.
			1	1	Both software PS_ON bit and hardware PSON pin must be enabled before the ADP1043A is enabled.
5	PS_ON	R/W	Software PS_ON bit. 0 = power supply off. 1 = power supply on.		
[4:3]	PS_ON delay	R/W	These bits set the time from when the PS_ON control signal is set to when the soft start begins.		
			Bit 4	**Bit 3**	**Delay (sec)**
			0	0	0
			0	1	0.5
			1	0	1
			1	1	2
2	Soft stop enable	R/W	If the soft stop feature is enabled, a soft stop occurs even if a fault flag causes a shutdown event. This may cause the ADP1043A to continue switching for longer than desired. The user needs to consider this factor before enabling the soft stop feature. 1 = soft stop time is the same as the soft start time. 0 = no active discharge time. The ADP1043A shuts down the PWM outputs immediately.		
[1:0]	Soft start	R/W	These bits set the soft start ramp time, that is, the amount of time that it takes for the power supply to reach its nominal value.		
			Bit 1	**Bit 0**	**Ramp Time**
			0	0	360 µs
			0	1	10 ms
			1	0	20 ms
			1	1	40 ms

Table 41. Register 0x2D—Pin Polarity Setting

Bits	Name	R/W	Description				
[7:4]	PGOOD1 on/off debounce	R/W	These bits set the debounce time before the PGOOD1 pin is enabled or disabled. At startup, PGOOD1 is not enabled until a period of time after the following signals are all within normal limits: power supply, CS1 fast OCP, CS1 accurate OCP, CS2 accurate OCP, UVP, local OVP, and load OVP. When PSON is disabled, there is a debounce before PGOOD1 is disabled.				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Delay Time (ms)**
			0	0	0	0	320
			0	1	0	1	200
			1	0	1	0	600
			1	1	1	1	0
3	PGOOD2 flags	R/W	0 = any flag can set the PGOOD2 pin. 1 = any flag that has not been configured to be ignored can set the PGOOD2 pin.				
2	FLAGIN polarity	R/W	This bit sets the polarity of the FLAGIN input pin: 1 = inverted (low = on).				
1	GATE polarity	R/W	This bit sets the polarity of the OrFET GATE control pin: 1 = inverted (low = on).				
0	PSON polarity	R/W	This bit sets the polarity of the PSON input pin: 1 = inverted (low = on).				

Table 42. Register 0x2E—Modulation Limit

Bits	Name	R/W	Description				
7	Full bridge	R/W	Enable this bit when operating in full-bridge mode. This mode distributes the modulation equally between two PWM outputs instead of one. It affects the modulation high limit and the modulation low limit settings.				
[6:4]	Modulation high limit	R/W	These bits set the maximum allowed modulation that is applied to a PWM output. The value is a percentage of the switching period.				
			Bit 6	**Bit 5**	**Bit 4**	**Limit (%)**	**Limit (%) in Full-Bridge Mode**
			0	0	0	Nominal + 12.5%	Nominal + 6.25%
			0	0	1	Nominal + 25%	Nominal + 12.5%
			0	1	0	Nominal + 31.25%	Nominal + 15.625%
			0	1	1	Nominal + 37.5%	Nominal + 18.75%
			1	0	0	Nominal + 43.75%	Nominal + 21.875%
			1	0	1	Nominal + 46.88%	Nominal + 23.44%
			1	1	0	Nominal + 48.44%	Nominal + 24.22%
			1	1	1	Nominal + 50%	Nominal + 25%
3	Reserved		Reserved.				
2	Pulse skipping	R/W	Setting this bit enables pulse skipping mode. If the ADP1043A requires a duty cycle lower than the modulation low limit, pulse skipping is enabled.				
[1:0]	Modulation low limit	R/W	These bits set the minimum allowed modulation that is applied to a PWM output. The value is a percentage of the switching period. If the modulation calculated is lower than this limit, pulse skipping can be enabled.				
			Bit 1	**Bit 0**	**Limit (%)**	**Limit (%) in Full-Bridge Mode**	
			0	0	Nominal – 50%	Nominal – 25%	
			0	1	Nominal – 48.44%	Nominal – 24.22%	
			1	0	Nominal – 46.88%	Nominal – 23.44%	
			1	1	Nominal – 43.75%	Nominal – 21.875%	

Table 43. Register 0x2F—OTP Threshold

Bits	Name	R/W	Description							
[7:0]	OTP threshold	R/W	The OTP threshold value is compared to the RTD ADC reading (Register 0x1A). If the RTD ADC reading is lower than the threshold set in this register, the OTP flag is set. (The flag is set below the threshold because using an NTC thermistor causes the reading to decrease as the temperature increases.) Each LSB typically corresponds to an increased OTP threshold of 3.04 mV. The RTD ADC range is 0 V to 1.55 V; the OTP threshold is 9.12 mV to 760 mV. There is a hysteresis of 16 mV on the OTP flag.							
			Bit 7	**Bit 6**	…	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**OTP Limit (mV)**
			0	0	…	0	0	1	1	9.12
			0	0	…	0	1	0	0	12.16
			0	0	…	0	1	0	1	15.20
			…	…	…	…	…	…	…	…
			1	1	…	1	0	0	1	756.96
			1	1	…	1	0	1	0	760

Table 44. Register 0x30—OrFET

Bits	Name	R/W	Description				
[7:6]	Accurate OrFET threshold	R/W	These bits program the voltage difference between CS2+ and CS2− at which the accurate OrFET flag is set. The CS2+ and CS2− input pins are used to control this function.				
			Bit 7	**Bit 6**	**Voltage Drop Across Sense Resistor from CS2+ to CS2− (Threshold)**		
			0	0	0 mV		
			0	1	Reserved		
			1	0	Reserved		
			1	1	Reserved		
[5:4]	OrFET enable threshold	R/W	These bits program the voltage difference between VS1 and VS2 before the OrFET is enabled. The VS1 and VS2 input pins are used to control the OrFET enable function.				
						Voltage Difference from VS1 to VS2	
			Bit 5	**Bit 4**	**% of ADC Full Range**	**12 V V_{OUT} (mV)**	**48 V V_{OUT} (mV)**
			0	0	−0.5	−93	−372
			0	1	0	0	0
			1	0	1	186	744
			1	1	2	372	1488
[3:2]	Fast OrFET threshold	R/W	These bits program the threshold voltage difference between CS2+ and CS2− at which the OrFET is disabled. The CS2+ and CS2− input pins are used to control this function. The internal circuit is an analog comparator.				
			Bit 3	**Bit 2**	**Voltage Difference from CS2+ to CS2− (mV)**		
			0	0	−100		
			0	1	−75		
			1	0	−50		
			1	1	−25		
1	Fast OrFET debounce	R/W	These bits determine the debounce on the fast OrFET control before it disables the OrFET. 0 = 40 ns. 1 = 200 ns.				
0	Fast OrFET bypass	R/W	Set this bit to completely bypass the fast OrFET control. To also bypass the accurate OrFET disable control, the response to the accurate OrFET disable flag should be set to ignore.				

VOLTAGE SENSE REGISTERS

Table 45. Register 0x31—VS3 Voltage Setting (Remote Voltage)

Bits	Name	R/W	Description
[7:0]	VS3 voltage setting	R/W	This register is used to set the output voltage (voltage differential at the VS3+ and VS3− pins). Programmable from 0% to 155% of nominal voltage. Each LSB corresponds to a 0.6% increase. Setting this register to a value of 0xA5 gives an output voltage setting of 100% of the nominal voltage. This is the default value and is stored in this register when shipped from the factory. Updating the VS3 voltage setting is a two-stage process. First, the user must change the value in this register; this information is stored in a shadow register. To latch the new VS3 voltage setting into the state machine, the user must set the GO bit (Register 0x5D[0]).

Table 46. Register 0x32—VS1 Overvoltage Limit (OVP)

Bits	Name	R/W	Description
[7:3]	VS1 OVP setting	R/W	Local overvoltage limit. This limit is programmable from 107.7% to 145.3% of the nominal VS1 voltage; 0x00 corresponds to 107.7%. Each LSB results in an increase of 1.21%. The VS1 OVP threshold is calculated as follows: *VS1_OVP_Threshold* = [(89 + *VS1_OVP_Setting*)/128] × 1.55 V For example, if the VS1 OVP setting is 10, then *VS1_OVP_Threshold* = [(89 + 10)/128] × 1.55 V = 1.2 V Setting these bits to 0 gives an OVP limit of 107.7% of the nominal VS1 voltage. Setting these bits to 10 gives an OVP limit of 120% of the nominal VS1 voltage. Setting these bits to 20 gives an OVP limit of 132% of the nominal VS1 voltage. Setting these bits to 31 gives an OVP limit of 145.3% of the nominal VS1 voltage.
2	Reserved	R/W	Reserved.

Bits	Name	R/W	Description		
[1:0]	OVP sampling	R/W	The OVP flag is set if the average voltage during the OVP sampling period is greater than the OVP threshold. This OVP flag sampling period is 80 µs. The number of samples can be increased using these bits. If the number of samples is increased, the average voltage must be greater than the OVP threshold for each of those cycles. For example, if this value is set to two cycles, the average voltage must be greater than the OVP threshold for both cycles.		
			Bit 1	**Bit 0**	**Additional Sampling (µs)**
			0	0	0 (one sample sets the OVP flag)
			0	1	80 (two samples set the OVP flag)
			1	0	160 (three samples set the OVP flag)
			1	1	240 (four samples set the OVP flag)

Table 47. Register 0x33—VS2 and VS3 Overvoltage Limit (OVP)

Bits	Name	R/W	Description		
[7:3]	VS2 and VS3 OVP setting	R/W	Load overvoltage limit. This limit is programmable from 107.7% to 145.3% of the nominal VS2 or VS3 voltage; 0x00 corresponds to 107.7%. Each LSB results in an increase of 1.21%. The VS2/VS3 OVP threshold is calculated as follows: *VSx_OVP_Threshold* = [(89 + *VSx_OVP_Setting*)/128] × 1.55 V For example, if the VS3 OVP setting is 10, then *VS3_OVP_Threshold* = [(89 + 10)/128] × 1.55 V = 1.2 V Setting these bits to 0 gives an OVP limit of 107.7% of the nominal VS2/VS3 voltage. Setting these bits to 10 gives an OVP limit of 120% of the nominal VS2/VS3 voltage. Setting these bits to 20 gives an OVP limit of 132% of the nominal VS2/VS3 voltage. Setting these bits to 31 gives an OVP limit of 145.3% of the nominal VS2/VS3 voltage.		
2	Regulating point	R/W	When this bit is set, the ADP1043A regulates from the VS3 node at all times. When this bit is not set, the ADP1043A uses the VS1 voltage as the regulating point during soft start and when the OrFET is disabled.		
[1:0]	OVP sampling	R/W	The OVP flag is set if the average voltage during the OVP sampling period is greater than the OVP threshold. This OVP flag sampling period is 80 µs. The number of samples can be increased using these bits. If the number of samples is increased, the average voltage must be greater than the OVP threshold for each of those cycles. For example, if this value is set to two cycles, the average voltage must be greater than the OVP threshold for both cycles.		
			Bit 1	**Bit 0**	**Additional Sampling (µs)**
			0	0	0 (one sample sets the OVP flag)
			0	1	80 (two samples set the OVP flag)
			1	0	160 (three samples set the OVP flag)
			1	1	240 (four samples set the OVP flag)

Table 48. Register 0x34—VS1 Undervoltage Limit (UVP)

Bits	Name	R/W	Description
7	End of cycle shutdown	R/W	This bit is valid only when the OUTAUX pin is used for regulation. When any flag shuts down the power supply, the OUTAUX PWM is immediately shut down. This bit specifies when the other PWM outputs are shut down. 1: All other PWM outputs are shut down at the end of the switching cycle. 0: All other PWM outputs are immediately shut down.
[6:0]	VS1 UVP setting	R/W	These bits set the UVP limit to one of 128 settings. The UVP limit can be programmed from 0% to 155% of the nominal VS1 voltage. Each LSB increases the voltage by 155%/128 = 1.21%. In reality, there are 82 usable settings, which program the UVP threshold from 0% to 100% of the nominal VS1 voltage. The VS1 UVP threshold is calculated as follows: *VS1_UVP_Threshold* = [(*VS1_UVP_Setting*)/128] × 1.55 V For example, if the VS1 UVP setting is 60, then *VS1_UVP_Threshold* = [60/128] × 1.55 V = 726 mV Setting these bits to 0 gives a UVP limit of 0% of the nominal VS1 voltage. Setting these bits to 66 (0x42) gives a UVP limit of 80% of the nominal VS1 voltage. Setting these bits to 82 (0x52) gives a UVP limit of 100% of the nominal VS1 voltage. Setting these bits to 127 (0x7F) gives a UVP limit of 155% of the nominal VS1 voltage.

Table 49. Register 0x35—Line Impedance Limit

Bits	Name	R/W	Description
[7:0]	Line impedance limit	R/W	This value sets the threshold at which the line impedance flag is enabled. This 8-bit value is compared with the line impedance value (Register 0x1F). If the line impedance value exceeds this value, the line impedance flag is set (Register 0x02, Bit 2).

Table 50. Register 0x36—Load Line Impedance

Bits	Name	R/W	Description				
[7:4]	Reserved	R/W	Reserved.				
3	Enable	R/W	Set this bit to enable the load line.				
[2:0]	Load line	R/W	This value specifies how much the output voltage decreases from nominal at full load.				
			Bit 2	**Bit 1**	**Bit 0**	**Impedance Setting**	**Equivalent Load Line (mΩ)**
			0	0	0	Setting 7	51.5
			0	0	1	Setting 6	26
			0	1	0	Setting 5	12.5
			0	1	1	Setting 4	6.25
			1	0	0	Setting 3	3
			1	0	1	Setting 2	1.5
			1	1	0	Setting 1	0.7
			1	1	1	Setting 0	0

Table 51. Register 0x38—VS1 Trim

Bits	Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VS1 trim	R/W	These bits set the amount of gain trim that is applied to the VS1 ADC reading. This register trims the voltage at the VS1 pin for external resistor tolerances. When there is 1 V on the VS1 pin, this register is trimmed until the VS1 voltage value register (Register 0x15) reads 2643 (0xA53).

Table 52. Register 0x39—VS2 Trim

Bits	Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VS2 trim	R/W	These bits set the amount of gain trim that is applied to the VS2 ADC reading. This register trims the voltage at the VS2 pin for external resistor tolerances. When there is 1 V on the VS2 pin, this register is trimmed until the VS2 voltage value register (Register 0x16) reads 2643 (0xA53).

Table 53. Register 0x3A—VS3 Trim

Bits	Name	R/W	Description
7	Trim polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VS3 trim	R/W	These bits set the amount of gain trim that is applied to the VS3 ADC reading. This register trims the voltage at the VS3 pins for external resistor tolerances. When there is 1 V on each VS3 pin, this register is trimmed until the VS3 voltage value register (Register 0x17) reads 2643 (0xA53). The VS3 trim must be performed before the load OVP and load UVP trims are performed.

Table 54. Register 0x3B—Light Load Mode Disable Setting

Bits	Name	R/W	Description
7	Disable OUTAUX	R/W	Setting this bit means that OUTAUX is also disabled if the load current drops below the light load SR disable threshold.
6	Disable OUTD	R/W	Setting this bit means that OUTD is also disabled if the load current drops below the light load SR disable threshold.
5	Disable OUTC	R/W	Setting this bit means that OUTC is also disabled if the load current drops below the light load SR disable threshold.
4	Disable OUTB	R/W	Setting this bit means that OUTB is also disabled if the load current drops below the light load SR disable threshold.
3	Disable OUTA	R/W	Setting this bit means that OUTA is also disabled if the load current drops below the light load SR disable threshold.
[2:0]	Light load SR disable	R/W	These bits set the load current limit on the CS2 ADC below which the synchronous rectifier outputs (SR1 and SR2) are disabled. This value also determines the point at which the power supply goes into light load mode. Below this limit, the light load mode filter registers are used. Above this limit, the normal mode filter registers are used. This value is programmable from 0 mV to 46 mV of the CS2 ADC. The hysteresis on this signal is 8 mV. The settings for Bits[2:0] are shown in terms of the voltage across the CS2 pins, as well as the percentage of load current for the different nominal CS2 settings.

				Threshold for Each Nominal CS2 Setting (mV)		
Bit 2	Bit 1	Bit 0	% of Full Load	37.5 mV Setting	75 mV Setting	150 mV Setting
0	0	0	0	0	0	0
0	0	1	4	1.5	3	6
0	1	0	8.5	3.1	6.3	12.5
0	1	1	13	4.9	9.8	19.5
1	0	0	18	6.6	13.3	26.5
1	0	1	22	8.3	16.5	33
1	1	0	26	9.8	19.5	39
1	1	1	30	11.5	23	46

ID REGISTERS

Table 55. Register 0x3C—Silicon Revision ID

Bits	Name	R/W	Description
[7:0]	Silicon revision	R	This register contains the manufacturer's silicon revision code for the device. This value is used by the manufacturer for test purposes and should not be read from in normal operation.

Table 56. Register 0x3D—Manufacturer ID (Power-On Default: 0x41)

Bits	Name	R/W	Description
[7:0]	Manufacturer ID code	R	This register contains the manufacturer's ID code for the device. It is used by the manufacturer for test purposes and should not be read from in normal operation. This value is hardwired to 0x41 to represent the Analog Devices ID code.

Table 57. Register 0x3E—Device ID (Power-On Default: 0x43)

Bits	Name	R/W	Description
[7:0]	Device ID code	R	This register contains the ID code for the device. This value is hardwired to 0x43 to represent the ADP1043A.

PWM AND SYNCHRONOUS RECTIFIER TIMING REGISTERS

Figure 36 and Table 58 to Table 88 describe the implementation and programming of the seven PWM signals that are output from the ADP1043A. In general, it is recommended that t_1 be set to 0 and that t_1 be set as the reference point for the other signals.

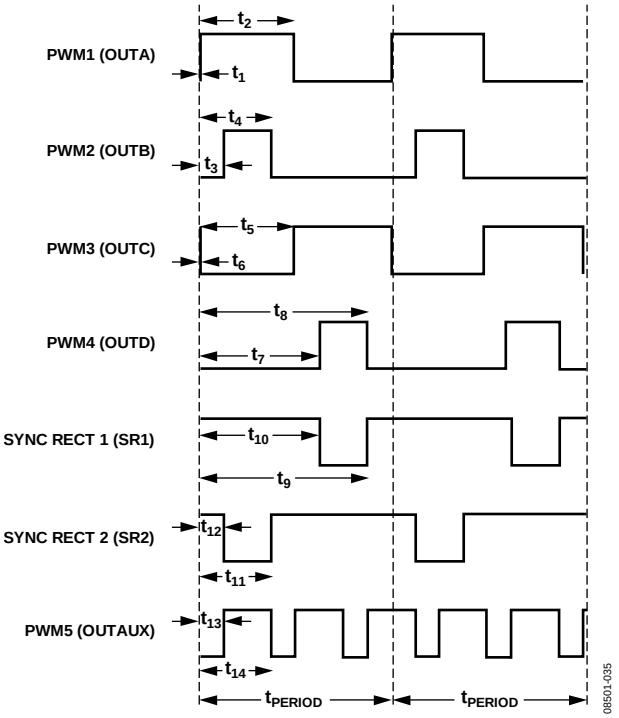


Figure 36. PWM Timing Diagram

Table 58. Register 0x3F—OUTAUX Switching Frequency Setting

Bits	Name	R/W	Description						
[7:6]	Reserved	R/W	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency of the OUTAUX signal.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	48.8
			0	0	0	0	0	1	50.4
			0	0	0	0	1	0	52.0
			0	0	0	0	1	1	53.8
			0	0	0	1	0	0	55.8
			0	0	0	1	0	1	57.9
			0	0	0	1	1	0	60.1
			0	0	0	1	1	1	62.5
			0	0	1	0	0	0	65.1
			0	0	1	0	0	1	67.9
			0	0	1	0	1	0	71.0
			0	0	1	0	1	1	74.4
			0	0	1	1	0	0	78.1
			0	0	1	1	0	1	82.2
			0	0	1	1	1	0	86.8
			0	0	1	1	1	1	91.9
			0	1	0	0	0	0	97.6
			0	1	0	0	0	1	100.8
			0	1	0	0	1	0	104.1
			0	1	0	0	1	1	107.7
			0	1	0	1	0	0	111.6

Bits	Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	1	0	1	0	1	115.7
			0	1	0	1	1	0	120.2
			0	1	0	1	1	1	125.0
			0	1	1	0	0	0	130.2
			0	1	1	0	0	1	135.8
			0	1	1	0	1	0	142.0
			0	1	1	0	1	1	148.8
			0	1	1	1	0	0	156.2
			0	1	1	1	0	1	164.5
			0	1	1	1	1	0	173.6
			0	1	1	1	1	1	183.8
			1	0	0	0	0	0	195.3
			1	0	0	0	0	1	201.6
			1	0	0	0	1	0	208.3
			1	0	0	0	1	1	215.5
			1	0	0	1	0	0	223.2
			1	0	0	1	0	1	231.5
			1	0	0	1	1	0	240.4
			1	0	0	1	1	1	250
			1	0	1	0	0	0	260
			1	0	1	0	0	1	271
			1	0	1	0	1	0	284
			1	0	1	0	1	1	297
			1	0	1	1	0	0	312
			1	0	1	1	0	1	328
			1	0	1	1	1	0	347
			1	0	1	1	1	1	367
			1	1	0	0	0	0	390
			1	1	0	0	0	1	416
			1	1	0	0	1	0	446
			1	1	0	0	1	1	480
			1	1	0	1	0	0	521
			1	1	0	1	0	1	568
			1	1	0	1	1	0	625

Table 59. Register 0x40—PWM Switching Frequency Setting

Bits	Name	R/W	Description						
[7:6]	Reserved	R/W	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency of all the PWM pins other than the OUTAUX pin.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	48.8
			0	0	0	0	0	1	50.4
			0	0	0	0	1	0	52.0
			0	0	0	0	1	1	53.8
			0	0	0	1	0	0	55.8
			0	0	0	1	0	1	57.9
			0	0	0	1	1	0	60.1
			0	0	0	1	1	1	62.5
			0	0	1	0	0	0	65.1
			0	0	1	0	0	1	67.9

Bits	Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	1	0	1	0	71.0
			0	0	1	0	1	1	74.4
			0	0	1	1	0	0	78.1
			0	0	1	1	0	1	82.2
			0	0	1	1	1	0	86.8
			0	0	1	1	1	1	91.9
			0	1	0	0	0	0	97.6
			0	1	0	0	0	1	100.8
			0	1	0	0	1	0	104.1
			0	1	0	0	1	1	107.7
			0	1	0	1	0	0	111.6
			0	1	0	1	0	1	115.7
			0	1	0	1	1	0	120.2
			0	1	0	1	1	1	125.0
			0	1	1	0	0	0	130.2
			0	1	1	0	0	1	135.8
			0	1	1	0	1	0	142.0
			0	1	1	0	1	1	148.8
			0	1	1	1	0	0	156.2
			0	1	1	1	0	1	164.5
			0	1	1	1	1	0	173.6
			0	1	1	1	1	1	183.8
			1	0	0	0	0	0	195.3
			1	0	0	0	0	1	201.6
			1	0	0	0	1	0	208.3
			1	0	0	0	1	1	215.5
			1	0	0	1	0	0	223.2
			1	0	0	1	0	1	231.5
			1	0	0	1	1	0	240.4
			1	0	0	1	1	1	250
			1	0	1	0	0	0	260
			1	0	1	0	0	1	271
			1	0	1	0	1	0	284
			1	0	1	0	1	1	297
			1	0	1	1	0	0	312
			1	0	1	1	0	1	328
			1	0	1	1	1	0	347
			1	0	1	1	1	1	367
			1	1	0	0	0	0	390
			1	1	0	0	0	1	416
			1	1	0	0	1	0	446
			1	1	0	0	1	1	480
			1	1	0	1	0	0	521
			1	1	0	1	0	1	568
			1	1	0	1	1	0	625
			1	1	1	1	1	1	Resonant mode

Table 60. Register 0x41—OUTA Rising Edge Timing (OUTA Pin)

Bits	Name	R/W	Description
[7:0]	t_1	R/W	This register contains the eight MSBs of the 12-bit t_1 time. This value is always used with the top four bits of Register 0x42, which contains the four LSBs of the t_1 time. Each LSB corresponds to 5 ns resolution.

Table 61. Register 0x42—OUTA Rising Edge Setting (OUTA Pin)

Bits	Name	R/W	Description
[7:4]	t_1	R/W	These bits contain the four LSBs of the 12-bit t_1 time. This value is always used with the eight bits of Register 0x41, which contains the eight MSBs of the t_1 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_1 edge. 0 = no PWM modulation of the t_1 edge.
2	t_1 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_1 right. 0 = positive sign. Increase of PWM modulation moves t_1 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 62. Register 0x43—OUTA Falling Edge Timing (OUTA Pin)

Bits	Name	R/W	Description
[7:0]	t_2	R/W	This register contains the eight MSBs of the 12-bit t_2 time. This value is always used with the top four bits of Register 0x44, which contains the four LSBs of the t_2 time. Each LSB corresponds to 5 ns resolution.

Table 63. Register 0x44—OUTA Falling Edge Setting (OUTA Pin)

Bits	Name	R/W	Description
[7:4]	t_2	R/W	These bits contain the four LSBs of the 12-bit t_2 time. This value is always used with the eight bits of Register 0x43, which contains the eight MSBs of the t_2 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_2 edge. 0 = no PWM modulation of the t_2 edge.
2	t_2 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_2 right. 0 = positive sign. Increase of PWM modulation moves t_2 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 64. Register 0x45—OUTB Rising Edge Timing (OUTB Pin)

Bits	Name	R/W	Description
[7:0]	t_3	R/W	This register contains the eight MSBs of the 12-bit t_3 time. This value is always used with the top four bits of Register 0x46, which contains the four LSBs of the t_3 time. Each LSB corresponds to 5 ns resolution.

Table 65. Register 0x46—OUTB Rising Edge Setting (OUTB Pin)

Bits	Name	R/W	Description
[7:4]	t_3	R/W	These bits contain the four LSBs of the 12-bit t_3 time. This value is always used with the eight bits of Register 0x45, which contains the eight MSBs of the t_3 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_3 edge. 0 = no PWM modulation of the t_3 edge.
2	t_3 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_3 right. 0 = positive sign. Increase of PWM modulation moves t_3 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 66. Register 0x47—OUTB Falling Edge Timing (OUTB Pin)

Bits	Name	R/W	Description
[7:0]	t_4	R/W	This register contains the eight MSBs of the 12-bit t_4 time. This value is always used with the top four bits of Register 0x48, which contains the four LSBs of the t_4 time. Each LSB corresponds to 5 ns resolution.

Table 67. Register 0x48—OUTB Falling Edge Setting (OUTB Pin)

Bits	Name	R/W	Description
[7:4]	t_4	R/W	These bits contain the four LSBs of the 12-bit t_4 time. This value is always used with the eight bits of Register 0x47, which contains the eight MSBs of the t_4 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_4 edge. 0 = no PWM modulation of the t_4 edge.
2	t_4 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_4 right. 0 = positive sign. Increase of PWM modulation moves t_4 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 68. Register 0x49—OUTC Rising Edge Timing (OUTC Pin)

Bits	Name	R/W	Description
[7:0]	t_5	R/W	This register contains the eight MSBs of the 12-bit t_5 time. This value is always used with the top four bits of Register 0x4A, which contains the four LSBs of the t_5 time. Each LSB corresponds to 5 ns resolution.

Table 69. Register 0x4A—OUTC Rising Edge Setting (OUTC Pin)

Bits	Name	R/W	Description
[7:4]	t_5	R/W	These bits contain the four LSBs of the 12-bit t_5 time. This value is always used with the eight bits of Register 0x49, which contains the eight MSBs of the t_5 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_5 edge. 0 = no PWM modulation of the t_5 edge.
2	t_5 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_5 right. 0 = positive sign. Increase of PWM modulation moves t_5 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 70. Register 0x4B—OUTC Falling Edge Timing (OUTC Pin)

Bits	Name	R/W	Description
[7:0]	t_6	R/W	This register contains the eight MSBs of the 12-bit t_6 time. This value is always used with the top four bits of Register 0x4C, which contains the four LSBs of the t_6 time. Each LSB corresponds to 5 ns resolution.

Table 71. Register 0x4C—OUTC Falling Edge Setting (OUTC Pin)

Bits	Name	R/W	Description
[7:4]	t_6	R/W	These bits contain the four LSBs of the 12-bit t_6 time. This value is always used with the eight bits of Register 0x4B, which contains the eight MSBs of the t_6 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_6 edge. 0 = no PWM modulation of the t_6 edge.
2	t_6 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_6 right. 0 = positive sign. Increase of PWM modulation moves t_6 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 72. Register 0x4D—OUTD Rising Edge Timing (OUTD Pin)

Bits	Name	R/W	Description
[7:0]	t_7	R/W	This register contains the eight MSBs of the 12-bit t_7 time. This value is always used with the top four bits of Register 0x4E, which contains the four LSBs of the t_7 time. Each LSB corresponds to 5 ns resolution.

Table 73. Register 0x4E—OUTD Rising Edge Setting (OUTD Pin)

Bits	Name	R/W	Description
[7:4]	t_7	R/W	These bits contain the four LSBs of the 12-bit t_7 time. This value is always used with the eight bits of Register 0x4D, which contains the eight MSBs of the t_7 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_7 edge. 0 = no PWM modulation of the t_7 edge.
2	t_7 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_7 right. 0 = positive sign. Increase of PWM modulation moves t_7 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 74. Register 0x4F—OUTD Falling Edge Timing (OUTD Pin)

Bits	Name	R/W	Description
[7:0]	t_8	R/W	This register contains the eight MSBs of the 12-bit t_8 time. This value is always used with the top four bits of Register 0x50, which contains the four LSBs of the t_8 time. Each LSB corresponds to 5 ns resolution.

Table 75. Register 0x50—OUTD Falling Edge Setting (OUTD Pin)

Bits	Name	R/W	Description
[7:4]	t_8	R/W	These bits contain the four LSBs of the 12-bit t_8 time. This value is always used with the eight bits of Register 0x4F, which contains the eight MSBs of the t_8 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_8 edge. 0 = no PWM modulation of the t_8 edge.
2	t_8 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_8 right. 0 = positive sign. Increase of PWM modulation moves t_8 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 76. Register 0x51—SR1 Rising Edge Timing (SR1 Pin)

Bits	Name	R/W	Description
[7:0]	t_9	R/W	This register contains the eight MSBs of the 12-bit t_9 time. This value is always used with the top four bits of Register 0x52, which contains the four LSBs of the t_9 time. Each LSB corresponds to 5 ns resolution.

Table 77. Register 0x52—SR1 Rising Edge Setting (SR1 Pin)

Bits	Name	R/W	Description
[7:4]	t_9	R/W	These bits contain the four LSBs of the 12-bit t_9 time. This value is always used with the eight bits of Register 0x51, which contains the eight MSBs of the t_9 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_9 edge. 0 = no PWM modulation of the t_9 edge.
2	t_9 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_9 right. 0 = positive sign. Increase of PWM modulation moves t_9 left.
1	VS balance with SR1 and SR2	R/W	1 = volt-second balance circuit modulates SR1 and SR2, along with OUTB and OUTD. When this bit is set, the volt-second balance modulation is applied to the rising edge of SR1 and SR2.
0	Reserved	R/W	Reserved. This bit should be set to 0 for normal operation.

Table 78. Register 0x53—SR1 Falling Edge Timing (SR1 Pin)

Bits	Name	R/W	Description
[7:0]	t_{10}	R/W	This register contains the eight MSBs of the 12-bit t_{10} time. This value is always used with the top four bits of Register 0x54, which contains the four LSBs of the t_{10} time. Each LSB corresponds to 5 ns resolution.

Table 79. Register 0x54—SR1 Falling Edge Setting (SR1 Pin)

Bits	Name	R/W	Description
[7:4]	t_{10}	R/W	These bits contain the four LSBs of the 12-bit t_{10} time. This value is always used with the eight bits of Register 0x53, which contains the eight MSBs of the t_{10} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{10} edge. 0 = no PWM modulation of the t_{10} edge.
2	t_{10} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{10} right. 0 = positive sign. Increase of PWM modulation moves t_{10} left.
1	SR soft start setting	R/W	1 = SR signals perform a soft start every time that they are enabled. 0 = SR signals perform a soft start only the first time that they are enabled.
0	SR soft start enable	R/W	Setting this bit enables the soft start function for the SR signals.

Table 80. Register 0x55—SR2 Rising Edge Timing (SR2 Pin)

Bits	Name	R/W	Description
[7:0]	t_{11}	R/W	This register contains the eight MSBs of the 12-bit t_{11} time. This value is always used with the top four bits of Register 0x56, which contains the four LSBs of the t_{11} time. Each LSB corresponds to 5 ns resolution.

Table 81. Register 0x56—SR2 Rising Edge Setting (SR2 Pin)

Bits	Name	R/W	Description
[7:4]	t_{11}	R/W	These bits contain the four LSBs of the 12-bit t_{11} time. This value is always used with the eight bits of Register 0x55, which contains the eight MSBs of the t_{11} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{11} edge. 0 = no PWM modulation of the t_{11} edge.
2	t_{11} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{11} right. 0 = positive sign. Increase of PWM modulation moves t_{11} left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 82. Register 0x57—SR2 Falling Edge Timing (SR2 Pin)

Bits	Name	R/W	Description
[7:0]	t_{12}	R/W	This register contains the eight MSBs of the 12-bit t_{12} time. This value is always used with the top four bits of Register 0x58, which contains the four LSBs of the t_{12} time. Each LSB corresponds to 5 ns resolution.

Table 83. Register 0x58—SR2 Falling Edge Setting (SR2 Pin)

Bits	Name	R/W	Description
[7:4]	t_{12}	R/W	These bits contain the four LSBs of the 12-bit t_{12} time. This value is always used with the eight bits of Register 0x57, which contains the eight MSBs of the t_{12} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{12} edge. 0 = no PWM modulation of the t_{12} edge.
2	t_{12} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{12} right. 0 = positive sign. Increase of PWM modulation moves t_{12} left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 84. Register 0x59—OUTAUX Rising Edge Timing (OUTAUX Pin)

Bits	Name	R/W	Description
[7:0]	t_{13}	R/W	This register contains the eight MSBs of the 12-bit t_{13} time. This value is always used with the top four bits of Register 0x5A, which contains the four LSBs of the t_{13} time. Each LSB corresponds to 5 ns resolution.

Table 85. Register 0x5A—OUTAUX Rising Edge Setting (OUTAUX Pin)

Bits	Name	R/W	Description
[7:4]	t_{13}	R/W	These bits contain the four LSBs of the 12-bit t_{13} time. This value is always used with the eight bits of Register 0x59, which contains the eight MSBs of the t_{13} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{13} edge. 0 = no PWM modulation of the t_{13} edge.
2	t_{13} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{13} right. 0 = positive sign. Increase of PWM modulation moves t_{13} left.
[1:0]	Reserved	R/W	Reserved. Set these bits to 00 for normal operation.

Table 86. Register 0x5B—OUTAUX Falling Edge Timing (OUTAUX Pin)

Bits	Name	R/W	Description
[7:0]	t_{14}	R/W	This register contains the eight MSBs of the 12-bit t_{14} time. This value is always used with the top four bits of Register 0x5C, which contains the four LSBs of the t_{14} time. Each LSB corresponds to 5 ns resolution.

Table 87. Register 0x5C—OUTAUX Falling Edge Setting (OUTAUX Pin)

Bits	Name	R/W	Description
[7:4]	t_{14}	R/W	These bits contain the four LSBs of the 12-bit t_{14} time. This value is always used with the eight bits of Register 0x5B, which contains the eight MSBs of the t_{14} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{14} edge. 0 = no PWM modulation of the t_{14} edge.
2	t_{14} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{14} right. 0 = positive sign. Increase of PWM modulation moves t_{14} left.
1	Regulate with OUTAUX	R/W	1 = control loop PWM modulation is regulated by OUTAUX. When this bit is set, the CS1 blanking signal is synchronized with OUTAUX. 0 = control loop PWM modulation is regulated by OUTA, OUTB, OUTC, OUTD, SR1, and SR2 (normal mode).
0	Reserved	R/W	Reserved. Set this bit to 0 for normal operation.

Table 88. Register 0x5D—OUTx and SRx Pin Disable Setting

Bits	Name	R/W	Description
7	OUTAUX disable	R/W	Setting this bit disables the OUTAUX output.
6	SR2 disable	R/W	Setting this bit disables the SR2 output.
5	SR1 disable	R/W	Setting this bit disables the SR1 output.
4	OUTD disable	R/W	Setting this bit disables the OUTD output.
3	OUTC disable	R/W	Setting this bit disables the OUTC output.
2	OUTB disable	R/W	Setting this bit disables the OUTB output.
1	OUTA disable	R/W	Setting this bit disables the OUTA output.
0	GO	W	This bit latches in all registers from Address 0x3F to Address 0x5D. This bit prevents the PWM timing from being temporarily incorrect, if changing PWM timing while the power supply is on. This bit also latches in any changes made to Register 0x31 (VS3 voltage setting).

Table 89. Register 0x5E—Password Lock

Bits	Name	R/W	Description
[7:0]	Password	W	This register contains the 8-bit EEPROM lock password. This password is used to protect the register contents from being changed. The EEPROM is always locked. When the EEPROM downloads its contents to the registers, the password is also downloaded. If the user writes the same password to this register twice, the EEPROM is unlocked and can be updated. To lock the EEPROM again, the user must write any value other than the password value into this register.

DIGITAL FILTER PROGRAMMING REGISTERS

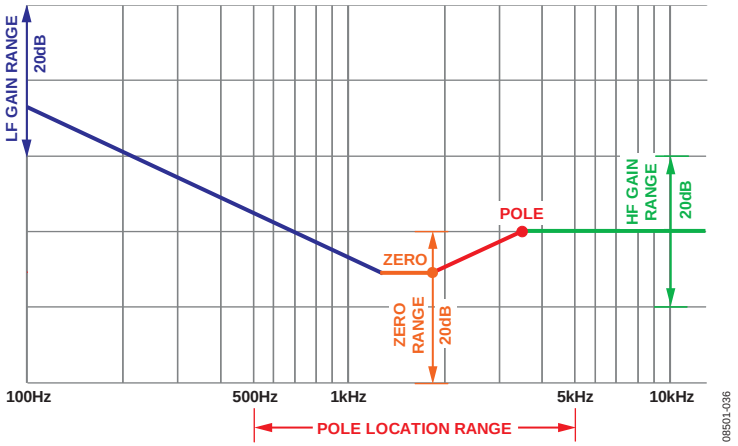


Figure 37. Digital Filter Programmability

Table 90. Register 0x5F—Soft Start Digital Filter LF Gain Setting

Bits	Name	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	Soft start filter gain	R/W	These bits set the gain of the low-pass digital filter that is used during soft start.		
			Bit 1	**Bit 0**	**Filter Gain**
			0	0	1
			0	1	2
			1	0	4
			1	1	8

Table 91. Register 0x60—Normal Mode Digital Filter LF Gain Setting

Bits	Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 37.

Table 92. Register 0x61—Normal Mode Digital Filter Zero Setting

Bits	Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final 0. See Figure 37.

Table 93. Register 0x62—Normal Mode Digital Filter Pole Setting

Bits	Name	R/W	Description
[7:0]	Pole location	R/W	This register determines the position of the final pole. See Figure 37.

Table 94. Register 0x63—Normal Mode Digital Filter HF Gain Setting

Bits	Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 37.

Table 95. Register 0x64—Light Load Mode Digital Filter LF Gain Setting

Bits	Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 37.

Table 96. Register 0x65—Light Load Mode Digital Filter Zero Setting

Bits	Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final 0. See Figure 37.

Table 97. Register 0x66—Light Load Mode Digital Filter Pole Setting

Bits	Name	R/W	Description
[7:0]	Pole location	R/W	This register determines the position of the final pole. See Figure 37.

Table 98. Register 0x67—Light Load Mode Digital Filter HF Gain Setting

Bits	Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 37.

ADAPTIVE DEAD TIME REGISTERS

Table 99. Register 0x68—Dead Time Threshold

Bits	Name	R/W	Description					
[7:3]	Reserved	R/W	Reserved.					
[2:0]	Adaptive dead time threshold	R/W	This value determines the adaptive dead time threshold. Below this threshold, the offsets from Register 0x69 to Register 0x6F are introduced.					
						Threshold for Each Nominal CS2 Setting (mV)		
			Bit 2	Bit 1	Bit 0	37.5 mV Setting	75 mV Setting	150 mV Setting
			0	0	0	0	0	0
			0	0	1	3.9	7.8	15.6
			0	1	0	7.8	15.6	31.25
			0	1	1	11.7	23.5	47
			1	0	0	15.5	31	62.5
			1	0	1	19.5	39	78
			1	1	0	23.5	47	94
			1	1	1	27	54	109

Table 100. Register 0x69—Dead Time 1

Bits	Name	R/W	Description			
7	t_1 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_1 offset	R/W	This value determines the t_1 offset from the nominal timing.			
			Bit 6	Bit 5	Bit 4	Offset (ns)
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_2 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_2 offset	R/W	This value determines the t_2 offset from the nominal timing.			
			Bit 2	Bit 1	Bit 0	Offset (ns)
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 101. Register 0x6A—Dead Time 2

Bits	Name	R/W	Description			
7	t_3 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_3 offset	R/W	This value determines the t_3 offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_4 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_4 offset	R/W	This value determines the t_4 offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 102. Register 0x6B—Dead Time 3

Bits	Name	R/W	Description			
7	t_5 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_5 offset	R/W	This value determines the t_5 offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_6 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_6 offset	R/W	This value determines the t_6 offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 103. Register 0x6C—Dead Time 4

Bits	Name	R/W	Description			
7	t_7 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_7 offset	R/W	This value determines the t_7 offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_8 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_8 offset	R/W	This value determines the t_8 offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 104. Register 0x6D—Dead Time 5

Bits	Name	R/W	Description			
7	t_9 polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_9 offset	R/W	This value determines the t_9 offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_{10} polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_{10} offset	R/W	This value determines the t_{10} offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 105. Register 0x6E—Dead Time 6

Bits	Name	R/W	Description			
7	t_{11} polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_{11} offset	R/W	This value determines the t_{11} offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_{12} polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_{12} offset	R/W	This value determines the t_{12} offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

Table 106. Register 0x6F—Dead Time 7

Bits	Name	R/W	Description			
7	t_{13} polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[6:4]	t_{13} offset	R/W	This value determines the t_{13} offset from the nominal timing.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35
3	t_{14} polarity	R/W	0 = positive polarity; 1 = negative polarity.			
[2:0]	t_{14} offset	R/W	This value determines the t_{14} offset from the nominal timing.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	5
			0	1	0	10
			0	1	1	15
			1	0	0	20
			1	0	1	25
			1	1	0	30
			1	1	1	35

EEPROM REGISTERS

Table 107. Register 0x7B—EEPROM Restore Factory Default Register Settings

Bits	Name	R/W	Description
[7:0]	EEPROM restore factory default settings	R/W	The user can write one of the following command codes to this register to perform a specific EEPROM operation: 0x00: Upload registers to Page 0 of the main block (user settings). 0x01: Download factory settings (factory block) to the registers. 0x02: Page erase operation. For more information, see the EEPROM section.

Table 108. Register 0x7C—EEPROM X Address

Bits	Name	R/W	Description
7	Reserved	R/W	Reserved.
[6:0]	EEPROM X address	R/W	This register is used to point to the page and row of the byte to be accessed in EEPROM main memory. Bits[6:3] select one of 16 pages in the main block; Bits[2:0] select one of eight rows on the selected page. The byte to be accessed is specified using Register 0x7D. For more information, see the EEPROM section.

Table 109. Register 0x7D—EEPROM Y Address

Bits	Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	EEPROM Y address	R/W	This register is used to point to the byte to be accessed in EEPROM main memory. The page and row of the byte are specified using Register 0x7C. For more information, see the EEPROM section.

Table 110. Register 0x7E—EEPROM Register

Bits	Name	R/W	Description
[7:0]	EEPROM register	R/W	Read or write to this register to read or program a byte in EEPROM main memory. For more information, see the EEPROM section.

RESONANT MODE OPERATION

The ADP1043A supports control of a resonant converter. Resonant converters are an alternative to traditional fixed frequency converters. They offer high switching frequency, small size, and high efficiency. Figure 38 illustrates a widely used series resonant converter.

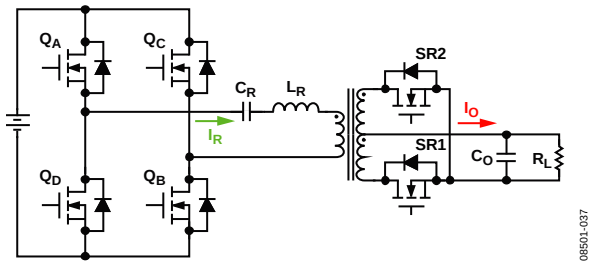


Figure 38. Series Resonant Converter

RESONANT MODE ENABLE

To enable the ADP1043A to control a resonant switching converter, Register 0x40 must be set to a value of 0x3F. In resonant mode, the PWM outputs have a fixed duty cycle with variable frequency.

PWM TIMING IN RESONANT MODE

With variable frequency control, OUTA and OUTB can only be high during the first half of the switching cycle (t_A to t_B), whereas OUTC and OUTD can only be high during the second half of the switching cycle (t_B to t_C), as shown in Figure 39.

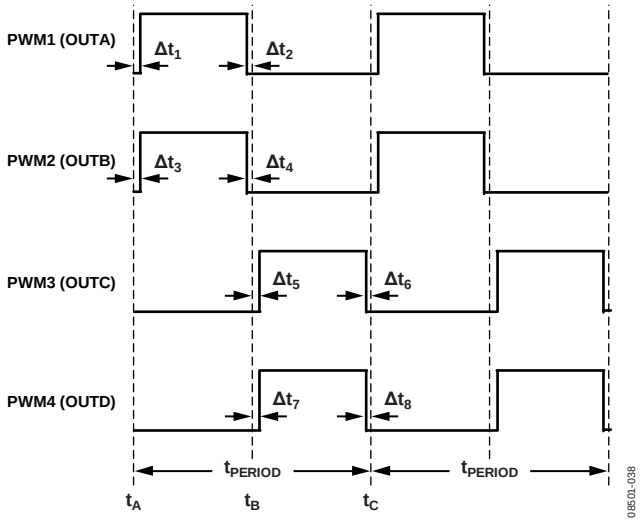


Figure 39. OUTA, OUTB, OUTC, and OUTD PWM Timing Diagram in Resonant Mode

SYNCHRONOUS RECTIFICATION IN RESONANT MODE

Control of the synchronous rectifiers in a resonant controller is a complicated issue. The ADP1043A ACSNS comparator can be used to control the SR signals. In resonant mode operation, the SR1 output is driven by the rising edge of the ACSNS comparator, and the SR2 output is driven by the falling edge of the comparator, as shown in Figure 40.

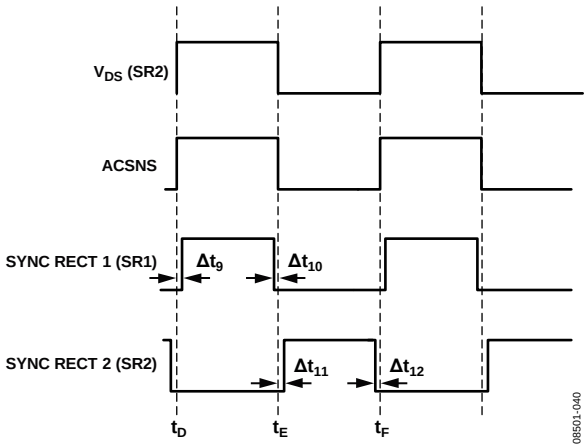


Figure 40. SR1 and SR2 PWM Timing Diagram in Resonant Mode

Following is an example of how the ADP1043A can be used in a series resonant topology and also achieve control of the synchronous rectifiers. The V_{DS} voltage of SR2 can be used to control the SR signals. The ACSNS pin is connected to the divided-down SR2 V_{DS} voltage. This provides the timing information for both synchronous rectifiers (see Figure 41).

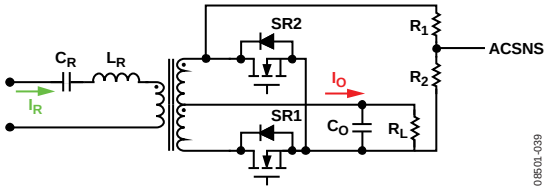


Figure 41. Resonant Synchronous Rectifier Control Circuit

After the timing information is obtained, SR1 is driven by the rising edge of the ACSNS comparator, and SR2 is driven by the falling edge of the comparator, as shown in Figure 40. In this way, it is possible to achieve synchronous rectification. Turn-on and turn-off delays can be programmed for the SR1 and SR2 signals individually.

This example is not the only way to control the SR signals. If the user has another method to control the SR signals, this method can be used to connect to the ACSNS input instead of the V_{DS} voltage of SR2.

ADJUSTING THE TIMING OF THE PWM OUTPUTS

To accurately adjust the timing of the PWM outputs, the following registers can be used to set the dead time and delays of the PWM outputs: Register 0x41, Register 0x43, Register 0x45, Register 0x47, Register 0x49, Register 0x4B, Register 0x4D, Register 0x4F, Register 0x51, Register 0x53, Register 0x55, and Register 0x57. The resolution for adjusting the dead time is 5 ns. Refer to the Resonant Mode Register Descriptions section for more detailed information. The software GUI for the ADP1043A can be used to set the frequency limit registers, as well as all other settings related to the resonant mode of operation.

FREQUENCY LIMIT SETTING

The minimum frequency is set by Register 0x42 and by the first four bits of Register 0x44.

For example, Register 0x42 is set to 0xA0 (160 decimal) and Bits[7:4] of Register 0x44 are set to 0xF (15 decimal).

The maximum switching cycle is

$$(160 \times 16 + 15) \times 5 \text{ ns} = 12.875 \text{ µs}$$

The lowest switching frequency limit is

$$1/12.875 \text{ µs} = 77.7 \text{ kHz}$$

The maximum frequency is set by Register 0x46 and by Bits[7:4] of Register 0x48.

For example, Register 0x46 is set to 0x10 (16 decimal) and Bits[7:4] of Register 0x48 are set to 0x9 (9 decimal).

The minimum switching cycle is

$$(16 \times 16 + 9) \times 5 \text{ ns} = 1.325 \text{ µs}$$

The highest switching frequency limit is

$$1/1.325 \text{ µs} = 755 \text{ kHz}$$

FEEDBACK CONTROL IN RESONANT MODE

In contrast to a traditional fixed frequency PWM converter, the output voltage of a resonant converter is regulated by changing the switching frequency. When the ADP1043A is operated in resonant mode, the switching frequency decreases when the sensed voltage is lower than the reference voltage. This makes the ADP1043A capable of controlling a resonant converter in zero-voltage switching (ZVS) mode.

Although the switching frequency is variable, the feedback voltage sampling frequency is fixed at 400 kHz. The parameters of the feedback filter are based on this frequency. The method for calculating the filter parameters (gains, zeros, and poles) is the same as that for the fixed frequency PWM mode (see the Digital Filter section).

SOFT START IN RESONANT MODE

During soft start, the reference voltage of the ADP1043A ramps up. With the feedback loop closed, the switching frequency is reduced from the highest limit to a regulation value. The soft start timing settings and the filter settings are the same as those for the fixed frequency PWM mode (see the Soft Start section).

LIGHT LOAD OPERATION (BURST MODE)

To control the converter at very light load, the ADP1043A can operate in burst mode. Burst mode can be enabled or disabled using Bits[7:6] of Register 0x4A. When the desired switching frequency is higher than the burst mode threshold, the part enters burst mode. The threshold is determined by the maximum frequency and the burst mode offset setting.

The threshold value used to enter burst mode is determined as follows:

Threshold value for burst mode =
((Register 0x46 × 16) + Register 0x48[7:4]) +
(Register 0x4A[5:0] × 2)

The threshold value used to exit burst mode is determined by the entrance value plus 0x10.

For example, Register 0x46 is set to 0x10 (16 decimal), Bits[7:4] of Register 0x48 are set to 0, and Bits[5:0] of Register 0x4A are set to 0x8 (8 decimal).

The minimum switching cycle is

$$(16 \times 16 + 0) \times 5 \text{ ns} = 1.28 \text{ µs}$$

The highest switching frequency limit is

$$1/1.28 \text{ µs} = 781 \text{ kHz}$$

The threshold to enter burst mode is

$$[(16 \times 16 + 0) + (8 \times 2)] \times 5 \text{ ns} = 1.36 \text{ µs}$$

When the desired switching frequency is higher than 1/1.36 µs = 735 kHz, the PWM outputs are shut down and the part enters burst mode.

The threshold to exit burst mode is

$$[(16 \times 16 + 0) + (8 \times 2) + 16] \times 5 \text{ ns} = 1.44 \text{ µs}$$

Therefore, when the desired switching frequency becomes lower than 1/1.44 µs = 694 kHz, the PWM signals are reenabled, and the part exits burst mode.

OUTAUX IN RESONANT MODE

In resonant mode, the OUTAUX pin cannot be used as a control signal. However, OUTAUX can be used as a fixed frequency PWM signal with a fixed duty cycle.

PROTECTIONS IN RESONANT MODE

All of the flags and protections that are available in resonant mode behave in the same manner as in fixed frequency PWM mode.

RESONANT MODE REGISTER DESCRIPTIONS

Table 111. Register 0x40—PWM Switching Frequency Setting in Resonant Mode

Bits	Name	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	Switching frequency	R/W	This register sets the switching frequency of the PWM pins and enables resonant mode. To enable resonant mode, set these bits to 0x3F (11 1111).

Table 112. Register 0x41—OUTA Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_1 (rising edge dead time of OUTA)	R/W	This register sets Δt_1, which is the delay of the rising edge of OUTA from the start of the switching cycle, t_A. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_1 (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 113. Register 0x42—Lowest Switching Frequency Limit Setting (Maximum Switching Cycle in Resonant Mode)

Bits	Name	R/W	Description
[7:0]	Lowest frequency	R/W	This register contains the eight MSBs of the 12-bit value of the lowest switching frequency (maximum switching cycle) limit. This value is always used with the top four bits of Register 0x44, which contain the four LSBs of the lowest switching frequency limit. Each LSB of the 12-bit value corresponds to 5 ns of resolution for the switching cycle. For example, if Register 0x42 is set to 0xA0 (160 decimal) and Bits[7:4] of Register 0x44 are set to 0xF (15 decimal), the maximum switching cycle is (160 × 16 + 15) × 5 ns = 12.875 µs, and the lowest switching frequency limit is 1/12.875 µs = 77.7 kHz.

Table 114. Register 0x43—OUTA Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_2 (falling edge dead time of OUTA)	R/W	This register sets Δt_2, which is the difference between the falling edge of OUTA and the midpoint of the switching cycle, t_B. Each LSB corresponds to 5 ns of resolution. When the register value is from 0x00 to 0x7F, the falling edge of OUTA is trailing t_B. When the value is from 0x80 to 0xFF, the falling edge of OUTA is leading t_B.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_2
0	0	0	0	0	0	0	0	0 ns
0	0	0	0	0	0	0	1	5 ns trailing
…	…	…	…	…	…	…	…	…
0	1	1	1	1	1	1	1	635 ns trailing
1	0	0	0	0	0	0	0	640 ns leading
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	5 ns leading

Table 115. Register 0x44—Lowest Switching Frequency Limit Setting (Maximum Switching Cycle in Resonant Mode)

Bits	Name	R/W	Description
[7:4]	Lowest frequency	R/W	This register contains the four LSBs of the 12-bit value of the lowest switching frequency (maximum switching cycle) limit. This value is always used with the eight bits of Register 0x42, which contain the eight MSBs of the lowest switching frequency limit. Each LSB of the 12-bit value corresponds to 5 ns of resolution for the switching cycle. For example, if Register 0x42 is set to 0xA0 (160 decimal) and Bits[7:4] of Register 0x44 are set to 0xF (15 decimal), the maximum switching cycle is (160 × 16 + 15) × 5 ns = 12.875 µs, and the lowest switching frequency limit is 1/12.875 µs = 77.7 kHz.
[3:0]	Reserved	R/W	Reserved.

Table 116. Register 0x45—OUTB Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_3 (rising edge dead time of OUTB)	R/W	This register sets Δt_3, which is the delay time of the rising edge of OUTB from the start of the switching cycle, t_A. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_3 (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 117. Register 0x46—Highest Switching Frequency Limit Setting (Minimum Switching Cycle in Resonant Mode)

Bits	Name	R/W	Description
[7:0]	Highest frequency	R/W	This register contains the eight MSBs of the 12-bit value of the highest switching frequency (minimum switching cycle) limit. This value is always used with the top four bits of Register 0x48, which contain the four LSBs of the highest switching frequency limit. Each LSB of the 12-bit value corresponds to 5 ns of resolution for the switching cycle. For example, if Register 0x46 is set to 0x10 (16 decimal) and Bits[7:4] of Register 0x48 are set to 0x9 (9 decimal), the minimum switching cycle is (16 × 16 + 9) × 5 ns = 1.325 µs, and the highest switching frequency limit is 1/1.325 µs = 755 kHz.

Table 118. Register 0x47—OUTB Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_4 (falling edge dead time of OUTB)	R/W	This register sets Δt_4, which is the difference between the falling edge of OUTB and the midpoint of the switching cycle, t_B. Each LSB corresponds to 5 ns of resolution. When the register value is from 0x00 to 0x7F, the falling edge of OUTB is trailing t_B. When the value is from 0x80 to 0xFF, the falling edge of OUTB is leading t_B.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_4
0	0	0	0	0	0	0	0	0 ns
0	0	0	0	0	0	0	1	5 ns trailing
…	…	…	…	…	…	…	…	…
0	1	1	1	1	1	1	1	635 ns trailing
1	0	0	0	0	0	0	0	640 ns leading
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	5 ns leading

Table 119. Register 0x48—Highest Switching Frequency Limit Setting (Minimum Switching Cycle in Resonant Mode)

Bits	Name	R/W	Description
[7:4]	Highest frequency	R/W	This register contains the four LSBs of the 12-bit value of the highest switching frequency (minimum switching cycle) limit. This value is always used with the eight bits of Register 0x46, which contain the eight MSBs of the highest switching frequency limit. Each LSB of the 12-bit value corresponds to 5 ns of resolution for the switching cycle. For example, if Register 0x46 is set to 0x10 (16 decimal) and Bits[7:4] of Register 0x48 are set to 0x9 (9 decimal), the minimum switching cycle is (16 × 16 + 9) × 5 ns = 1.325 µs, and the highest switching frequency limit is 1/1.325 µs = 755 kHz.
[3:0]	Reserved	R/W	Reserved.

Table 120. Register 0x49—OUTC Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description								
[7:0]	Δt_5 (rising edge dead time of OUTC)	R/W	This register sets Δt_5, which is the difference between the rising edge of OUTC and the midpoint of the switching cycle, t_B. Each LSB corresponds to 5 ns of resolution. When the register value is from 0x00 to 0x7F, the rising edge of OUTC is trailing t_B. When the value is from 0x80 to 0xFF, the rising edge of OUTC is leading t_B.								
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Δt_5**
			0	0	0	0	0	0	0	0	0 ns
			0	0	0	0	0	0	0	1	5 ns trailing
			…	…	…	…	…	…	…	…	…
			0	1	1	1	1	1	1	1	635 ns trailing
			1	0	0	0	0	0	0	0	640 ns leading
			…	…	…	…	…	…	…	…	…
			1	1	1	1	1	1	1	1	5 ns leading

Table 121. Register 0x4A—Burst Mode Operation in Resonant Mode

Bits	Name	R/W	Description		
[7:6]	Burst mode enable	R/W	These bits are used to enable or disable burst mode operation.		
			Bit 7	**Bit 6**	**Burst Mode**
			0	0	Disabled
			0	1	Enabled for normal operation, but disabled during soft start
			1	0	Disabled
			1	1	Enabled for normal operation and during soft start
[5:0]	Burst mode offset	R/W	These bits, along with the highest switching frequency limit, determine the threshold value for enabling burst mode operation. For information about how to set this value, see the Light Load Operation (Burst Mode) section.		

Table 122. Register 0x4B—OUTC Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description								
[7:0]	Δt_6 (falling edge dead time of OUTC)	R/W	This register sets Δt_6, which is the leading time of the falling edge of OUTC from the end of the switching cycle, t_C. Each LSB corresponds to 5 ns of resolution.								
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Δt_6 (ns)**
			0	0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	1	5
			…	…	…	…	…	…	…	…	…
			1	1	1	1	1	1	1	1	1275

Table 123. Register 0x4D—OUTD Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description								
[7:0]	Δt_7 (rising edge dead time of OUTD)	R/W	This register sets Δt_7, which is the difference between the rising edge of OUTD and the mid-point of the switching cycle, t_B. Each LSB corresponds to 5 ns of resolution. When the register value is from 0x00 to 0x7F, the rising edge of OUTD is trailing t_B. When the value is from 0x80 to 0xFF, the rising edge of OUTD is leading t_B.								
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Δt_7**
			0	0	0	0	0	0	0	0	0 ns
			0	0	0	0	0	0	0	1	5 ns trailing
			…	…	…	…	…	…	…	…	…
			0	1	1	1	1	1	1	1	635 ns trailing
			1	0	0	0	0	0	0	0	640 ns leading
			…	…	…	…	…	…	…	…	…
			1	1	1	1	1	1	1	1	5 ns leading

Table 124. Register 0x4F—OUTD Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_8 (falling edge dead time of OUTD)	R/W	This register sets Δt_8, which is the leading time of the falling edge of OUTD from the end of the switching cycle, t_C. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_8 (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 125. Register 0x51—SR1 Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_9 (rising edge dead time of SR1)	R/W	This register sets Δt_9, which is the delay time of the rising edge of SR1 from the ACSNS rising edge, t_D. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_9 (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 126. Register 0x53—SR1 Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_{10} (falling edge dead time of SR1)	R/W	This register sets Δt_{10}, which is the leading time of the falling edge of SR1 from the ACSNS falling edge, t_E. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_{10} (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 127. Register 0x55—SR2 Rising Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_{11} (rising edge dead time of SR2)	R/W	This register sets Δt_{11}, which is the delay time of the rising edge of SR2 from the ACSNS falling edge, t_E. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_{11} (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

Table 128. Register 0x57—SR2 Falling Edge Dead Time in Resonant Mode

Bits	Name	R/W	Description
[7:0]	Δt_{12} (falling edge dead time of SR2)	R/W	This register sets Δt_{12}, which is the leading time of the falling edge of SR2 from the ACSNS rising edge, t_F. Each LSB corresponds to 5 ns of resolution.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Δt_{12} (ns)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	5
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1275

OUTLINE DIMENSIONS

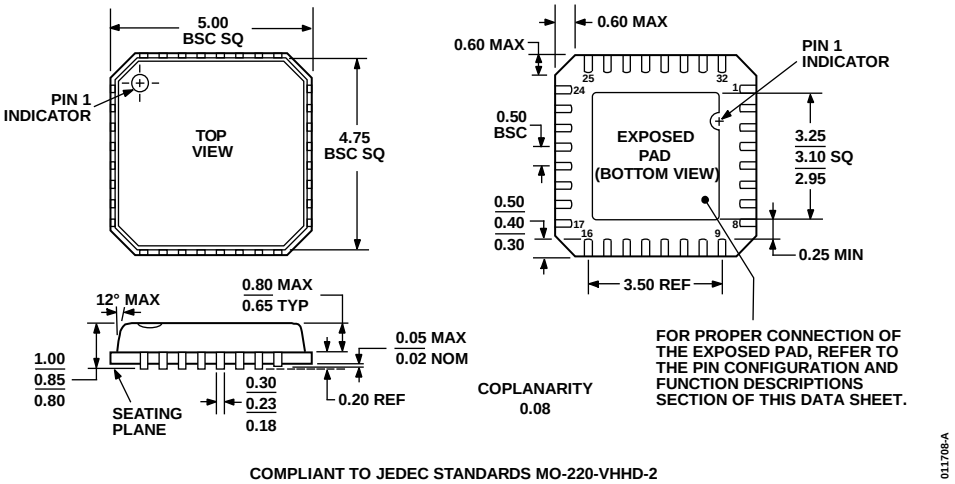


Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP1043AACPZ-RL[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2

[1] Z = RoHS Compliant Part.

NOTES

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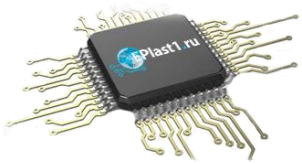
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