SINGLE-ENDED, ANALOG-INPUT 24-BIT, 96-kHz STEREO A/D CONVERTER

FEATURES

- **24-Bit Delta-Sigma Stereo A/D Converter**
- **Single-Ended Voltage Input: 3 Vp-p**
- **Oversampling Decimation Filter:**
  - **Oversampling Frequency: ×64, ×128**
  - **Pass-Band Ripple: ±0.05 dB**
  - **Stop-Band Attenuation: –65 dB**
  - **On-Chip High-Pass Filter: 0.84 Hz (44.1 kHz)**
- **High-Performance:**
  - **THD+N: –95 dB (Typically)**
  - **SNR: 103 dB (Typically)**
  - **Dynamic Range: 103 dB (Typically)**
- **PCM Audio Interface:**
  - **Master/Slave Mode Selectable**
  - **Data Formats:**
    - **24-Bit Left-Justified**
    - **24-Bit I^2S**
    - **20-, 24-Bit Right-Justified**
- **Sampling Rate: 16 kHz to 96 kHz**
- **System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S**
- **Dual Power Supplies: 5 V for Analog, 3.3 V for Digital**
- **Package: 20-Pin SSOP**

APPLICATIONS

- **AV Amplifier Receiver**
- **MD Player**
- **CD Recorder**
- **Multitrack Receiver**
- **Electric Musical Instrument**

DESCRIPTION

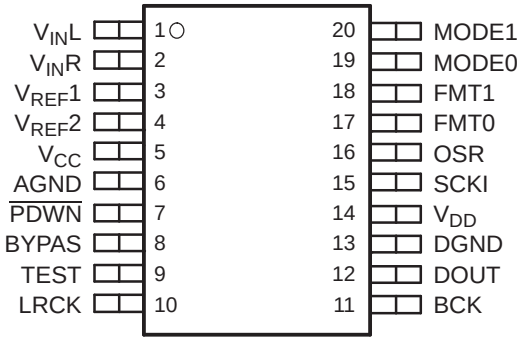
The PCM1803A is high-performance, low-cost, single-chip stereo analog-to-digital converter with single-ended analog voltage input. The PCM1803A uses a delta-sigma modulator with 64- and 128-times oversampling, and includes a digital decimation filter and high-pass filter, which removes the dc component of the input signal. For various applications, the PCM1803A supports master and slave modes and four data formats in serial interface. The PCM1803A is suitable for a wide variety of cost-sensitive consumer applications where good performance and operation from a 5-V analog supply and 3.3-V digital supply are required. The PCM1803A is fabricated using a highly advanced CMOS process and is available in a small 20-pin SSOP package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

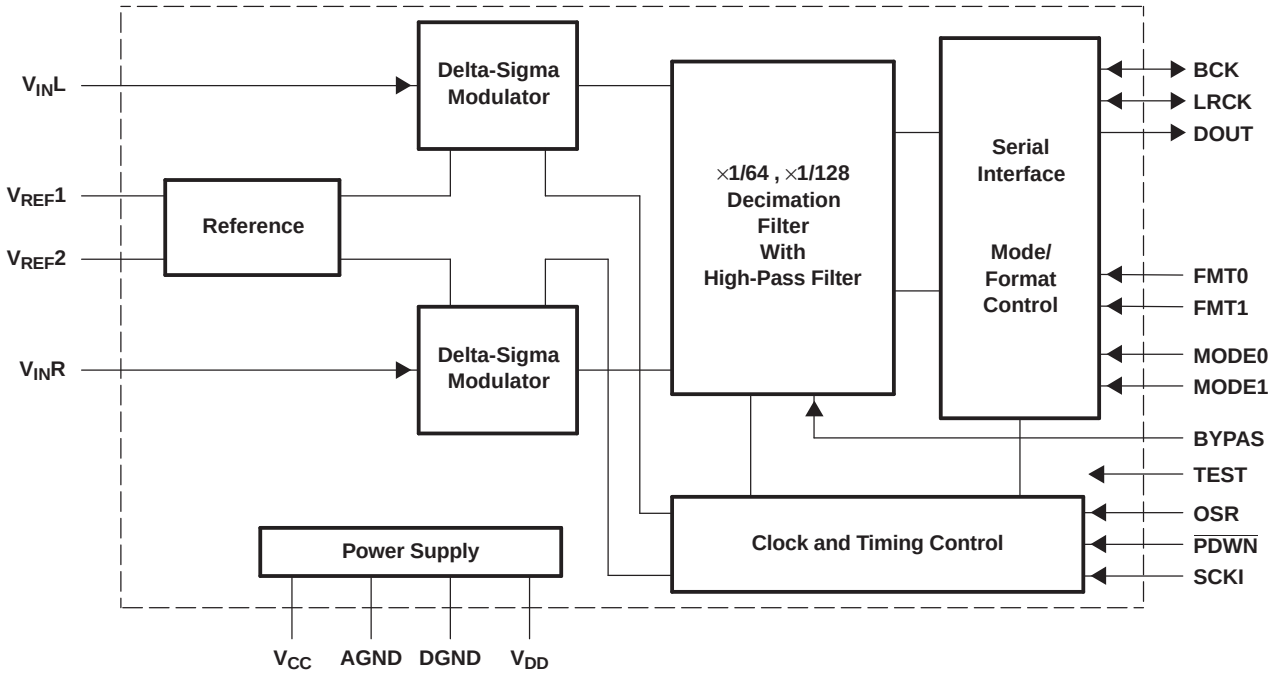
PIN ASSIGNMENTS

PCM1803A
(TOP VIEW)



P0009-03

BLOCK DIAGRAM



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DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6	–	Analog GND
BCK	11	I/O	Audio data bit clock input/output (1)
BYPAS	8	I	HPF bypass control. LOW: Normal mode (dc reject); HIGH: Bypass mode (through) (2)
DGND	13	–	Digital GND
DOUT	12	O	Audio data digital output
FMT0	17	I	Audio data format select input 0. See *Data Format* section. (2)
FMT1	18	I	Audio data format select input 1. See *Data Format* section. (2)
LRCK	10	I/O	Audio data latch enable input/output (1)
MODE0	19	I	Mode select input 0. See *Data Format* section. (2)
MODE1	20	I	Mode select input 1. See *Data Format* section. (2)
OSR	16	I	Oversampling ratio select input. LOW: ×64 f_S, HIGH: ×128 f_S (2)
$\overline{\text{PDWN}}$	7	I	Power-down control, active-low (2)
SCKI	15	I	System clock input: 256 f_S, 384 f_S, 512 f_S, or 768 f_S (3)
TEST	9	I	Test, must be connected to DGND (2)
V_{CC}	5	–	Analog power supply, 5-V
V_{DD}	14	–	Digital power supply, 3.3-V
$V_{IN}L$	1	I	Analog input, L-channel
$V_{IN}R$	2	I	Analog input, R-channel
$V_{REF}1$	3	–	Reference-voltage-1 decoupling capacitor
$V_{REF}2$	4	–	Reference-voltage-2 decoupling capacitor

(1) Schmitt-trigger input
(2) Schmitt-trigger input with internal pulldown (50 kΩ, typically), 5-V tolerant
(3) Schmitt-trigger input, 5-V tolerant

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

Supply voltage	V_{CC}	–0.3 V to 6.5 V
Supply voltage	V_{DD}	–0.3 V to 4 V
Ground voltage differences	AGND, DGND	±0.1 V
Digital input voltage, V_I	LRCK, BCK, DOUT	–0.3 V to (V_{DD} + 0.3 V) < 4 V
Digital input voltage, V_I	$\overline{\text{PDWN}}$, BYPAS, TEST, SCKI, OSR, FMT0, FMT1, MODE0, MODE1	–0.3 V to 6.5 V
Analog input voltage, V_I	$V_{IN}L$, $V_{IN}R$, $V_{REF}1$, $V_{REF}2$	–0.3 V to (V_{CC} + 0.3 V) < 6.5 V
Input current, I_I	Any pins except supplies	±10 mA
Ambient temperature under bias, T_{bias}		–40°C to 125°C
Storage temperature, T_{stg}		–55°C to 150°C
Junction temperature, T_J		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		2.7	3.3	3.6	V
Analog input voltage, full-scale (–0 dB)			3		Vp-p
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		49.152	MHz
	Sampling clock	32		96	kHz
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			Left-justified, I^2S, right-justified		
	Audio data bit length			20, 24		Bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		16	44.1	96	kHz
	System clock frequency	256 f_S	4.096	11.2896	24.576	MHz
		384 f_S	6.144	16.9344	36.864	
		512 f_S	8.192	22.5792	49.152	
		768 f_S	12.288	33.8688	–	
INPUT LOGIC						
V_{IH} (1)	Input logic-level voltage		2		V_{DD}	Vdc
V_{IL} (1)			0		0.8	
V_{IH} (2)(3)			2		5.5	
V_{IL} (2)(3)			0		0.8	
I_{IH} (1)(2)	Input logic-level current	$V_{IN} = V_{DD}$			±10	µA
I_{IL} (1)(2)		V_{IN} = 0			±10	
I_{IH} (3)		$V_{IN} = V_{DD}$		65	100	
I_{IL} (3)		V_{IN} = 0			±10	
OUTPUT LOGIC						
V_{OH} (4)	Output logic-level voltage	I_{OUT} = –4 mA	2.8			Vdc
V_{OL} (4)		I_{OUT} = 4 mA			0.5	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±2	±4	% of FSR
	Bipolar zero error	HPF bypass		±0.4		% of FSR

(1) Pins 10–11: LRCK, BCK (Schmitt-trigger input, in slave mode)
(2) Pin 15: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 7–9, 16–20: $\overline{\text{PDWN}}$, BYPAS, TEST, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(4) Pins 10–12: LRCK, BCK (in master mode), DOUT

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(5)						
THD+N	Total harmonic distortion + noise	V_{IN} = –0.5 dB, f_S = 44.1 kHz		–95	–89	dB
		V_{IN} = –0.5 dB, f_S = 96 kHz(6)		–93		
		V_{IN} = –60 dB, f_S = 44.1 kHz		–41		
		V_{IN} = –60 dB, f_S = 96 kHz(6)		–41		
	Dynamic range	f_S = 44.1 kHz, A-weighted	100	103		dB
		f_S = 96 kHz, A-weighted(6)		103		
SNR	Signal-to-noise ratio	f_S = 44.1 kHz, A-weighted	100	103		dB
		f_S = 96 kHz, A-weighted(6)		103		
	Channel separation	f_S = 44.1 kHz	95	98		dB
		f_S = 96 kHz(6)		99		
ANALOG INPUT						
V_I	Input voltage			0.6 V_{CC}		Vp-p
	Center voltage (V_{REF}1)			0.5 V_{CC}		V
	Input impedance			40		kΩ
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
t_{GD}	Group delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.019 f_S		mHz
POWER SUPPLY REQUIREMENTS						
V_{CC}	Supply voltage range		4.5	5	5.5	Vdc
V_{DD}			2.7	3.3	3.6	Vdc
I_{CC}	Supply current(7)			7.7	10	mA
		Power down(8)		5		µA
I_{DD}		f_S = 44.1 kHz		6.5	9	mA
		f_S = 96 kHz (6)		11.7		mA
		Power down(8)		1		µA
	Power dissipation	f_S = 44.1 kHz		60	80	mW
		f_S = 96 kHz (6)		77		mW
		Power down(8)		28		µW
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		85	°C
θ_{JA}	Thermal resistance	20-pin SSOP		115		°C/W

(5) Analog performance specifications are tested using the System Two™ audio measurement system by Audio Precision™, using 400-Hz HPF, 20-kHz LPF in rms mode.
(6) f_S = 96 kHz, system clock = 256 f_S, oversampling ratio = ×64.
(7) Minimum load on DOUT (pin 12), BCK (pin 11), LRCK (pin 10)
(8) Halt SCKI, BCK, LRCK

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

Decimation Filter Frequency Response

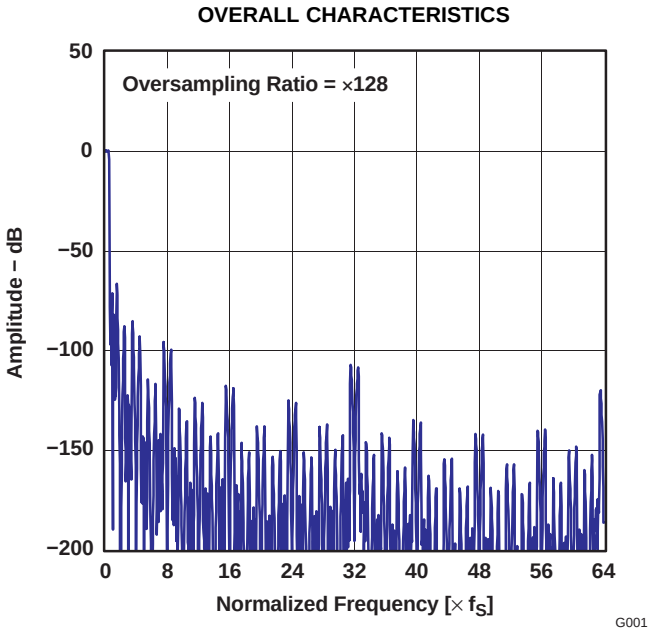


Figure 1.

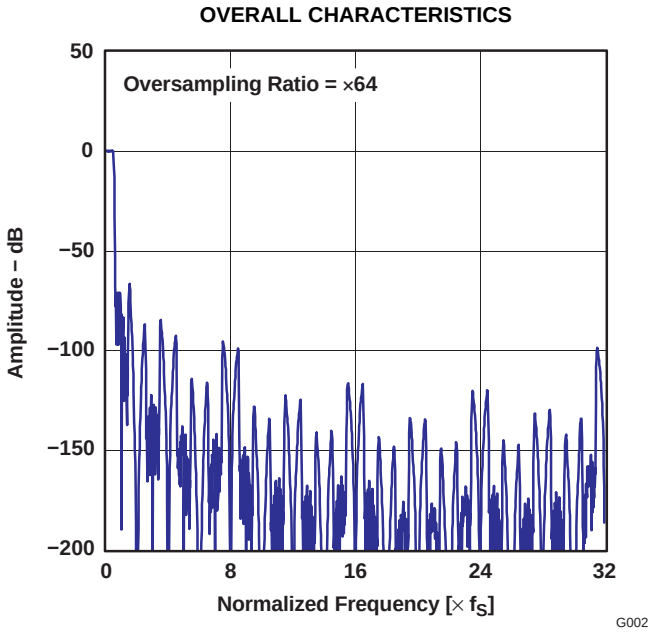


Figure 2.

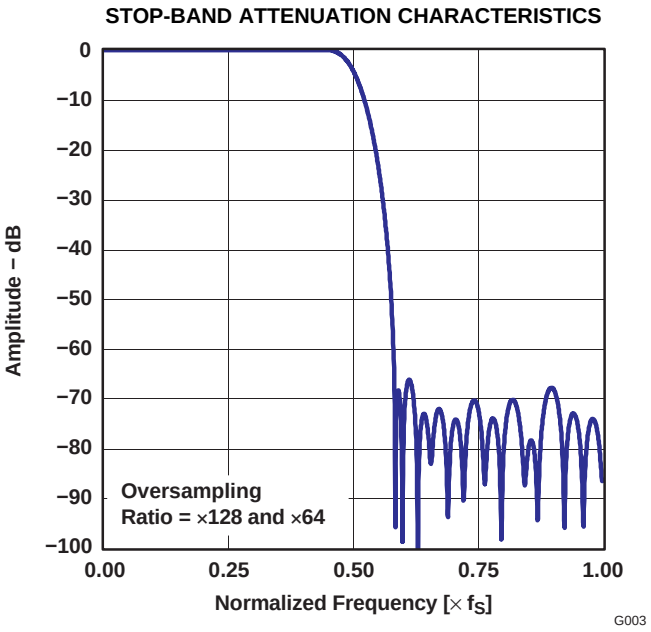


Figure 3.

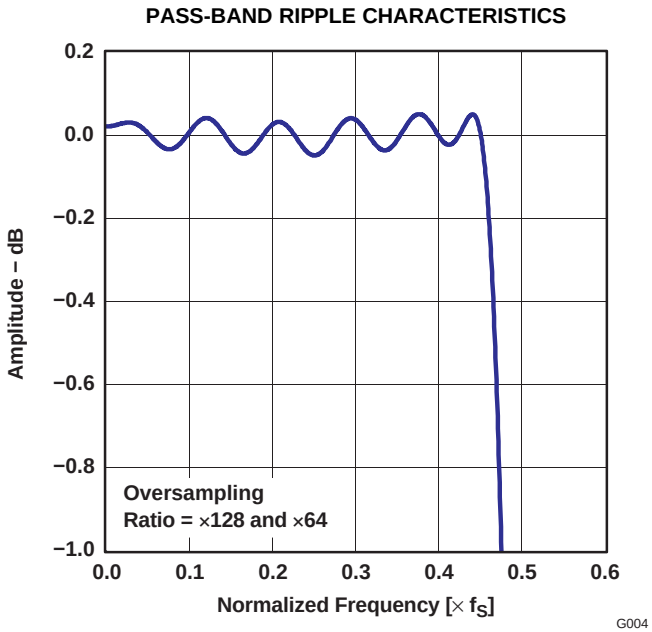


Figure 4.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

LOW-CUT FILTER FREQUENCY RESPONSE

HPF STOP-BAND CHARACTERISTICS

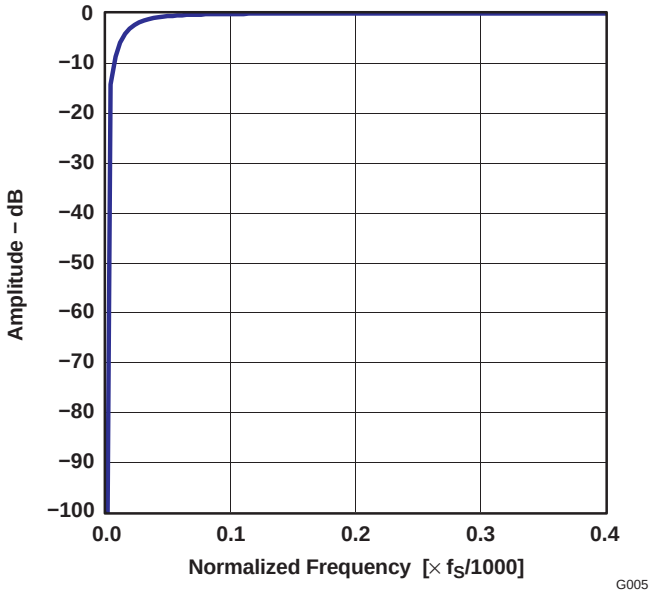


Figure 5.

HPF PASS-BAND CHARACTERISTICS

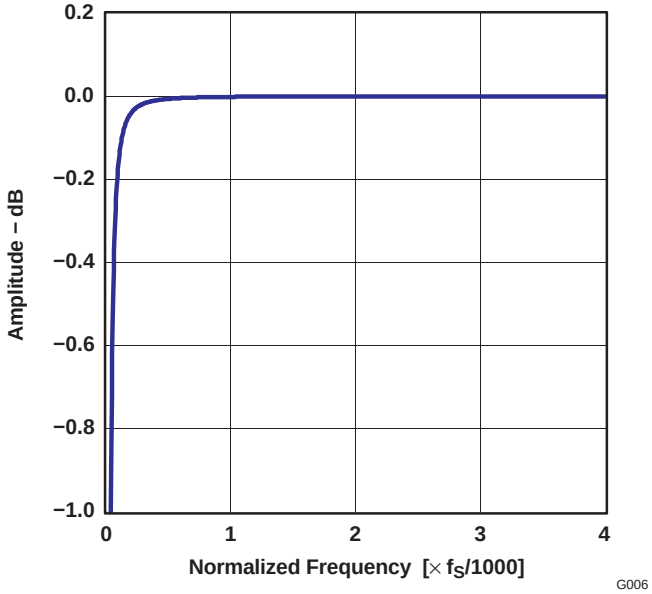


Figure 6.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE

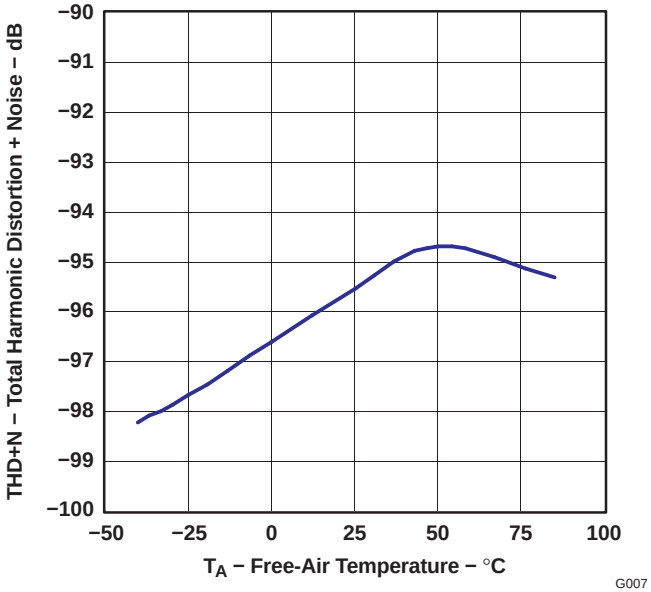


Figure 7.

DYNAMIC RANGE and SIGNAL-TO-NOISE RATIO vs TEMPERATURE

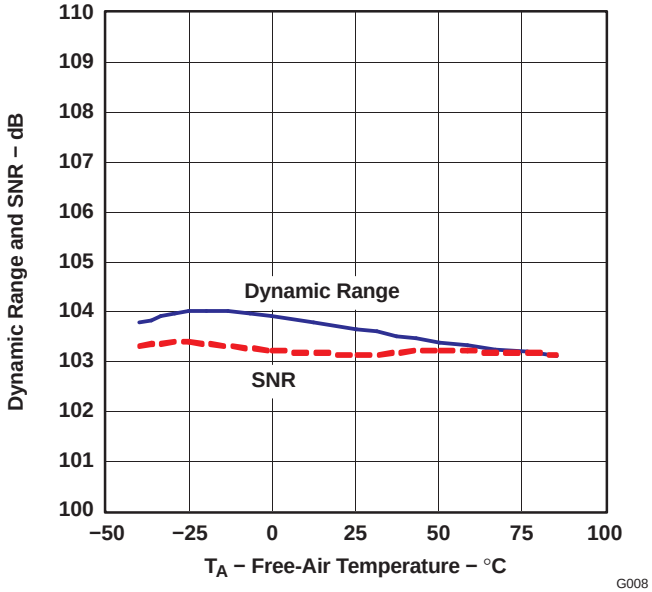


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

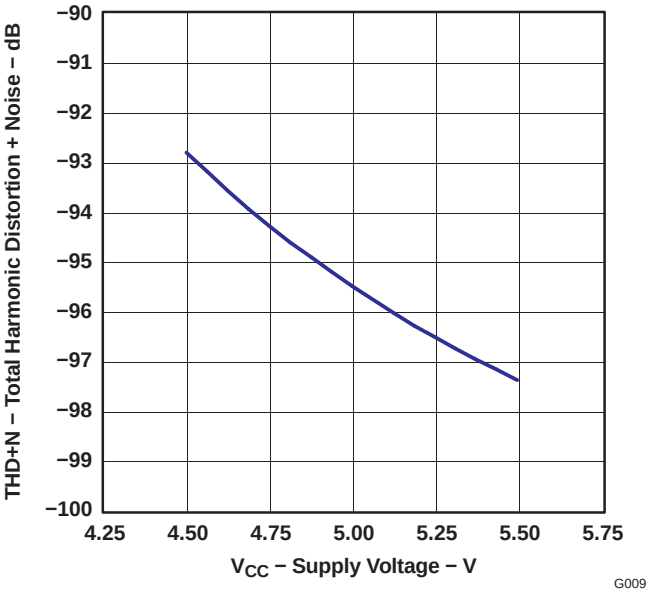


Figure 9.

DYNAMIC RANGE and SIGNAL-TO-NOISE RATIO vs SUPPLY VOLTAGE

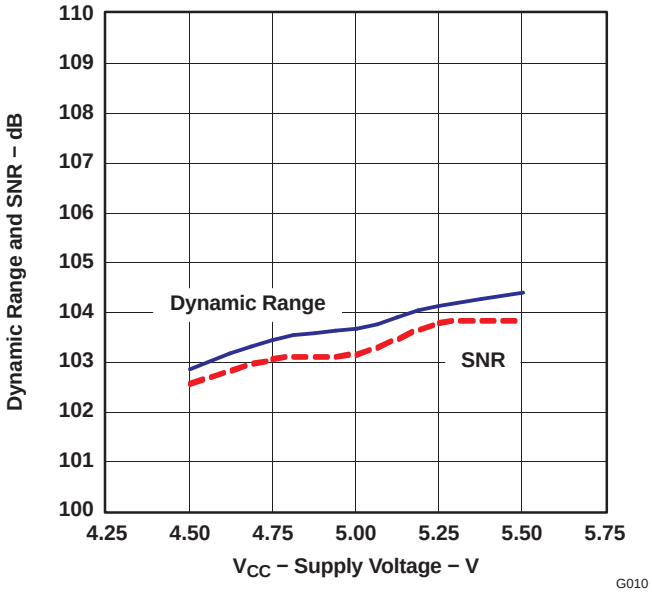


Figure 10.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

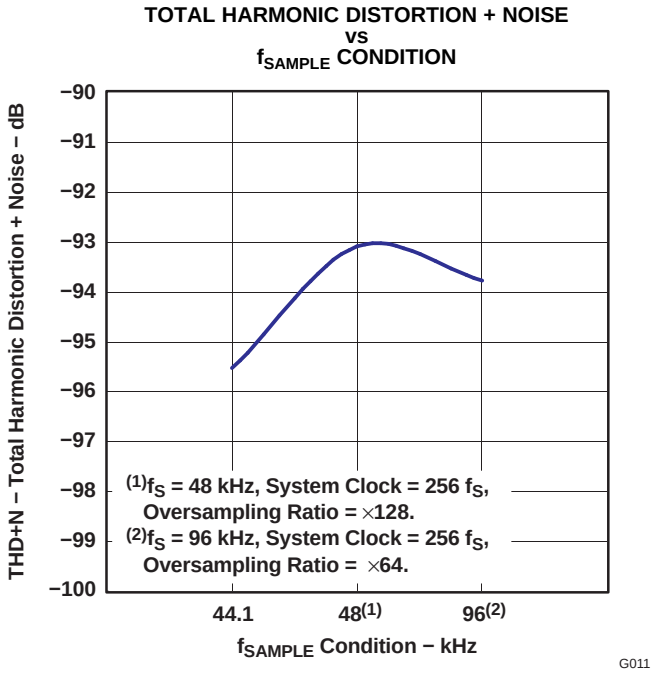


Figure 11.

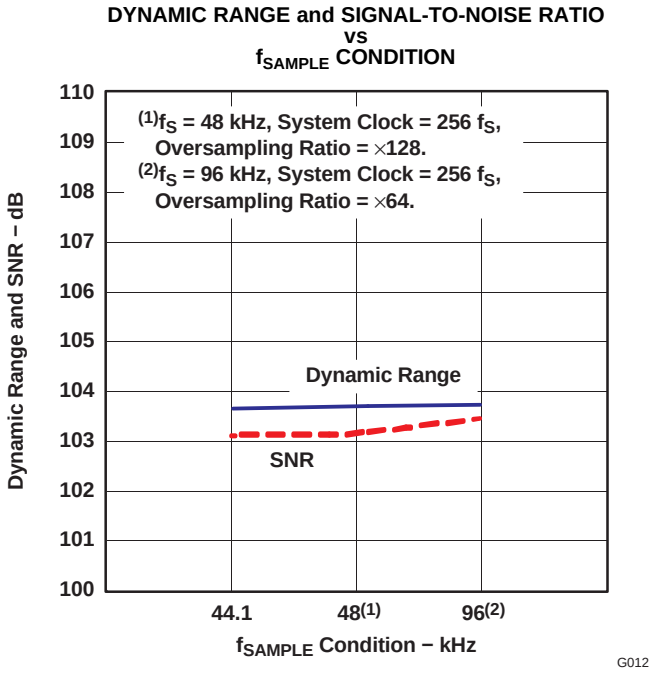


Figure 12.

OUTPUT SPECTRUM

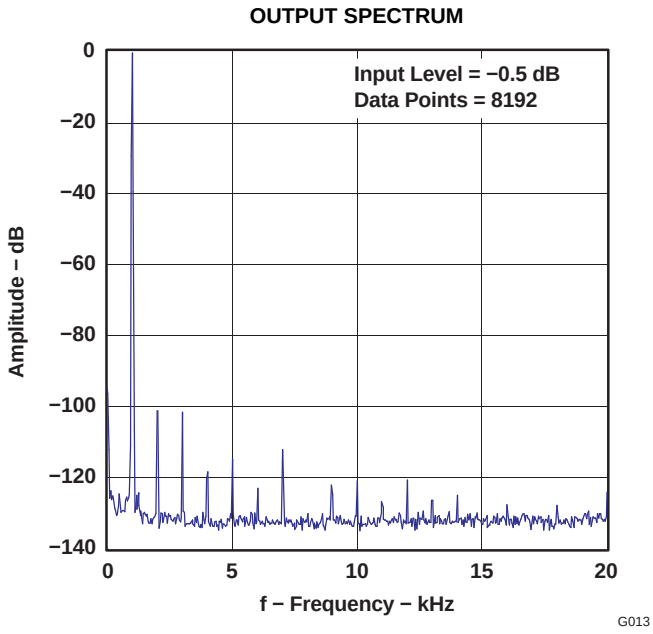


Figure 13.

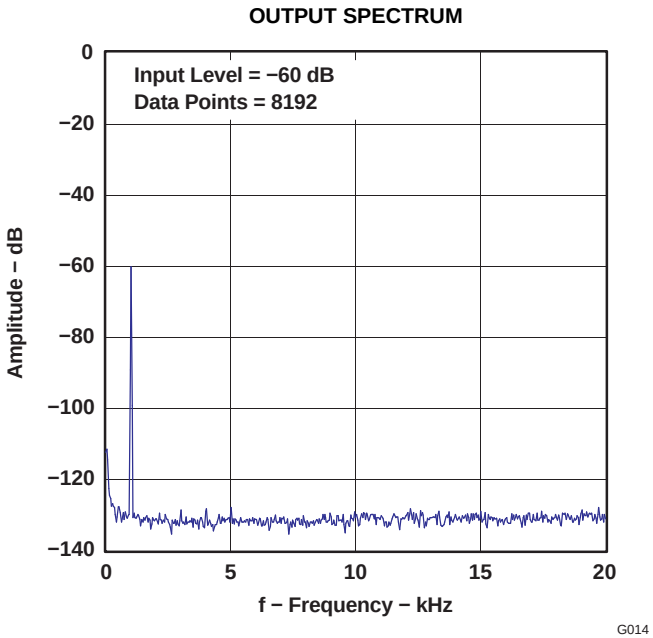


Figure 14.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

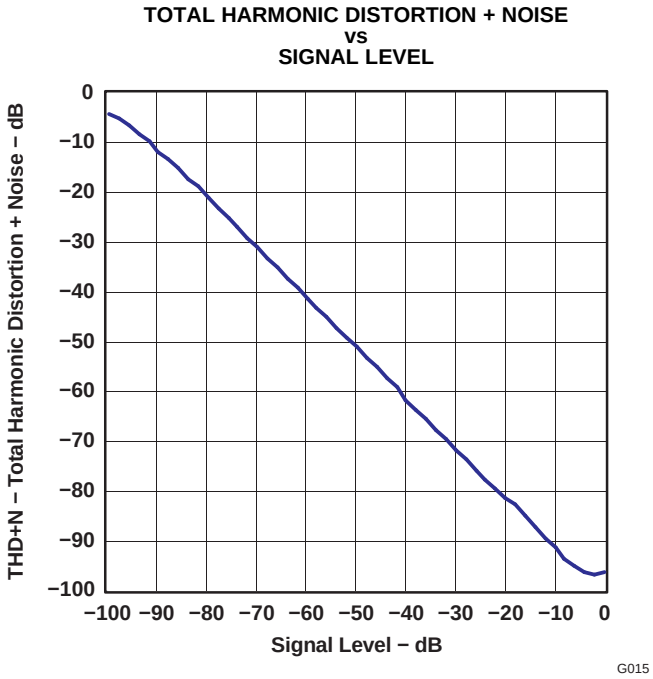


Figure 15.

SUPPLY CURRENT

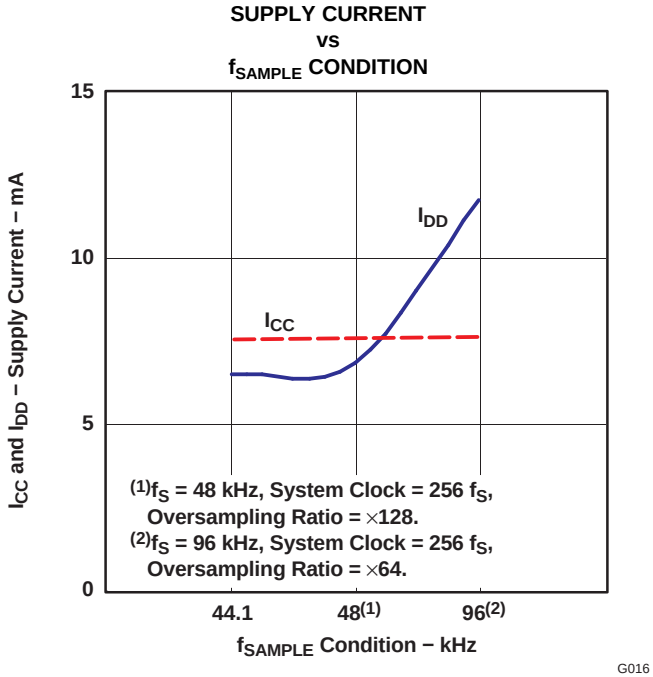


Figure 16.

DEVICE INFORMATION

SYSTEM CLOCK

The PCM1803A supports 256 f_S, 384 f_S, 512 f_S, and 768 f_S as the system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 15).

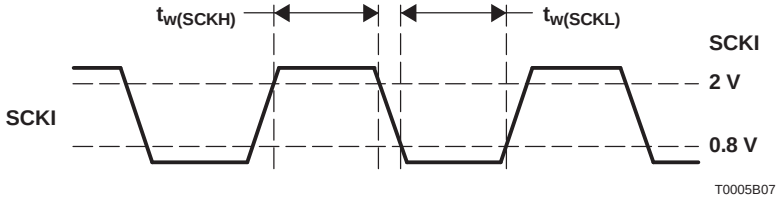
The PCM1803A has a system clock-detection circuit that automatically senses if the system clock is operating at 256 f_S, 384 f_S, 512 f_S, or 768 f_S in slave mode. In master mode, the system clock frequency must be selected by MODE0 (pin 19) and MODE1 (pin 20), and 768 f_S is not available. The system clock is divided automatically into 128 f_S and 64 f_S, and these frequencies are used to operate the digital filter and the delta-sigma modulator.

Table 1 shows the relationship of typical sampling frequency and system clock frequency, and Figure 17 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)			
	256 f_S	384 f_S	512 f_S	768 f_S (1)
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640
64	16.3840	24.5760	32.7680	49.1520
88.2	22.5792	33.8688	45.1584	–
96	24.5760	36.8640	49.1520	–

(1) Slave mode only



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	8		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	8		ns

Figure 17. System Clock Timing

POWER-ON-RESET SEQUENCE

The PCM1803A has an internal power-on-reset circuit, and initialization (reset) is performed automatically at the time when power-supply voltage (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical) and for 1024 system clock cycles after V_{DD} > 2.2 V (typical), the PCM1803A stays in the reset state, and the digital output is forced to zero. The digital output becomes valid when a time period of 4480/f_S has elapsed following release from the reset state. Figure 18 illustrates the internal power-on-reset timing and the digital output for power-on reset.

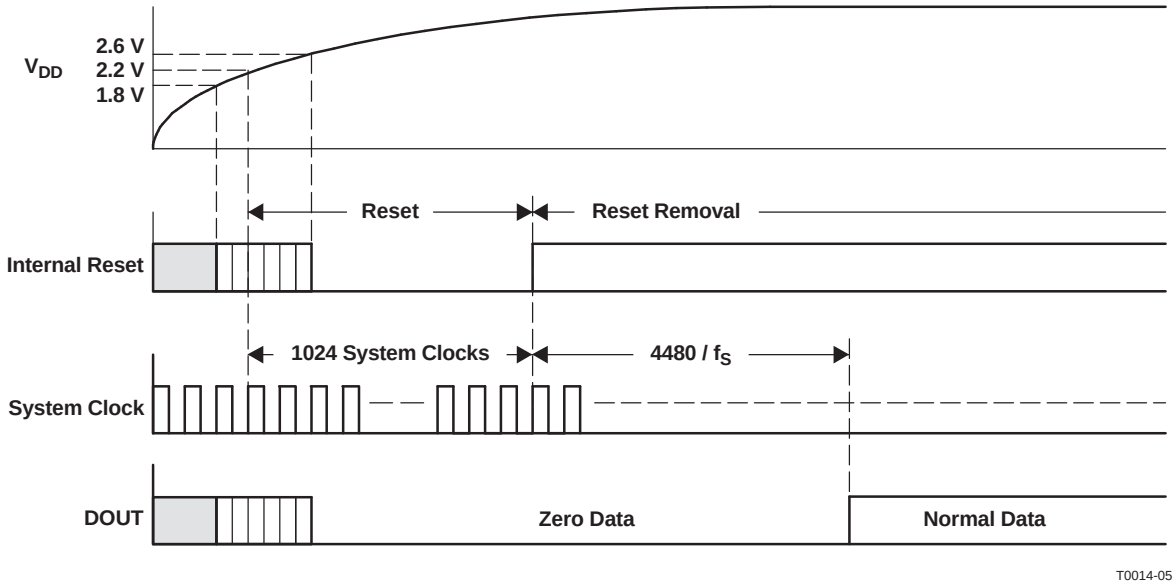


Figure 18. Internal Power-On-Reset Timing

SERIAL AUDIO DATA INTERFACE

The PCM1803A interfaces the audio system through BCK (pin 11), LRCK (pin 10), and DOUT (pin 12).

INTERFACE MODE

The PCM1803A supports master mode and slave mode as interface modes, and they are selected by MODE1 (pin 20) and MODE0 (pin 19) as shown in Table 2.

In master mode, the PCM1803A provides the timing of serial audio data communications between the PCM1803A and the digital audio processor or external circuit. While in slave mode, the PCM1803A receives the timing for data transfers from an external controller.

Table 2. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S, 768 f_S)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

Master Mode

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing, which is generated in the clock circuit of the PCM1803A. The frequency of BCK is fixed at LRCK × 64. The 768-f_S system clock is not available in master mode.

Slave Mode

In slave mode, BCK and LRCK work as input pins. The PCM1803A accepts the 64-BCK/LRCK or 48-BCK/LRCK format (only for 384 f_S and 768 f_S system clocks), not the 32-BCK/LRCK format.

DATA FORMAT

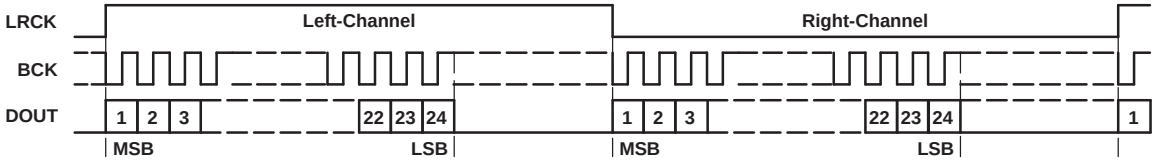
The PCM1803A supports four audio data formats in both master and slave modes, and the data formats are selected by FMT1 (pin 18) and FMT0 (pin 17) as shown in Table 3. Figure 19 illustrates the data formats in slave and master modes.

Table 3. Data Formats

FORMAT	FMT1	FMT0	DESCRIPTION
0	0	0	Left-justified, 24-bit
1	0	1	I²S, 24-bit
2	1	0	Right-justified, 24-bit
3	1	1	Right-justified, 20-bit

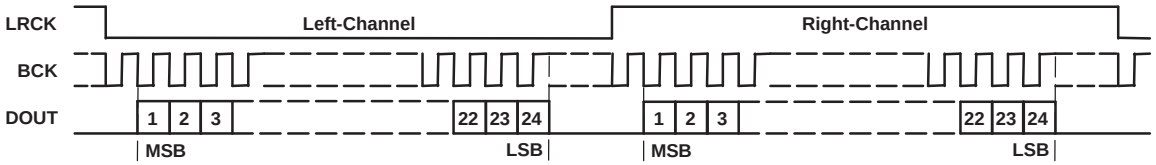
FORMAT 0: FMT[1:0] = 00

24-Bit, MSB-First, Left-Justified



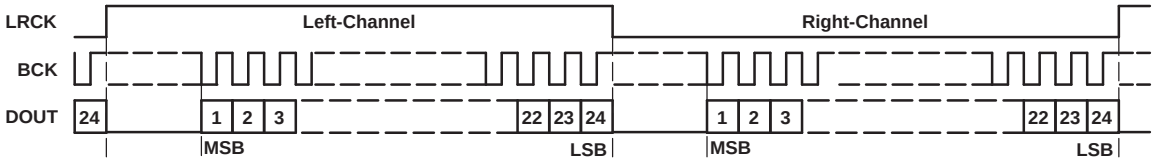
FORMAT 1: FMT[1:0] = 01

24-Bit, MSB-First, I²S



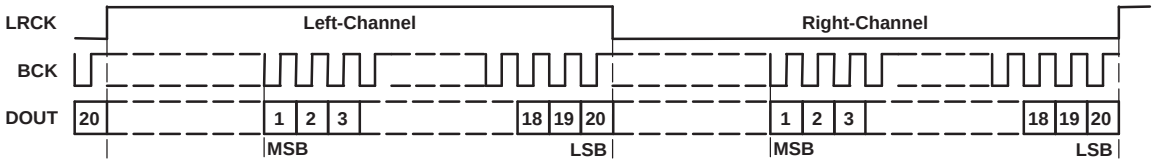
FORMAT 2: FMT[1:0] = 10

24-Bit, MSB-First, Right-Justified



FORMAT 3: FMT[1:0] = 11

20-Bit, MSB-First, Right-Justified

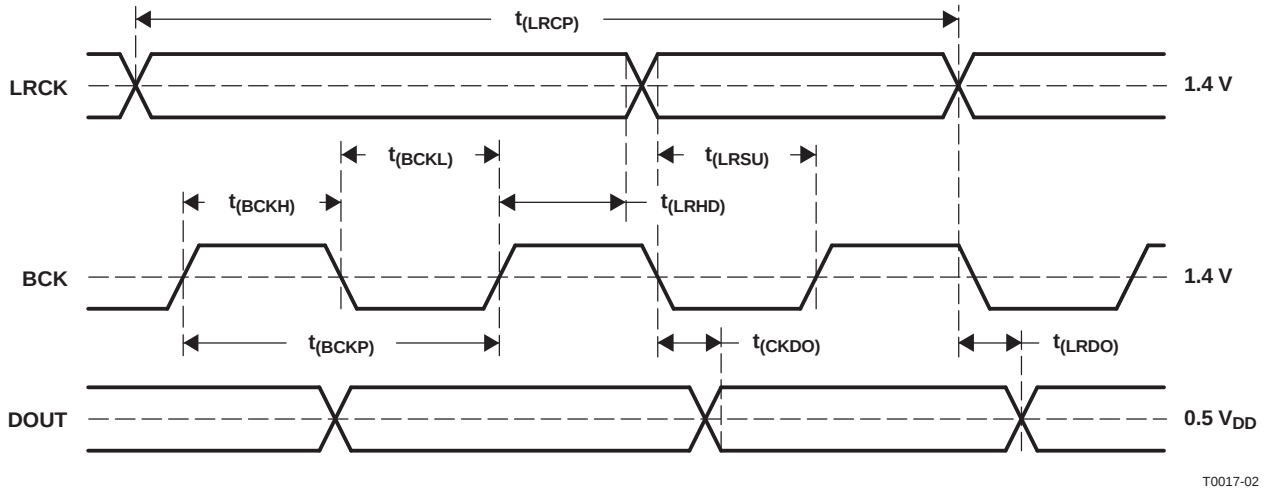


T0016-11

Figure 19. Audio Data Formats (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

INTERFACE TIMING

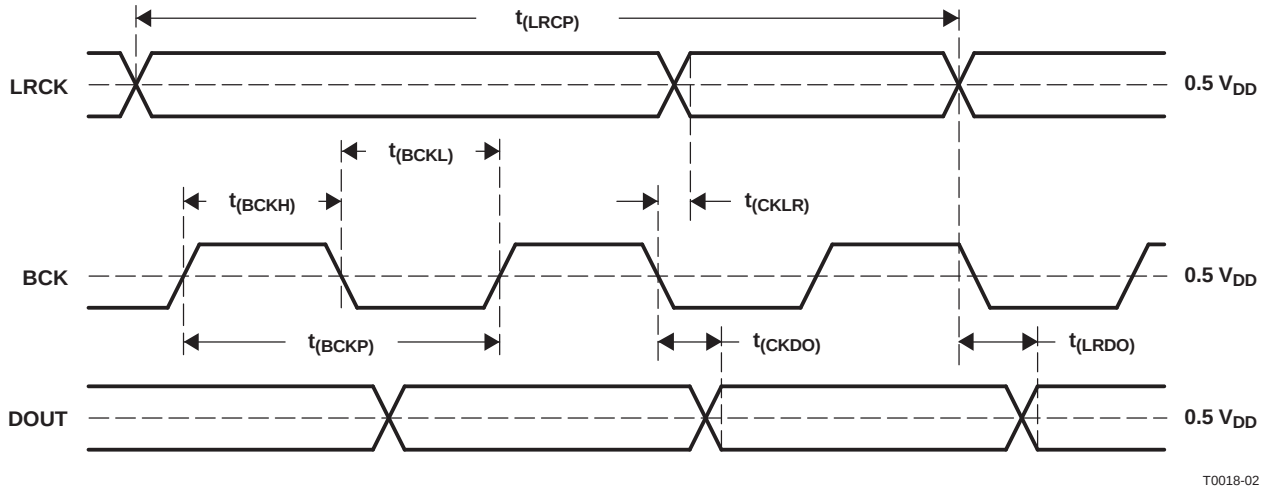
Figure 20 illustrates the interface timing in slave mode; Figure 21 and Figure 22 illustrate the interface timing in master mode.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	1/(64 f_S)			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	1.5 × $t_{(SCKI)}$			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	1.5 × $t_{(SCKI)}$			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	40			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	20			ns
$t_{(LRCP)}$	LRCK period	10			µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		40	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		40	ns
t_r	Rising time of all signals			20	ns
t_f	Falling time of all signals			20	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ means SCKI period time.

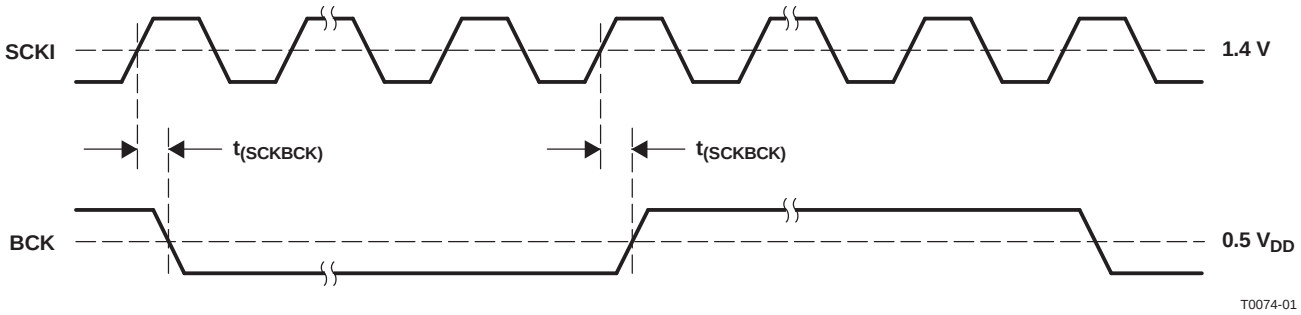
Figure 20. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1/(64 f_S)	1000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	65		600	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	65		600	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1/f_S	65	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rising time of all signals			20	ns
t_f	Falling time of all signals			20	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of all signals is 20 pF.

Figure 21. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(SCKBCK)}$	Delay time, SCKI rising edge to BCK edge	5		30	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of BCK is 20 pF.

Figure 22. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1803A operates under LRCK, synchronized with system clock SCKI. The PCM1803A does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$, and digital output is forced to zero data (BPZ code) until resynchronization between LRCK and SCKI occurs.

In case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur and the previously explained digital output control and discontinuity do not occur.

Figure 23 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1803A can generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a discontinuity in the data of the digital output, which can generate some noise in the audio signal.

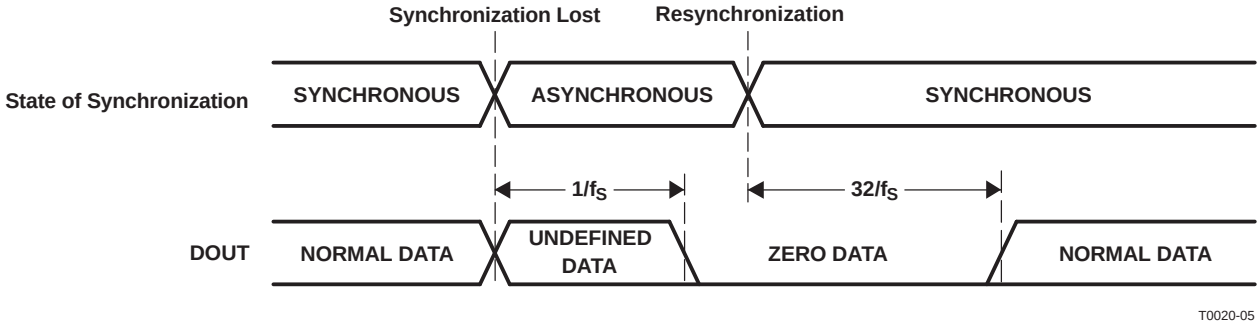


Figure 23. ADC Digital Output for Loss of Synchronization and Resynchronization

POWER DOWN

$\overline{\text{PDWN}}$ (pin 7) controls operation of the entire ADC. During power-down mode, supply current for the analog portion is shut down and the digital portion is reset; also, DOUT (pin 12) is disabled. It is acceptable to halt the system clock during power-down mode so that power dissipation is minimized. The minimum LOW pulse duration on the $\overline{\text{PDWN}}$ pin is 100 ns.

It is recommended to set $\overline{\text{PWDN}}$ (pin 7) to LOW once to obtain stable analog performance when the sampling rate, interface mode, data format, or oversampling control is changed.

Table 4. Power-Down Control

$\overline{\text{PWDN}}$	Power-Down Mode
LOW	Power-down mode
HIGH	Normal operation mode

HPF BYPASS

The built-in function for dc-component rejection can be bypassed by BYPAS (pin 8) control. In bypass mode, the dc component of the input analog signal, internal dc offset, etc., also are converted and included in the digital output data.

Table 5. HPF Bypass Control

BYPAS	HPF (High-Pass Filter) Mode
LOW	Normal (no dc component in DOUT) mode
HIGH	Bypass (dc component in DOUT) mode

OVERSAMPLING RATIO CONTROL

OSR (pin 16) controls the oversampling ratio of the delta-sigma modulator, ×64 or ×128. The ×128 mode is available for $f_S \leq 48$ kHz.

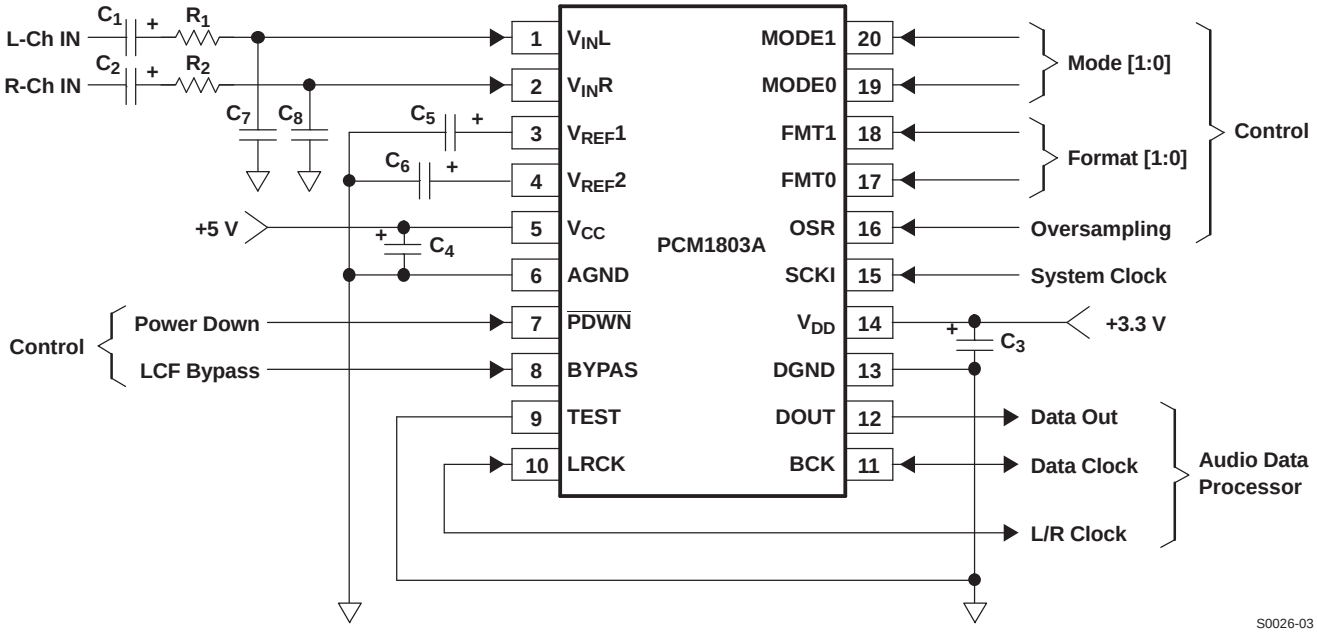
Table 6. Oversampling Control

OSR	Oversampling Ratio
LOW	×64
HIGH	×128 ($f_S \leq 48$ kHz)

APPLICATION INFORMATION

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 24 illustrates a typical circuit connection diagram where the cutoff frequency of the input HPF is about 160 kHz.



NOTES:

A. C_1, C_2: A 1-µF electrolytic capacitor gives a 4-Hz (τ = 1 µF × 40 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 40-ms time constant during the power-on initialization period.

B. C_3, C_4: Bypass capacitors are 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply.

C. C_5, C_6: Recommended capacitors are 0.1-µF ceramic and 10-µF electrolytic.

D. C_7, C_8, R_1, R_2: A 0.01-µF film-type capacitor and 100-Ω resistor give a 160-kHz (τ = 0.01 µF × 100 Ω) cutoff frequency for the anti-aliasing filter in normal operation.

Figure 24. Typical Application Diagram

APPLICATION INFORMATION (continued)

BOARD DESIGN and LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} Pins

The digital and analog power-supply lines to the PCM1803A should be bypassed to the corresponding ground pins with 0.1-µF ceramic and 10-µF electrolytic capacitors, as close to the pins as possible, to maximize the dynamic performance of the ADC.

AGND, DGND Pins

To maximize the dynamic performance of the PCM1803A, the analog and digital grounds are not connected internally. These grounds should have low impedance to avoid digital noise feeding back into the analog ground. Therefore, they should be connected directly to each other under the part to reduce potential noise problems.

V_{IN}L, V_{IN}R Pins

The V_{IN}L and V_{IN}R pins need a simple external RC filter (f_C = 160 kHz) as an antialiasing filter to remove out-of-band noise from the audio band. If the input signal includes noise with a frequency near the oversampling frequency (64 f_S or 128 f_S), the noise is folded into the baseband (audio band) signal through A-to-D conversion. The recommended R value is 100 Ω. Film-type capacitors of 0.01-µF should be located as close as possible to the V_{IN}L and V_{IN}R pins and should be terminated to GND as close as possible to the AGND pin to maximize the dynamic performance of ADC, by suppressing kickback noise from the PCM1803A.

V_{REF}1 Pin

A 0.1-µF ceramic capacitor and 10-µF electrolytic capacitor are recommended between V_{REF}1 and AGND to ensure low source impedance of the ADC references. These capacitors should be located as close as possible to the V_{REF}1 pin to reduce dynamic errors on the ADC reference.

V_{REF}2 Pin

The differential voltage between V_{REF}2 and AGND sets the analog input full-scale range. A 0.1-µF ceramic capacitor and 10-µF electrolytic capacitor are recommended between V_{REF}2 and AGND. These capacitors should be located as close as possible to the V_{REF}2 pin to reduce dynamic errors on the ADC reference.

DOUT Pin

The DOUT pin has enough load drive capability, but if the DOUT line is long, locating a buffer near the PCM1803A and minimizing load capacitance is recommended to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

System Clock

The quality of the system clock can influence the dynamic performance, because the PCM1803A operates based on a system clock. Therefore, it may be required to consider the system-clock duty, jitter, and the time difference between system-clock transition and BCK or LRCK transition in the slave mode.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM1803ADB	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1803ADBG4	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1803ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM1803ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

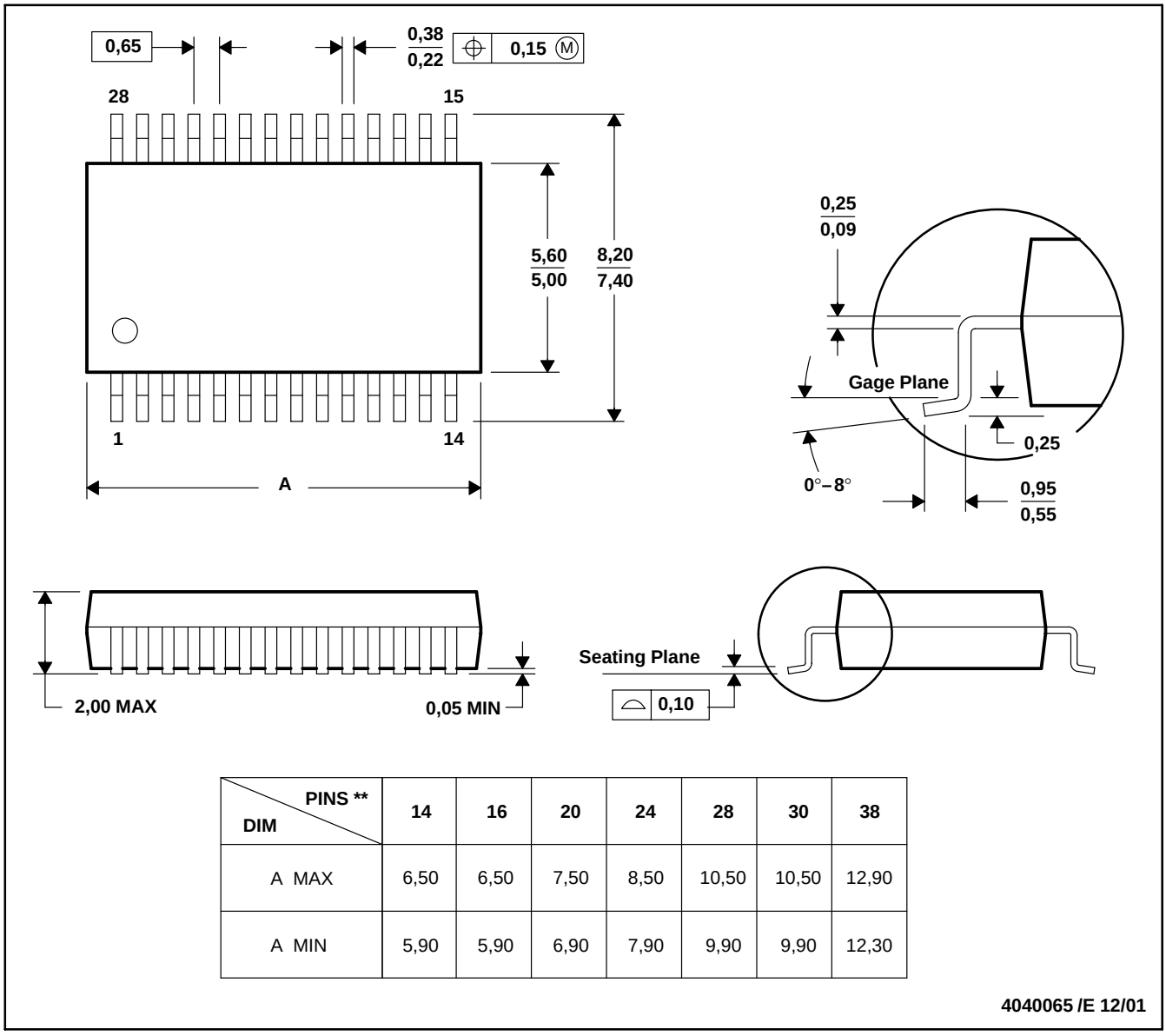
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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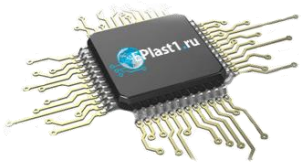

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