

**FDD306P****P-Channel 1.8V Specified PowerTrench® MOSFET****Features**

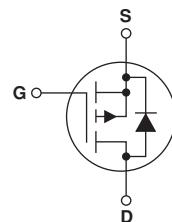
- -6.7 A, -12 V.  $R_{DS(ON)} = 28 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 41 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$   
 $R_{DS(ON)} = 90 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability

**Applications**

- DC/DC converter

**General Description**

This P-Channel 1.8V Specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management.

**Absolute Maximum Ratings**  $T_A=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-12	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current – Continuous	(Note 3)	A
	– Pulsed	(Note 1a)	
$P_D$	Power Dissipation for Single Operation	(Note 1)	W
		(Note 1a)	
		(Note 1b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$
Thermal Characteristics			
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	$^\circ\text{C/W}$

**Package Marking and Ordering Information**

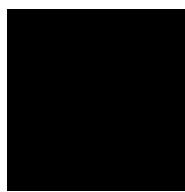
Device Marking	Device	Reel Size	Tape width	Quantity
FDD306P	FDD306P	13"	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain–Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_D = -250 \mu\text{A}$	-12			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.6		$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = -10 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$			-1	$\mu\text{A}$
$I_{\text{GSSF}}$	Gate–Body Leakage	$V_{\text{GS}} = \pm 8 \text{ V}$ , $V_{\text{DS}} = 0 \text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = -250 \mu\text{A}$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{\text{GS}(\text{th})}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$		2.2		$\text{mV}/^\circ\text{C}$
$R_{\text{DS}(\text{on})}$	Static Drain–Source On–Resistance	$V_{\text{GS}} = -4.5 \text{ V}$ , $I_D = -6.7 \text{ A}$ $V_{\text{GS}} = -2.5 \text{ V}$ , $I_D = -6.1 \text{ A}$ $V_{\text{GS}} = -1.8 \text{ V}$ , $I_D = -4.8 \text{ A}$ $V_{\text{GS}} = -4.5 \text{ V}$ , $I_D = -6.7 \text{ A}$ , $T_J = 125^\circ\text{C}$	21 29 42 25	28 41 90		$\text{m}\Omega$
$I_{\text{D}(\text{on})}$	On–State Drain Current	$V_{\text{GS}} = -4.5 \text{ V}$ , $V_{\text{DS}} = -5 \text{ V}$	-45			A
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = -5 \text{ V}$ , $I_D = -6.7 \text{ A}$		22		S
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = -6 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$		1290		pF
$C_{\text{oss}}$	Output Capacitance			590		pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			430		pF
$R_G$	Gate Resistance	$V_{\text{GS}} = 15 \text{ mV}$ , $f = 1.0 \text{ MHz}$		4.2		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{\text{d}(\text{on})}$	Turn–On Delay Time	$V_{\text{DD}} = -6 \text{ V}$ , $I_D = -1 \text{ A}$ , $V_{\text{GS}} = -4.5 \text{ V}$ , $R_{\text{GEN}} = 6 \Omega$		16	29	ns
$t_r$	Turn–On Rise Time			8	16	ns
$t_{\text{d}(\text{off})}$	Turn–Off Delay Time			34	54	ns
$t_f$	Turn–Off Fall Time			41	65	ns
$Q_g$	Total Gate Charge	$V_{\text{DS}} = -6 \text{ V}$ , $I_D = -6.7 \text{ A}$ , $V_{\text{GS}} = -4.5 \text{ V}$		15	21	nC
$Q_{\text{gs}}$	Gate–Source Charge			2.0		nC
$Q_{\text{gd}}$	Gate–Drain Charge			4.4		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-3.2	A
$V_{\text{SD}}$	Drain–Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_S = -3.2 \text{ A}$ (Note 2)		-0.8	-1.2	V
$\text{Trr}$	Diode Reverse Recovery Time	$\text{IF} = -6.7 \text{ A}$ , $d\text{IF}/dt = 100 \text{ A}/\mu\text{s}$ (Note 3)		37		ns
$\text{Irm}$	Diode Reverse Recovery Current			0.9		A
$\text{Qrr}$	Diode Reverse Recovery Charge			17		nC

**Notes:**

1.  $R_{\thetaJA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  
 $R_{\thetaJC}$  is guaranteed by design while  $R_{\thetaCA}$  is determined by the user's board design.



a)  $R_{\thetaJA} = 40^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $R_{\thetaJA} = 96^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

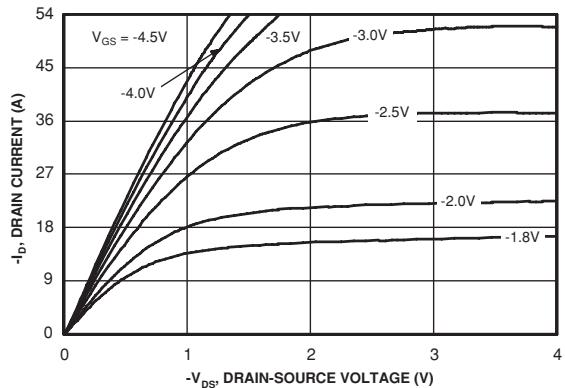
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

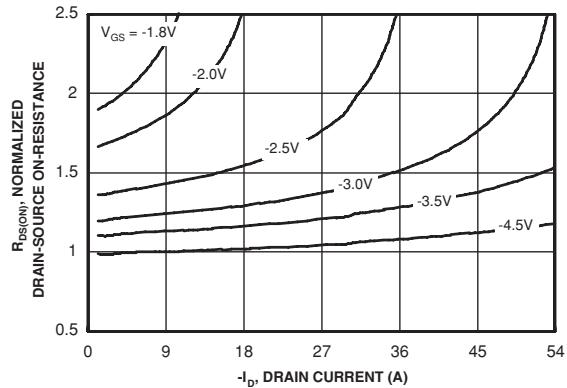
3. Maximum current is calculated as:  $\sqrt{\frac{P_D}{R_{\text{DS}(\text{ON})}}}$  where  $P_D$  is maximum power dissipation at  $T_C = 25^\circ\text{C}$  and  $R_{\text{DS}(\text{ON})}$  is at  $T_{J(\text{max})}$  and  $V_{\text{GS}} = 10 \text{ V}$ .

4. Starting  $T_J = 25^\circ\text{C}$ ,  $L = \text{TBD}$ ,  $I_{AS} = -6.7 \text{ A}$

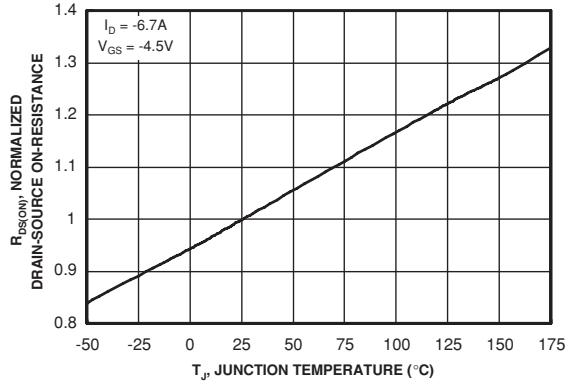
## Typical Characteristics



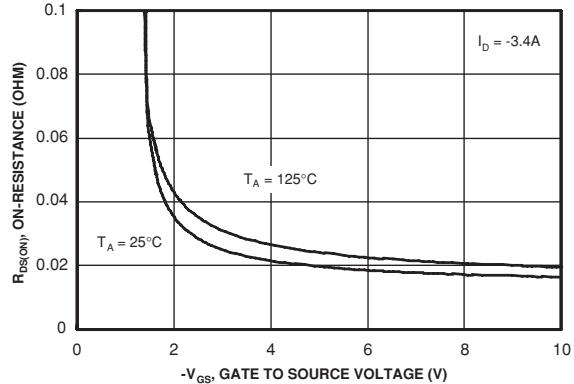
**Figure 1. On-Region Characteristics.**



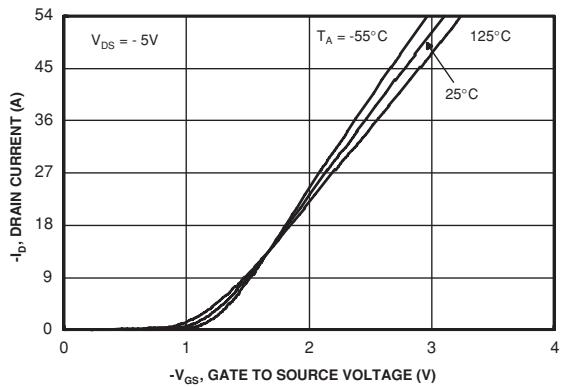
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



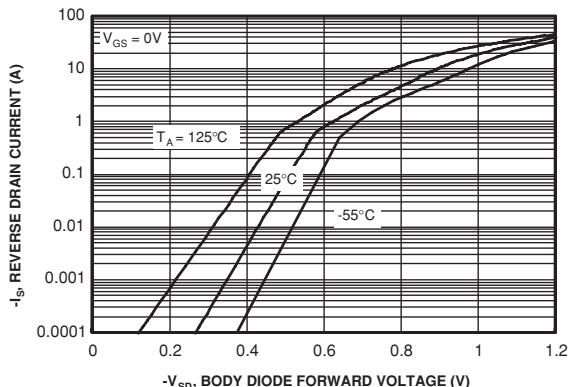
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**



**Figure 5. Transfer Characteristics.**



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

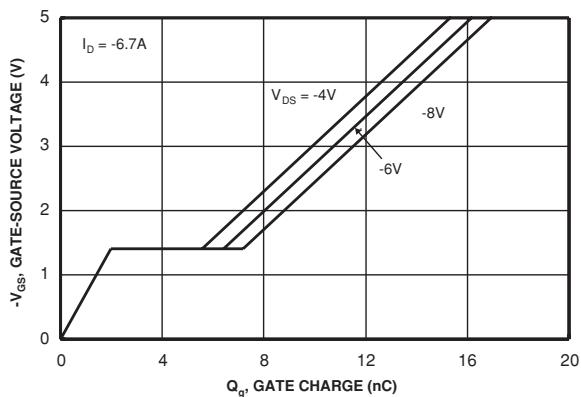


Figure 7. Gate Charge Characteristics.

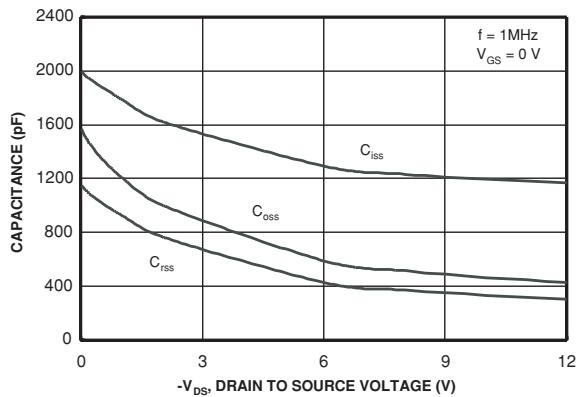


Figure 8. Capacitance Characteristics.

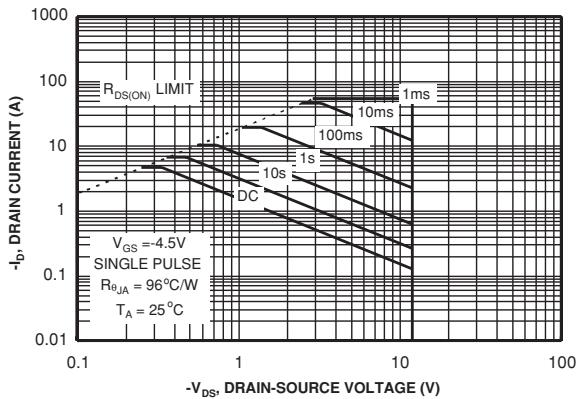


Figure 9. Maximum Safe Operating Area.

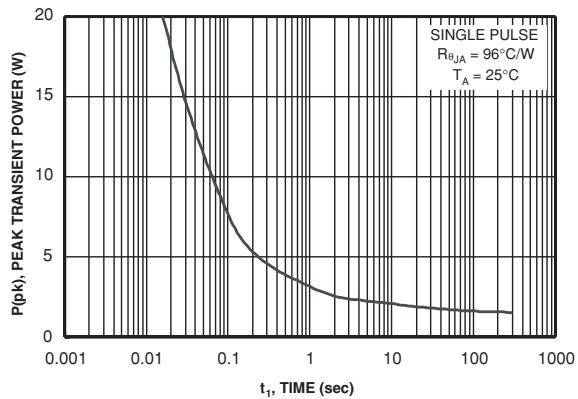


Figure 10. Single Pulse Maximum Power Dissipation.

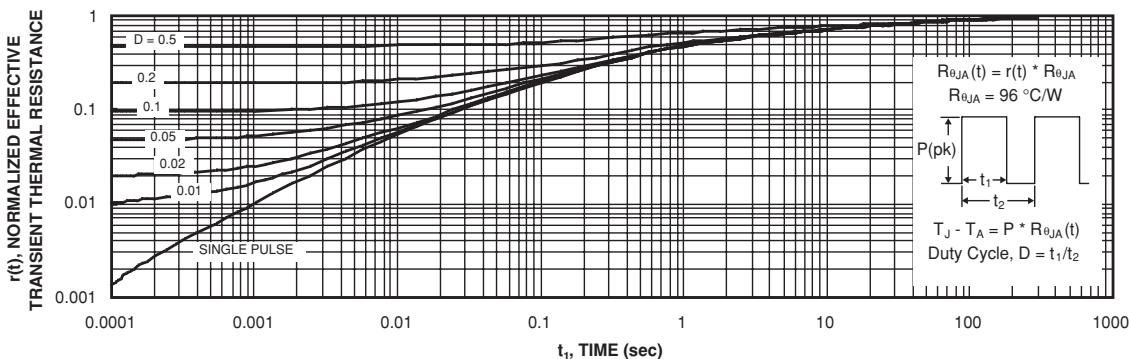


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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Rev. I15



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#### Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: [org@eplast1.ru](mailto:org@eplast1.ru)

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.