

# TL431, A, B Series, NCV431A, B

## Programmable Precision References

The TL431, A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from  $V_{ref}$  to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22  $\Omega$ . The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

### Features

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance:  $\pm 0.4\%$ , Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22  $\Omega$  Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- These are Pb-Free and Halide-Free Devices



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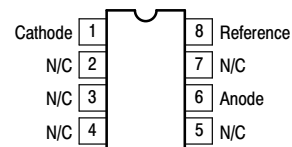
Pin 1. Reference  
2. Anode  
3. Cathode

**TO-92 (TO-226)  
LP SUFFIX  
CASE 29**



**PDIP-8  
P SUFFIX  
CASE 626**

**Micro8™  
DM SUFFIX  
CASE 846A**



(Top View)



**SOIC-8  
D SUFFIX  
CASE 751**



(Top View)

This is an internally modified SOIC-8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification increases power dissipation capability when appropriately mounted on a printed circuit board. This modified package conforms to all external dimensions of the standard SOIC-8 package.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 14 of this data sheet.

# TL431, A, B Series, NCV431A, B

## Symbol



## Representative Schematic Diagram

Component values are nominal



## Representative Block Diagram



This device contains 12 active transistors.

### MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	$V_{KA}$	37	V
Cathode Current Range, Continuous	$I_K$	-100 to +150	mA
Reference Input Current Range, Continuous	$I_{ref}$	-0.05 to +10	mA
Operating Junction Temperature	$T_J$	150	°C
Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC NCV431AI, NCV431B, TL431BV	$T_A$	-40 to +85 0 to +70 -40 to +125	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package	$P_D$	0.70 1.10 0.52	W
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package	$P_D$	1.5 3.0	W
ESD Rating	HBM MM	>2000 >200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	$V_{KA}$	$V_{ref}$	36	V
Cathode Current	$I_K$	1.0	100	mA

### THERMAL CHARACTERISTICS

Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83	41	-	°C/W

# TL431, A, B Series, NCV431A, B

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> (Note 1)	V <sub>ref</sub>	2.44 2.41	2.495 -	2.55 2.58	2.44 2.423	2.495 -	2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA	ΔV <sub>ref</sub>	-	7.0	30	-	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I <sub>K</sub> = 10 mA (Figure 2), ΔV <sub>KA</sub> = 10 V to V <sub>ref</sub> ΔV <sub>KA</sub> = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	- -	-1.4 -1.0	-2.7 -2.0	- -	-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current (Figure 2) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞ T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> (Note 1)	I <sub>ref</sub>	- -	1.8 -	4.0 6.5	- -	1.8 -	4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞	ΔI <sub>ref</sub>	-	0.8	2.5	-	0.4	1.2	μA
Minimum Cathode Current For Regulation V <sub>KA</sub> = V <sub>ref</sub> (Figure 1)	I <sub>min</sub>	-	0.5	1.0	-	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V <sub>KA</sub> = 36 V, V <sub>ref</sub> = 0 V	I <sub>off</sub>	-	20	1000	-	20	1000	nA
Dynamic Impedance (Figure 1, Note 3) V <sub>KA</sub> = V <sub>ref</sub> , ΔI <sub>K</sub> = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z <sub>KA</sub>	-	0.22	0.5	-	0.22	0.5	Ω

- T<sub>low</sub> = -40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM;  
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM  
T<sub>high</sub> = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM  
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
- The deviation parameter ΔV<sub>ref</sub> is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV<sub>ref</sub> = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C} \quad \alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

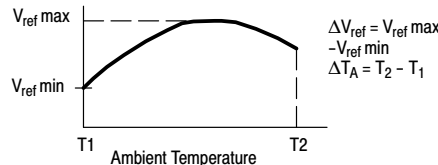
- The dynamic impedance Z<sub>KA</sub> is defined as:  $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$ . When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:  $|Z_{KA}'| \approx |Z_{KA}| \left( 1 + \frac{R1}{R2} \right)$

# TL431, A, B Series, NCV431A, B

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI / NCV431AI			TL431AC			TL431BC / TL431BI / TL431BV / NCV431BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>	V <sub>ref</sub>	2.47 2.44	2.495 –	2.52 2.55	2.47 2.453	2.495 –	2.52 2.537	2.485 2.475	2.495 2.495	2.505 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 4, 5) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA	ΔV <sub>ref</sub>	–	7.0	30	–	3.0	17	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I <sub>K</sub> = 10 mA (Figure 2), ΔV <sub>KA</sub> = 10 V to V <sub>ref</sub> ΔV <sub>KA</sub> = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–1.4 –1.0	–2.7 –2.0	–	–1.4 –1.0	–2.7 –2.0	–	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞ T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> (Note 4)	I <sub>ref</sub>	–	1.8 –	4.0 6.5	–	1.8 –	4.0 5.2	–	1.1 –	2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 4) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞	ΔI <sub>ref</sub>	–	0.8	2.5	–	0.4	1.2	–	0.8	2.5	μA
Minimum Cathode Current For Regulation V <sub>KA</sub> = V <sub>ref</sub> (Figure 1)	I <sub>min</sub>	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V <sub>KA</sub> = 36 V, V <sub>ref</sub> = 0 V	I <sub>off</sub>	–	20	1000	–	20	1000	–	0.23	500	nA
Dynamic Impedance (Figure 1, Note 6) V <sub>KA</sub> = V <sub>ref</sub> , ΔI <sub>K</sub> = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z <sub>KA</sub>	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

4. T<sub>low</sub> = –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431BV, TL431AIDM, TL431IDM, TL431BIDM, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G  
= 0°C for TL431ACP, TL431ACL, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM  
T<sub>high</sub> = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM  
= +70°C for TL431ACP, TL431ACL, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM  
= +125°C TL431BV, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, NCV431BVDR2G
5. The deviation parameter ΔV<sub>ref</sub> is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV<sub>ref</sub> = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

6. The dynamic impedance Z<sub>KA</sub> is defined as  $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$  When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:  $|Z_{KA}'| \approx |Z_{KA}| \left( 1 + \frac{R1}{R2} \right)$
7. NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, NCV431BVDR2G T<sub>low</sub> = –40°C, T<sub>high</sub> = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring unique site and control change requirements.

# TL431, A, B Series, NCV431A, B



Figure 1. Test Circuit for  $V_{KA} = V_{ref}$



Figure 2. Test Circuit for  $V_{KA} > V_{ref}$



Figure 3. Test Circuit for  $I_{off}$

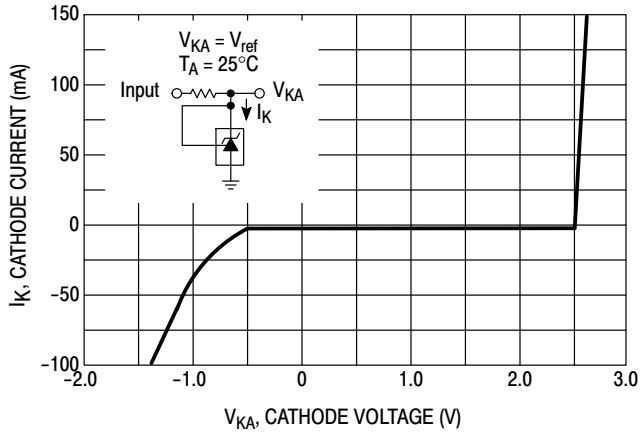


Figure 4. Cathode Current versus Cathode Voltage

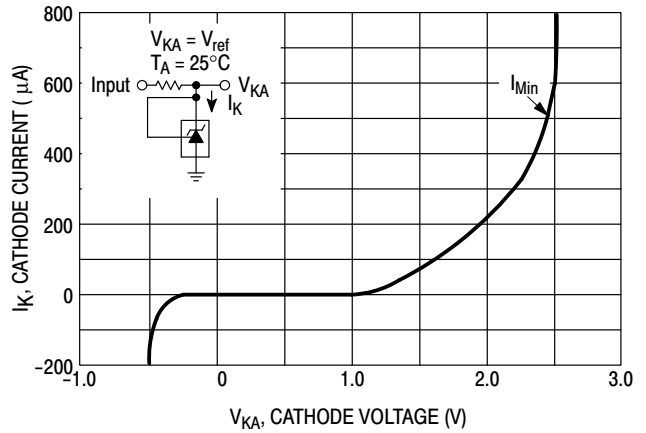


Figure 5. Cathode Current versus Cathode Voltage



Figure 6. Reference Input Voltage versus Ambient Temperature

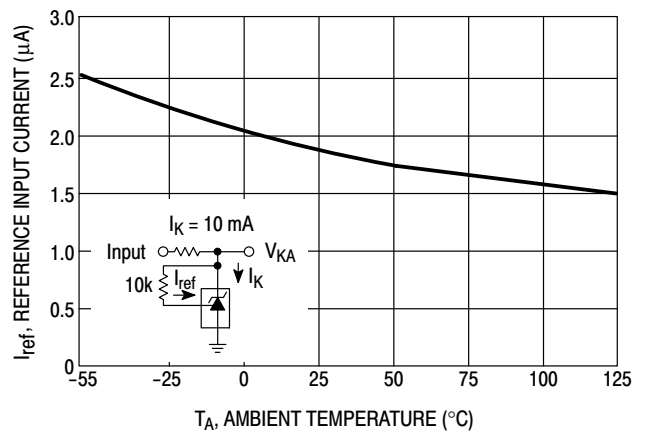


Figure 7. Reference Input Current versus Ambient Temperature

# TL431, A, B Series, NCV431A, B



**Figure 8. Change in Reference Input Voltage versus Cathode Voltage**



**Figure 9. Off-State Cathode Current versus Ambient Temperature**



**Figure 10. Dynamic Impedance versus Frequency**



**Figure 11. Dynamic Impedance versus Ambient Temperature**



**Figure 12. Open-Loop Voltage Gain versus Frequency**



**Figure 13. Spectral Noise Density**

# TL431, A, B Series, NCV431A, B



Figure 14. Pulse Response



Figure 15. Stability Boundary Conditions



Figure 16. Test Circuit For Curve A of Stability Boundary Conditions



Figure 17. Test Circuit For Curves B, C, and D of Stability Boundary Conditions

## TYPICAL APPLICATIONS



Figure 18. Shunt Regulator



Figure 19. High Current Shunt Regulator

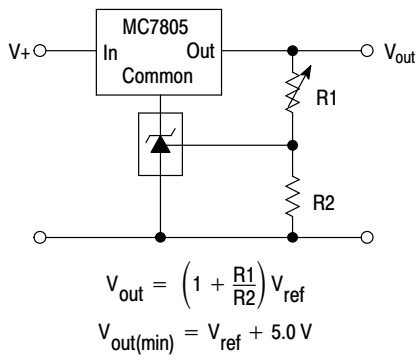


Figure 20. Output Control for a Three-Terminal Fixed Regulator



Figure 21. Series Pass Regulator



Figure 22. Constant Current Source

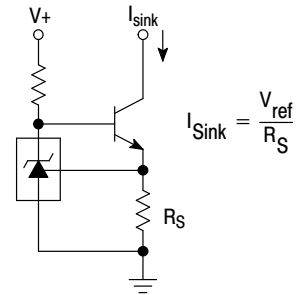


Figure 23. Constant Current Sink



Figure 24. TRIAC Crowbar

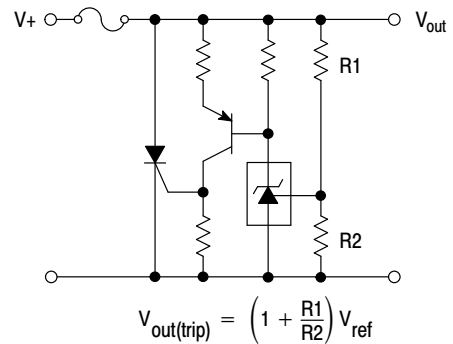


Figure 25. SRC Crowbar



# TL431, A, B Series, NCV431A, B



$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

**Figure 26. Voltage Monitor**



**Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold**



**Figure 28. Linear Ohmmeter**



**Figure 29. Simple 400 mW Phono Amplifier**

## TL431, A, B Series, NCV431A, B



**Figure 30. High Efficiency Step-Down Switching Converter**

Test	Conditions	Results
Line Regulation	$V_{in} = 10\text{ V to } 20\text{ V}$ , $I_o = 1.0\text{ A}$	53 mV (1.1%)
Load Regulation	$V_{in} = 15\text{ V}$ , $I_o = 0\text{ A to } 1.0\text{ A}$	25 mV (0.5%)
Output Ripple	$V_{in} = 10\text{ V}$ , $I_o = 1.0\text{ A}$	50 mVpp P.A.R.D.
Output Ripple	$V_{in} = 20\text{ V}$ , $I_o = 1.0\text{ A}$	100 mVpp P.A.R.D.
Efficiency	$V_{in} = 15\text{ V}$ , $I_o = 1.0\text{ A}$	82%

# TL431, A, B Series, NCV431A, B

## APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non-standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, G<sub>m</sub>, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of G<sub>m</sub> flows through compensation capacitance, C<sub>P2</sub>. The voltage across C<sub>P2</sub> drives the output dependent current source, G<sub>o</sub>, which is connected across the device cathode and anode.

Model component values are:

$$V_{\text{ref}} = 1.78 \text{ V}$$

$$G_m = 0.3 + 2.7 \exp(-I_C/26 \text{ mA})$$

where I<sub>C</sub> is the device cathode current and G<sub>m</sub> is in mhos

$$G_o = 1.25 (V_{\text{cp2}}) \mu\text{mhos.}$$

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P_1 = \frac{1}{2\pi R_{\text{GM}} C_{\text{P1}}} = \frac{1}{2\pi * 1.0 \text{ M} * 20 \text{ pF}} = 7.96 \text{ kHz}$$

$$P_2 = \frac{1}{2\pi R_{\text{P2}} C_{\text{P2}}} = \frac{1}{2\pi * 10 \text{ M} * 0.265 \text{ pF}} = 60 \text{ kHz}$$

$$Z_1 = \frac{1}{2\pi R_{\text{Z1}} C_{\text{P1}}} = \frac{1}{2\pi * 15.9 \text{ k} * 20 \text{ pF}} = 500 \text{ kHz}$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the TL431 is:

$$G = G_M R_{\text{GM}} G_o R_L$$

Example 1:

I<sub>C</sub> = 10 mA, R<sub>L</sub> = 230 Ω, C<sub>L</sub> = 0. Define the transfer gain.

The DC gain is:

$$G = G_M R_{\text{GM}} G_o R_L = (2.138)(1.0 \text{ M})(1.25 \mu)(230) = 615 = 56 \text{ dB}$$

$$\text{Loop gain} = G \frac{8.25 \text{ k}}{8.25 \text{ k} + 15 \text{ k}} = 218 = 47 \text{ dB}$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open-Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

# TL431, A, B Series, NCV431A, B



**Figure 31. Simplified TL431 Device Model**



**Figure 32. Example 1 Circuit Open Loop Gain Plot**

Example 2.

$I_C = 7.5 \text{ mA}$ ,  $R_L = 2.2 \text{ k}\Omega$ ,  $C_L = 0.01 \text{ }\mu\text{F}$ . Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_o R_L =$$

$$(2.323)(1.0 \text{ M})(1.25 \text{ }\mu)(2200) = 6389 = 76 \text{ dB}$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)\left(1 + \frac{jf}{7.2 \text{ kHz}}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about  $-46$  degrees. Therefore, instability of this circuit is likely.



**Figure 33. Example 2 Circuit Open Loop Gain Plot**

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

# TL431, A, B Series, NCV431A, B

## ORDERING INFORMATION

Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance	
TL431ACDG	AC	0°C to 70°C	SOIC-8 (Pb-Free)	98 Units / Rail	1.0%	
TL431BCDG	BC				0.4%	
TL431CDG	C				2.2%	
TL431ACDR2G	AC		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel	1.0%	
TL431BCDR2G	BC				0.4%	
TL431CDR2G	C				2.2%	
TL431ACDMR2G	TAC		Micro8 (Pb-Free)	4000 Units / Tape & Reel	1.0%	
TL431BCDMR2G	TBC				0.4%	
TL431CDMR2G	T-C				2.2%	
TL431ACPG	ACP		PDIP-8 (Pb-Free)	50 Units / Rail	1.0%	
TL431BCPG	BCP				0.4%	
TL431CPG	CP				2.2%	
TL431ACLPG	ACLP		TO-92 (Pb-Free)	2000 Units / Bag	1.0%	
TL431BCLPG	BCLP				0.4%	
TL431CLPG	CLP				2.2%	
TL431ACLPRAG	ACLP		TO-92 (Pb-Free)	2000 Units / Tape & Reel	1.0%	
TL431BCLPRAG	BCLP				0.4%	
TL431CLPRAG	CLP				2.2%	
TL431ACLPRAG	ACLP				1.0%	
TL431BCLPRAG	BCLP				0.4%	
TL431CLPRAG	CLP	2.2%				
TL431ACLPRPG	ACLP	TO-92 (Pb-Free)	2000 / Tape & Ammo Box	1.0%		
TL431BCLPRMG	BCLP	TO-92 (Pb-Free)	2000 Units / Fan-Fold	0.4%		
TL431CLPRMG	CLP			2.2%		
TL431CLPRPG	CLP			2.2%		
TL431AIDG	AI	-40°C to 85°C	SOIC-8 (Pb-Free)	98 Units / Rail	1.0%	
TL431BIDG	BI				0.4%	
TL431IDG	I				2.2%	
TL431AIDR2G	AI		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel	1.0%	
TL431BIDR2G	BI				0.4%	
TL431IDR2G	I				2.2%	
TL431AIDMR2G	TAI		Micro8 (Pb-Free)	4000 Units / Tape & Reel	1.0%	
TL431BIDMR2G	TBI				0.4%	
TL431IDMR2G	T-I				2.2%	
TL431AIPG	AIP		PDIP-8 (Pb-Free)	50 Units / Rail	1.0%	
TL431BIPG	BIP				0.4%	
TL431IPG	IP				2.2%	
TL431AILPG	AILP		TO-92 (Pb-Free)	2000 Units / Bag	1.0%	
TL431BILPG	BILP				0.4%	
TL431ILPG	ILP				2.2%	
TL431AILPRAG	AILP		TO-92 (Pb-Free)	2000 Units / Tape & Reel	1.0%	
TL431BILPRAG	BILP				0.4%	
SC431ILPRAG	ILP				2.2%	
TL431ILPRAG	ILP				2.2%	
TL431AILPRMG	AILP				TO-92 (Pb-Free)	2000 / Tape & Ammo Box
TL431AILPRPG		1.0%				
TL431ILPRPG	ILP	2.2%				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# TL431, A, B Series, NCV431A, B

## ORDERING INFORMATION

Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance
TL431BV DG	BV	-40°C to 125°C	SOIC-8 (Pb-Free)	98 Units / Rail	0.4%
TL431BV DR2G				2500 Units / Tape & Reel	0.4%
TL431BV DMR2G	TBV		Micro8 (Pb-Free)	4000 Units / Tape & Reel	0.4%
TL431BV LPG	BVLP		TO-92 (Pb-Free)	2000 Units / Bag	0.4%
TL431BV LPRAG			2000 Units / Tape & Reel	0.4%	
TL431BV PG	BVP		PDIP-8 (Pb-Free)	50 Units / Rail	0.4%
NCV431AIDMR2G	RAN		Micro8 (Pb-Free)	4000 Units / Tape & Reel	1%
NCV431AIDR2G	AV		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel	1%
NCV431BV DMR2G	NVB		Micro8 (Pb-Free)	4000 Units / Tape & Reel	0.4%
NCV431BV DR2G	BV		SOIC-8 (Pb-Free)	2500 Units / Tape & Reel	0.4%

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

**SOIC-8**  
**D SUFFIX**  
**CASE 751**



(Exception for the TL431CD and TL431ID only)

**Micro8**  
**CASE 846A**



**PDIP-8**  
**CASE 626**



**TO-92 (TO-226)**  
**CASE 29**



xxxx = See Specific Marking Code  
A = Assembly Location  
Y, YY = Year  
WW, W = Work Week  
▪ or G = Pb-Free Package

(Note: Microdot may be in either location)

# TL431, A, B Series, NCV431A, B

## PACKAGE DIMENSIONS



TO-92 (TO-226)  
CASE 29-11  
ISSUE AM

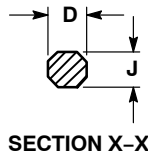


STRAIGHT LEAD  
BULK PACK

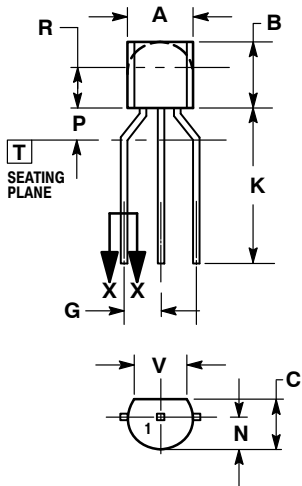
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



SECTION X-X

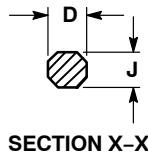


BENT LEAD  
TAPE & REEL  
AMMO PACK

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

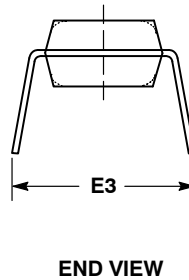
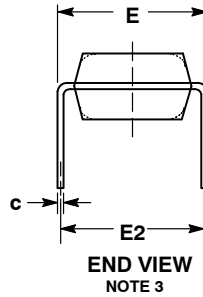
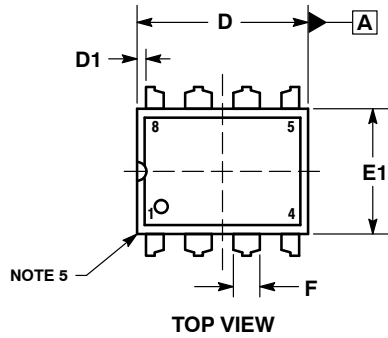


SECTION X-X

# TL431, A, B Series, NCV431A, B

## PACKAGE DIMENSIONS

PDIP-8  
P SUFFIX  
CASE 626-05  
ISSUE M



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION E IS MEASURED WITH THE LEADS RESTRAINED PARALLEL AT WIDTH E2.
4. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

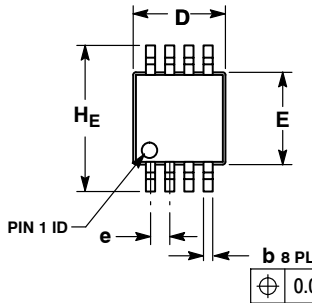
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	----	----	0.210	----	----	5.33
A1	0.015	----	----	0.38	----	----
b	0.014	0.018	0.022	0.35	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	0.355	0.365	0.400	9.02	9.27	10.02
D1	0.005	----	----	0.13	----	----
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
E2	0.300 BSC			7.62 BSC		
E3	----	----	0.430	----	----	10.92
e	0.100 BSC			2.54 BSC		
L	0.115	0.130	0.150	2.92	3.30	3.81



# TL431, A, B Series, NCV431A, B

## PACKAGE DIMENSIONS

**Micro8  
DM SUFFIX  
CASE 846A-02  
ISSUE G**

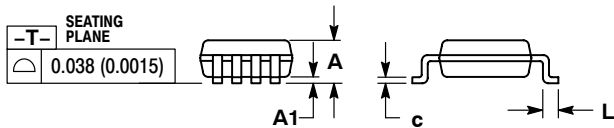


$\oplus$	0.08 (0.003)	M	T	B	S	A	S
----------	--------------	---	---	---	---	---	---

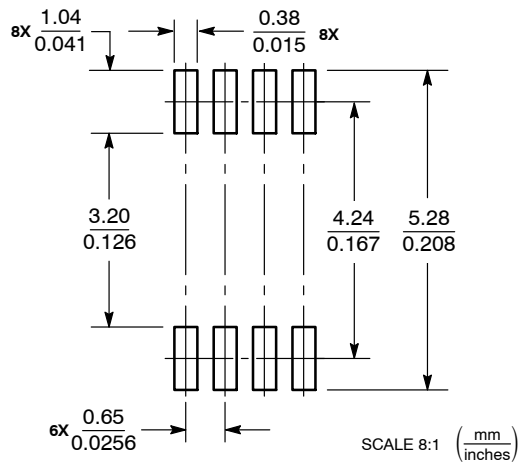
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
HE	4.75	4.90	5.05	0.187	0.193	0.199



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# TL431, A, B Series, NCV431A, B

## PACKAGE DIMENSIONS

### SOIC-8 D SUFFIX CASE 751-07 ISSUE AK

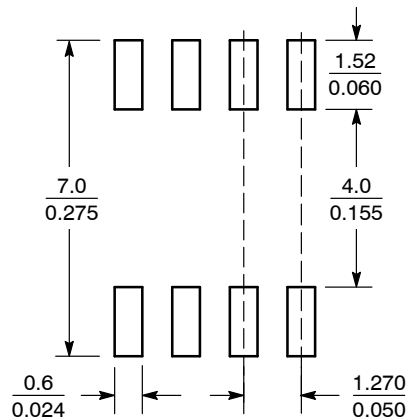


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.