

# Single 8-Ch/Differential 4-Ch Latchable Analog Multiplexers

## DESCRIPTION

The DG428, DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

## FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low  $R_{DS(on)}$ : 55  $\Omega$
- Low Charge Injection: 1 pC
- On-Board TTL Compatible Address Latches
- High Speed -  $t_{TRANS}$ : 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## BENEFITS

- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

## APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor-Controlled Analog Systems
- Medical Instrumentation

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE - DG428                |                |                |    |    |    |                                     |
|------------------------------------|----------------|----------------|----|----|----|-------------------------------------|
| 8-Channel Single-Ended Multiplexer |                |                |    |    |    |                                     |
| A <sub>2</sub>                     | A <sub>1</sub> | A <sub>0</sub> | EN | WR | RS | On Switch                           |
| <b>Latching</b>                    |                |                |    |    |    |                                     |
| X                                  | X              | X              | X  |    | 1  | Maintains previous switch condition |
| <b>Reset</b>                       |                |                |    |    |    |                                     |
| X                                  | X              | X              | X  | X  | 0  | None (latches cleared)              |
| <b>Transparent Operation</b>       |                |                |    |    |    |                                     |
| X                                  | X              | X              | 0  | 0  | 1  | None                                |
| 0                                  | 0              | 0              | 1  | 0  | 1  | 1                                   |
| 0                                  | 0              | 1              | 1  | 0  | 1  | 2                                   |
| 0                                  | 1              | 0              | 1  | 0  | 1  | 3                                   |
| 0                                  | 1              | 1              | 1  | 0  | 1  | 4                                   |
| 1                                  | 0              | 0              | 1  | 0  | 1  | 5                                   |
| 1                                  | 0              | 1              | 1  | 0  | 1  | 6                                   |
| 1                                  | 1              | 0              | 1  | 0  | 1  | 7                                   |
| 1                                  | 1              | 1              | 1  | 0  | 1  | 8                                   |

| TRUTH TABLE - DG429                |                |    |    |    |                                     |
|------------------------------------|----------------|----|----|----|-------------------------------------|
| Differential 4-Channel Multiplexer |                |    |    |    |                                     |
| A <sub>1</sub>                     | A <sub>0</sub> | EN | WR | RS | On Switch                           |
| <b>Latching</b>                    |                |    |    |    |                                     |
| X                                  | X              | X  |    | 1  | Maintains previous switch condition |
| <b>Reset</b>                       |                |    |    |    |                                     |
| X                                  | X              | X  | X  | 0  | None (latches cleared)              |
| <b>Transparent Operation</b>       |                |    |    |    |                                     |
| X                                  | X              | 0  | 0  | 1  | None                                |
| 0                                  | 0              | 1  | 0  | 1  | 1                                   |
| 0                                  | 1              | 1  | 0  | 1  | 2                                   |
| 1                                  | 0              | 1  | 0  | 1  | 3                                   |
| 1                                  | 1              | 1  | 0  | 1  | 4                                   |

Logic "0" =  $V_{AL} \leq 0.8\text{ V}$   
 Logic "1" =  $V_{AH} \geq 2.4\text{ V}$   
 X = Don't Care

| ORDERING INFORMATION - DG428 |                    |             |
|------------------------------|--------------------|-------------|
| Temp Range                   | Package            | Part Number |
| - 40 °C to 85 °C             | 18-pin Plastic DIP | DG428DJ     |
|                              |                    | DG428DJ-E3  |
|                              | 20-pin PLCC        | DG428DN     |
|                              |                    | DG428DN-E3  |

| ORDERING INFORMATION - DG429 |                      |             |
|------------------------------|----------------------|-------------|
| Temp Range                   | Package              | Part Number |
| - 40 °C to 85 °C             | 18-pin Plastic DIP   | DG429DJ     |
|                              |                      | DG429DJ-E3  |
|                              | 20-pin PLCC          | DG429DN     |
|                              |                      | DG429DN-E3  |
|                              | 18-pin Widebody SOIC | DG429DW     |
|                              |                      | DG429DW-E3  |



| <b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                                   |        |  |      |
|--|-----------------------------------|--------|--|------|
| Parameter  |                                   | Symbol | Limit  | Unit |
| Voltages Referenced to V-  | V+                                |        | 44   | V    |
|  | GND                               |        | 25   |      |
| Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>                                |                                   |        | (V-) - 2 V to (V+) + 2 V<br>or 30 mA, whichever occurs first |      |
| Current (Any Terminal)   |                                   |        | 30   | mA   |
| Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max)                                   |                                   |        | 100  |      |
| Storage Temperature  | (AK Suffix)                       |        | - 65 to 150  | °C   |
|  | (DJ, DN Suffix)                   |        | - 65 to 125  |      |
| Power Dissipation (Package) <sup>b</sup>   | 18-pin Plastic DIP <sup>c</sup>   |        | 470  | mW   |
|  | 18-pin CerDIP <sup>d</sup>        |        | 900  |      |
|  | 20-pin PLCC <sup>e</sup>          |        | 800  |      |
|  | 28-Pin Widebody SOIC <sup>f</sup> |        | 450  |      |

**Notes:**

- a. Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 6.3 mW/°C above 75 °C.
- d. Derate 12 mW/°C above 75 °C.
- e. Derate 10 mW/°C above 75 °C.
- f. Derate 6 mW/°C above 75 °C.



| SPECIFICATIONS <sup>a</sup>                                   |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
|---|---------------------|---|-------------------|-------------------|--------------------|-------------------|------------------------------|------------|-----------------------------|------------|---------------|
| Parameter   | Symbol              | Test Conditions<br>Unless Otherwise Specified<br>$V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ , $WR = 0$ ,<br>$\overline{RS} = 2.4\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$ |                   |                   | Temp. <sup>b</sup> | Typ. <sup>c</sup> | A Suffix<br>-55 °C to 125 °C |            | D Suffix<br>-40 °C to 85 °C |            | Unit          |
|   |                     | Min. <sup>d</sup>   | Max. <sup>d</sup> | Min. <sup>d</sup> |                    |                   | Max. <sup>d</sup>            |            |                             |            |               |
| <b>Analog Switch</b>  |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
| Analog Signal Range <sup>e</sup>                              | $V_{ANALOG}$        |   |                   | Full              |                    |                   | -15                          | 15         | -15                         | 15         | V             |
| Drain-Source On-Resistance                                    | $R_{DS(on)}$        | $V_D = \pm 10\text{ V}$ , $V_{AL} = 0.8\text{ V}$<br>$I_S = -1\text{ mA}$ , $V_{AH} = 2.4\text{ V}$   |                   | Room<br>Full      | 55                 |                   |                              | 100<br>125 |                             | 100<br>125 | $\Omega$      |
| Greatest Change in $R_{DS(on)}$ Between Channels <sup>g</sup> | $\Delta R_{DS(on)}$ | $-10\text{ V} < V_S < 10\text{ V}$<br>$I_S = -1\text{ mA}$  |                   | Room              | 5                  |                   |                              |            |                             |            | %             |
| Source Off Leakage Current                                    | $I_{S(off)}$        | $V_S = \pm 10\text{ V}$ ,<br>$V_{EN} = 0\text{ V}$ , $V_D = \pm 10\text{ V}$  |                   | Room<br>Full      | $\pm 0.03$         |                   | -0.5<br>-50                  | 0.5<br>50  | -0.5<br>-50                 | 0.5<br>50  |               |
| Drain Off Leakage Current                                     | $I_{D(off)}$        | $V_{EN} = 0\text{ V}$<br>$V_D = \pm 10\text{ V}$<br>$V_S = \pm 10\text{ V}$   | DG428             | Room<br>Full      | $\pm 0.07$         |                   | -1<br>-100                   | 1<br>100   | -1<br>-100                  | 1<br>100   | nA            |
|   |                     |   | DG429             | Room<br>Full      | $\pm 0.05$         |                   | -1<br>-50                    | 1<br>50    | -1<br>-50                   | 1<br>50    |               |
| Drain On Leakage Current                                      | $I_{D(on)}$         | $V_S = V_D = \pm 10\text{ V}$<br>$V_{EN} = 2.4\text{ V}$<br>$V_{AL} = 0.8\text{ V}$<br>$V_{AH} = 2.4\text{ V}$  | DG428             | Room<br>Full      | $\pm 0.07$         |                   | -1<br>-100                   | 1<br>100   | -1<br>-100                  | 1<br>100   | nA            |
|   |                     |   | DG429             | Room<br>Full      | $\pm 0.05$         |                   | -1<br>-50                    | 1<br>50    | -1<br>-50                   | 1<br>50    |               |
| <b>Digital Control</b>  |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
| Logic Input Current Input Voltage High                        | $I_{AH}$            | $V_A = 2.4\text{ V}$<br>$V_A = 15\text{ V}$   |                   | Full              | 0.01               |                   |                              | 1          |                             | 1          | $\mu\text{A}$ |
|   |                     |   |                   | Full              | 0.01               |                   |                              | 1          |                             | 1          |               |
| Logic Input Current Input Voltage Low                         | $I_{AL}$            | $V_{EN} = 0\text{ V}$ , $2.4\text{ V}$ , $V_A = 0\text{ V}$<br>$\overline{RS} = 0\text{ V}$ , $WR = 0\text{ V}$   |                   | Full              | -0.01              |                   | -1                           |            | -1                          |            | $\mu\text{A}$ |
| Logic Input Capacitance                                       | $C_{in}$            | $f = 1\text{ MHz}$  |                   | Room              | 8                  |                   |                              |            |                             |            | pF            |
| <b>Dynamic Characteristics</b>                                |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
| Transition Time   | $t_{TRANS}$         | See Figure 5  |                   | Room<br>Full      | 150                |                   |                              | 250<br>300 |                             | 250<br>300 | ns            |
| Break-Before-Make Interval                                    | $t_{OPEN}$          | See Figure 4  |                   | Full              | 30                 | 10                |                              |            | 10                          |            |               |
| Enable and Write Turn-On Time                                 | $t_{ON(EN,WR)}$     | See Figure 6 and 7  |                   | Room<br>Full      | 90                 |                   |                              | 150<br>225 |                             | 150<br>225 |               |
| Enable and Reset Turn-Off Time                                | $t_{OFF(EN,RS)}$    | See Figure 6 and 8  |                   | Room<br>Full      | 55                 |                   |                              | 150<br>300 |                             | 150<br>300 |               |
| Charge Injection  | Q                   | $V_{GEN} = 0\text{ V}$ , $R_{GEN} = 0\ \Omega$<br>$C_L = 1\text{ nF}$ , See Figure 9  |                   | Room              | 1                  |                   |                              |            |                             |            | pC            |
| Off Isolation   | OIRR                | $V_{EN} = 0\text{ V}$ , $R_L = 300\ \Omega$<br>$C_L = 15\text{ pF}$ , $V_S = 7\text{ V}_{RMS}$<br>$f = 100\text{ kHz}$  |                   | Room              | -75                |                   |                              |            |                             |            | dB            |
| Source Off Capacitance  | $C_{S(off)}$        | $V_S = 0\text{ V}$ , $V_{EN} = 0\text{ V}$ , $f = 1\text{ MHz}$   |                   | Room              | 11                 |                   |                              |            |                             |            | pF            |
| Drain Off Capacitance   | $C_{D(off)}$        | $V_D = 0\text{ V}$<br>$V_{EN} = 0\text{ V}$<br>$f = 1\text{ MHz}$   | DG428             | Room              | 40                 |                   |                              |            |                             |            |               |
|   |                     |   | DG429             | Room              | 20                 |                   |                              |            |                             |            |               |
| Drain On Capacitance  | $C_{D(on)}$         | $f = 1\text{ MHz}$  | DG428             | Room              | 54                 |                   |                              |            |                             |            |               |
|   |                     |   | DG429             | Room              | 34                 |                   |                              |            |                             |            |               |
| <b>Minimum Input Timing Requirements</b>                      |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
| Write Pulse Width   | $t_W$               | See Figure 2  |                   | Full              |                    |                   | 100                          |            | 100                         |            | ns            |
| $A_X$ , EN Data Set Up time                                   | $t_S$               |   | Full              |                   | 100                |                   |                              | 100        |                             |            |               |
| $A_X$ , EN Data Hold Time                                     | $t_H$               |   | Full              |                   | 10                 |                   |                              | 10         |                             |            |               |
| Reset Pulse Width   | $t_{RS}$            | $V_S = 5\text{ V}$ , See Figure 3   |                   | Full              |                    |                   | 100                          |            | 100                         |            |               |
| <b>Power Supplies</b>   |                     |   |                   |                   |                    |                   |                              |            |                             |            |               |
| Positive Supply Current                                       | I+                  | $V_{EN} = V_A = 0$ , $\overline{RS} = 5\text{ V}$   |                   | Room              | 20                 |                   |                              | 100        |                             | 100        | $\mu\text{A}$ |
| Negative Supply Current                                       | I-                  |   | Room              | -0.001            |                    | -5                |                              |            | -5                          |            |               |



| SPECIFICATIONS <sup>a</sup> (for single supply) |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
|---|-------------------------|--|------------------------------------|-------------------|------------------------------|-------------------|------------------------------|-------------------|----------|----------|
| Parameter                                       | Symbol                  | Test Conditions<br>Unless Otherwise Specified<br>V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V, WR = 0,<br>RS = 2.4 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup> | Temp. <sup>b</sup>                 | Typ. <sup>c</sup> | A Suffix<br>- 55°C to 125 °C |                   | D Suffix<br>- 40 °C to 85 °C |                   | Unit     |          |
|   |                         |  |                                    |                   | Min. <sup>d</sup>            | Max. <sup>d</sup> | Min. <sup>d</sup>            | Max. <sup>d</sup> |          |          |
| <b>Analog Switch</b>                            |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
| Analog Signal Range <sup>e</sup>                | V <sub>ANALOG</sub>     |  | Full                               |                   | 0                            | 12                | 0                            | 12                | V        |          |
| Drain-Source On-Resistance                      | R <sub>DS(on)</sub>     | V <sub>D</sub> = ± 10 V, V <sub>AL</sub> = 0.8 V<br>I <sub>S</sub> = - 500 µA, V <sub>AH</sub> = 2.4 V   | Room                               | 80                |                              | 150               |                              | 150               | Ω        |          |
| R <sub>DS(on)</sub> Match <sup>g</sup>          | ΔR <sub>DS(on)</sub>    | 0 V < V <sub>S</sub> < 10 V<br>I <sub>S</sub> = - 1 mA   | Room                               | 5                 |                              |                   |                              |                   | %        |          |
| Source Off Leakage Current                      | I <sub>S(off)</sub>     | V <sub>S</sub> = 0 V, 10 V,<br>V <sub>EN</sub> = 0 V, V <sub>D</sub> = 10 V, 0 V   | Room Full                          | ± 0.03            | - 0.5<br>- 50                | 0.5<br>50         | - 0.5<br>- 50                | 0.5<br>50         | nA       |          |
| Drain Off Leakage Current                       | I <sub>D(off)</sub>     | V <sub>D</sub> = 0 V, 10 V<br>V <sub>S</sub> = 10 V, 0 V<br>V <sub>EN</sub> = 0 V  | DG428                              | Room Full         | ± 0.07                       | - 1<br>- 100      | 1<br>100                     | - 1<br>- 100      |          | 1<br>100 |
|   |                         |  | DG429                              | Room Full         | ± 0.05                       | - 1<br>- 50       | 1<br>50                      | - 1<br>- 50       |          | 1<br>50  |
| Drain On Leakage Current                        | I <sub>D(on)</sub>      | V <sub>S</sub> = V <sub>D</sub> = 0 V, 10 V<br>V <sub>EN</sub> = 2.4 V<br>V <sub>AL</sub> = 0.8 V<br>V <sub>AH</sub> = 2.4 V                                     | DG428                              | Room Full         | ± 0.07                       | - 1<br>- 100      | 1<br>100                     | - 1<br>- 100      | 1<br>100 |          |
|   |                         |  | DG429                              | Room Full         | ± 0.05                       | - 1<br>- 50       | 1<br>50                      | - 1<br>- 50       | 1<br>50  |          |
| <b>Digital Control</b>                          |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
| Logic Input Current<br>Input Voltage High       | I <sub>AH</sub>         | V <sub>A</sub> = 2.4 V   | Full                               |                   |                              | 1                 |                              | 1                 | µA       |          |
|   |                         | V <sub>A</sub> = 12 V  | Full                               |                   |                              | 1                 |                              | 1                 |          |          |
| Logic Input Current<br>Input Voltage Low        | I <sub>AL</sub>         | V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V<br>RS = 0 V, WR = 0 V   | Full                               |                   | - 1                          |                   | - 1                          |                   |          |          |
| <b>Dynamic Characteristics</b>                  |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
| Transition Time                                 | t <sub>TRANS</sub>      | S <sub>1</sub> = 10 V/ 2 V, S <sub>8</sub> = 2 V/ 10 V<br>See Figure 5   | Room Full                          | 160               |                              | 280<br>350        |                              | 280<br>350        | ns       |          |
| Break-Before-Make Interval                      | t <sub>OPEN</sub>       | See Figure 4   | Room Full                          | 40                | 25<br>10                     |                   | 25<br>10                     |                   |          |          |
| Enable and Write Turn-On Time                   | t <sub>ON(EN,WR)</sub>  | S <sub>1</sub> = 5 V<br>See Figure 6 and 7   | Room Full                          | 110               |                              | 300<br>400        |                              | 300<br>400        |          |          |
| Enable and Reset Turn-Off Time                  | t <sub>OFF(EN,RS)</sub> | S <sub>1</sub> = 5 V<br>See Figure 6 and 8   | Room Full                          | 70                |                              | 300<br>400        |                              | 300<br>400        |          |          |
| Charge Injection                                | Q                       | V <sub>GEN</sub> = 6 V, R <sub>GEN</sub> = 0 Ω<br>C <sub>L</sub> = 1 nF, See Figure 9  | Room                               | 4                 |                              |                   |                              |                   | pC       |          |
| Off Isolation                                   | OIRR                    | V <sub>EN</sub> = 0 V, R <sub>L</sub> = 300 Ω<br>C <sub>L</sub> = 15 pF, V <sub>S</sub> = 7 V <sub>RMS</sub><br>f = 100 kHz                                      | Room                               | - 75              |                              |                   |                              |                   | dB       |          |
| <b>Minimum Input Timing Requirements</b>        |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
| Write Pulse Width                               | t <sub>W</sub>          | See Figure 2   | Full                               |                   | 100                          |                   | 100                          |                   | ns       |          |
| A <sub>X</sub> , EN Data Set Up time            | t <sub>S</sub>          |  | Full                               |                   | 100                          |                   | 100                          |                   |          |          |
| A <sub>X</sub> , EN Data Hold Time              | t <sub>H</sub>          |  | Full                               |                   | 10                           |                   | 10                           |                   |          |          |
| Reset Pulse Width                               | t <sub>RS</sub>         |  | V <sub>S</sub> = 5 V, See Figure 3 | Full              |                              | 100               |                              | 100               |          |          |
| <b>Power Supplies</b>                           |                         |  |                                    |                   |                              |                   |                              |                   |          |          |
| Positive Supply Current                         | I <sub>+</sub>          | V <sub>EN</sub> = 0 V, V <sub>A</sub> = 0, RS = 5 V  | Room                               | 20                |                              | 100               |                              | 100               | µA       |          |

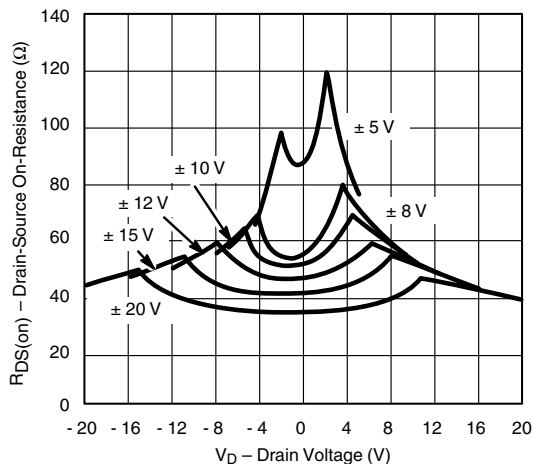
Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V<sub>IN</sub> = input voltage to perform proper function.

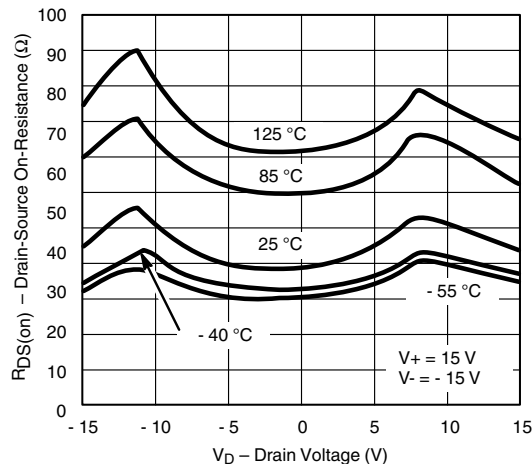
$$g. \Delta R_{DS(on)} = \left( \frac{R_{DS(on) \text{ MAX}} - R_{DS(on) \text{ MIN}}}{R_{DS(on) \text{ AVE}}} \right) \times 100 \%$$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

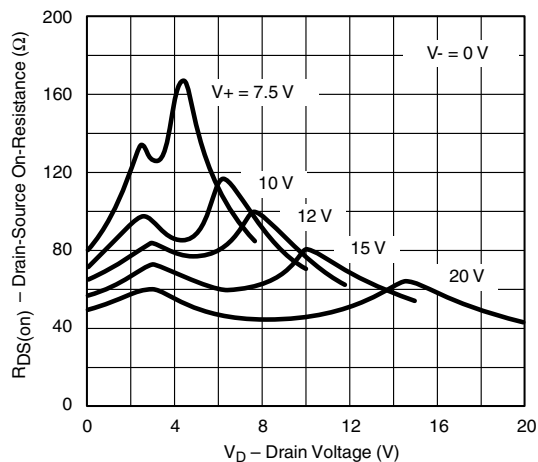
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



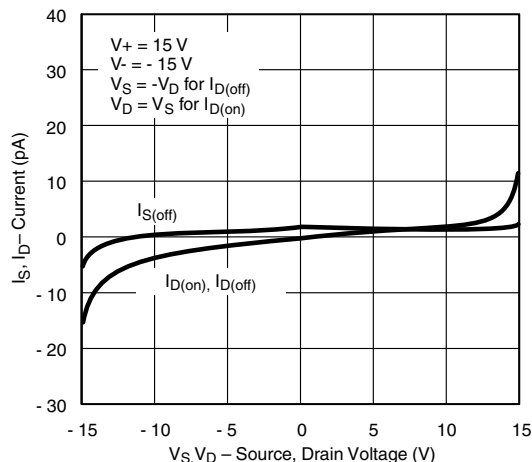
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Supply Voltage**



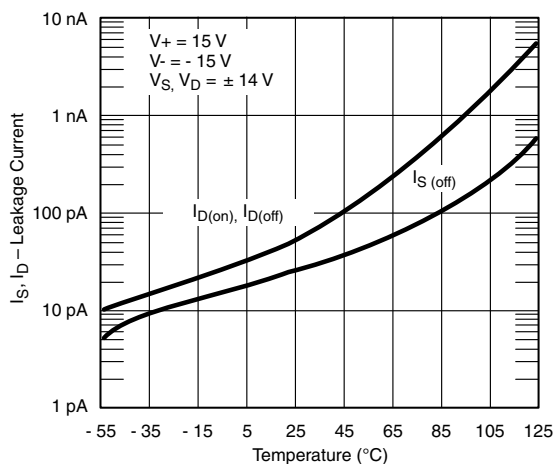
**R<sub>DS(on)</sub> vs. V<sub>D</sub> and Temperature**



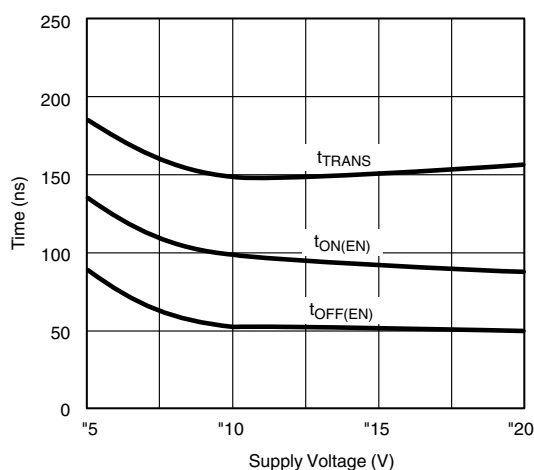
**Single Supply R<sub>DS(on)</sub> vs. V<sub>D</sub> and Supply**



**I<sub>D</sub>, I<sub>S</sub> Leakage Currents vs. Analog Voltage**

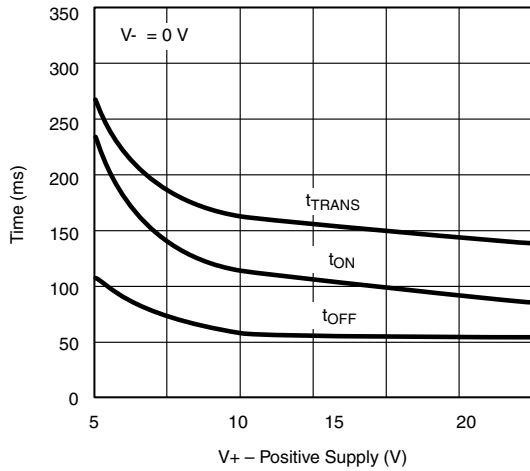


**I<sub>D</sub>, I<sub>S</sub> Leakages vs. Temperature**

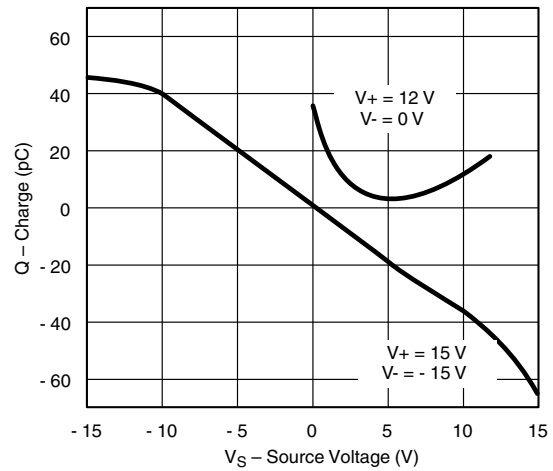


**Switching Times vs. Power Supply Voltage**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



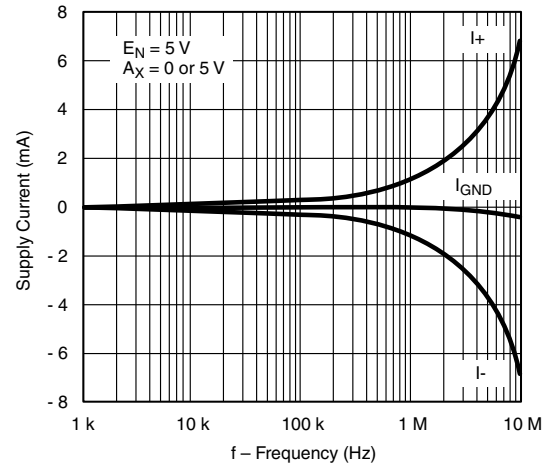
**Switching Times vs. Single Supply**



**Charge Injection vs. Analog Voltage**



**Off-Isolation vs. Frequency**



**Supply Currents vs. Switching Frequency**



**Switching Times vs. Temperature**



**Input Switching Threshold vs. Positive Supply Voltage**

## SCHEMATIC DIAGRAM (Typical Channel)



Figure 1.

## TIMING DIAGRAMS



Figure 2.

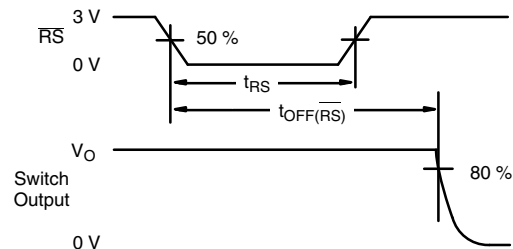


Figure 3.

## TEST CIRCUITS



Figure 4. Break-Before-Make





## TEST CIRCUITS

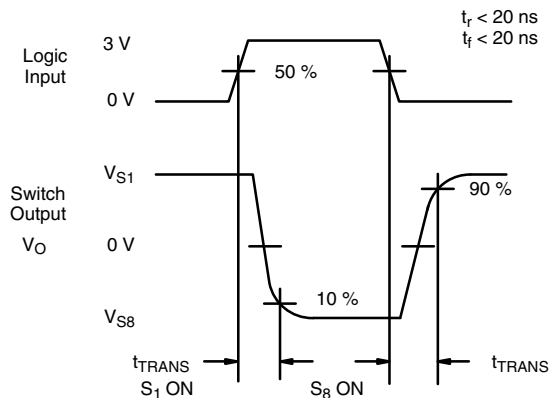


Figure 5. Transition Time

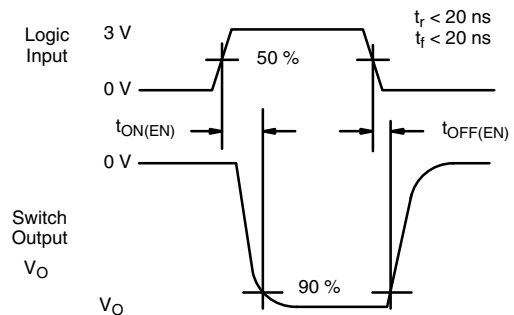
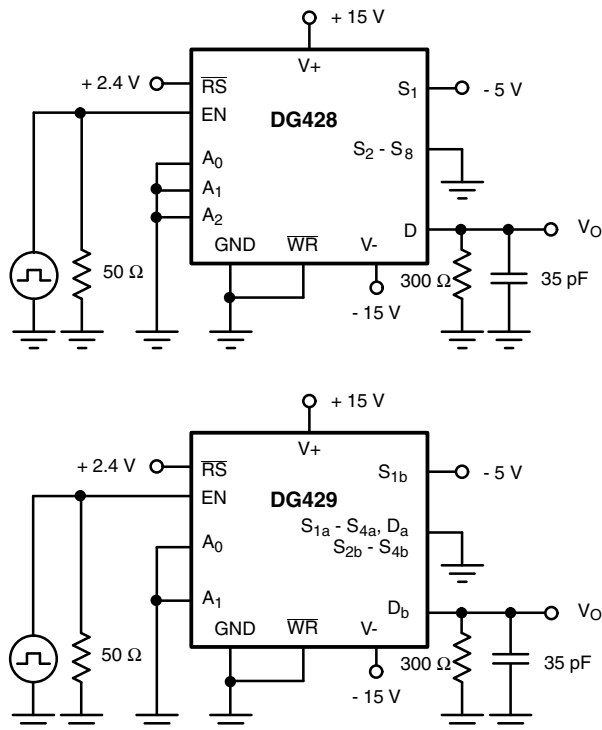


Figure 6. Enable  $t_{ON}/t_{OFF}$  Time

## TEST CIRCUITS



Figure 7. Write Turn-On Time  $t_{ON(WR)}$

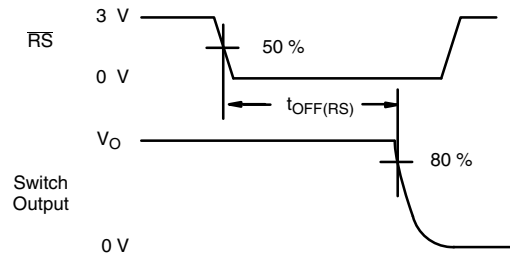


Figure 8. Reset Turn-Off Time  $t_{OFF(RS)}$

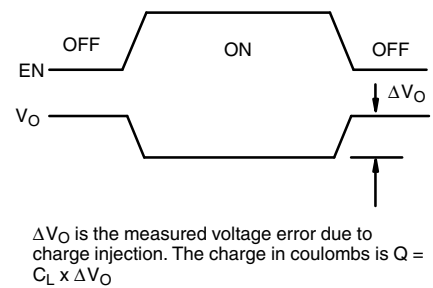


Figure 9. Charge Injection

## DETAILED DESCRIPTION

The internal structure of the DG428, DG429 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The input protection on the logic lines  $A_0$ ,  $A_1$ ,  $A_2$ , EN and control lines  $\overline{WR}$ ,  $\overline{RS}$  shown in Figure 1 minimizes susceptibility to ESD that may be encountered during handling and operational transients.

The logic interface is a CMOS logic input with its supply voltage from an internal + 5 V reference voltage. The output of the input inverter feeds the data input of a D type latch. The level sensitive D latch continuously places the  $D_X$  input signal on the  $Q_X$  output when the  $\overline{WR}$  input is low, resulting in transparent latch operation. As soon as  $\overline{WR}$  returns high the latch holds the data last present on the  $D_n$  input, subject to the "Minimum Input Timing Requirements" table.

Following the latches the  $Q_n$  signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting ensures full on/off switch operation for any analog signal level between the  $V+$  and  $V-$  supply rails.

The EN pin is used to enable the address latches during the  $\overline{WR}$  pulse. It can be hard wired to the logic supply or to  $V+$  if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The  $\overline{RS}$  pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The  $\overline{WR}$  pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

## APPLICATIONS HINTS

### Bus Interfacing

The DG428, DG429 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 10).

The input latches become transparent when  $\overline{WR}$  is held low; therefore, these multiplexers operate by direct command of the coded switch state on  $A_2$ ,  $A_1$ ,  $A_0$ . In this mode the DG428 is identical to the popular DG408. The same is true of the DG429 versus the popular DG409.

During system power-up,  $\overline{RS}$  would be low, maintaining all eight switches in the off state. After  $\overline{RS}$  returned high the DG428 maintains all switches in the off state.

When the system program performs a write operation to the address assigned to the DG428, the address decoder provides a  $\overline{CS}$  active low signal which is gated with the WRITE ( $\overline{WR}$ ) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the  $\overline{WR}$  signal returns to the high state, (positive edge) the input latches of the DG428 save the data from the DATA BUS. The coded information in the  $A_0$ ,  $A_1$ ,  $A_2$  and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG428s are cascaded to build 16-line and larger multiplexers.



Figure 10. Bus Interface

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**PLCC: 20-LEAD**



| Dim                  | MILLIMETERS |       | INCHES    |       |
|----------------------|-------------|-------|-----------|-------|
|                      | Min         | Max   | Min       | Max   |
| <b>A</b>             | 4.20        | 4.57  | 0.165     | 0.180 |
| <b>A<sub>1</sub></b> | 2.29        | 3.04  | 0.090     | 0.120 |
| <b>A<sub>2</sub></b> | 0.51        | –     | 0.020     | –     |
| <b>B</b>             | 0.331       | 0.553 | 0.013     | 0.021 |
| <b>B<sub>1</sub></b> | 0.661       | 0.812 | 0.026     | 0.032 |
| <b>D</b>             | 9.78        | 10.03 | 0.385     | 0.395 |
| <b>D<sub>1</sub></b> | 8.890       | 9.042 | 0.350     | 0.356 |
| <b>D<sub>2</sub></b> | 7.37        | 8.38  | 0.290     | 0.330 |
| <b>e<sub>1</sub></b> | 1.27 BSC    |       | 0.050 BSC |       |

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DWG: 5306

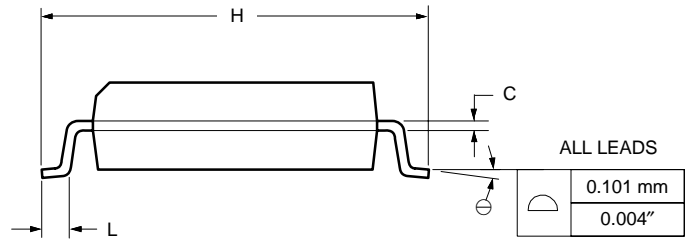
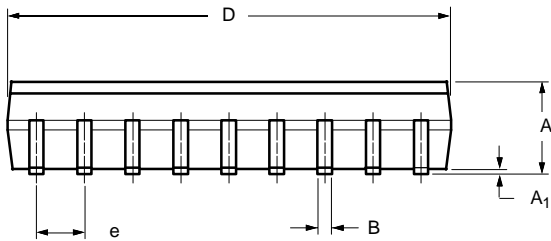


**SOIC (WIDE-BODY): 18-LEAD**



| Dim            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | Min         | Max   | Min       | Max   |
| A              | 2.15        | 2.90  | 0.085     | 0.114 |
| A <sub>1</sub> | 0.10        | 0.30  | 0.004     | 0.012 |
| B              | 0.35        | 0.45  | 0.014     | 0.018 |
| C              | 0.23        | 0.28  | 0.009     | 0.011 |
| D              | 11.25       | 12.45 | 0.443     | 0.490 |
| E              | 7.25        | 8.00  | 0.285     | 0.315 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H              | 9.80        | 10.60 | 0.386     | 0.417 |
| L              | 0.60        | 1.00  | 0.024     | 0.039 |
| ⊖              | 0°          | 8°    | 0°        | 8°    |

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DWG: 5302





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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.