CAT34TS02

Digital Output Temperature Sensor with On-board SPD EEPROM

Description

The CAT34TS02 combines a JC42.4 compliant Temperature Sensor (TS) with 2−Kb of Serial Presence Detect (SPD) EEPROM.

The TS measures temperature at least 10 times every second. Temperature readings can be retrieved by the host via the serial interface, and are compared to high, low and critical trigger limits stored into internal registers. Over or under limit conditions can be signaled on the open−drain $\overline{\text{EVENT}}$ pin.

The integrated 2−Kb SPD EEPROM is internally organized as 16 pages of 16 bytes each, for a total of 256 bytes. It features a 16−byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I^2C protocol.

Write operations to the lower half memory can be inhibited via software commands. The CAT34TS02 features Permanent, as well as Reversible Software Write Protection, as defined for DDR3 DIMMs.

Features

- JEDEC JC42.4 Compliant Temperature Sensor
- Temperature Range: −20°C to +125°C
- DDR3 DIMM Compliant SPD EEPROM
- Supply Range: 3.3 V ± 10%
- I^2C / SMBus Interface
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- Low Power CMOS Technology
- 2 x 3 x 0.75 mm TDFN Package
- These Devices are Pb−Free and are RoHS Compliant

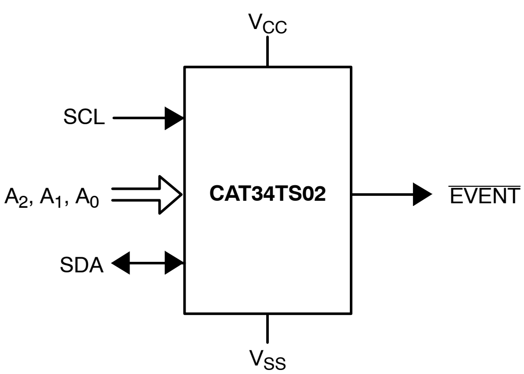
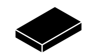


Figure 1. Functional Symbol

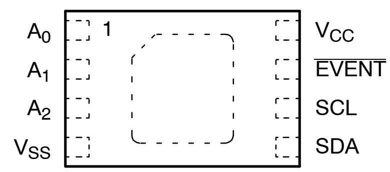
ON Semiconductor®

http://onsemi.com



TDFN−8
VP2 SUFFIX
CASE 511AK

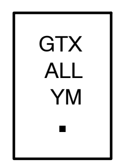
PIN CONFIGURATION



(Top View)

For the location of Pin 1, please consult the corresponding package drawing.

MARKING DIAGRAM



GTX	=	Specific Device Code
A	=	Assembly Location Code
LL	=	Assembly Lot Number (Last Two Digits)
Y	=	Production Year (Last Digit)
M	=	Production Month (1 − 9, O, N, D)
▪	=	Pb−Free Package

PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
$\overline{\text{EVENT}}$	Open−drain Event Output
V_{CC}	Power Supply
V_{SS}	Ground
DAP	Backside Exposed DAP at V_{SS}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

February, 2013 − Rev. 10

Publication Order Number:
CAT34TS02/D

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any pin (except A_0) with respect to Ground (Note 1)	−0.5 to +6.5	V
Voltage on pin A_0 with respect to Ground	−0.5 to +10.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. The A_0 pin can be raised to a HV level for RSWP command execution. SCL and SDA inputs can be raised to the maximum limit, irrespective of V_{CC}.

Table 2. RELIABILITY CHARACTERISTICS (Note 3)

Symbol	Parameter	Min	Units
N_{END} (Note 2)	Endurance (EEPROM)	1,000,000	Write Cycles
T_{DR}	Data Retention (EEPROM)	100	Years

2. Page Mode, V_{CC} = 3.3 V, 25°C

Table 3. TEMPERATURE CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −20°C to +125°C, unless otherwise specified)

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	−20°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	ms
Thermal Resistance (Note 3) θ_{JA}	Junction−to−Ambient (Still Air)	92	°C/W

3. Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2−layer PCB.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −20°C to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
I_{CC}	Supply Current	TS active, SPD and Bus idle		500	μA
		SPD Write, TS shut−down		500	μA
I_{SHDN}	Standby Current	TS shut−down; SPD and Bus idle		10	μA
I_{LKG}	I/O Pin Leakage Current	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage		−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} > 2.7 V		0.4	V
V_{OL2}	Output Low Voltage	I_{OL} = 1 mA, V_{CC} < 2.7 V		0.2	V

Table 5. A.C. CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −20°C to +125°C) (Note 4)

Symbol	Parameter	Min	Max	Units
F_{SCL} (Note 5)	Clock Frequency	10	400	kHz
t_{HIGH}	High Period of SCL Clock	600		ns
t_{LOW}	Low Period of SCL Clock	1300		ns
$t_{TIMEOUT}$ (Note 5)	SMBus SCL Clock Low Timeout	25	35	ms
t_R (Note 6)	SDA and SCL Rise Time		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300	ns
$t_{SU:DAT}$ (Note 7)	Data Setup Time	100		ns
$t_{SU:STA}$	START Condition Setup Time	600		ns
$t_{HD:STA}$	START Condition Hold Time	600		ns
$t_{SU:STO}$	STOP Condition Setup Time	600		ns
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
$t_{HD:DAT}$	Input Data Hold Time	0		ns
t_{DH} (Note 6)	Output Data Hold Time	200	900	ns
T_i	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU} (Note 8)	Power−up Delay to Valid Temperature Recording		100	ms

4. Timing reference points are set at 30%, respectively 70% of V_{CC}, as illustrated in Figure 23. Bus loading must be such as to allow meeting the V_{IL}, V_{OL} as well as the various timing limits.
5. For the CAT34TS02 Rev. B, the TS interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count is started (and then re−started) on every negative transition of SCL in the time interval between START and STOP. The minimum clock frequency of 10 kHz is an SMBus recommendation; the minimum operating clock frequency for the CAT34TS02's SPD component is DC, while the minimum operating frequency for the TS component is limited only by the SMBus time−out. For the CAT34TS02 Rev. C, both the TS and the SPD implement the time−out feature.
6. In a "Wired−OR" system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull−down device must be able to sink the (external) bus pull−up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} - t_{DH} - t_{SU:DAT}$, where t_{LOW} and t_{DH} are actual values (rather than spec limits). A shorter t_{DH} leaves more room for a longer SDA t_R, allowing for a more capacitive bus or a larger bus pull−up resistor. At the minimum t_{LOW} spec limit of 1300 ns, the maximum t_{DH} of 900 ns demands a maximum SDA t_R of 300 ns. The CAT34TS02's maximum t_{DH} is <700 ns, thus allowing for an SDA t_R of up to 500 ns at minimum t_{LOW}.
7. The minimum $t_{SU:DAT}$ of 100 ns is a limit recommended by standards. The CAT34TS02 will accept a $t_{SU:DAT}$ of 0 ns.
8. The first valid temperature recording can be expected after t_{PU} at nominal supply voltage.

Table 6. PIN CAPACITANCE (T_A = 25°C, V_{CC} = 3.3 V, f = 1 MHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, $\overline{EVENT}$ Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (other pins)	V_{IN} = 0		6	pF

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3 V, T_A = −20°C to +125°C, unless otherwise specified.)

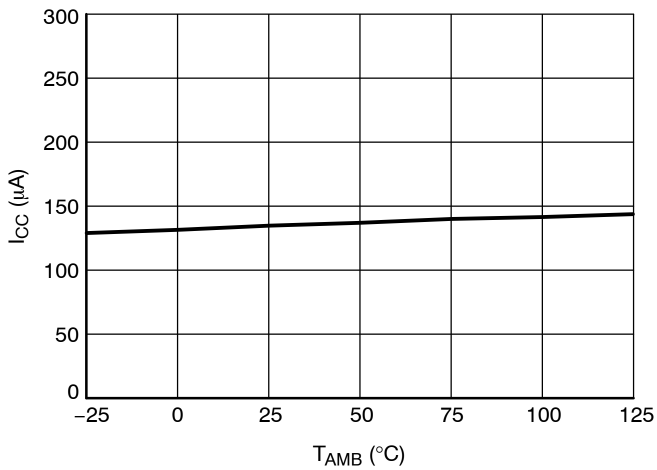


Figure 2. TS Active Current (Rev. B) (I^2C−bus and SPD EEPROM Idle)

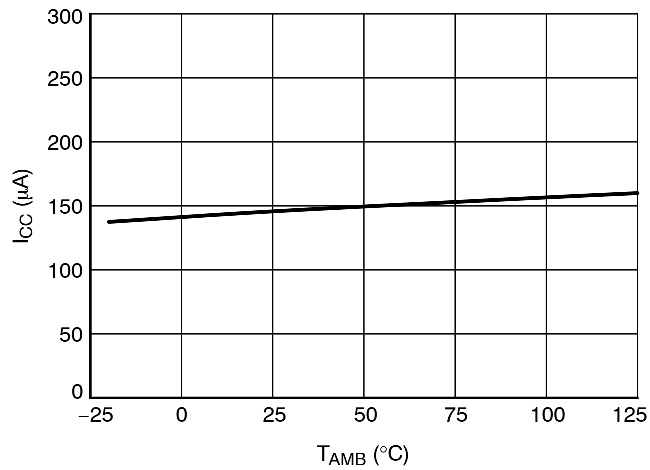


Figure 3. TS Active Current (Rev. C) (I^2C−bus and SPD EEPROM Idle)

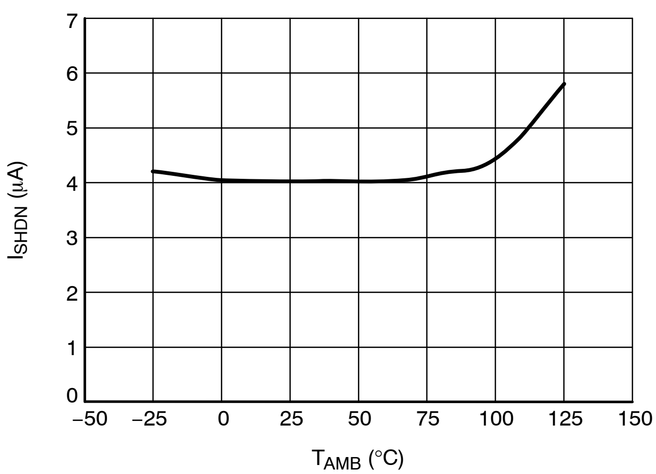


Figure 4. Standby Current (Rev. B) (I^2C−bus and SPD EEPROM Idle, TS Shut−down)

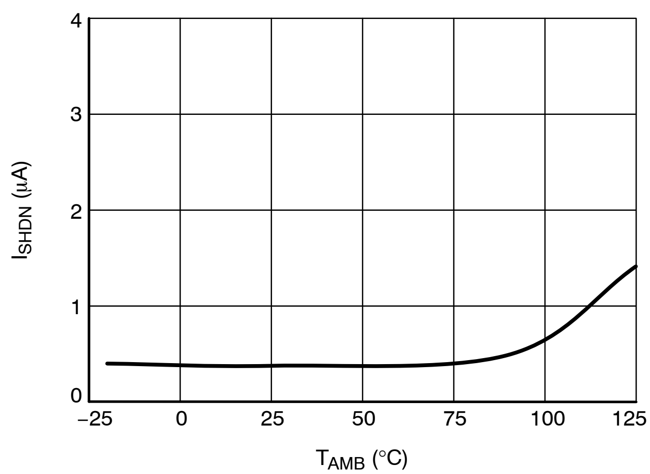


Figure 5. Standby Current (Rev. C) (I^2C−bus and SPD EEPROM Idle, TS Shut−down)

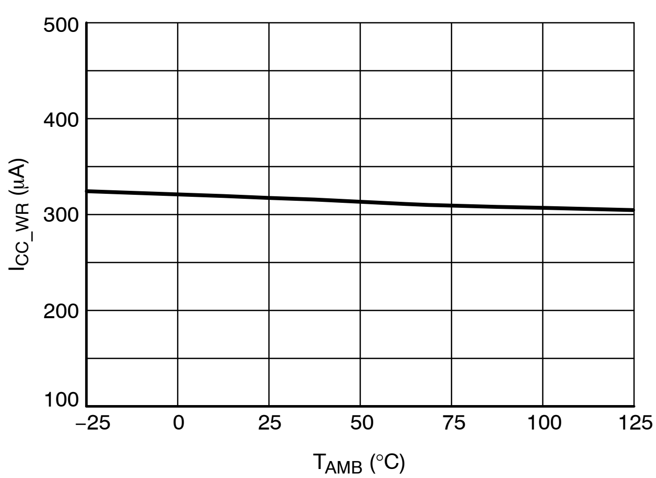


Figure 6. SPD EEPROM Write Current (Rev. B) (I^2C−bus Idle, TS Shut−down)

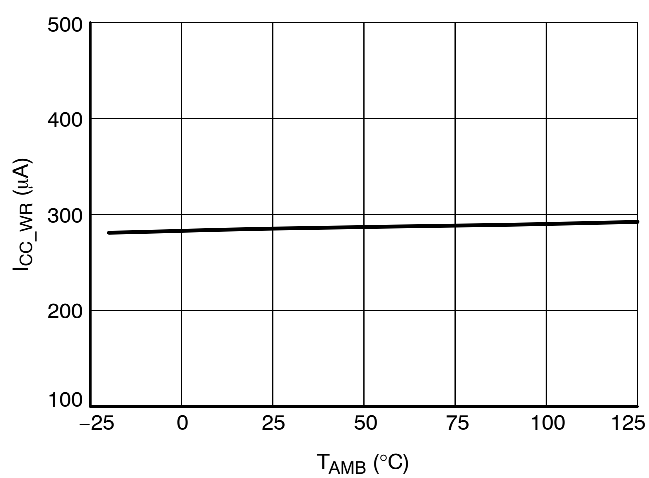


Figure 7. SPD EEPROM Write Current (Rev. C) (I^2C−bus Idle, TS Shut−down)

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3 V, T_A = −20°C to +125°C, unless otherwise specified.)

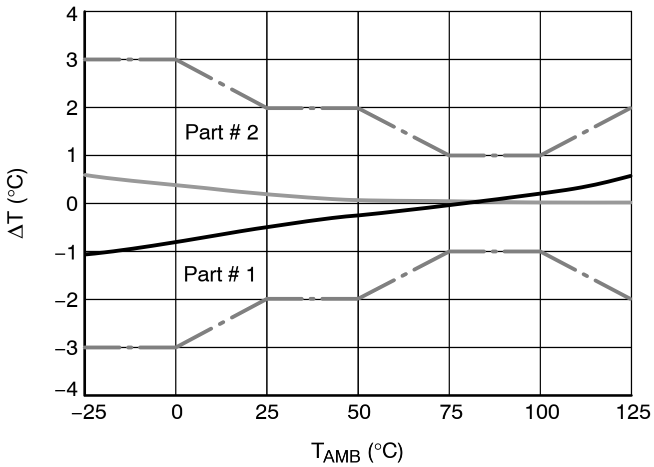


Figure 8. Temperature Read−Out Error (Rev. B)

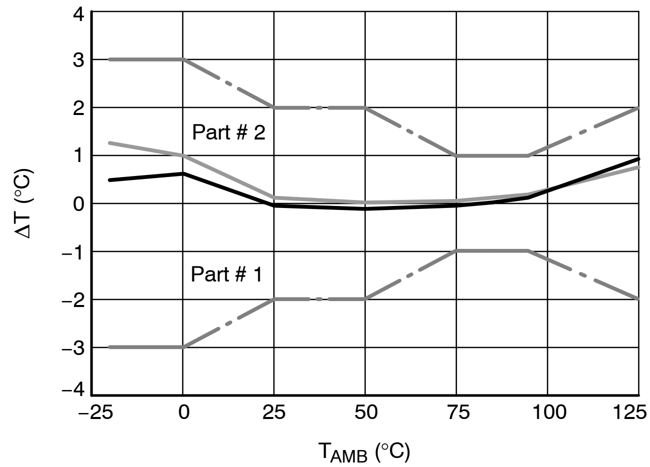


Figure 9. Temperature Read−Out Error (Rev. C)

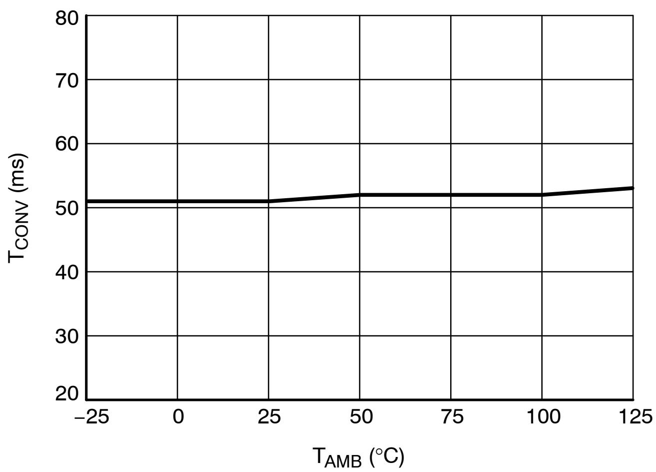


Figure 10. A/D Conversion Time (Rev. B)

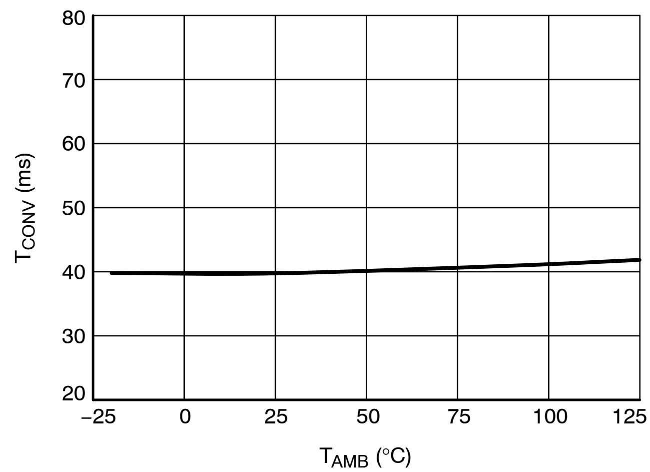


Figure 11. A/D Conversion Time (Rev. C)

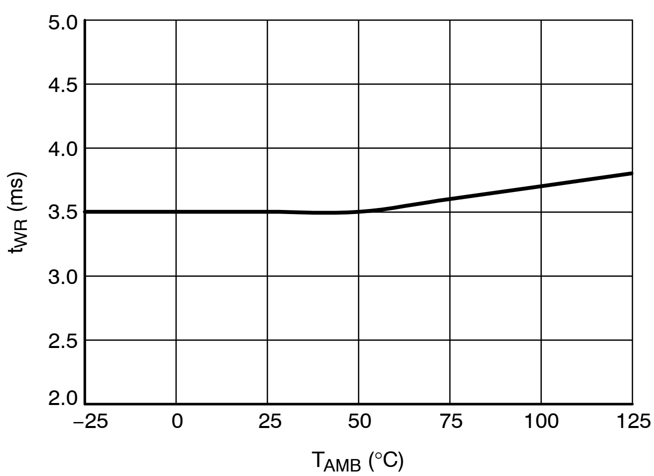


Figure 12. EEPROM Write Time (Rev. B)

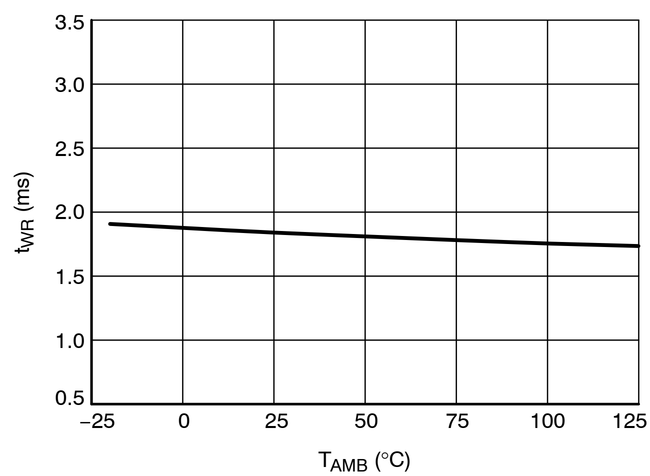


Figure 13. EEPROM Write Time (Rev. C)

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3 V, T_A = −20°C to +125°C, unless otherwise specified.)

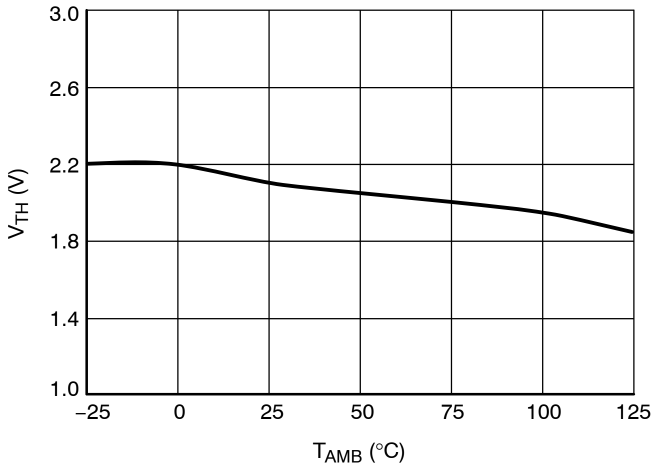


Figure 14. TS POR Threshold Voltage (Rev. B)

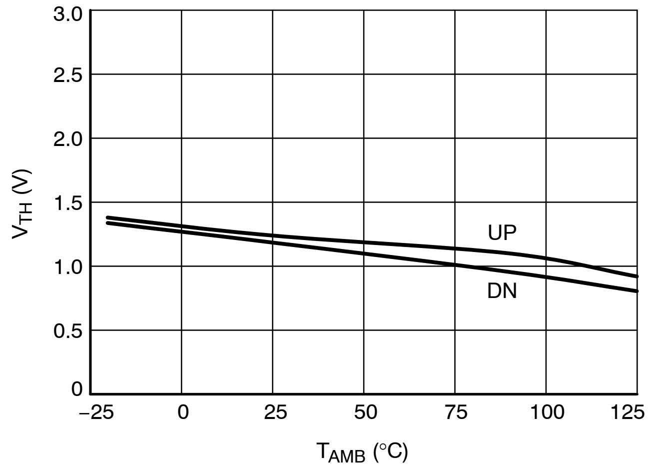


Figure 15. TS POR Threshold Voltage (Rev. C)

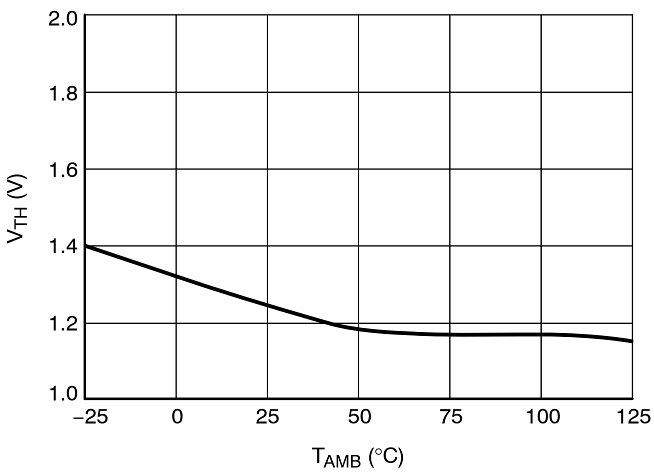


Figure 16. SPD POR Threshold Voltage (Rev. B)

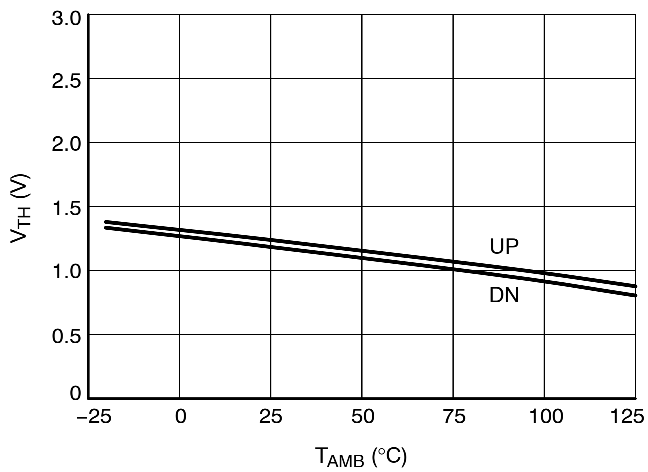


Figure 17. SPD POR Threshold Voltage (Rev. C)

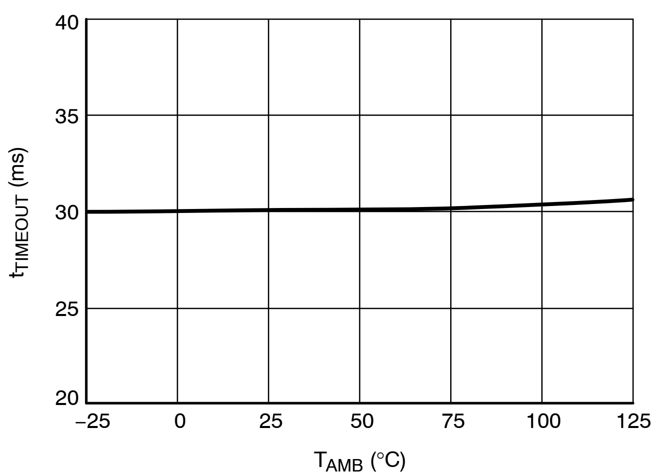


Figure 18. SMBus SCL Clock Low Timeout (Rev. B)

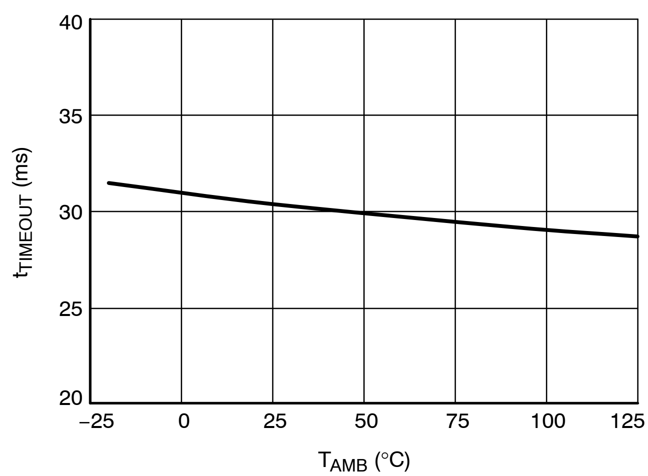


Figure 19. SMBus SCL Clock Low Timeout (Rev. C)

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset (POR)

The CAT34TS02 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to invalid state. The TS component will power up into conversion mode after V_{CC} exceeds the TS POR trigger level and the SPD component will power up into standby mode after V_{CC} exceeds the SPD POR trigger level. Both the TS and SPD components will power down into Reset mode when V_{CC} drops below their respective POR trigger levels. This bi−directional POR behavior protects the CAT34TS02 against brown−out failure following a temporary loss of power. The POR trigger levels are set below the minimum operating V_{CC} level.

Device Interface

The CAT34TS02 supports the Inter−Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34TS02 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34TS02 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

I^2C/SMBus Protocol

The I^2C/SMBus uses two 'wires', one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 20).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake−up' call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address (the preamble) select either the Temperature Sensor (TS) registers (0011) or the EEPROM memory contents (1010), as shown in Figure 21. The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit, R/$\overline{\text{W}}$, specifies whether a Read (1) or Write (0) operation is being performed.

Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9^{th} clock cycle (Figure 22). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9^{th} clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 23.

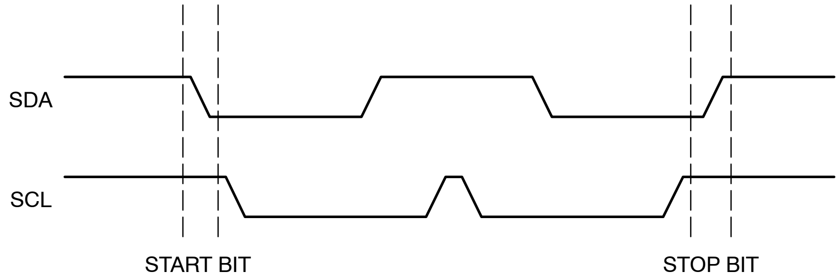


Figure 20. Start/Stop Timing

EEPROM	1	0	1	0	A_2	A_1	A_0	$R/\overline{W}$
TEMPERATURE SENSOR	0	0	1	1	A_2	A_1	A_0	$R/\overline{W}$
	PREAMBLE				DEVICE ADDRESS			

Figure 21. Slave Address Bits

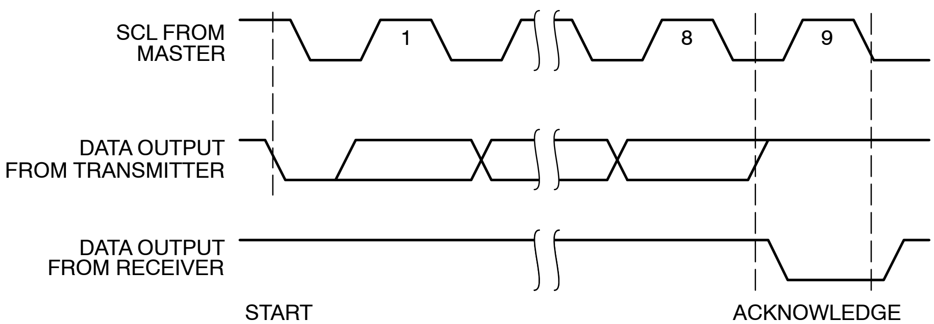


Figure 22. Acknowledge Timing

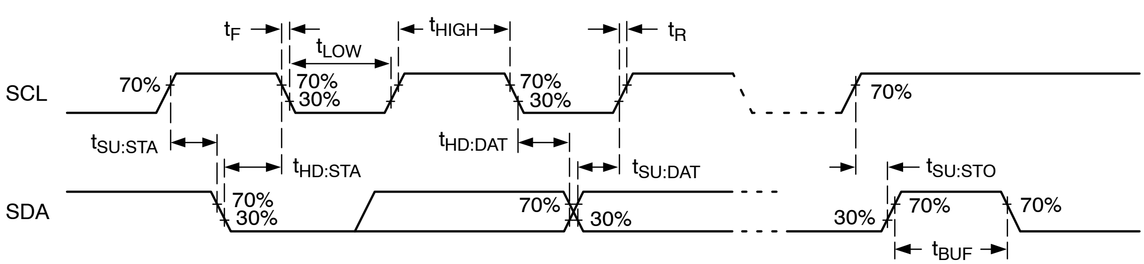


Figure 23. Bus Timing

Write Operations

EEPROM Byte and TS Register Write

To write data to a TS register, or to the on−board EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to '0'), followed by an address byte and data byte(s). The matching Slave will acknowledge the Slave address, EEPROM byte or TS register address and the data byte(s), one for EEPROM data (Figure 24) and two for TS register data (Figure 25). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the (volatile) TS register update or starts the internal Write cycle for the (non−volatile) EEPROM data (Figure 26).

EEPROM Page Write

The on−board EEPROM contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte immediately following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 27).

The internal EEPROM byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be overwritten by later data in a 'wrap−around' fashion within the selected page. The internal Write cycle, using the most recently loaded data, then starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34TS02 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a 'Selective Read' command (see READ OPERATIONS). The CAT34TS02 will not acknowledge the Slave address as long as internal EEPROM Write is in progress.

Delivery State

The CAT34TS02 is shipped 'unprotected', i.e. neither Software Write Protection (SWP) flag is set. The entire 2−Kb memory is erased, i.e. all bytes are 0xFF.

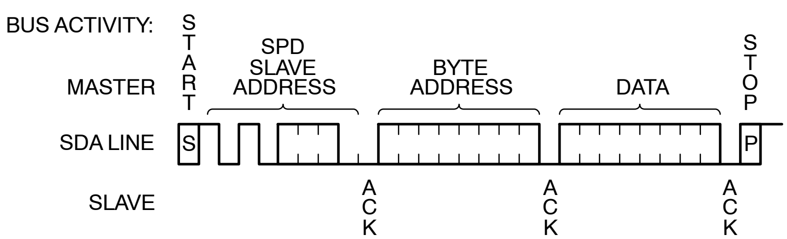


Figure 24. EEPROM Byte Write

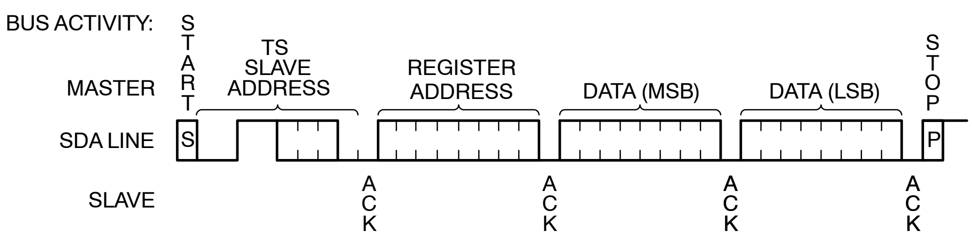


Figure 25. Temperature Sensor Register Write

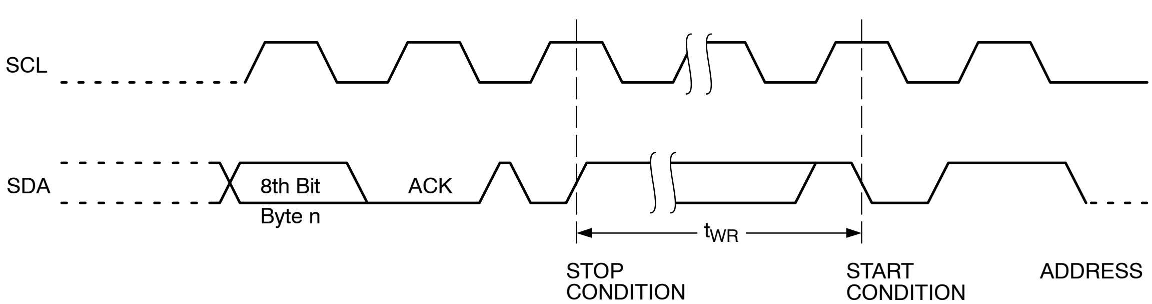
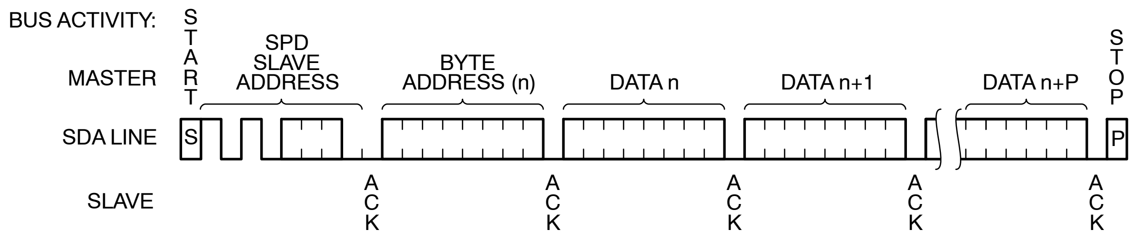


Figure 26. EEPROM Write Cycle Timing



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Figure 27. EEPROM Page Write

Read Operations

Immediate Read

Upon power−up, the address counters for both the Temperature Sensor (TS) and on−board EEPROM are initialized to 00h. The TS address counter will thus point to the Capability Register and the EEPROM address counter will point to the first location in memory. The two address counters may be updated by subsequent operations.

A CAT34TS02 presented with a Slave address containing a '1' in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting data being pointed at by the current EEPROM data or respectively TS register address counter. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 28).

Selective Read

The Read operation can be started at an address different from the one stored in the respective address counters, by preceding the Immediate Read sequence with a 'data less' Write operation. The Master sends out a START, Slave address and address byte, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figure 29).

Sequential EEPROM Read

EEPROM data can be read out indefinitely, as long as the Master responds with ACK (Figure 30). The internal address count is automatically incremented after every data byte sent to the bus. If the end of memory is reached during continuous Read, then the address counter 'wraps−around' to beginning of memory, etc. Sequential Read works with either Immediate Read or Selective Read, the only difference being that in the latter case the starting address is intentionally updated.

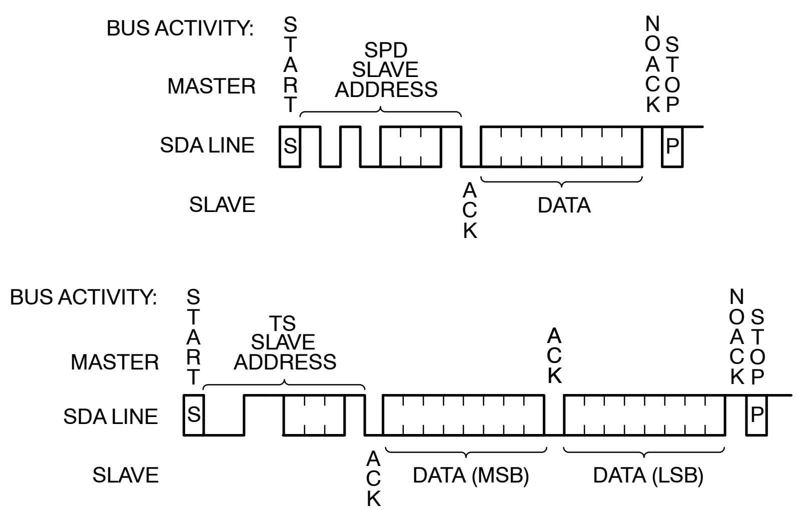


Figure 28. Immediate Read

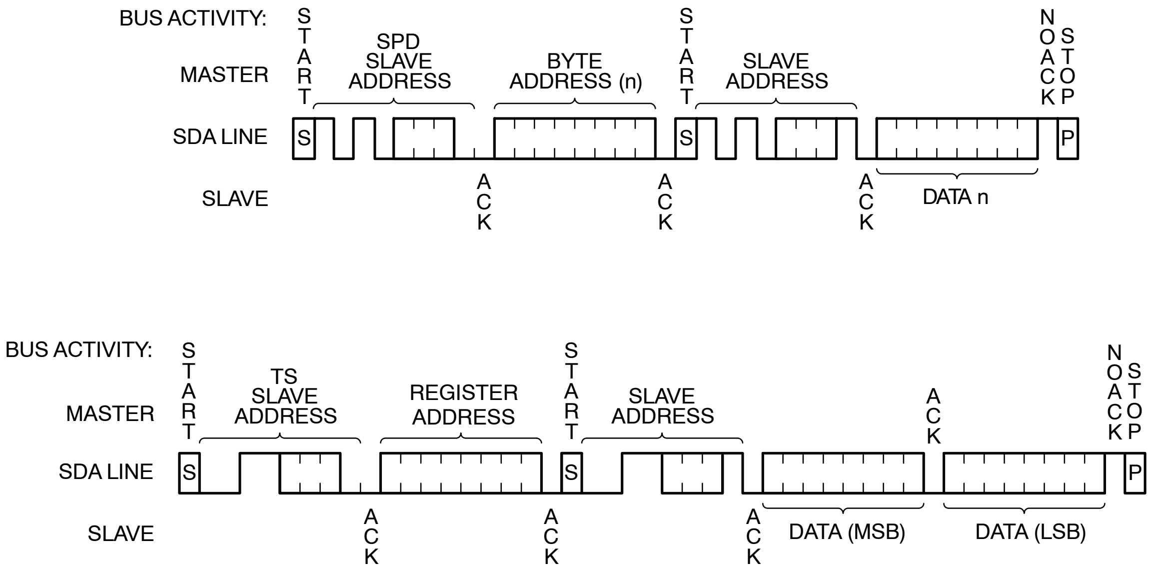


Figure 29. Selective Read

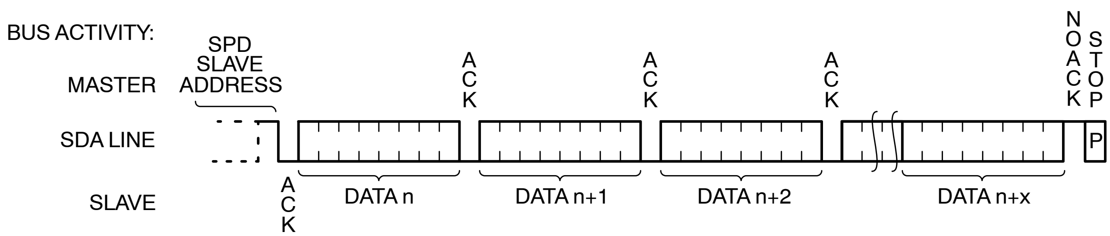


Figure 30. EEPROM Sequential Read

Software Write Protection

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or V_{CC}), whereas the very high voltage V_{HV} must be present on address pin A0 to set, clear or read the Reversible Software Write Protection (**RSWP**) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 7.

The SWP commands are listed in Table 8. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the CAT34TS02. All SWP related Slave addresses use the pre−amble: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any logic level, whereas for **RSWP** commands the address pins must be at pre−assigned logic levels.

V_{HV} is interpreted as logic ‘1’. The V_{HV} condition must be established on pin A0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the CAT34TS02 as a PSWP request.

The SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be ‘1’, and to set or clear a flag, it must be ‘0’. For Write commands a dummy byte address and dummy data byte must be provided (Figure 31). In contrast to a regular memory Read, a SWP Read does not return Data. Instead the CAT34TS02 will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 32).

Table 7. RSWP D.C. OPERATION CONDITION

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive ($V_{HV} - V_{CC}$)	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V

Table 8. SWP COMMANDS

Action	Control Pin Levels (Note 9)			Flag State (Note 10)		Slave Address					ACK ?	Address Byte	ACK ?	Data Byte	ACK ?	Write Cycle
	A_2	A_1	A_0	PSWP	RSWP	b7 to b4	b3	b2	b1	b0						
Set PSWP	A_2	A_1	A_0	1	X	0110	A_2	A_1	A_0	X	No					
	A_2	A_1	A_0	0	X		A_2	A_1	A_0	0	Yes	X	Yes	X	Yes	Yes
	A_2	A_1	A_0	0	X		A_2	A_1	A_0	1	Yes					
Set RSWP	GND	GND	V_{HV}	1	X		0	0	1	X	No					
	GND	GND	V_{HV}	0	1		0	0	1	X	No					
	GND	GND	V_{HV}	0	0		0	0	1	0	Yes	X	Yes	X	Yes	Yes
	GND	GND	V_{HV}	0	0		0	0	1	1	Yes					
Clear RSWP	GND	V_{CC}	V_{HV}	1	X		0	1	1	X	No					
	GND	V_{CC}	V_{HV}	0	X		0	1	1	0	Yes	X	Yes	X	Yes	Yes
	GND	V_{CC}	V_{HV}	0	X		0	1	1	1	Yes					

9. Here A_2, A_1 and A_0 are either at V_{CC} or GND.
10. 1 stands for 'Set', 0 stands for 'Not Set', X stands for 'don't care'.

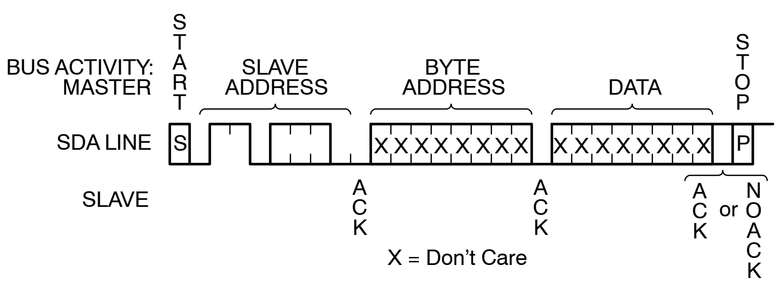


Figure 31. Software Write Protect (Write)

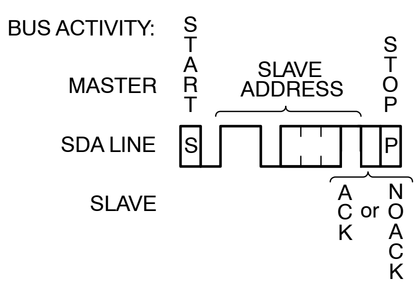


Figure 32. Software Write Protect (Read)

Temperature Sensor Operation

The TS component in the CAT34TS02 combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ−Δ modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

Registers

The CAT34TS02 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 9. Upon power−up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The CAT34TS02 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the $\overline{\text{EVENT}}$ pin. To avoid undesirable $\overline{\text{EVENT}}$ pin activity, this pin is automatically disabled at power−up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two's complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

Temperature Data Register (User Read Only)

This register stores the measured temperature, as well as trip status information. B15, B14, and B13 are the trip status bits, representing the relationship between measured temperature and the 3 limit values; these bits are not affected by EVENT status or by Configuration register settings. Measured temperature is represented by bits B12 to B0. Data format is two's complement, where B12 represents the sign, B11 represents 128°C, etc. and B0 represents 0.0625°C.

Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI−SIG trade organization to the CAT34TS02 device is fixed at 0x1B09.

Device ID and Revision Register (Read Only)

This register contains manufacturer specific device ID and device revision information.

Table 9. THE TS REGISTERS

Register Address	Register Name		Power−On Default	Read/Write
0x00	Capability Register		0x007F	Read
0x01	Configuration Register		0x0000	Read/Write
0x02	High Limit Register		0x0000	Read/Write
0x03	Low Limit Register		0x0000	Read/Write
0x04	Critical Limit Register		0x0000	Read/Write
0x05	Temperature Data Register		Undefined	Read
0x06	Manufacturer ID Register		0x1B09	Read
0x07	Device ID/Revision Register	Rev. B	0x0813	Read
		Rev. C	0x0A00	

Table 10. CAPABILITY REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
EVSD	TMOUT	RFU	TRES [1:0]		RANGE	ACC	EVENT

Bit	Description
B15:B8	Reserved for future use; can not be written; should be ignored; will read as 0
B7 (Note 11)	0: Configuration Register bit 4 is frozen upon Configuration Register bit 8 being set (i.e. a TS shut−down freezes the $\overline{\text{EVENT}}$ output) 1: Configuration Register bit 4 is cleared upon Configuration Register bit 8 being set (i.e. a TS shut−down de−asserts the $\overline{\text{EVENT}}$ output)
B6	0: The TS implements SMBus time−out within the range 10 to 60 ms 1: The TS implements SMBus time−out within the range 25 to 35 ms
B5	0: Pin A_0 V_{HV} compliance required for RSWP Write/Clear operations not explicitly stated 1: Pin A_0 V_{HV} compliance required for RSWP Write/Clear operations explicitly stated
B4:B3	00: LSB = 0.50°C (9 bit resolution) 01: LSB = 0.25°C (10 bit) 10: LSB = 0.125°C (11 bit) 11: LSB = 0.0625°C (12 bit)
B2	0: Positive Temperature Only 1: Positive and Negative Temperature
B1	0: ±2°C over the active range and ±3°C over the operating range (Class C) 1: ±1°C over the active range and ±2°C over the monitor range (Class B)
B0	0: Critical Temperature only 1: Alarm and Critical Temperature

11. Configuration Register bit 4 can be cleared (but not set) after Configuration Register bit 8 is set, by writing a “1” to Configuration Register bit 5 ($\overline{\text{EVENT}}$ output can be de-asserted during TS shut-down periods)

Table 11. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Bit	Description
B15:B11	Reserved for future use; can not be written; should be ignored; will read as 0
B10:B9 (Note 12)	00: Disable hysteresis 01: Set hysteresis at 1.5°C 10: Set hysteresis at 3°C 11: Set hysteresis at 6°C
B8 (Note 16)	0: Thermal Sensor is enabled; temperature readings are updated at sampling rate 1: Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN
B7 (Note 15)	0: Critical trip register can be updated 1: Critical trip register cannot be modified; this bit can be cleared only at POR
B6 (Note 15)	0: Alarm trip registers can be updated 1: Alarm trip registers cannot be modified; this bit can be cleared only at POR
B5 (Note 14)	0: Always reads as 0 (self−clearing) 1: Writing a 1 to this position clears an event recording in interrupt mode only
B4 (Note 13)	0: EVENT output pin is not being asserted 1: EVENT output pin is being asserted
B3 (Note 12)	0: EVENT output disabled; *polarity dependent*: open−drain for **B1** = 0; grounded for **B1** = 1 1: EVENT output enabled
B2 (Note 18)	0: event condition triggered by alarm or critical temperature limit crossing 1: event condition triggered by critical temperature limit crossing only
B1 (Notes 12, 17)	0: EVENT output active low 1: EVENT output active high
B0 (Note 12)	0: Comparator mode 1: Interrupt mode

12. Can not be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.
13. This bit is a *polarity independent* 'software' copy of the $\overline{\text{EVENT}}$ pin, i.e. it is under the control of B3. This bit is read−only.
14. Writing a '1' to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 24).
15. Cleared at power-on reset (POR). Once set, this bit can only be cleared by a POR condition.
16. The TS powers up into active mode, i.e. this bit is cleared at power-on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS can not be shut down (B8 can not be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.
17. The $\overline{\text{EVENT}}$ output is "open-drain" and requires an external pull-up resistor for either polarity. The "natural" polarity is "active low", as it allows "wired-or" operation on the EVENT bus.
18. Can not be set as long as lock bit B6 is set.

Table 12. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 13. LOW LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 14. TCRIT LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 15. TEMPERATURE DATA REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C (Note 19)	0.125°C (Note 19)	0.0625°C (Note 19)

19. When applicable (as defined by Capability bit TRES), unsupported bits will read as 0

Bit	Description
B15	0: Temperature is below the TCRIT limit 1: Temperature is equal to or above the TCRIT limit
B14	0: Temperature is equal to or below the High limit 1: Temperature is above the High limit
B13	0: Temperature is equal to or above the Low limit 1: Temperature is below the Low limit
B12	0: Positive temperature 1: Negative temperature

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 16. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

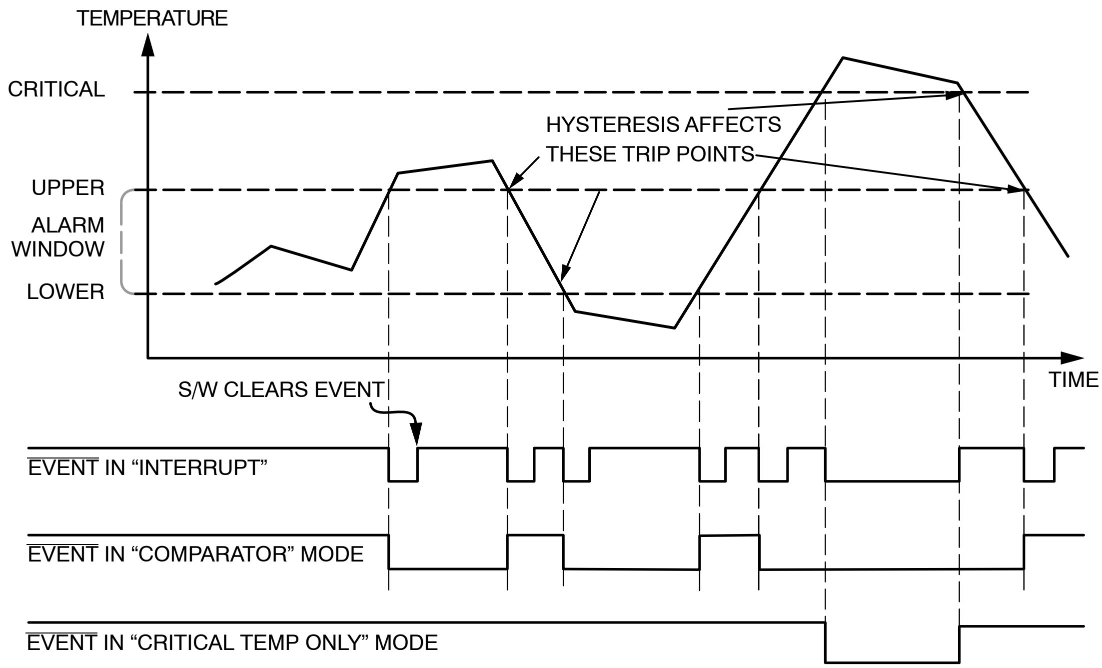
The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 33, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the enabled $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. When the temperature exceeds the critical limit, the event remains asserted as long as the temperature stays above the critical limit and can not be cleared.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 34.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT34TS02 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.



*$\overline{\text{EVENT}}$ cannot be cleared once the DUT temperature is greater than the critical temperature

Figure 33. Event Detail

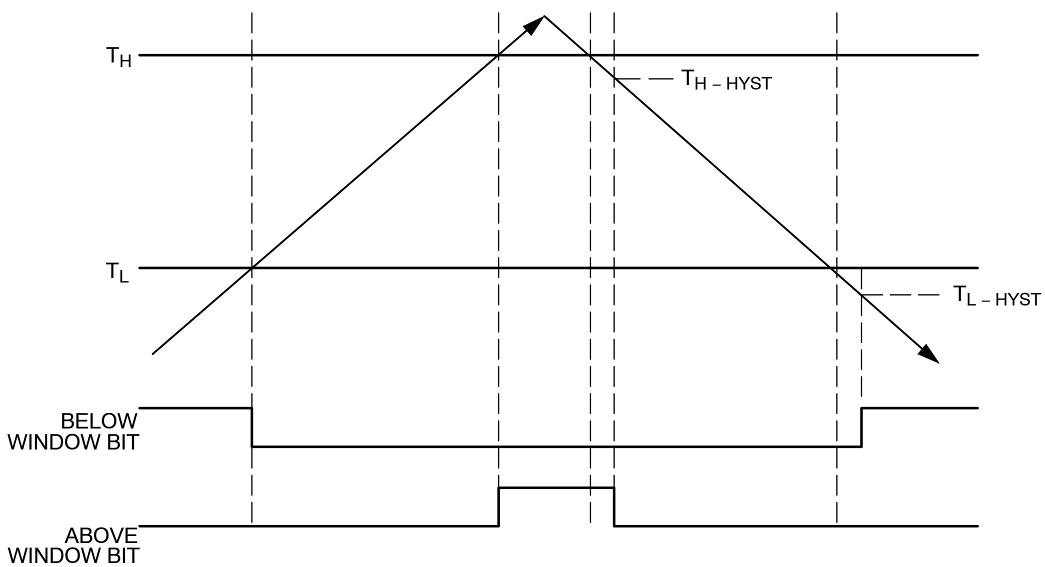
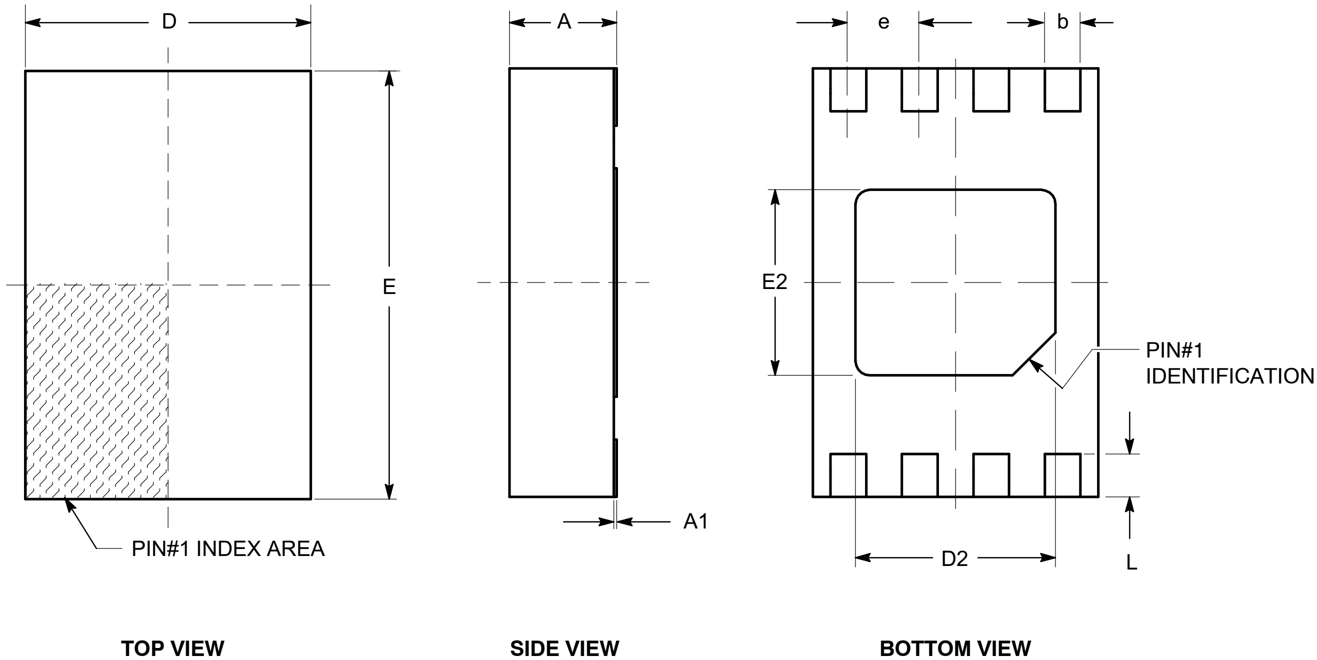


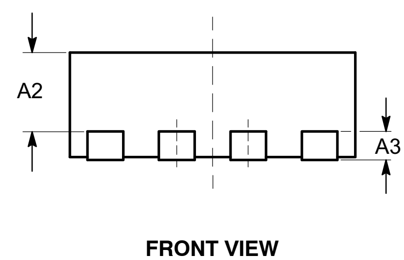
Figure 34. Hysteresis Detail

PACKAGE DIMENSIONS

TDFN8, 2x3
CASE 511AK
ISSUE A



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3	0.20 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e	0.50 TYP		
L	0.20	0.30	0.40



Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

Example of Ordering Information

Device Order Number	Specific Device Marking	Package Type	Lead Finish	Shipping	Device Revision
CAT34TS02VP2GT4B (Not recommended for new designs.)	GTB	TDFN−8	NiPdAu	Tape & Reel, 4,000 Units / Reel	B
CAT34TS02VP2GT4C	GTC	TDFN−8	NiPdAu	Tape & Reel, 4,000 Units / Reel	C

20. All packages are RoHS−compliant (Lead−free, Halogen−free)
21. The standard lead finish is NiPdAu.
22. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.