

MAX5487PMB1 Peripheral Module

General Description

The MAX5487PMB1 peripheral module provides the necessary hardware to interface the MAX5487 dual linear-taper digital potentiometer to any system that utilizes Pmod™-compatible expansion ports configurable for SPI communication. These digital potentiometers function like mechanical potentiometers with a simple 3-wire SPI-compatible interface that programs the wipers to any one of 256 tap positions. The terminals of each potentiometer are available at the output connector for attachment to external circuitry.

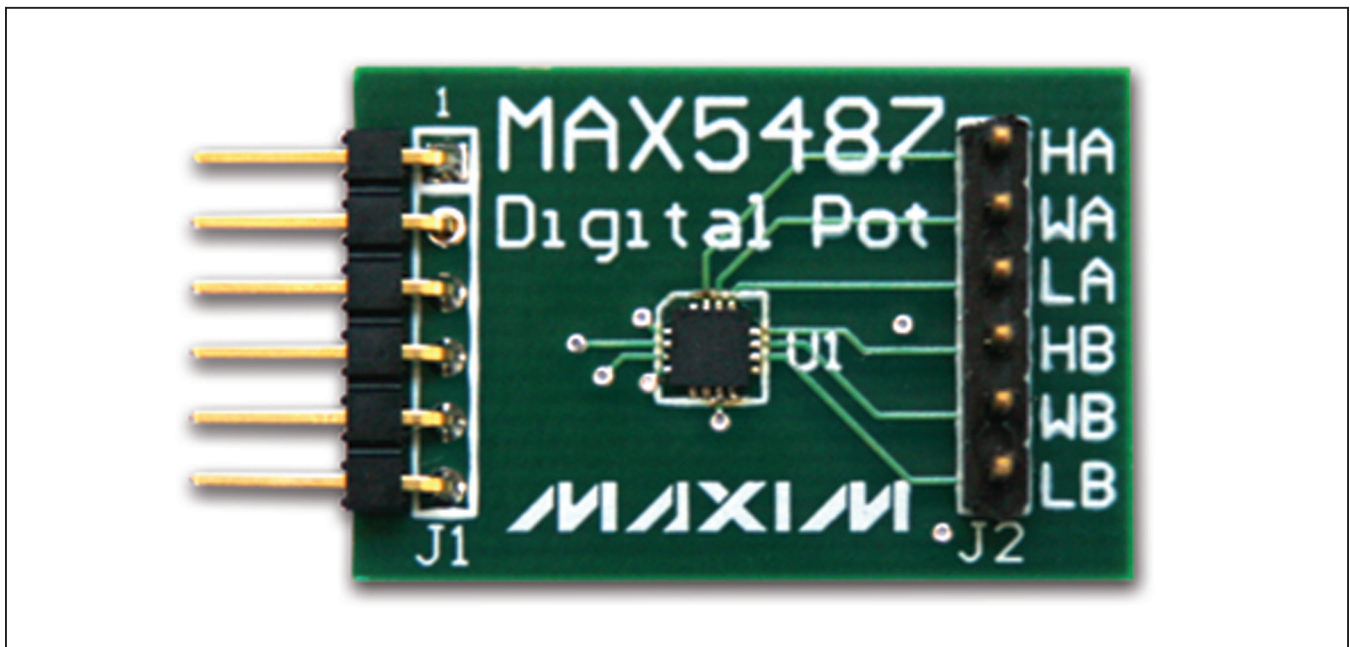
Refer to the MAX5487/MAX5488/MAX5489 IC data sheet for detailed information regarding operation of the IC.

Features

- ◆ Dual, 256-Tap, Linear-Taper 10kΩ Digital Potentiometers
- ◆ Wiper Position Stored in Nonvolatile Memory (EEPROM) and Recalled on Power-Up or by an Interface Command
- ◆ IC is Pin-Compatible with 50kΩ (MAX5488) and 100kΩ Versions (MAX5489)
- ◆ Solder Links Allowing Configuration as Variable Resistors
- ◆ 6-Pin Pmod-Compatible Connector (SPI)
- ◆ Example Software Written in C for Portability
- ◆ RoHS Compliant
- ◆ Proven PCB Layout
- ◆ Fully Assembled and Tested

[Ordering Information](#) appears at end of data sheet.

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Pmod is a trademark of Digilent Inc.

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Component List

DESIGNATION	QTY	DESCRIPTION
C1	1	0.1μF ±10%, 16V X7R ceramic capacitor (0603) Murata GRM188R71C104KA01D
J1	1	6-pin right-angle male header
J2	1	6-pin straight male header

DESIGNATION	QTY	DESCRIPTION
R1, R2, R3	3	150Ω ±5% resistors (0603)
U1	1	Dual, nonvolatile, 10kΩ digital potentiometer (16 TQFN-EP*) Maxim MAX5487ETE+
—	1	PCB: EPCB5487PM1

*EP = Exposed pad.

Component Supplier

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com

Note: Indicate that you are using the MAX5487PMB1 when contacting this component supplier.

Detailed Description

SPI Interface

The MAX5487PMB1 peripheral module can plug directly into a Pmod-compatible port (configured for SPI) through connector J1. For information on the SPI protocol, refer to the MAX5487/MAX5488/MAX5489 IC data sheet.

J1 provides connection of the module to the Pmod host. The pin functions and pin assignments adhere to the Pmod standard recommended by Digilent Inc. See Table 1.

Connector J2 provides connection to the potentiometers. See Table 2.

Software and FPGA Code

Example software and drivers are available that execute directly without modification on several FPGA development boards that support an integrated or synthesized microprocessor. These boards include the Digilent Nexys 3, Avnet LX9, and Avnet ZEDBoard, although other platforms can be added over time. Maxim provides complete Xilinx ISE projects containing HDL, Platform Studio, and SDK projects. In addition, a synthesized bit stream, ready for FPGA download, is provided for the demonstration application.

The software project (for the SDK) contains several source files intended to accelerate customer evaluation and design. These include a base application (maximModules.c) that demonstrates module functionality and uses an API interface (maximDeviceSpecificUtilities.c) to set and access Maxim device functions within a specific module.

Table 1. Connector J1 (SPI Communication)

PIN	SIGNAL	DESCRIPTION
1	\overline{SS}	Chip enable. Must be asserted low to enable the SPI interface.
2	MOSI	MAX5487 serial-data input
3	N.C.	Not connected
4	SCK	MAX5487 serial-clock input
5	GND	Ground
6	VCC	Power supply

Table 2. Connector J2 (SPI Communication)

PIN	SIGNAL	DESCRIPTION
1	HA	High terminal of resistor A
2	WA	Wiper terminal of resistor A
3	LA	Low terminal of resistor A
4	HB	High terminal of resistor B
5	WB	Wiper terminal of resistor B
6	LB	Low terminal of resistor B

The source code is written in standard ANSI C format, and all API documentation including theory/operation, register description, and function prototypes are documented in the API interface file (maximDeviceSpecificUtilities.h & .c).

The complete software kit is available for download at www.maxim-ic.com. Quick start instructions are also available as a separate document.

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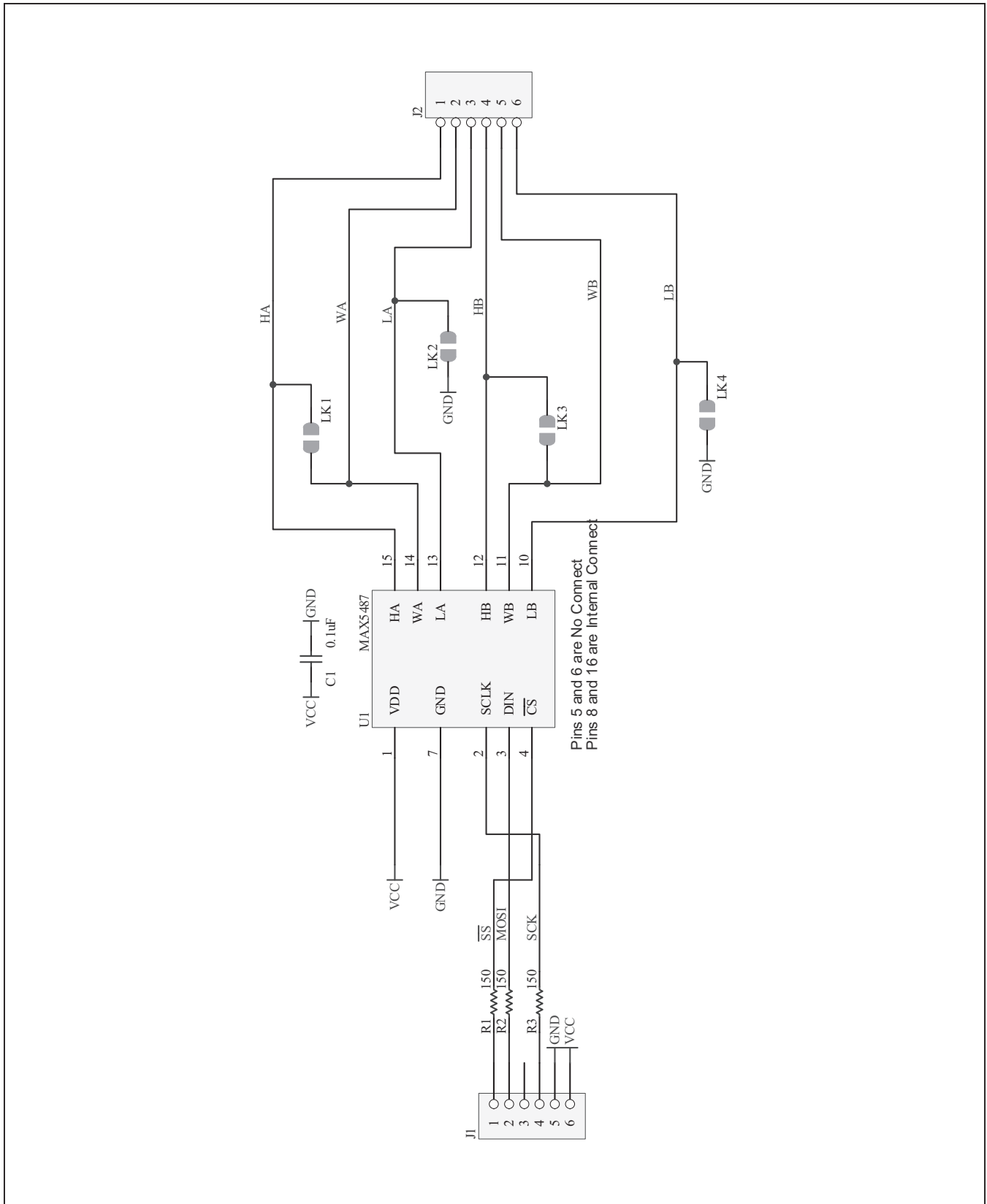


Figure 1. MAX5487PMB1 Peripheral Module Schematic

MAX5487PMB1 Peripheral Module

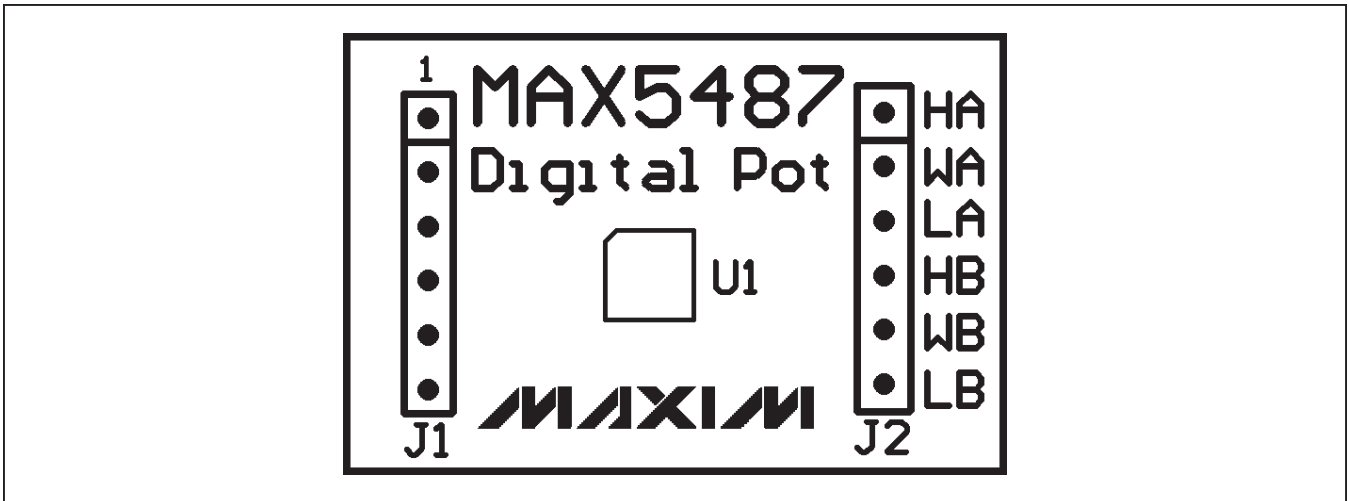


Figure 2. MAX5487PMB1 Peripheral Module Component Placement Guide—Component Side

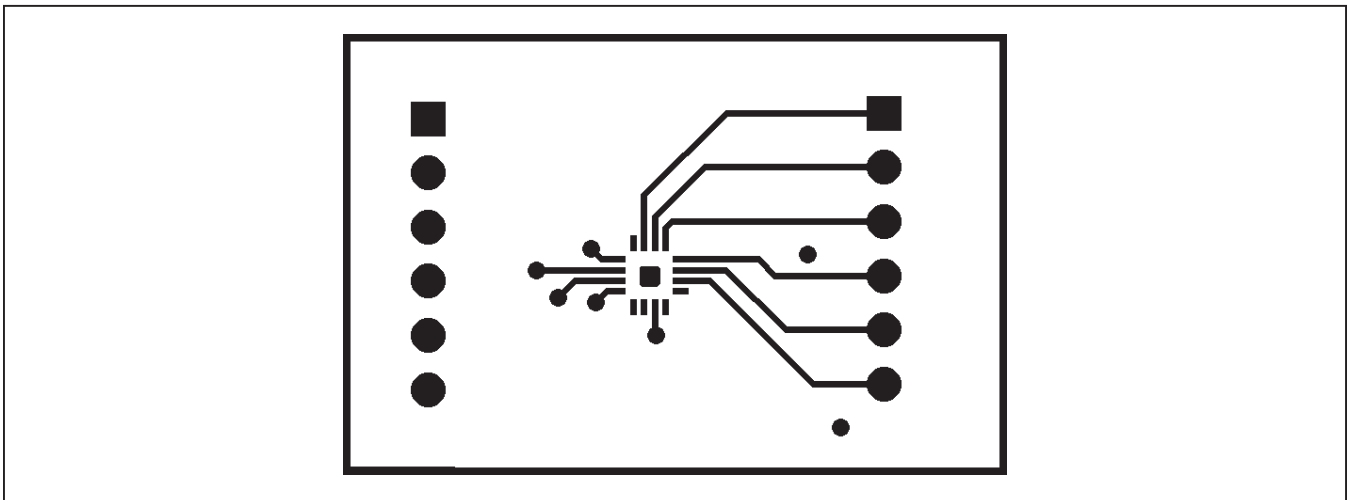


Figure 3. MAX5487PMB1 Peripheral Module PCB Layout—Component Side

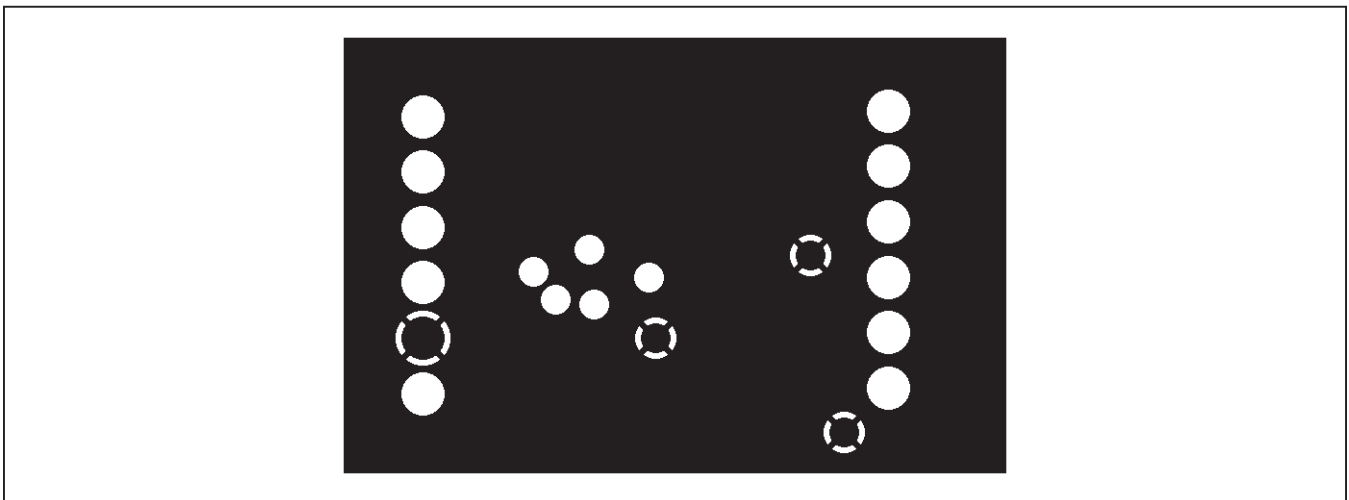


Figure 4. MAX5487PMB1 Peripheral Module PCB Layout—Inner Layer 1 (Ground)

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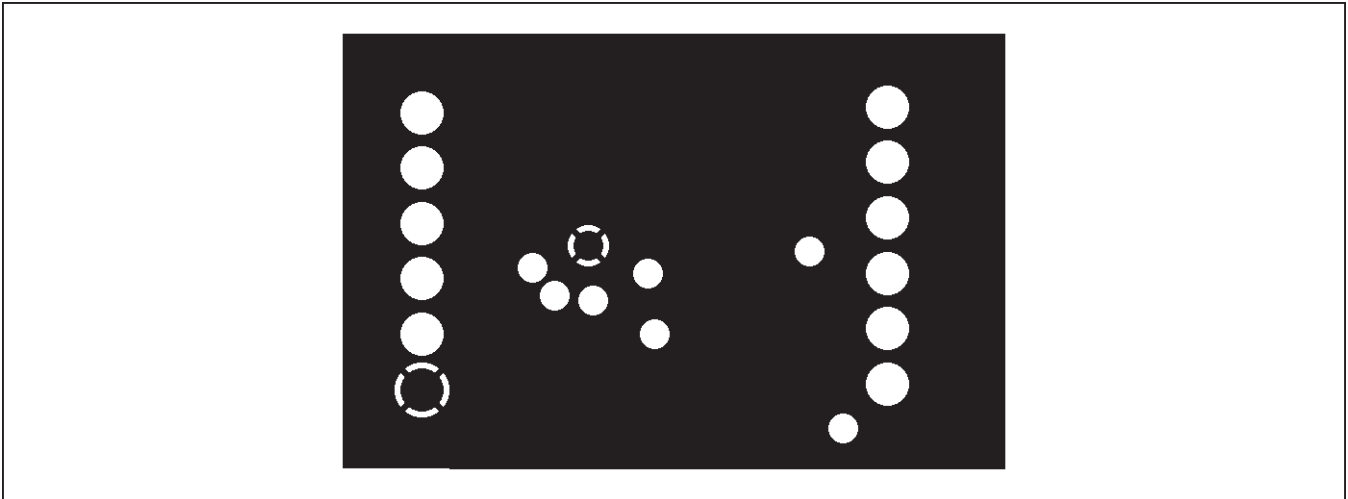


Figure 5. MAX5487PMB1 Peripheral Module PCB Layout—Inner Layer 2 (Power)

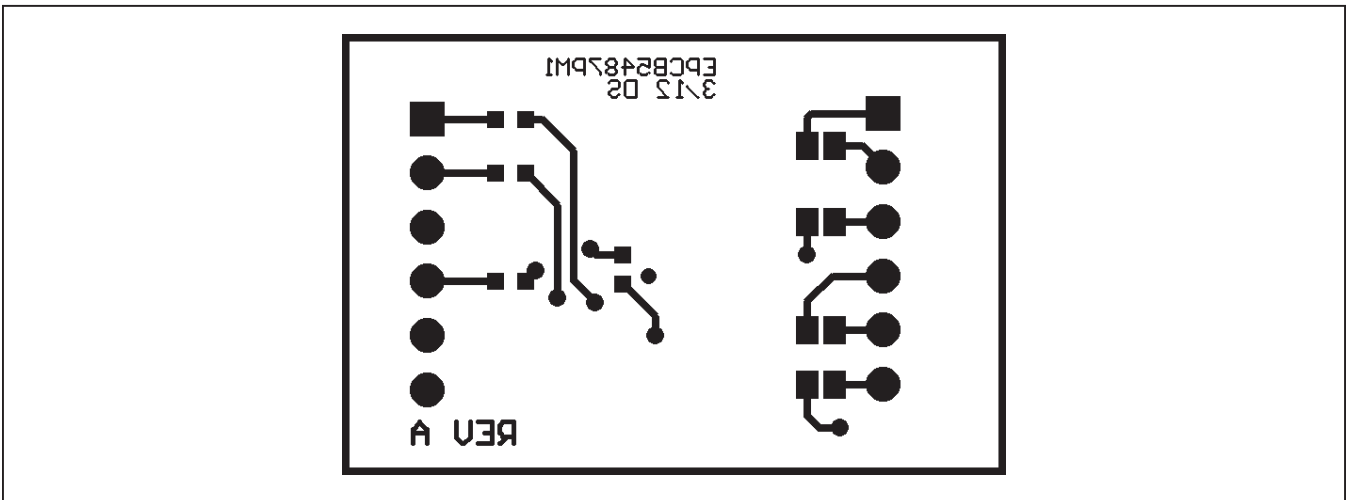


Figure 6. MAX5487PMB1 Peripheral Module PCB Layout—Solder Side

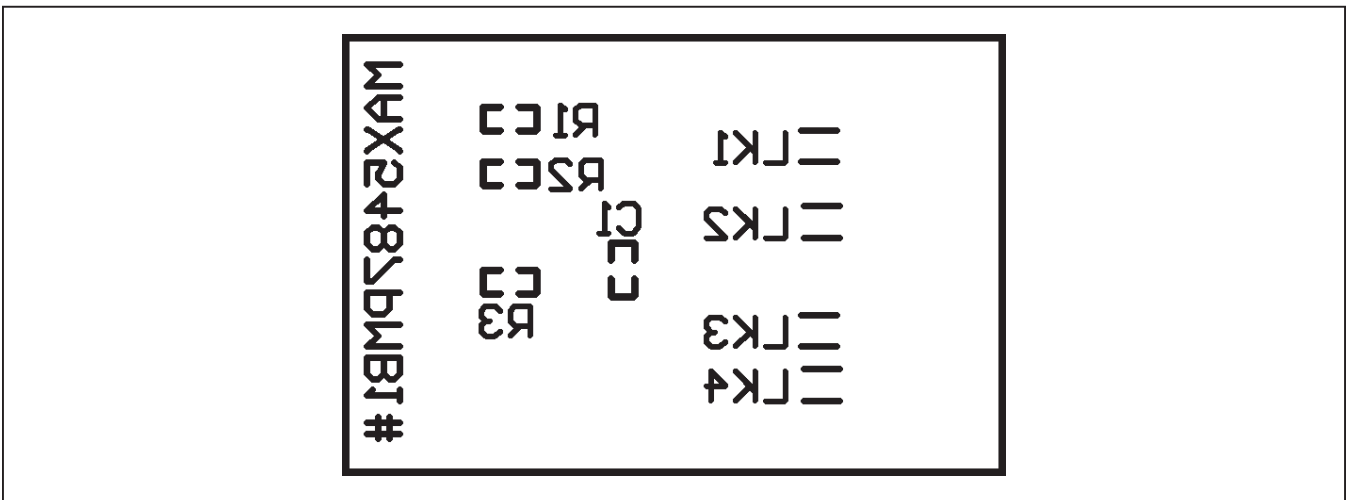


Figure 7. MAX5487PMB1 Peripheral Module Component Placement Guide—Solder Side

MAX5487PMB1 Peripheral Module

Ordering Information

PART	TYPE
MAX5487PMB1#	Peripheral Module

#Denotes RoHS compliant.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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