



# PMCM4401UNE

20 V, N-channel Trench MOSFET

29 May 2017

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a 4 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Ultra small package: 0.78 x 0.78 x 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

## 3. Applications

- Battery switch
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

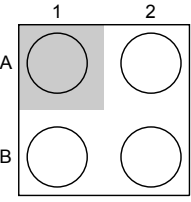
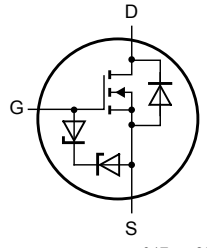
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	5.4	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ °C}$	-	43	52	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>

### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	 <p>Transparent top view <b>WLCSP4 (WLCSP4_2-2)</b></p>	 <p>017aaa255</p>
A2	S	source		
B1	D	drain		
B2	S	source		

### 6. Ordering information

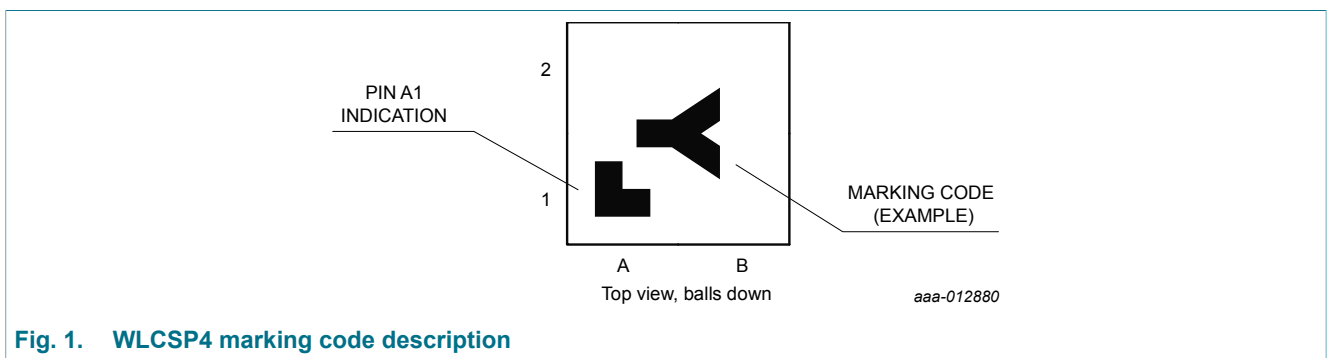
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM4401UNE	WLCSP4	wafer level chip-size package; 4 bumps (2 x 2)	WLCSP4_2-2

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM4401UNE	R



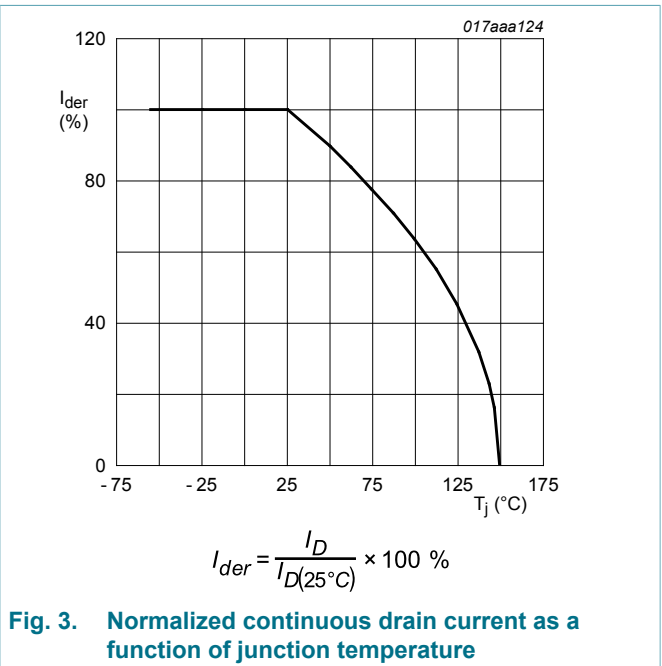
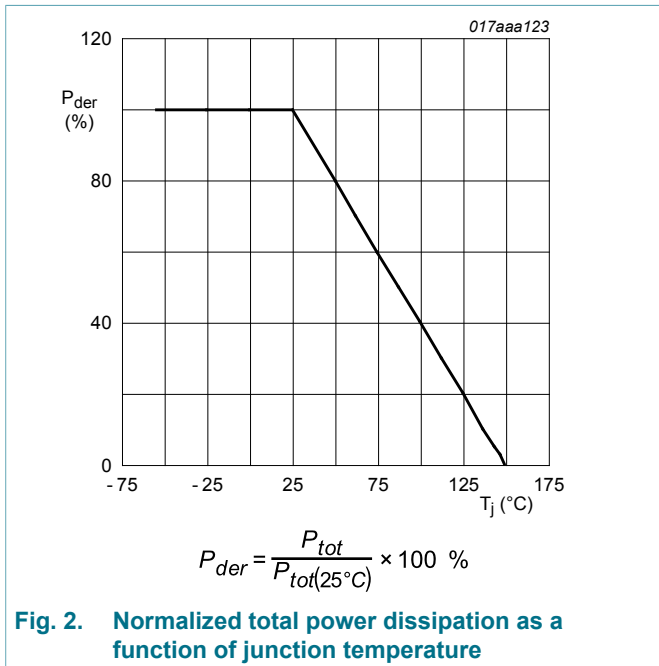
## 8. Limiting values

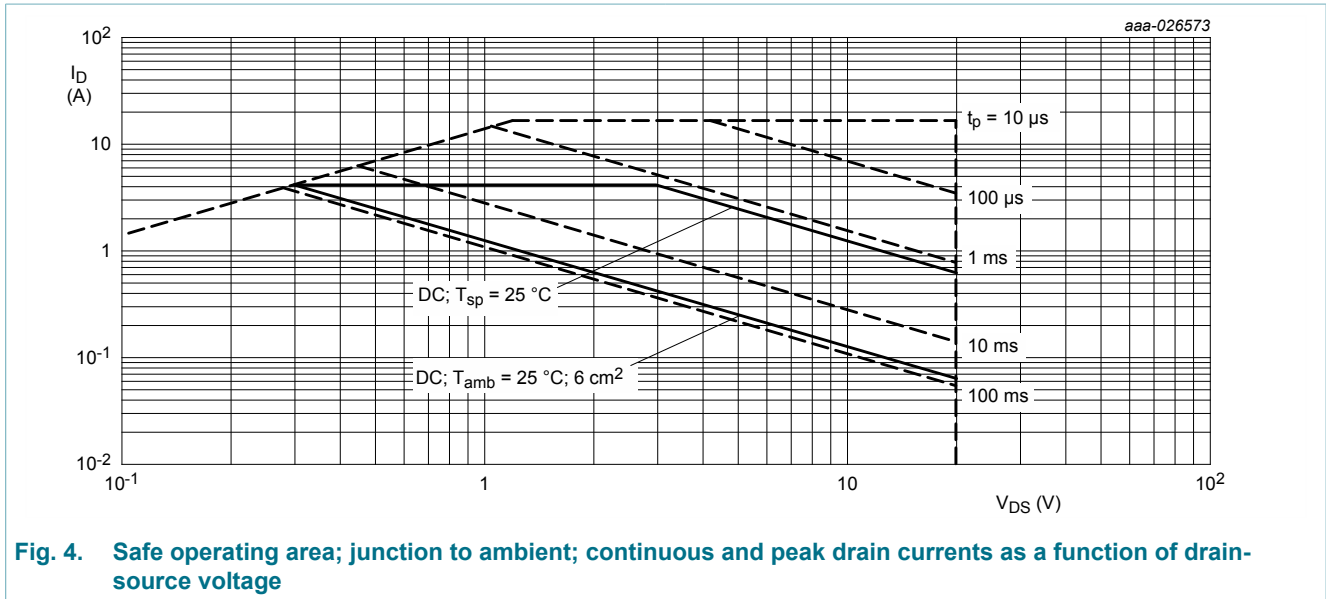
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	20	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	5.4	A
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	4.2	A
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	2.7	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	17	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	400	mW
			[1]	-	1.3	W
		T <sub>sp</sub> = 25 °C		-	12.5	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.2	A

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.



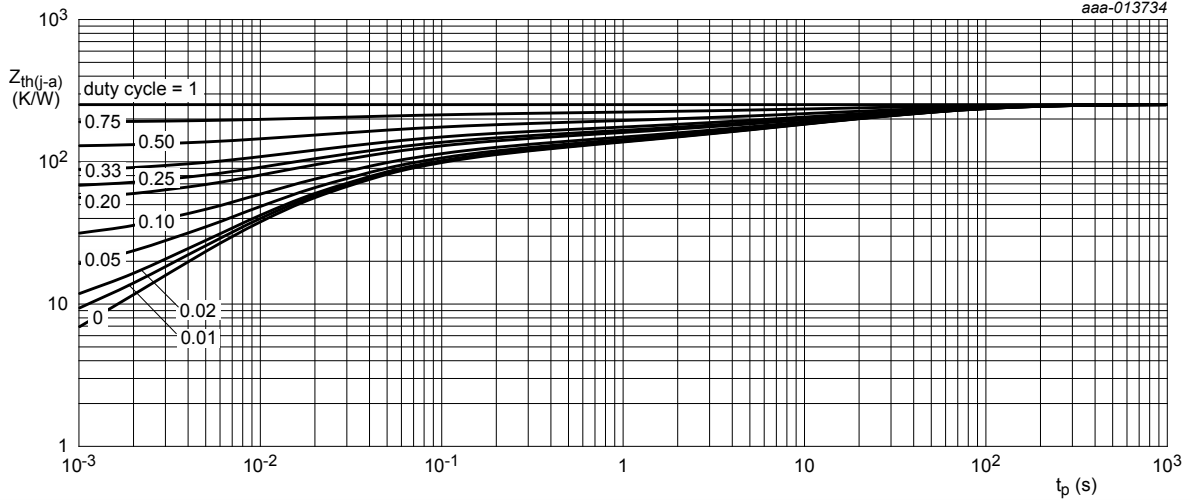


## 9. Thermal characteristics

Table 6. Thermal characteristics

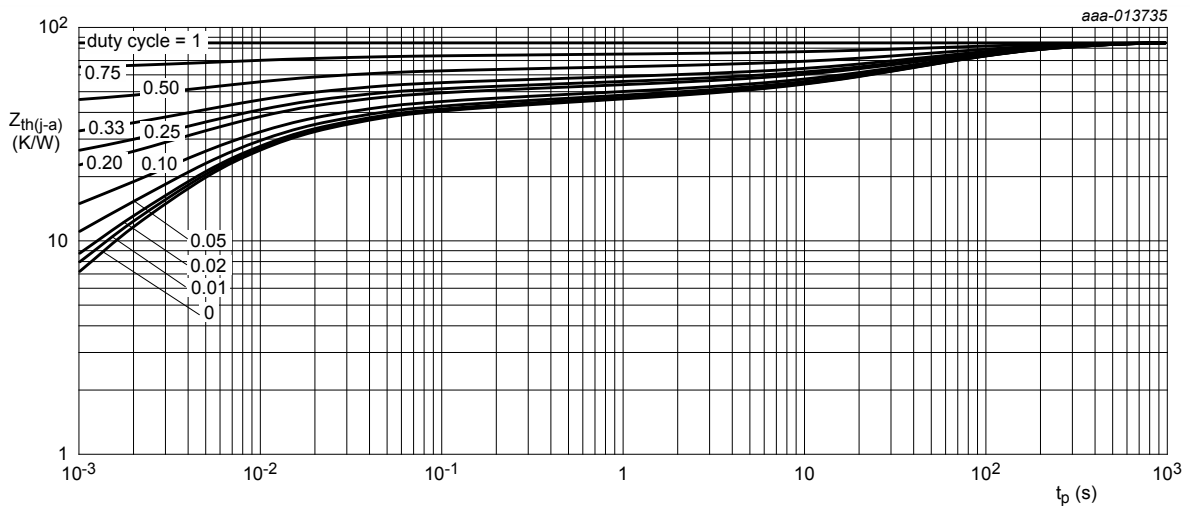
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	250	300	K/W
			[2]	-	70	85	K/W
			[3]	-	85	100	K/W
		t ≤ 5 s	[3]	-	50	60	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided-copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain, 4 layer, 1 cm<sup>2</sup>
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain  $6\text{ cm}^2$

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	0.4	0.6	0.9	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{GS} = 2.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	200	nA
		$V_{GS} = -2.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-200	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 3 A$ ; $T_j = 25 \text{ }^\circ C$	-	43	52	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 3 A$ ; $T_j = 150 \text{ }^\circ C$	-	60	71	m $\Omega$
		$V_{GS} = 2.5 V$ ; $I_D = 3 A$ ; $T_j = 25 \text{ }^\circ C$	-	55	64	m $\Omega$
		$V_{GS} = 1.8 V$ ; $I_D = 1 A$ ; $T_j = 25 \text{ }^\circ C$	-	65	85	m $\Omega$
		$V_{GS} = 1.5 V$ ; $I_D = 0.1 A$ ; $T_j = 25 \text{ }^\circ C$	-	75	120	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 5 V$ ; $I_D = 3 A$ ; $T_j = 25 \text{ }^\circ C$	-	22	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$	-	4.6	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V$ ; $I_D = 4 A$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	6.2	9	nC
$Q_{GS}$	gate-source charge		-	0.4	-	nC
$Q_{GD}$	gate-drain charge		-	2	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	315	-	pF
$C_{oss}$	output capacitance		-	70	-	pF
$C_{rss}$	reverse transfer capacitance		-	65	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V$ ; $I_D = 4 A$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	4.4	-	ns
$t_r$	rise time		-	23	-	ns
$t_{d(off)}$	turn-off delay time		-	27	-	ns
$t_f$	fall time		-	10	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.2 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.7	1.2	V

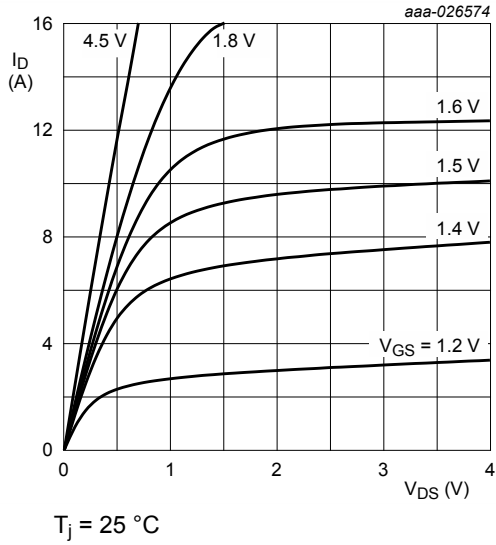


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

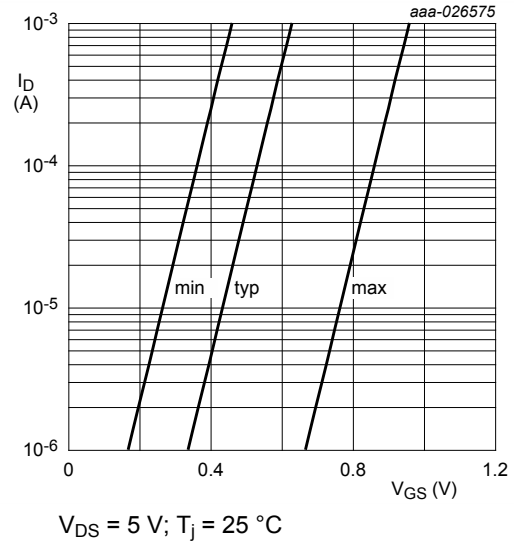


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

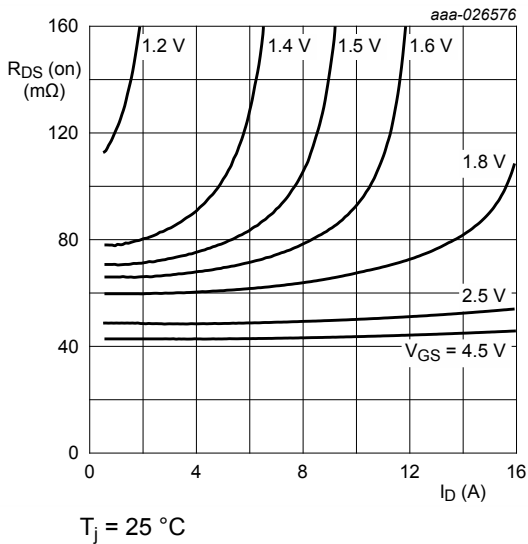


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

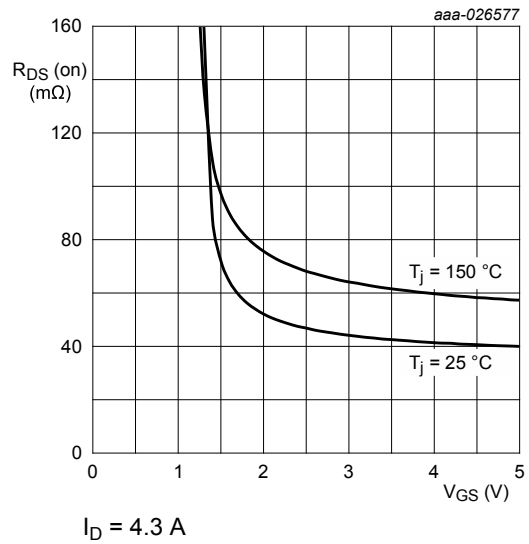
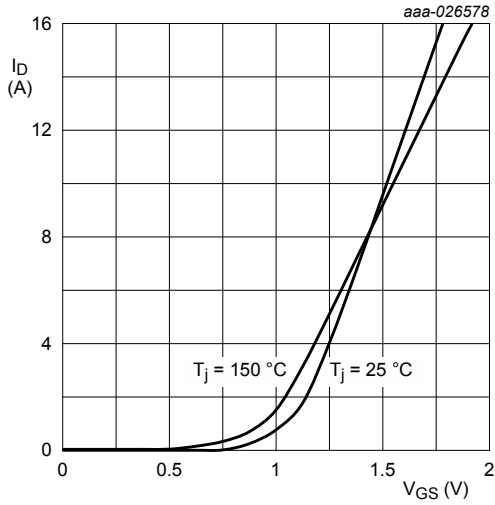
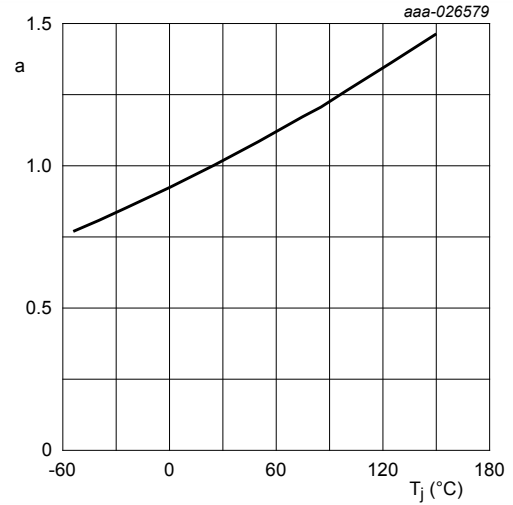


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



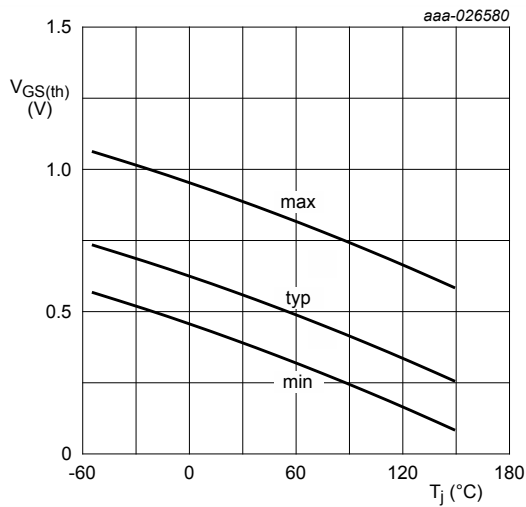
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics; drain current as a function of gate-source voltage; typical values



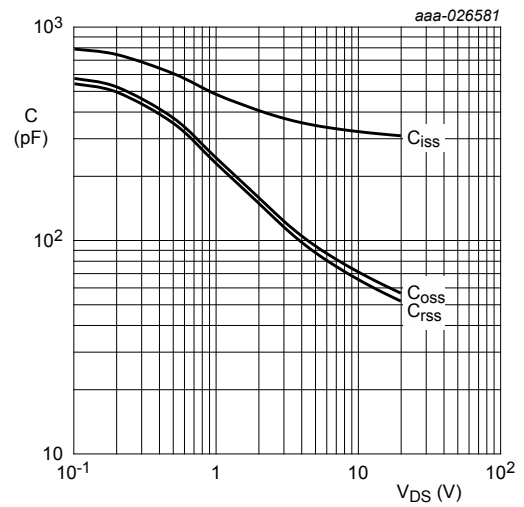
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$$I_D = 250 \mu A; V_{DS} = V_{GS}$$

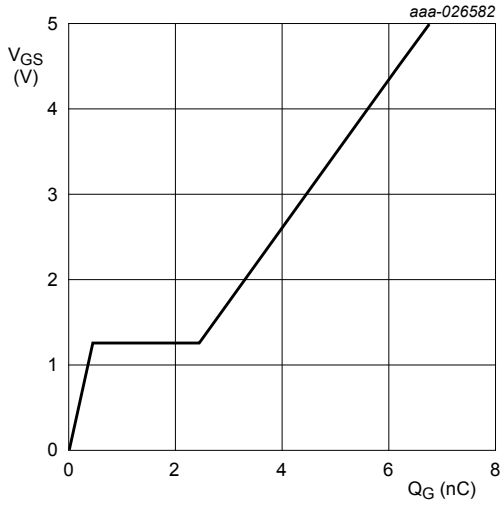
Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$V_{DS} = 10 \text{ V}; I_D = 4 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

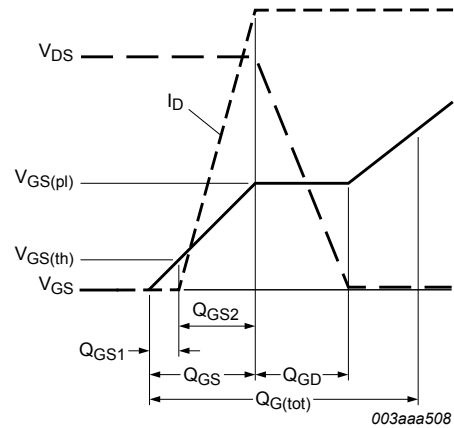
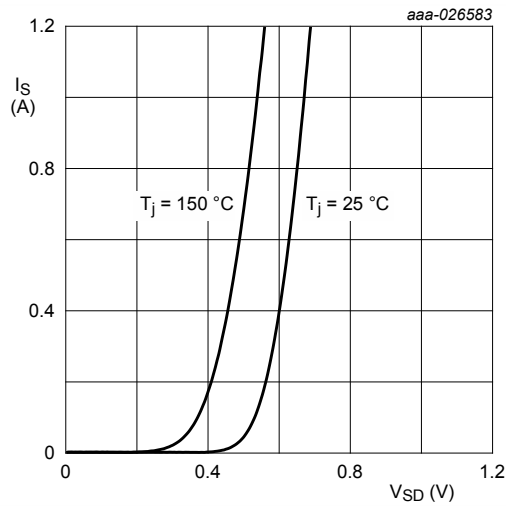


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

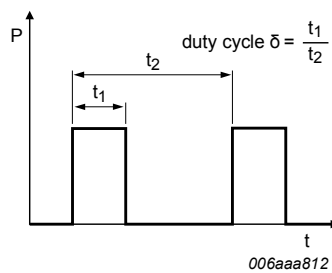
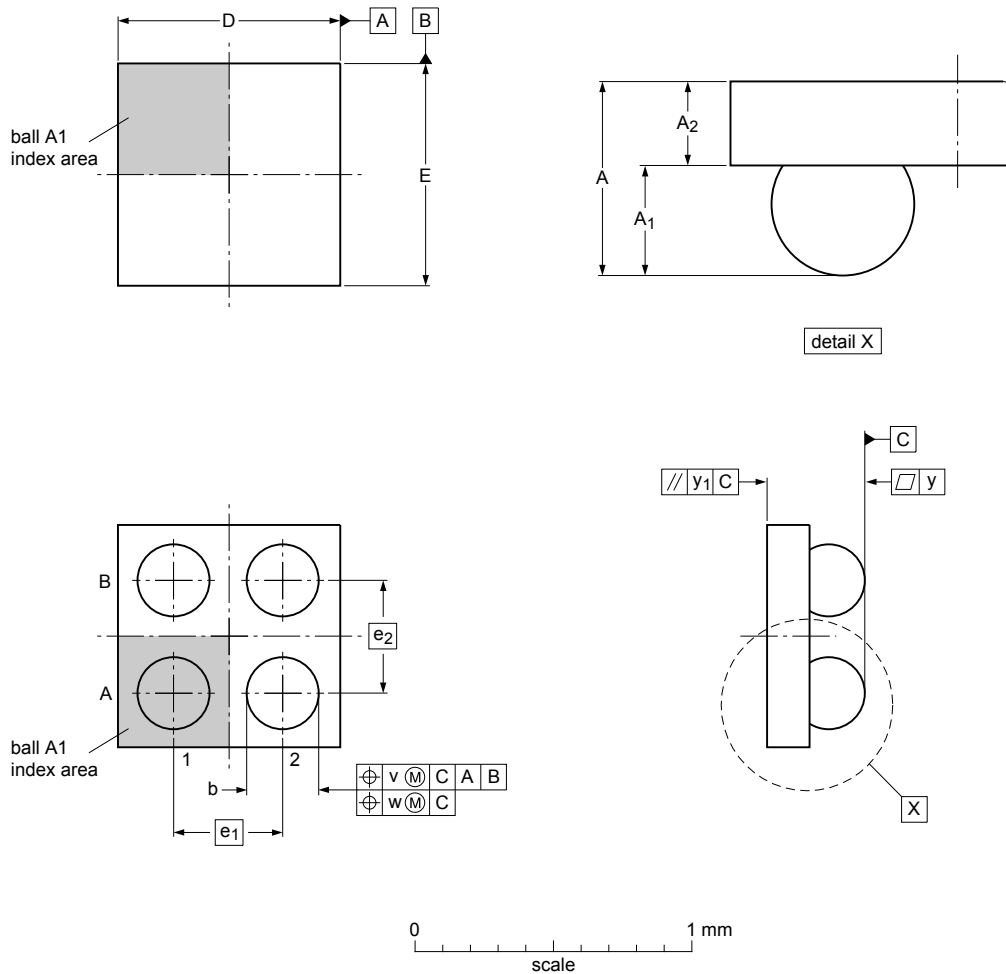


Fig. 18. Duty cycle definition

## 12. Package outline

WLCSP4: wafer level chip-size package; 4 bumps (2 x 2)

WLCSP4\_2-2



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e <sub>1</sub>	e <sub>2</sub>	v	w	y
max	0.375	0.215	0.160	0.275	0.81	0.81					
nom	0.345	0.200	0.145	0.260	0.78	0.78	0.40	0.40	0.15	0.05	0.05
min	0.315	0.185	0.130	0.245	0.75	0.75					

**Note**

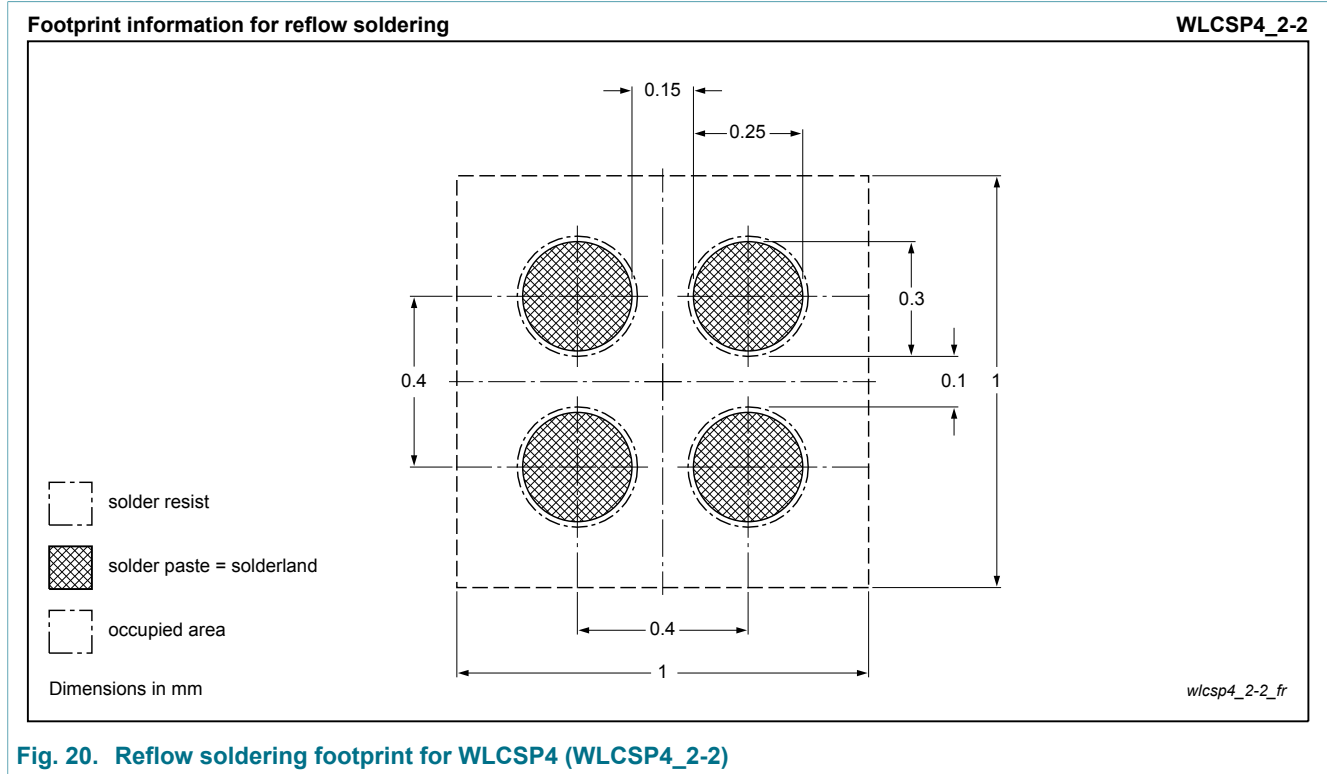
Device back is metal coated on Drain potential.

wlcs4\_2-2\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
WLCSP4_2-2					<del>17-04-26</del> 17-05-03

Fig. 19. Package outline WLCSP4 (WLCSP4\_2-2)

### 13. Soldering



## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM4401UNE v.1	20170529	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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