

Features

September 2005

- Complete DTMF transmitter/receiver
- Central office quality
- Low power consumption
- Microprocessor port
- Adjustable guard time
- Automatic tone burst mode
- Call progress mode

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Description

The MT8880C is a monolithic DTMF transceiver with call progress filter. It is fabricated in Zarlink Semiconductor's ISO²-CMOS technology, which

Ordering Information

| | | |
|------------|--------------|-------------|
| MT8880CE | 20 Pin PDIP | Tubes |
| MT8880CS | 20 Pin SOIC | Tubes |
| MT8880CN | 24 Pin SSOP | Tubes |
| MT8880CP | 28 Pin PLCC | Tubes |
| MT8880CP1 | 28 Pin PLCC* | Tubes |
| MT8880CS1 | 20 Pin SOIC* | Tubes |
| MT8880CE1 | 20 Pin PDIP* | Tubes |
| MT8880CN1 | 24 Pin SSOP* | Tubes |
| MT8880CSR | 20 Pin SOIC | Tape & Reel |
| MT8880CPR | 28 Pin PLCC | Tape & Reel |
| MT8880CPR1 | 28 Pin PLCC* | Tape & Reel |
| MT8880CSR1 | 20 Pin SOIC* | Tape & Reel |

*Pb Free Matte Tin

-40°C to +85°C

provides low power dissipation and high reliability. The DTMF receiver is based upon the industry standard MT8870 monolithic DTMF receiver; the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors.

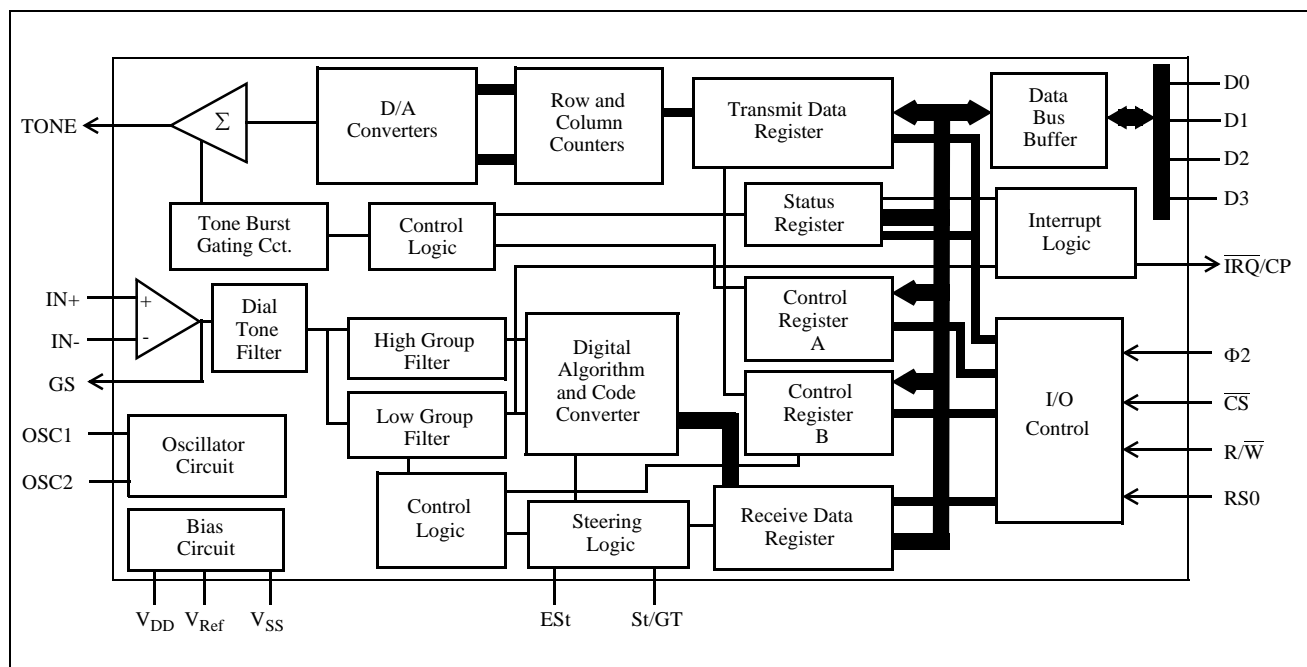


Figure 1 - Functional Block Diagram

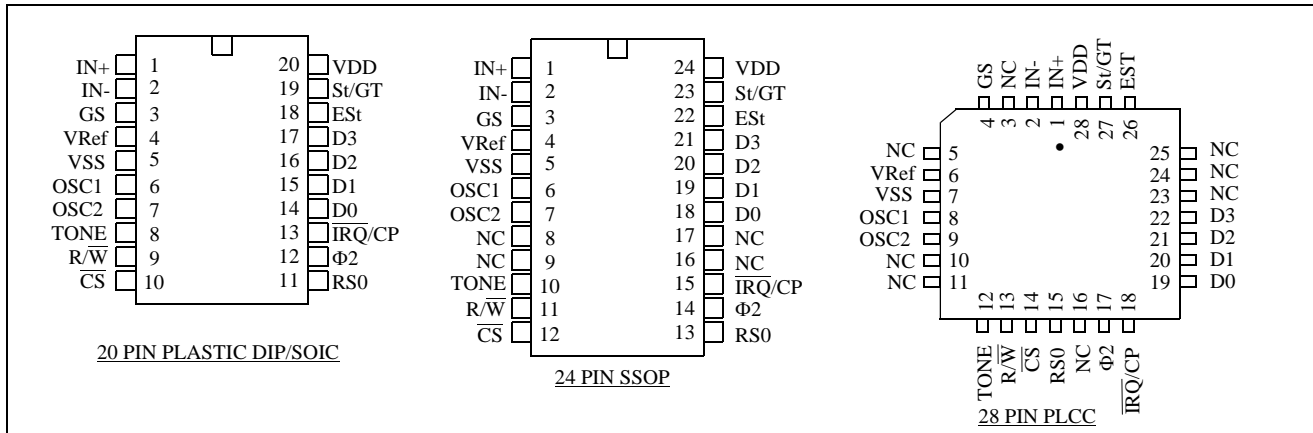


Figure 2 - Pin Connections

Pin Description

| Pin # | | | Name | Description |
|-------|-------|-------|----------------------|--|
| 20 | 24 | 28 | | |
| 1 | 1 | 1 | IN+ | Non-inverting op-amp input. |
| 2 | 2 | 2 | IN- | Inverting op-amp input. |
| 3 | 3 | 4 | GS | Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor. |
| 4 | 4 | 6 | V _{Ref} | Reference Voltage output, nominally V _{DD} /2 is used to bias inputs at mid-rail (see Fig. 13). |
| 5 | 5 | 7 | V _{SS} | Ground input (0 V). |
| 6 | 6 | 8 | OSC1 | DTMF clock/oscillator input. Connect a 4.7 MΩ resistor to VSS if crystal oscillator is used. |
| 7 | 7 | 9 | OSC2 | Clock output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is clock input. |
| 8 | 10 | 12 | TONE | Tone output (DTMF or single tone). |
| 9 | 11 | 13 | R/ \overline{W} | Read/Write input. Controls the direction of data transfer to and from the MPU and the transceiver registers. TTL compatible. |
| 10 | 12 | 14 | \overline{CS} | Chip Select , TTL input (\overline{CS} =0 to select the chip). |
| 11 | 13 | 15 | RS0 | Register Select input. See register decode table. TTL compatible. |
| 12 | 14 | 17 | Φ2 | System Clock input. TTL compatible. N.B. Φ2 clock input need not be active when the device is not being accessed. |
| 13 | 15 | 18 | \overline{IRQ}/C_P | Interrupt Request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupt enabled the \overline{IRQ}/C_P pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 8. |
| 14-17 | 18-21 | 19-22 | D0-D3 | Microprocessor Data Bus (TTL compatible). High impedance when \overline{CS} = 1 or Φ2 is low. |

Pin Description

| Pin # | | | Name | Description |
|-------|----------------|-----------------------------|-----------------|---|
| 20 | 24 | 28 | | |
| 18 | 22 | 26 | ES _t | Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ES _t to return to a logic low. |
| 19 | 23 | 27 | St/GT | Steering Input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ES _t and the voltage on St. |
| 20 | 24 | 28 | V _{DD} | Positive power supply input (+5 V typical). |
| | 8, 9, 16,17 | 3,5,10,1 1, 16, 23-25 | NC | No Connection. |

Functional Description

The MT8880C Integrated DTMF Transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified passband can be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the MT8880C provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

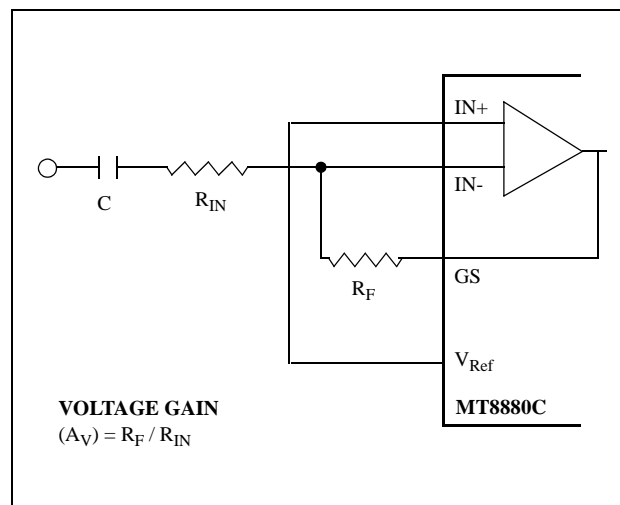


Figure 3 - Single-Ended Input Configuration

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Fig. 7). These filters also incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

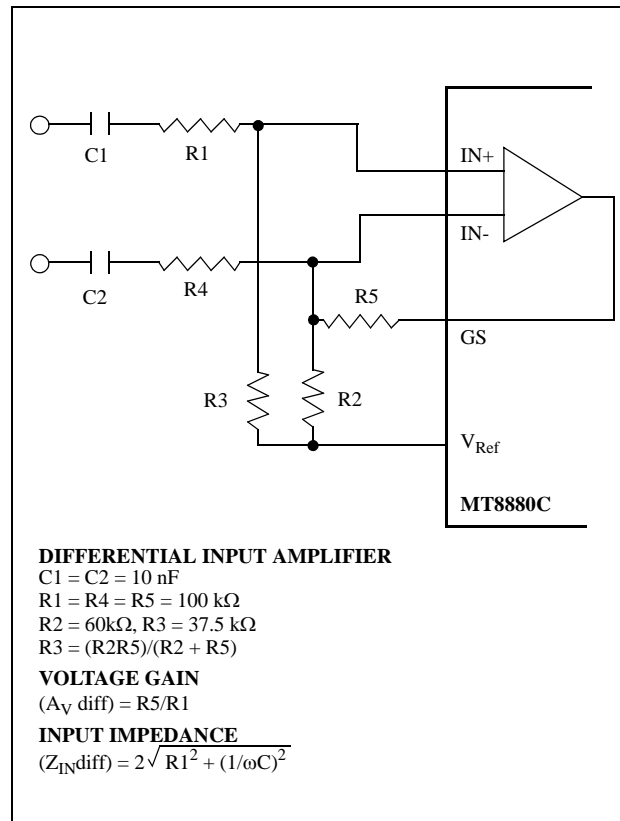


Figure 4 - Differential Input Configuration

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the “signal condition” in some industry specifications) the “Early Steering” (ES_t) output will go to an active state. Any subsequent loss of signal condition will cause ES_t to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ES_t. A logic high on ES_t causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ES_t remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TS}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Figure 7) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD} . GT continues to drive high as long as ES_t remains high. Finally, after a

short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{\text{IRQ/CP}}$ pin will pull low when the delayed steering is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

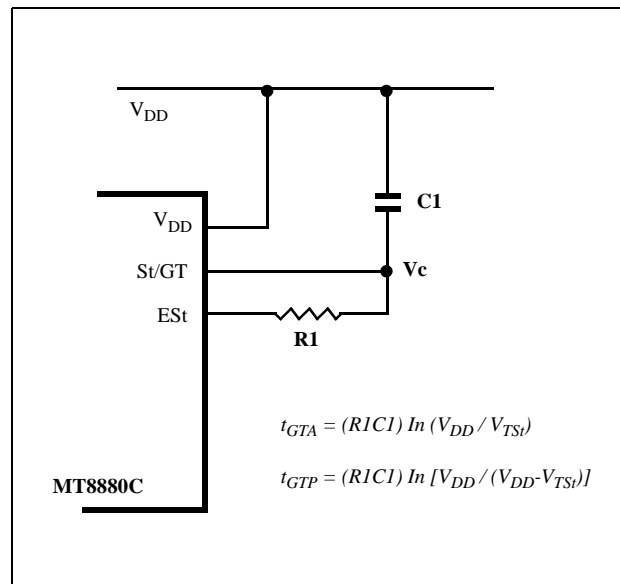


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 μF is recommended for most applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

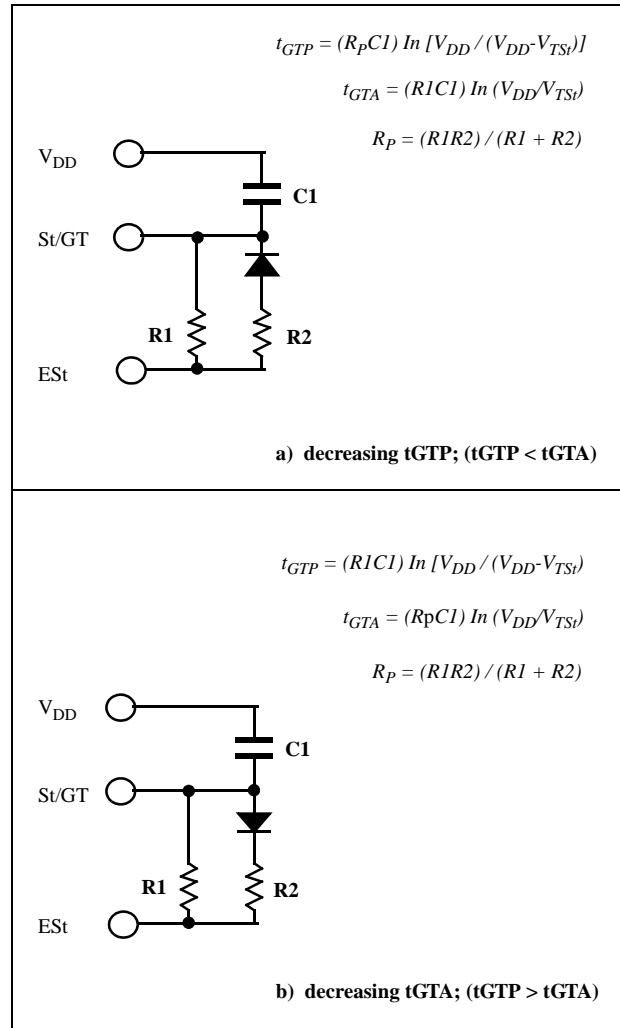


Figure 6 - Guard Time Adjustment

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 9 with a description of the events in Figure 11.

Call Progress Filter

A call progress mode, using the MT8880C, can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 5). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the \overline{IRQ}/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the \overline{IRQ}/CP pin will remain low.

DTMF Generator

The DTMF transmitter employed in the MT8880C is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Figure 7 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (pre-emphasis) is 2 dB to compensate for high group attenuation on long loops.

| F_{LOW} | F_{HIGH} | DIGIT | D_3 | D_2 | D_1 | D_0 |
|------------------|-------------------|-------|-------|-------|-------|-------|
| 697 | 1209 | 1 | 0 | 0 | 0 | 1 |
| 697 | 1336 | 2 | 0 | 0 | 1 | 0 |
| 697 | 1477 | 3 | 0 | 0 | 1 | 1 |
| 770 | 1209 | 4 | 0 | 1 | 0 | 0 |
| 770 | 1336 | 5 | 0 | 1 | 0 | 1 |
| 770 | 1477 | 6 | 0 | 1 | 1 | 0 |
| 852 | 1209 | 7 | 0 | 1 | 1 | 1 |
| 852 | 1336 | 8 | 1 | 0 | 0 | 0 |
| 852 | 1477 | 9 | 1 | 0 | 0 | 1 |
| 941 | 1336 | 0 | 1 | 0 | 1 | 0 |
| 941 | 1209 | * | 1 | 0 | 1 | 1 |
| 941 | 1477 | # | 1 | 1 | 0 | 0 |
| 697 | 1633 | A | 1 | 1 | 0 | 1 |
| 770 | 1633 | B | 1 | 1 | 1 | 0 |
| 852 | 1633 | C | 1 | 1 | 1 | 1 |
| 941 | 1633 | D | 0 | 0 | 0 | 0 |

0= LOGIC LOW, 1= LOGIC HIGH

Figure 7 - Functional Encode/Decode Table

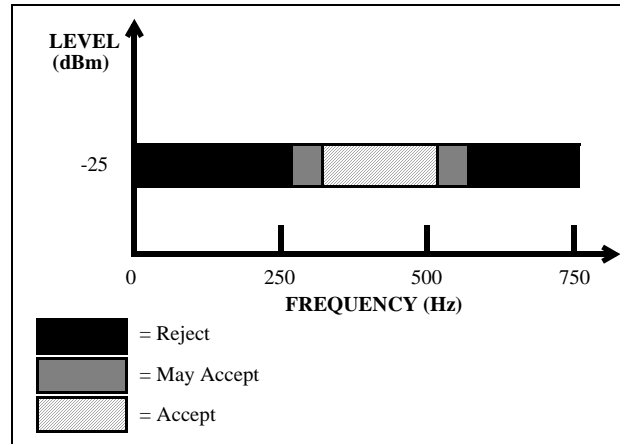


Figure 8 - Call Progress Response

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the tone output signal frequency will be varied. The divider output clocks another counter which addresses the sinewave lookup ROM.

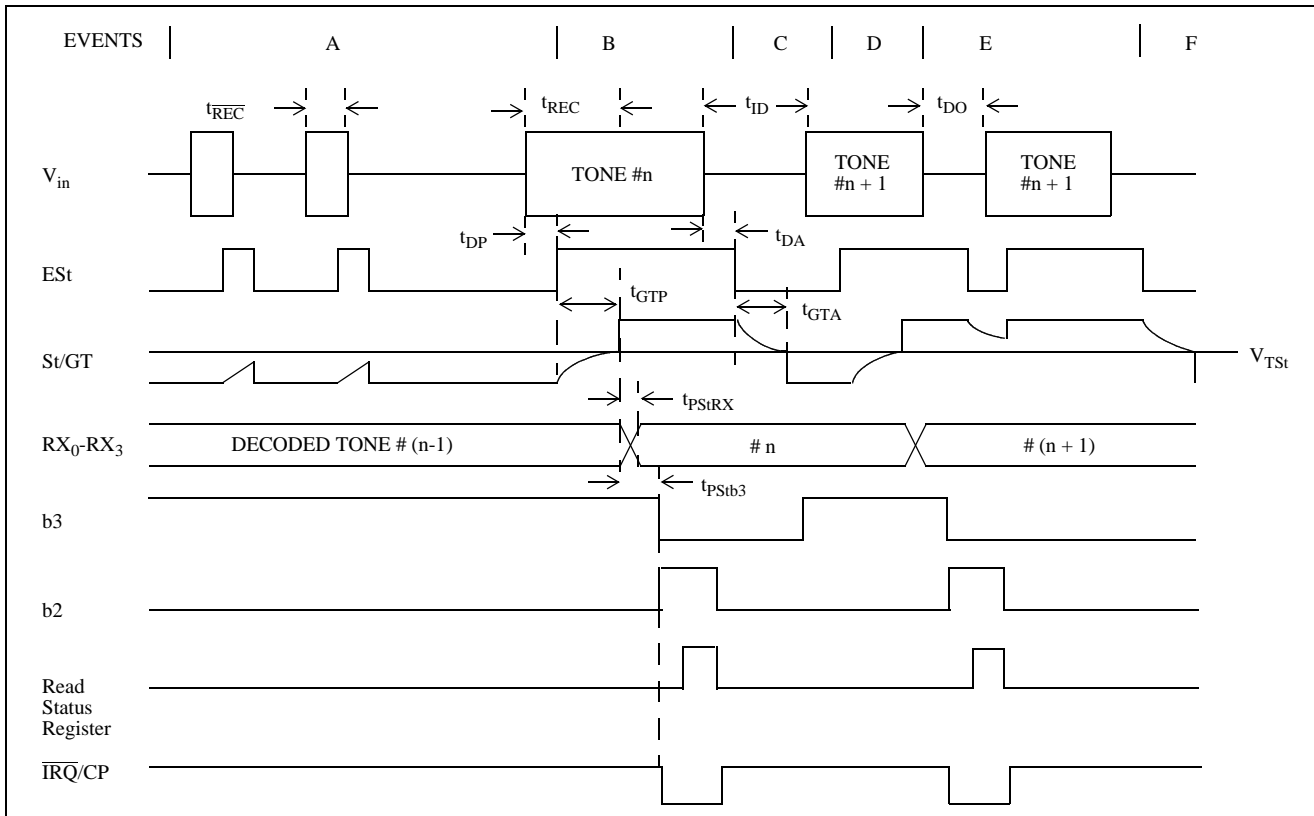


Figure 9 - Receiver Timing Diagram

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones which are then mixed using a low noise summing amplifier. The oscillator described needs no “start-up” time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 10 that the distortion products are very low in amplitude.

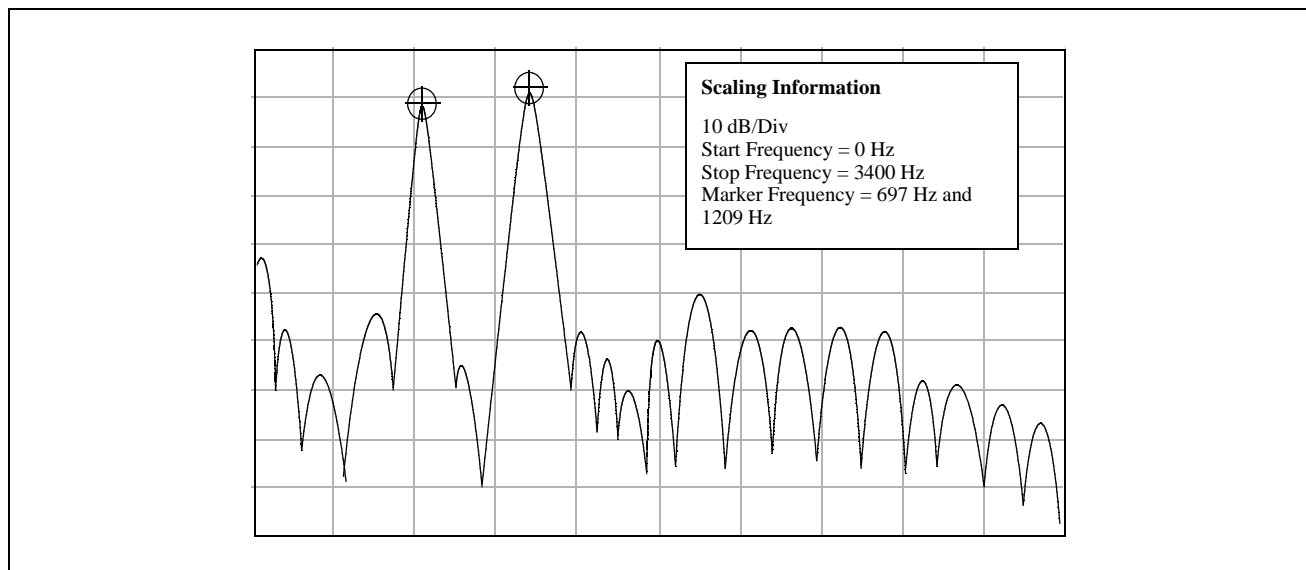


Figure 10 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is $51 \text{ ms} \pm 1 \text{ ms}$ which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, a second burst/pause time of $102 \text{ ms} \pm 2 \text{ ms}$ is available. This extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received.

In applications where a non-standard burst/pause duration is required, burst mode must be disabled and the transmitter gated on and off by an external hardware or software timer.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The MT8880C is capable of producing precise tone bursts with minimal error in frequency (see Table 1). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using

Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to $V_{2f} \dots V_{nf}$ as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively, and V_{IMD}^2 is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

EXPLANATION OF EVENTS

- A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
- B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
- C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
- D) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
- E) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
- F) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

| | |
|----------------------------------|---|
| V_{in} | DTMF COMPOSITE INPUT SIGNAL. |
| ES _t | EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES. |
| St/GT | STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT. |
| RX ₀ -RX ₃ | 4-BIT DECODED DATA IN RECEIVE DATA REGISTER |
| b3 | DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL. |
| b2 | INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ. |
| \overline{IRQ}/CP | INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ. |
| $t_{\overline{REC}}$ | MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID. |
| t_{REC} | MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION. |
| t_{ID} | MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS. |
| t_{DO} | MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL. |
| t_{DP} | TIME TO DETECT VALID FREQUENCIES PRESENT. |
| t_{DA} | TIME TO DETECT VALID FREQUENCIES ABSENT. |
| t_{GTP} | GUARD TIME, TONE PRESENT. |
| t_{GTA} | GUARD TIME, TONE ABSENT. |

Figure 11 - Description of Timing Events

$$THD(\%) = 100 \frac{\left(\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \dots + V_{nf}^2} \right)}{V_{\text{fundamental}}}$$

Equation 1. THD (%) For a Single Tone

$$\text{THD (\%)} = 100 \frac{\left(\sqrt{V_{2L}^2 + V_{3L}^2 + \dots V_{nL}^2 + V_{2H}^2 + V_{3H}^2 + \dots V_{nH}^2 + V_{\text{IMD}}^2} \right)}{\sqrt{V_L^2 + V_H^2}}$$

Equation 2. THD (%) For a Dual Tone

| ACTIVE INPUT | OUTPUT FREQUENCY (Hz) | | %ERROR |
|--------------|-----------------------|--------|--------|
| | SPECIFIED | ACTUAL | |
| L1 | 697 | 699.1 | +0.30 |
| L2 | 770 | 766.2 | -0.49 |
| L3 | 852 | 847.4 | -0.54 |
| L4 | 941 | 948.0 | +0.74 |
| H1 | 1209 | 1215.9 | +0.57 |
| H2 | 1336 | 1331.7 | -0.32 |
| H3 | 1477 | 1471.9 | -0.35 |
| H4 | 1633 | 1645.0 | +0.73 |

Table 1 - Actual Frequencies Versus Standard Requirements

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency: 3.579545 MHz
 Frequency Tolerance: $\pm 0.1\%$
 Resonance Mode: Parallel
 Load Capacitance: 18 pF
 Maximum Series Resistance: 150 ohms
 Maximum Drive Level: 2 mW

e.g. CTS Knights MP036S
 Toyocom TQC-203-A-9S

A number of MT8880C devices can be connected as shown in Figure 12 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

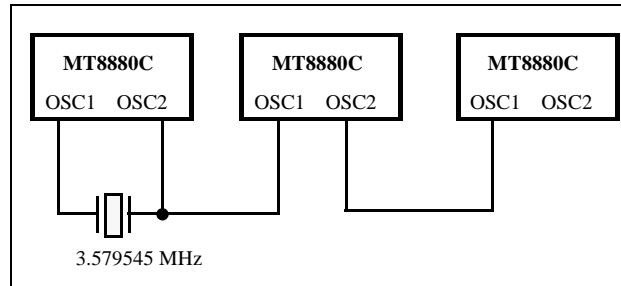


Figure 12 - Common Crystal Connection

Microprocessor Interface

The MT8880C employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, i.e., data transfer, transceiver control and transceiver status. There are two registers associated with data transfer operations.

The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read only register. The data entered in the Transmit Data Register will determine which tone pair is to be generated (see Figure 7 for coding details). Data can only be written to the transmit register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. A software reset must be included at the beginning of all programs to initialize the control and status registers after power up or power reset (see Figure 16). Refer to Tables 3, 4, 5 and 6 for details concerning the Control Registers. The $\overline{\text{IRQ/CP}}$ pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals or when the transmitter is ready for more data (Burst mode only). The $\overline{\text{IRQ/CP}}$ pin is configured as an open drain output device and as such requires a pull-up resistor (see Figure 13).

| RS0 | R/ $\overline{\text{W}}$ | FUNCTION |
|-----|--------------------------|---------------------------------|
| 0 | 0 | Write to Transmit Data Register |
| 0 | 1 | Read from Receive Data Register |
| 1 | 0 | Write to Control Register |
| 1 | 1 | Read from Status Register |

Table 2 - Internal Register Functions

| b3 | b2 | b1 | b0 |
|------|-----|------------------------------|------|
| RSEL | IRQ | CP/ $\overline{\text{DTMF}}$ | TOUT |

Table 3 - CRA Bit Positions

| b3 | b2 | b1 | b0 |
|--------------------------|--------------------------|------|-------|
| C/ $\overline{\text{R}}$ | S/ $\overline{\text{D}}$ | TEST | BURST |

Table 4 - CRB Bit Positions

| BIT | NAME | FUNCTION | DESCRIPTION |
|-----|------------------------------|------------------|---|
| b0 | TOUT | TONE OUTPUT | A logic '1' enables the tone output. This function can be implemented in either the burst mode or non-burst mode. |
| b1 | CP/ $\overline{\text{DTMF}}$ | MODE CONTROL | In DTMF mode (logic '0') the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1') a 6th order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones which are within the specified bandwidth will be presented at the $\overline{\text{IRQ}}/\text{CP}$ pin in rectangular wave format if the IRQ bit has been enabled (b2=1). Also, when the CP mode and BURST mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode of operation has been selected. |
| b2 | IRQ | INTERRUPT ENABLE | A logic '1' enables the INTERRUPT mode. When this mode is active and the DTMF mode has been selected (b1=0) the $\overline{\text{IRQ}}/\text{CP}$ pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (BURST mode only). |
| b3 | RSEL | REGISTER SELECT | A logic '1' selects Control Register B on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A. |

Table 5 - Control Register A Description

| BIT | NAME | FUNCTION | DESCRIPTION |
|-----|--------------------------------|------------------------------|--|
| b0 | BURST | BURST MODE | A logic '0' enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Register resulting in a tone burst of a specific duration (see AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Register is ready for further instructions and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic '1') tone bursts of any desired duration may be generated. |
| b1 | TEST | TEST MODE | By enabling the test mode (logic '1'), the $\overline{\text{IRQ}}/\text{CP}$ pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 9 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1=0) before test mode can be implemented. |
| b2 | $\text{S}/\overline{\text{D}}$ | SINGLE /DUAL TONE GENERATION | A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single tone generation is enabled (logic '1'), either row or column tones (low group or high group) can be generated depending on the state of b3 in Control Register B. |
| b3 | $\text{C}/\overline{\text{R}}$ | COLUMN/ROW TONES | When used in conjunction with b2 (above) the transmitter can be made to generate single row or single column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies. |

Table 6 - Control Register B Description

| BIT | NAME | STATUS FLAG SET | STATUS FLAG CLEARED |
|-----|--|--|--|
| b0 | IRQ | Interrupt has occurred. Bit one (b1) or bit two (b2) is set. | Interrupt is inactive. Cleared after Status Register is read. |
| b1 | TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY) | Pause duration has terminated and transmitter is ready for new data. | Cleared after Status Register is read or when in non-burst mode. |
| b2 | RECEIVE DATA REGISTER FULL | Valid data is in the Receive Data Register. | Cleared after Status Register is read. |
| b3 | $\overline{\text{DELAYED STEERING}}$ | Set upon the valid detection of the absence of a DTMF signal. | Cleared upon the detection of a valid DTMF signal. |

Table 7 - Status Register Description

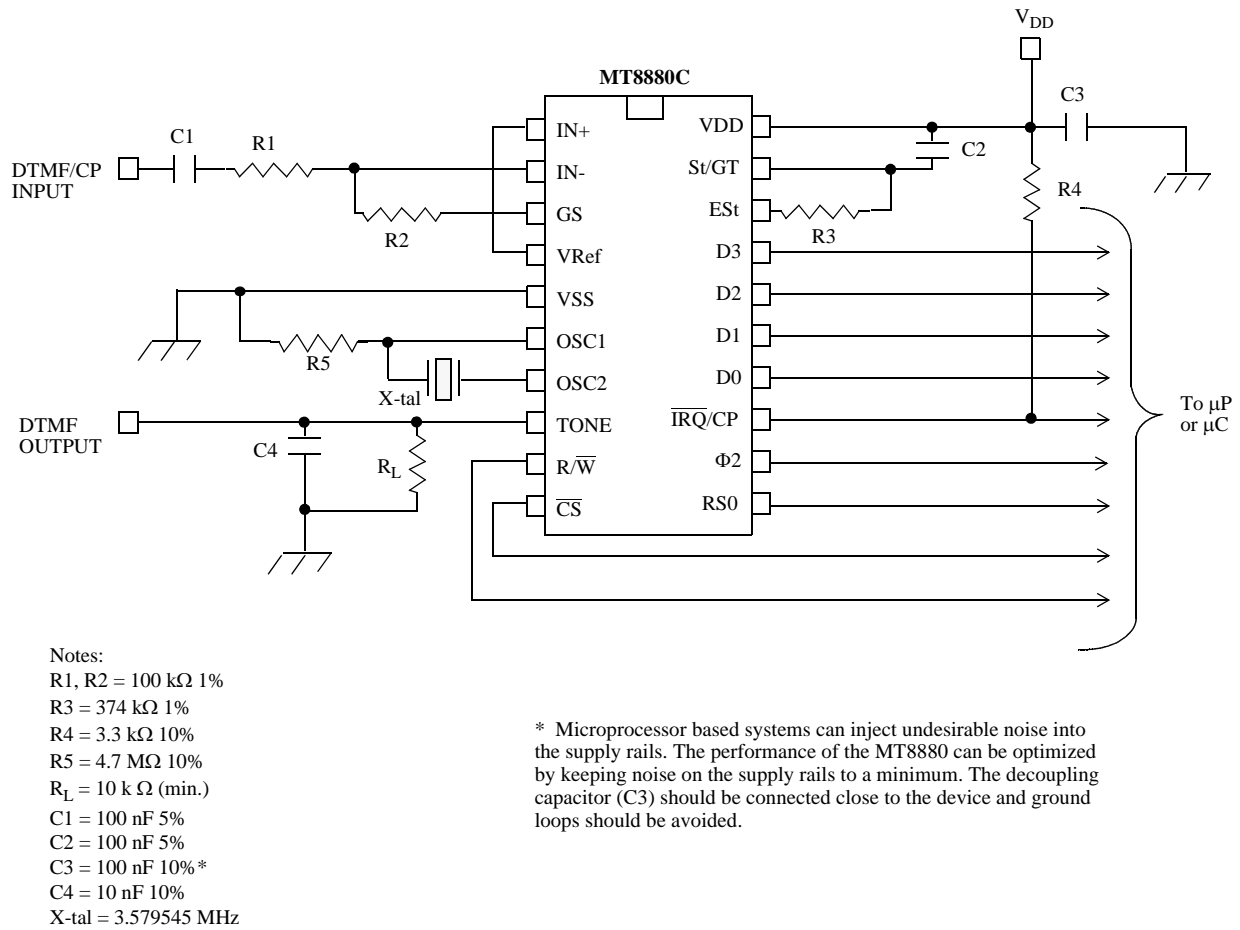


Figure 13 - Application Circuit (Single-Ended Input)

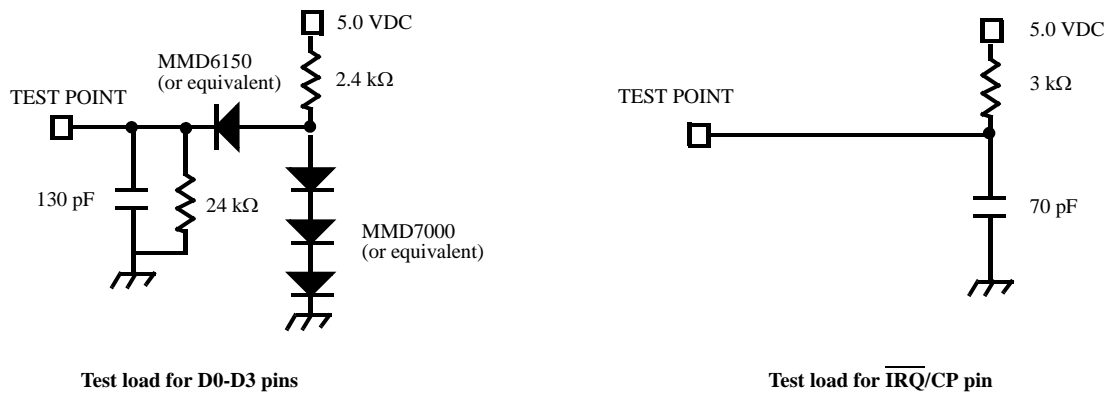


Figure 14 - Test Circuit

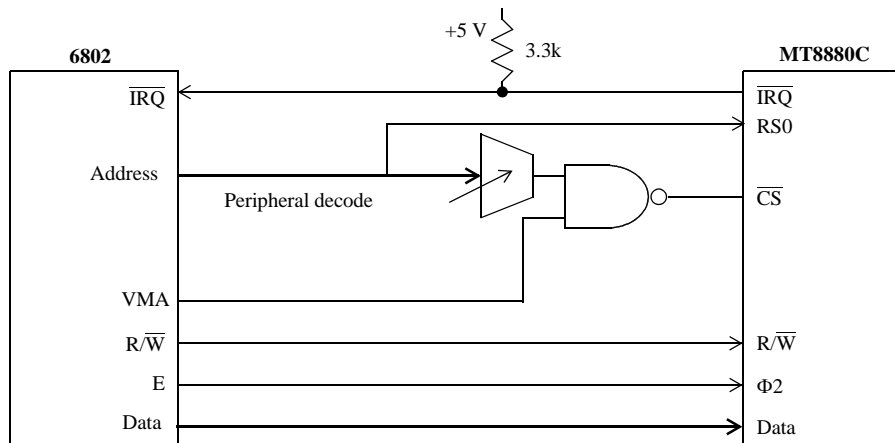


Figure 15 - MT8880C to 6802 Interface

EXAMPLE 1: A software reset must be included at the beginning of all programs to initialize the control registers after power up. The initialization procedure should be implemented 100ms after power up.

| Description | Control | | | Data | | | |
|------------------------------|-----------------|-----|------------------|------|----|----|----|
| | \overline{CS} | RS0 | R/\overline{W} | b3 | b2 | b1 | b0 |
| 1) Read Status Register | 0 | 1 | 1 | X | X | X | X |
| 2) Write to Control Register | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 3) Write to Control Register | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 4) Write to Control Register | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 5) Write to Control Register | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 6) Read Status Register | 0 | 1 | 1 | X | X | X | X |

EXAMPLE 2: Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones

| Description | \overline{CS} | RS0 | R/\overline{W} | b3 | b2 | b1 | b0 |
|--|-----------------|-----|------------------|----|----|----|----|
| 1) Write to Control Register A (tone out, DTMF, \overline{IRQ} , Select Control Register B) | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 2) Write to Control Register B (burst mode) | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 3) Write to Transmit Data Register (send a digit 7) | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| -----wait for an interrupt or poll Status Register ----- | | | | | | | |
| 4) Read the Status Register | 0 | 1 | 1 | X | X | X | X |
| -if bit 1 is set, the Tx is ready for the next tone, in which case... | | | | | | | |
| Write to Transmit Register (send a digit 5) | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| -if bit 2 is set, a DTMF tone has been received, in which case.... | | | | | | | |
| Read the Receive Data Register | 0 | 0 | 1 | X | X | X | X |
| -if both bits are set... | | | | | | | |
| Read the Receive Data Register | 0 | 0 | 1 | X | X | X | X |
| Write to Transmit Data Register | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (± 2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 16 - Application Hints

Absolute Maximum Ratings*

| | Parameter | Symbol | Min. | Max. | Units |
|---|--|----------|--------------|--------------|-------|
| 1 | Power supply voltage $V_{DD}-V_{SS}$ | V_{DD} | | 6 | V |
| 2 | Voltage on any pin | V_I | $V_{SS}-0.3$ | $V_{DD}+0.3$ | V |
| 3 | Current at any pin (Except V_{DD} and V_{SS}) | | | 10 | mA |
| 4 | Storage temperature | T_{ST} | -65 | +150 | °C |
| 5 | Package power dissipation | P_D | | 1000 | mW |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | Parameter | Sym. | Min. | Typ. [‡] | Max. | Units | Test Conditions |
|---|-------------------------|-----------|----------|-------------------|----------|-------|-----------------|
| 1 | Positive power supply | V_{DD} | 4.75 | 5.00 | 5.25 | V | |
| 2 | Operating temperature | T_O | -40 | | +85 | °C | |
| 3 | Crystal clock frequency | f_{CLK} | 3.575965 | 3.579545 | 3.583124 | MHz | |

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics[†] - $V_{SS}=0$ V.

| | | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Test Conditions |
|----|---------------------------------|----------------------------------|-----------|------|-------------------|------|-------|-----------------------------|
| 1 | S U P | Operating supply voltage | V_{DD} | 4.75 | 5.0 | 5.25 | V | |
| 2 | | Operating supply current | I_{DD} | | 7.0 | 11 | mA | |
| 3 | | Power consumption | P_C | | | 57.8 | mW | |
| 4 | I N P U T S | High level input voltage (OSC1) | V_{IHO} | 3.5 | | | V | |
| 5 | | Low level input voltage (OSC1) | V_{ILO} | | | 1.5 | V | |
| 6 | | Steering threshold voltage | V_{TSt} | 2.2 | 2.3 | 2.5 | V | $V_{DD}=5$ V |
| 7 | O U T P U T S | Low level output voltage (OSC2) | V_{OLO} | | | 0.1 | V | No load |
| 8 | | High level output voltage (OSC2) | V_{OHO} | 4.9 | | | V | No load $V_{DD}=5$ V |
| 9 | | Output leakage current (IRQ) | I_{OZ} | | 1 | 10 | μA | $V_{OH}=2.4$ V |
| 10 | | V_{Ref} output voltage | V_{Ref} | 2.4 | 2.5 | 2.6 | V | No load, $V_{DD}=5$ V |
| 11 | | V_{Ref} output resistance | R_{OR} | | 1.3 | | kΩ | |
| 12 | D i g i t a l | Low level input voltage | V_{IL} | | | 0.8 | V | |
| 13 | | High level input voltage | V_{IH} | 2.0 | | | V | |
| 14 | | Input leakage current | I_{IZ} | | | 10 | μA | $V_{IN}=V_{SS}$ to V_{DD} |

DC Electrical Characteristics[†] - $V_{SS}=0$ V.

| | | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Test Conditions |
|----|---------------------|-----------------|----------|------|-------------------|------|-------|-----------------|
| 15 | Data Bus | Source current | I_{OH} | -1.4 | -6.6 | | mA | $V_{OH}=2.4$ V |
| 16 | | Sink current | I_{OL} | 2.0 | 4.0 | | mA | $V_{OL}=0.4$ V |
| 17 | ESt and St/Gt | Source current | I_{OH} | -0.5 | -3.0 | | mA | $V_{OH}=4.6$ V |
| 18 | | Sink current | I_{OL} | 2 | 4 | | mA | $V_{OL}=0.4$ V |
| 19 | \overline{IRQ}/CP | Sink current | I_{OL} | 4 | 16 | | mA | $V_{OL}=0.4$ V |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25 °C, $V_{DD}=5$ V and for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, $V_{SS}=0$ V.

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Test Conditions |
|----|--------------------------------|-----------|------|------|--------------|------------|---------------------------------------|
| 1 | Input leakage current | I_{IN} | | | 100 | nA | $V_{SS} \leq V_{IN} \leq V_{DD}$ |
| 2 | Input resistance | R_{IN} | 10 | | | M Ω | |
| 3 | Input offset voltage | V_{OS} | | | 25 | mV | |
| 4 | Power supply rejection | PSRR | 50 | | | dB | 1 kHz |
| 5 | Common mode rejection | CMRR | 40 | | | dB | |
| 6 | DC open loop voltage gain | A_{VOL} | 40 | | | dB | $C_L = 20$ p |
| 7 | Unity gain bandwidth | BW | 1.0 | | | MHz | $C_L = 20$ p |
| 8 | Output voltage swing | V_O | 0.5 | | $V_{DD}-0.5$ | V | $R_L \geq 100$ k Ω to V_{SS} |
| 9 | Allowable capacitive load (GS) | C_L | | | 100 | pF | PM>40° |
| 10 | Allowable resistive load (GS) | R_L | 50 | | | k Ω | $V_O = 4$ Vpp |
| 11 | Common mode range | V_{CM} | 1.0 | | $V_{DD}-1.0$ | V | $R_L = 50$ k Ω |

Figures are for design aid only: not guaranteed and not subject to production testing.

Characteristics are over recommended operating conditions unless otherwise stated.

MT8880C AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | | Characteristics | Sym | Min. | Typ. [‡] | Max. | Units | Notes* |
|---|-----|---|-----|------|-------------------|------|-------------------|-------------|
| 1 | R X | Valid Input signal levels (each tone of composite signal) | | -29 | | | dBm | 1,2,3,5,6,9 |
| | | | | 27.5 | | | mV _{RMS} | 1,2,3,5,6,9 |
| | | | | | | +1 | dBm | 1,2,3,5,6,9 |
| | | | | | | 869 | mV _{RMS} | 1,2,3,5,6,9 |

[†] Characteristics are over recommended operating conditions (unless otherwise stated) using the test circuit shown in Figure 13.

AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated. $f_C=3.579545$ MHz.

| | | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Notes* |
|---|--------|------------------------|------|----------------------------|-------------------|------|-------|----------------|
| 1 | R X | Positive twist accept | | | | 8 | dB | 2,3,6,9 |
| 2 | | Negative twist accept | | | | 8 | dB | 2,3,6,9 |
| 3 | | Freq. deviation accept | | $\pm 1.5\% \pm 2\text{Hz}$ | | | | 2,3,5,9 |
| 4 | | Freq. deviation reject | | $\pm 3.5\%$ | | | | 2,3,5 |
| 5 | | Third tone tolerance | | | -16 | | dB | 2,3,4,5,9,10 |
| 6 | | Noise tolerance | | | -12 | | dB | 2,3,4,5,7,9,10 |
| 7 | | Dial tone tolerance | | | 22 | | dB | 2,3,4,5,8,9,11 |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, $V_{DD} = 5$ V, and for design aid only: not guaranteed and not subject to production testing.

* See "Notes" following AC Electrical Characteristics Tables.

AC Electrical Characteristics[†] - Call Progress - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Notes* |
|---|---|----------|------|-------------------|------|-------|-----------|
| 1 | Lower freq. (ACCEPT) | f_{LA} | | 320 | | Hz | @ -25 dBm |
| 2 | Upper freq. (ACCEPT) | f_{HA} | | 510 | | Hz | @ -25 dBm |
| 3 | Lower freq. (REJECT) | f_{LR} | | 290 | | Hz | @ -25 dBm |
| 4 | Upper freq. (REJECT) | f_{HR} | | 540 | | Hz | @ -25 dBm |
| 5 | Call progress tone detect level (total power) | | -30 | | | dBm | |

[†] Characteristics are over recommended operating conditions unless otherwise stated

[‡] Typical figures are at 25°C, $V_{DD} = 5$ V, and for design aid only: not guaranteed and not subject to production testing

* See "Notes" AC Electrical Characteristics Tables

AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Conditions |
|----|--------|--|--------------|------|-------------------|------|-------|------------------------------|
| 1 | R X | Tone present detect time | t_{DP} | 3 | 11 | 14 | ms | Note 12 |
| 2 | | Tone absent detect time | t_{DA} | 0.5 | 4 | 8.5 | ms | Note 12 |
| 3 | | Tone duration accept | t_{REC} | | | 40 | ms | User adjustable [#] |
| 4 | | Tone duration reject | t_{REC} | 20 | | | ms | User adjustable [#] |
| 5 | | Minimum interdigit pause duration | t_{ID} | | | 40 | ms | User adjustable [#] |
| 6 | | Maximum tone drop-out duration | t_{DO} | 20 | | | ms | User adjustable [#] |
| 7 | | Delay St to b3 | $t_{PS tb3}$ | | 13 | | μs | See figure 9 |
| 8 | | Delay St to RX ₀ -RX ₃ | $t_{PS tRX}$ | | 8 | | μs | See figure 9 |
| 9 | T X | Tone burst duration | t_{BST} | 50 | | 52 | ms | DTMF mode |
| 10 | | Tone pause duration | t_{PS} | 50 | | 52 | ms | DTMF mode |
| 11 | | Tone burst duration (extended) | t_{BSTE} | 100 | | 104 | ms | Call Progress mode |
| 12 | | Tone pause duration (extended) | t_{PSE} | 100 | | 104 | ms | Call Progress mode |

AC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | | Characteristics | Sym. | Min. | Typ. [‡] | Max. | Units | Conditions |
|----|---|---|-------------------|--------|-------------------|-----------|------------------|---|
| 13 | T O N E O U T | High group output level | V_{HOUT} | -6.1 | | -2.1 | dBm | $R_L=10\text{ k}\Omega$ |
| 14 | | Low group output level | V_{LOUT} | -8.1 | | -4.1 | dBm | $R_L=10\text{ k}\Omega$ |
| 15 | | Pre-emphasis | dB _P | 0 | 2 | 3 | dB | $R_L=10\text{ k}\Omega$ |
| 16 | | Output distortion (Single Tone) | THD | | -35 | | dB | 25 kHz Bandwidth $R_L=10\text{ k}\Omega$ |
| 17 | | Frequency deviation | f_D | | ± 0.7 | ± 1.5 | % | $f_C=3.579545\text{ MHz}$ |
| 18 | | Output load resistance | R_{LT} | 10 | | 50 | $\text{k}\Omega$ | |
| 19 | M P U | $\Phi 2$ cycle period | t_{CYC} | | 250 | | ns | |
| 20 | | $\Phi 2$ high pulse width | t_{CH} | | 115 | | ns | |
| 21 | | $\Phi 2$ low pulse width | t_{CL} | | 110 | | ns | |
| 22 | I N T E R F A C E | $\Phi 2$ rise and fall time | t_R, t_F | | | 25 | ns | |
| 23 | | Address, R/\overline{W} hold time | t_{AH}, t_{RWH} | 26 | | | ns | |
| 24 | | Address, R/\overline{W} setup time (before $\Phi 2$) | t_{AS}, t_{RWS} | 23 | | | ns | |
| 25 | | Data hold time (read) | t_{DHR} | 22 | | | ns | * |
| 26 | | $\Phi 2$ to valid data delay (read) | t_{DDR} | | | 100 | ns | 200 pF load |
| 27 | | Data setup time (write) | t_{DSW} | 45 | | | ns | |
| 28 | | Data hold time (write) | t_{DHW} | 10 | | | ns | |
| 29 | | Input Capacitance (data bus) | C_{IN} | | 5 | | pF | |
| 30 | | Output Capacitance (\overline{IRQ}/CP) | C_{OUT} | | 5 | | pF | |
| 31 | D T M F | Crystal/clock frequency | f_C | 3.5759 | 3.5795 | 3.5831 | MHz | |
| 32 | | Clock input rise time | t_{LHCL} | | | 110 | ns | Ext. clock |
| 33 | | Clock input duty cycle | t_{HLCL} | | | 110 | ns | Ext. clock |
| 34 | C L K | Clock input duty cycle | DC_{CL} | 40 | 50 | 60 | % | Ext. clock |
| 35 | | Capacitive load (OSC2) | C_{LO} | | | 30 | pF | |

[†] Timing is over recommended temperature & power supply voltages.

[‡] Typical figures are at 25°C and for design aid only; not guaranteed and not subject to production testing.

* The data bus output buffers are no longer sourcing or sinking current by t_{DHR} .

See Figure 6 regarding guard time adjustment.

NOTES: 1) dBm=decibels above or below a reference power of 1 mW into a 600 ohm load.
 2) Digit sequence consists of all 16 DTMF tones.
 3) Tone duration=40 ms. Tone pause=40 ms.
 4) Nominal DTMF frequencies are used.
 5) Both tones in the composite signal have an equal amplitude.
 6) The tone pair is deviated by $\pm 1.5\% \pm 2\text{ Hz}$.
 7) Bandwidth limited (3 kHz) Gaussian noise.
 8) The precise dial tone frequencies are 350 and 440 Hz ($\pm 2\%$).
 9) For an error rate of less than 1 in 10,000.
 10) Referenced to the lowest amplitude tone in the DTMF signal.
 11) Referenced to the minimum valid accept level.
 12) For guard time calculation purposes.

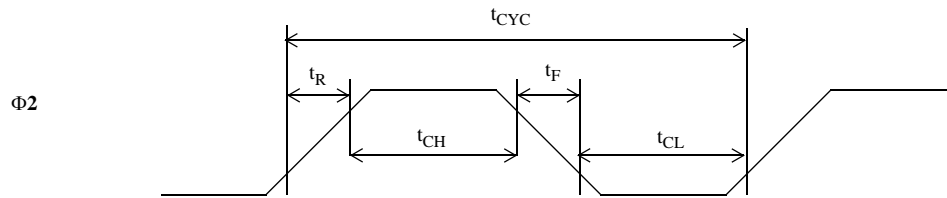
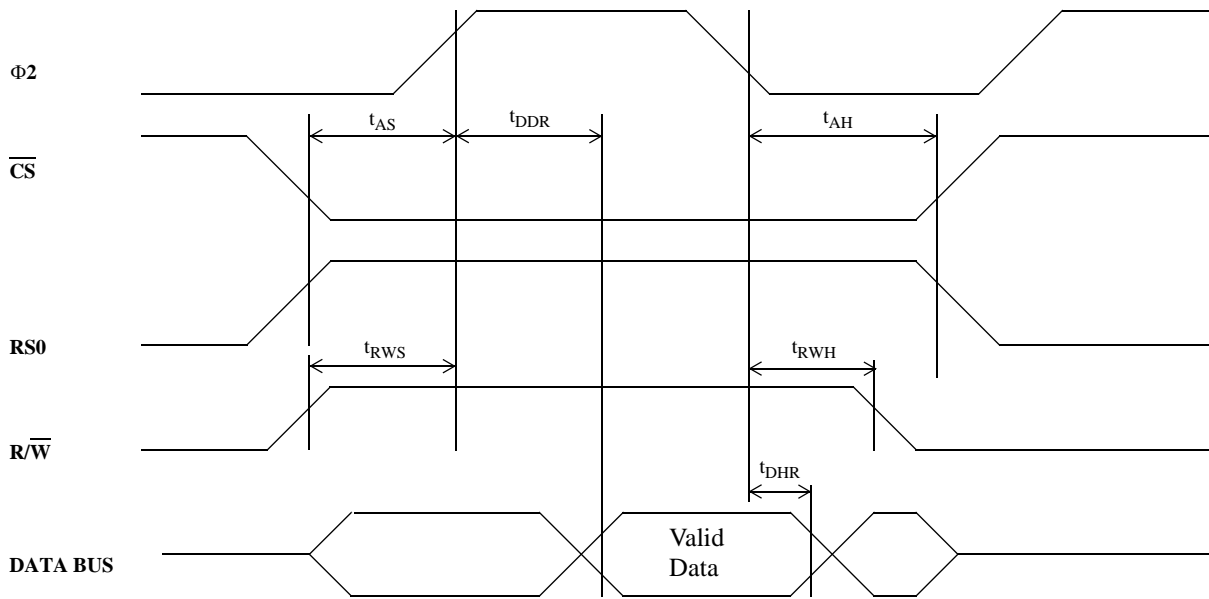
Figure 17 - $\Phi 2$ Pulse

Figure 18 - MPU Read Cycle

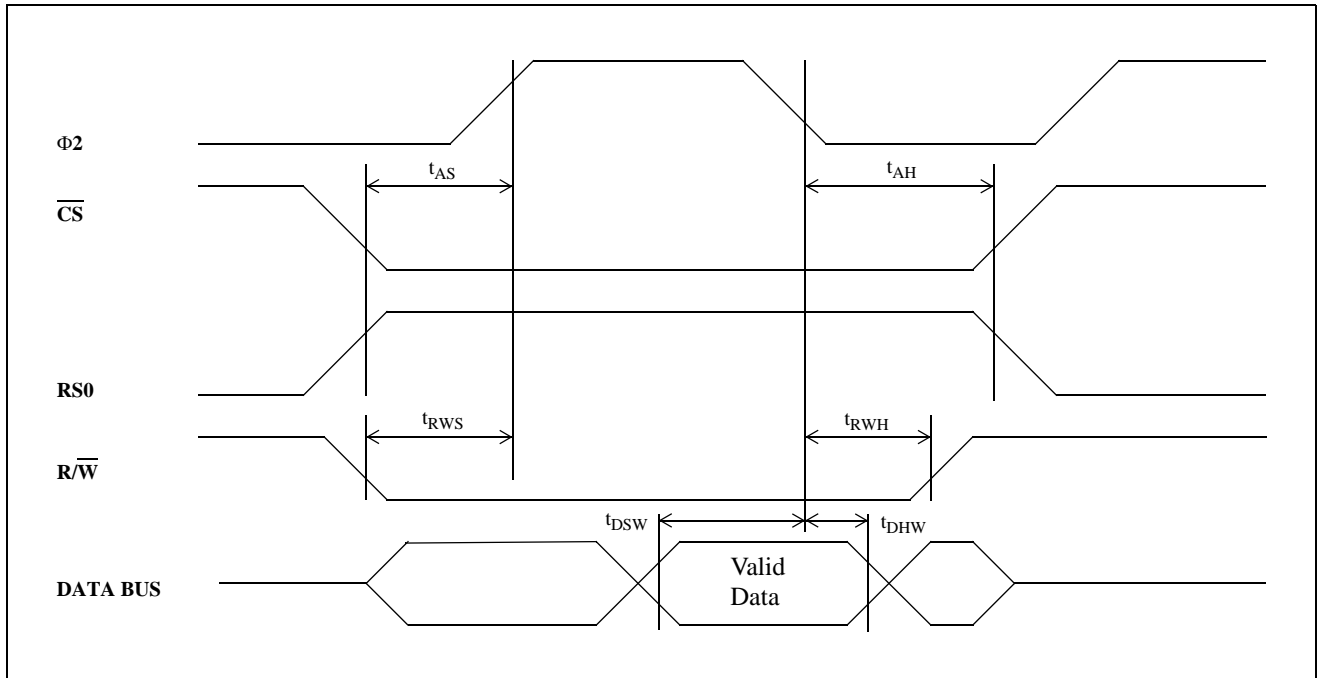
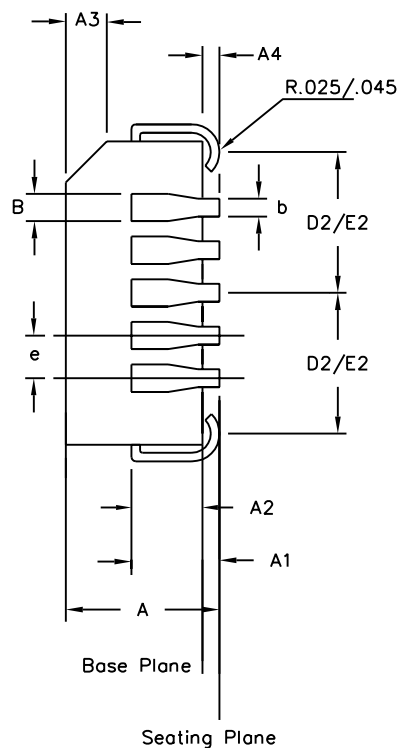
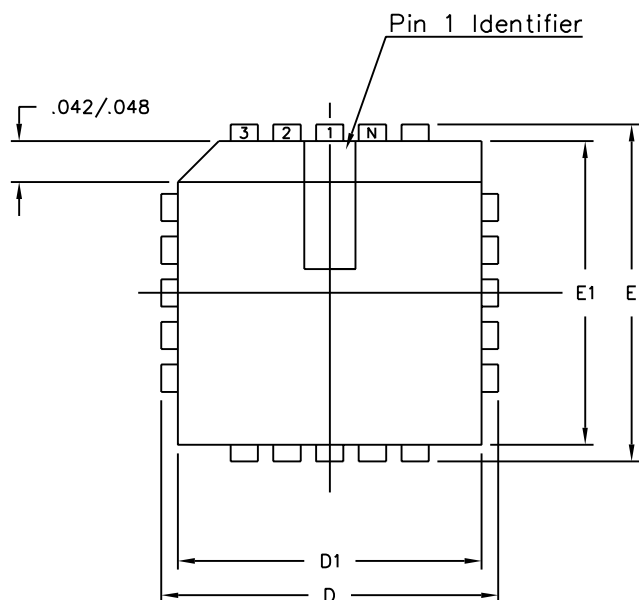


Figure 19 - MPU Write Cycle



| Symbol | Control Dimensions in inches | | Altern. Dimensions in millimetres | |
|----------------------------|---------------------------------|-------|--------------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.180 | 4.19 | 4.57 |
| A1 | 0.090 | 0.120 | 2.29 | 3.05 |
| A2 | 0.062 | 0.083 | 1.57 | 2.11 |
| A3 | 0.042 | 0.056 | 1.07 | 1.42 |
| A4 | 0.020 | — | 0.51 | — |
| D | 0.485 | 0.495 | 12.32 | 12.57 |
| D1 | 0.450 | 0.456 | 11.43 | 11.58 |
| D2 | 0.191 | 0.219 | 4.85 | 5.56 |
| E | 0.485 | 0.495 | 12.32 | 12.57 |
| E1 | 0.450 | 0.456 | 11.43 | 11.58 |
| E2 | 0.191 | 0.219 | 4.85 | 5.56 |
| B | 0.026 | 0.032 | 0.66 | 0.81 |
| b | 0.013 | 0.021 | 0.33 | 0.53 |
| e | 0.050 | BSC | 1.27 | BSC |
| | Pin features | | | |
| ND | 7 | | | |
| NE | 7 | | | |
| N | 28 | | | |
| Note | Square | | | |
| Conforms to JEDEC MS-018AB | | | Iss. A | |

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions.
Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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| ISSUE | 1 | 2 | 3 | |
|--------|---------|---------|---------|--|
| ACN | 5958 | 207469 | 212422 | |
| DATE | 15Aug94 | 10Sep99 | 22Mar02 | |
| APPRD. | | | | |



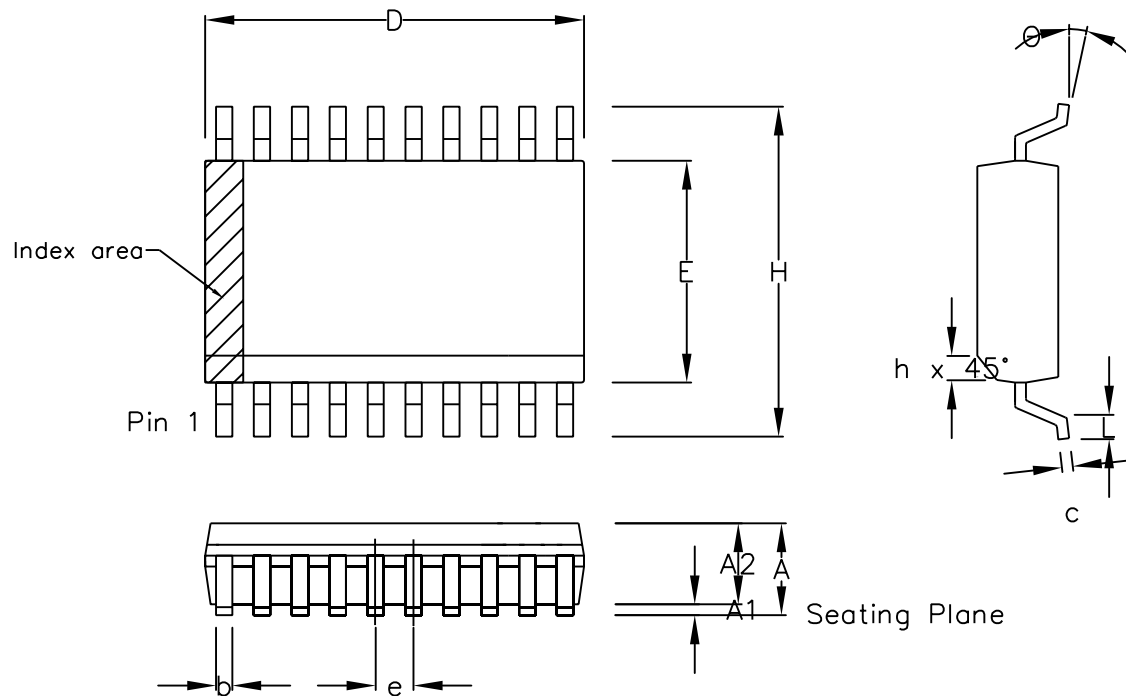
Previous package codes

HP / P

Package Code QA

Package Outline for
28 lead PLCC

GPD00002



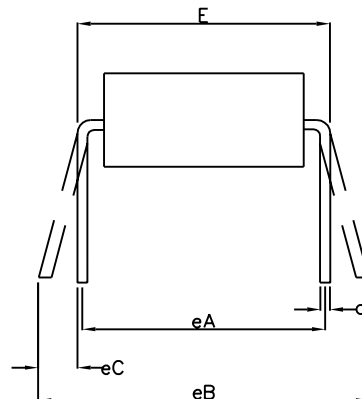
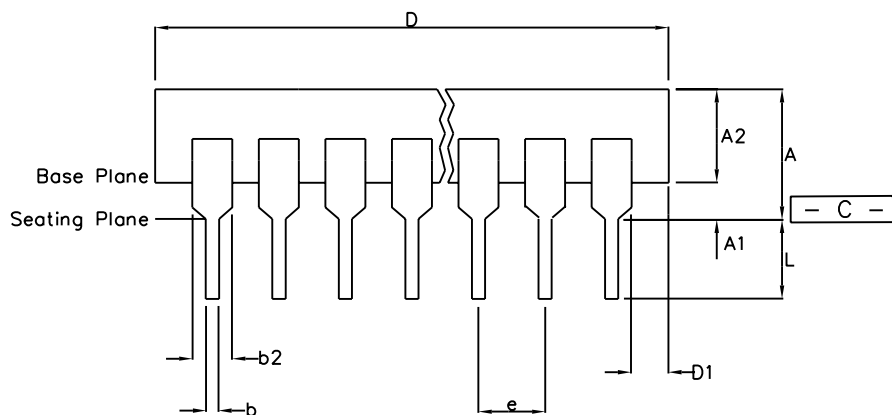
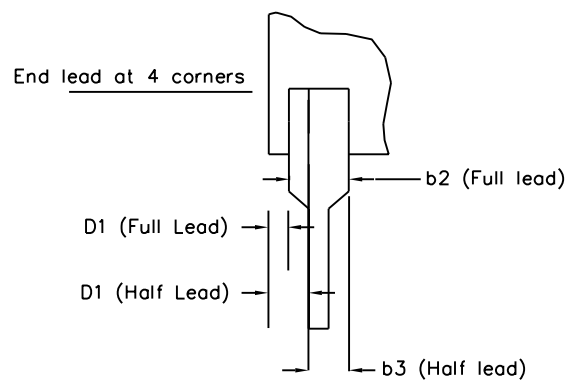
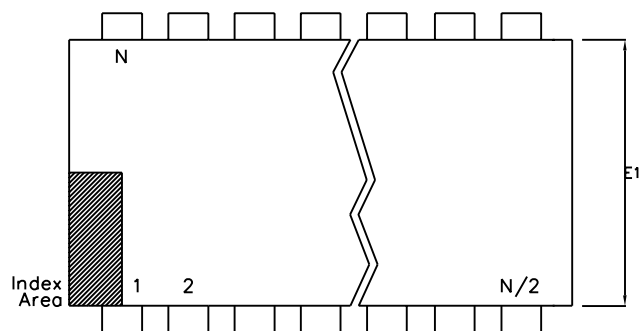
| Symbol | Control Dimensions in millimetres | | | Altern. Dimensions in inches | | |
|-----------------------------------|--------------------------------------|---------|-------|---------------------------------|---------|-------|
| | MIN | Nominal | MAX | MIN | Nominal | MAX |
| A | 2.35 | | 2.65 | 0.093 | | 0.104 |
| A1 | 0.10 | | 0.30 | 0.004 | | 0.012 |
| A2 | 2.25 | | 2.35 | 0.089 | | 0.092 |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| H | 10.00 | | 10.65 | 0.394 | | 0.419 |
| E | 7.40 | | 7.60 | 0.291 | | 0.299 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| b | 0.33 | | 0.51 | 0.013 | | 0.020 |
| c | 0.23 | | 0.32 | 0.009 | | 0.013 |
| θ | 0° | | 8° | 0° | | 8° |
| h | 0.25 | | 0.75 | 0.010 | | 0.029 |
| | Pin features | | | | | |
| N | 20 | | | | | |
| Conforms to JEDEC MS-013AC Iss. C | | | | | | |

Notes:

1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

| | | | | | | |
|---|--------|---------|---------|--|----------------------------------|--|
| © Zarlink Semiconductor 2002 All rights reserved. | | | | | Package Code DC | |
| ISSUE | 1 | 2 | 3 | | Previous package codes MP / S | Package Outline for 20 lead SOIC (0.300" Body Width) |
| ACN | 6746 | 201941 | 213098 | | | |
| DATE | 7Apr95 | 27Feb97 | 15Jul02 | | | GPD00015 |
| APPRD. | | | | | | |





| | Min mm | Max mm | Min Inches | Max Inches |
|------------------------------------|-----------|-----------|---------------|---------------|
| A | | 5.33 | | 0.210 |
| A1 | 0.38 | | 0.015 | |
| A2 | 2.92 | 4.95 | 0.115 | 0.195 |
| b | 0.36 | 0.56 | 0.014 | 0.022 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | n/a | n/a | n/a | n/a |
| c | 0.20 | 0.36 | 0.008 | 0.014 |
| D | 24.89 | 26.92 | 0.980 | 1.060 |
| D1 | 0.13 | | 0.005 | |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E1 | 6.10 | 7.11 | 0.240 | 0.280 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.62 BSC | | 0.300 BSC | |
| eB | | 10.92 | | 0.430 |
| eC | 0.00 | 1.52 | 0.000 | 0.060 |
| L | 2.92 | 3.81 | 0.115 | 0.150 |
| N | 20 | | 20 | |
| Conforms to Jedec MS-001AD Issue D | | | | |

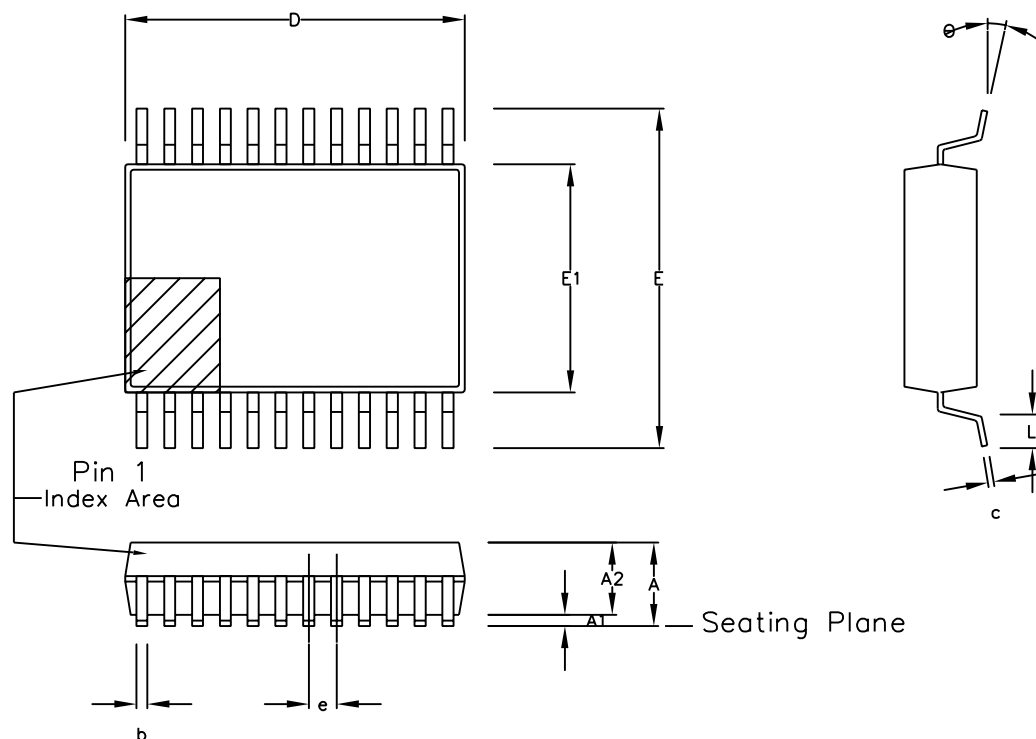
Notes:

1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum $\text{--- } \bar{C} \text{ ---}$
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: -
UK drawing # 418/ED/39502/005

| | | | | | | |
|---|--------|---------|--|--|----------------------------------|-------------------------------------|
| © Zarlink Semiconductor 2002 All rights reserved. | | | | | Package Code DA | |
| ISSUE | 1 | 2 | | | Previous package codes DP / E | Package Outline for 20 lead PDIP |
| ACN | 202562 | 213107 | | | | |
| DATE | 9Jun97 | 15Jul02 | | | | GPD00347 |
| APPRD. | | | | | | |





| Symbol | Control Dimensions in millimetres | | | Altern. Dimensions in inches | | |
|------------------------------------|--------------------------------------|---------|------|---------------------------------|---------|-------|
| | MIN | Nominal | MAX | MIN | Nominal | MAX |
| A | 1.70 | | 2.00 | 0.067 | | 0.079 |
| A1 | 0.05 | | 0.20 | 0.002 | | 0.008 |
| A2 | 1.65 | | 1.85 | 0.065 | | 0.073 |
| D | 7.90 | | 8.50 | 0.311 | | 0.335 |
| E | 7.40 | | 8.20 | 0.291 | | 0.323 |
| E1 | 5.00 | | 5.60 | 0.197 | | 0.220 |
| L | 0.55 | | 0.95 | 0.022 | | 0.037 |
| e | 0.65 BSC. | | | 0.026 BSC. | | |
| b | 0.22 | | 0.38 | 0.009 | | 0.015 |
| c | 0.09 | | 0.25 | 0.004 | | 0.010 |
| θ | 0° | | 8° | 0° | | 8° |
| | Pin features | | | | | |
| N | 24 | | | | | |
| Conforms to JEDEC MO-150 AG Iss. B | | | | | | |

This drawing supersedes: –
418/ED/51481/003 (UK)

Notes:

1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

| | | | | | | |
|---|---------|---------|---------|--|------------------------|---|
| © Zarlink Semiconductor 2002 All rights reserved. | | | | | Package Code DD | |
| ISSUE | 1 | 2 | 3 | | Previous package codes | Package Outline for 24 lead SSOP (5.3mm Body Width) |
| ACN | 201934 | 205233 | 213104 | | NP / N | |
| DATE | 27Feb97 | 25Sep98 | 15Jul02 | | | GPD00295 |
| APPRD. | | | | | | |





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