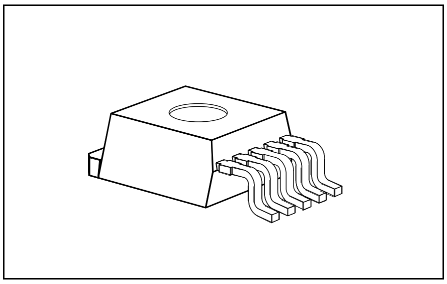
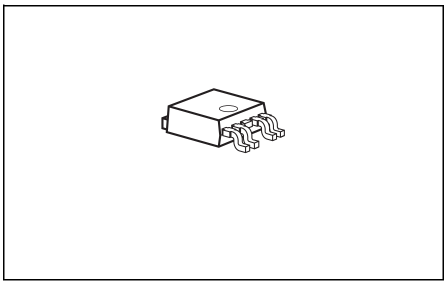
## 5-V Low Drop Fixed Voltage Regulator TLE 4270-2

### Features

- Output voltage tolerance ≤ ±2%
- 650 mA output current capability
- Low-drop voltage
- Reset functionality
- Adjustable reset time
- Suitable for use in automotive electronics
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Wide temperature range
- ESD protection: ±2kV HBM[1)]
- Green Product (RoHS compliant)
- AEC Qualified





### Functional Description

This device is a 5-V low drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V, ≤ 400 ms). Up to an input voltage of 26 V and for an output current up to 650 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and a temperature protection which turns off the device at high temperatures.

1) ESD susceptibility, Human Body Model (HBM) according to EIA/JESD 22-A114B

| Type | Package |
|---|---|
| TLE 4270-2 G | PG-TO263-5-1 |
| TLE 4270-2 D | PG-TO252-5-11 |

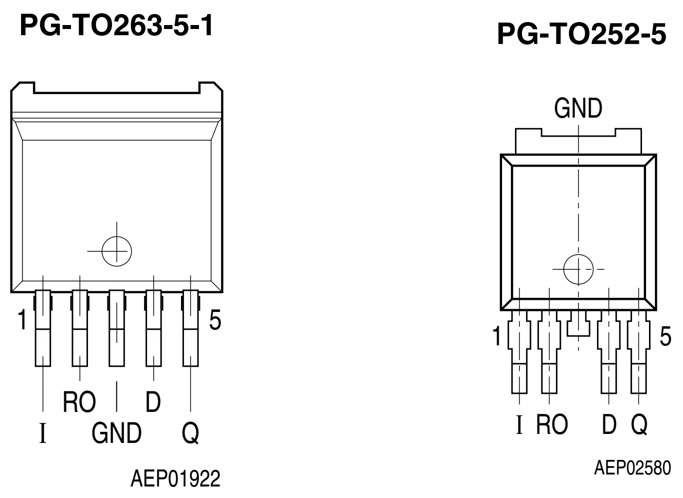



**Figure 1** **Pin Configuration** (top view)

**Table 1** **Pin Definitions and Functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | I | **Input;** block to ground directly at the IC with a ceramic capacitor. |
| 2 | RO | **Reset Output;** the open collector output is connected to the 5-V output via an integrated resistor of 30 kΩ. |
| 3 | GND | **Ground;** internally connected to heatsink. |
| 4 | D | **Reset Delay;** connect a capacitor to ground for delay time adjustment. |
| 5 | Q | **5-V Output;** block to ground with 22 µF capacitor, ESR < 3 Ω. |

## Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

## Application Description

The IC regulates an input voltage in the range of 5.5 V < $V_{\mathrm{I}}$ < 36 V to $V_{\mathrm{Q,nom}}$ = 5.0 V. Up to 26 V it produces a regulated output current of more than 650 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. A reset signal is generated for an output voltage of $V_{\mathrm{Q}}$ < 4.5 V. The delay for power-on reset can be set externally with a capacitor.

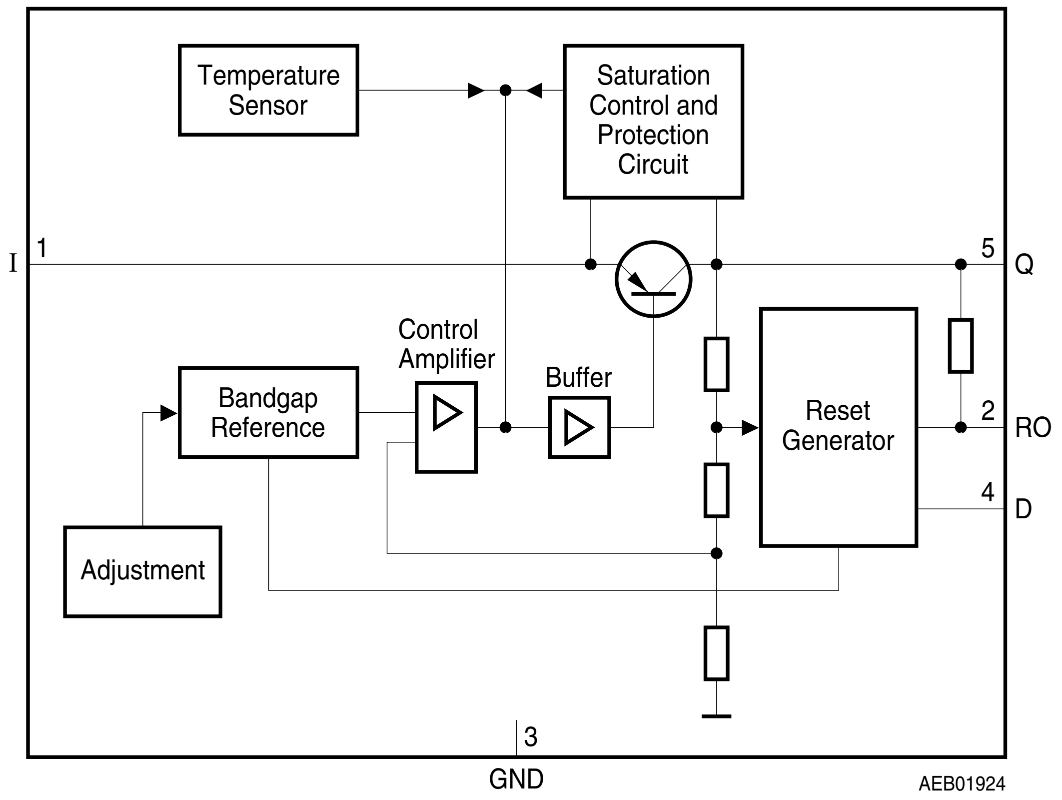



**Figure 2 Block Diagram**

**Table 2 Absolute Maximum Ratings**

$T_j$ = -40 to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| **Input I** | | | | | |
| Voltage | $V_I$ | -42 | 42 | V | – |
| Voltage | $V_I$ | – | 65 | V | $t \leq$ 400 ms |
| Current | $I_I$ | – | – | – | internally limited |
| **Reset Output RO** | | | | | |
| Voltage | $V_{RO}$ | -0.3 | 7 | V | – |
| Current | $I_{RO}$ | – | – | – | Internally limited |
| **Reset Delay D** | | | | | |
| Voltage | $V_D$ | -0.3 | 7 | V | – |
| Current | $I_D$ | – | – | – | Internally limited |
| **Output Q** | | | | | |
| Voltage | $V_Q$ | -1.0 | 16 | V | – |
| Current | $I_Q$ | – | – | – | Internally limited |
| **Ground GND** | | | | | |
| Current | $I_{GND}$ | -0.5 | – | A | – |
| **Temperatures** | | | | | |
| Junction temperature | $T_j$ | – | 150 | °C | – |
| Storage temperature | $T_{stg}$ | -50 | 150 | °C | – |

**Table 3 Operating Range**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Input voltage | $V_I$ | 6 | 42 | V | – |
| Junction temperature | $T_j$ | -40 | 150 | °C | – |
| **Thermal Resistance** | | | | | |
| Junction ambient | $R_{thj-a}$ | – | 65<br>79 | K/W<br>K/W | –<br>TO263, TO252[1)] |
| Junction case | $R_{thj-c}$ | – | 3 | K/W | TO-263 Packages |

1) Mounted on PCB, 80 × 80 × 1.5 mm$^3$; 35µ Cu; 5µ Sn; Footprint only; zero airflow.

**Table 4 Characteristics**

$V_I$ = 13.5 V; -40 °C ≤ $T_j$ ≤ 125 °C (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 5 mA ≤ $I_Q$ ≤ 550 mA; 6 V ≤ $V_I$ ≤ 26 V |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 26 V ≤ $V_I$ ≤ 36 V; $I_Q$ ≤ 300 mA |
| Output current limiting | $I_{Qmax}$ | 650 | 850 | – | mA | $V_Q$ = 0 V |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 1 | 1.5 | mA | $I_Q$ = 5 mA |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 55 | 75 | mA | $I_Q$ = 550 mA |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 70 | 90 | mA | $I_Q$ = 550 mA; $V_I$ = 5 V |
| Drop voltage | $V_{DR}$ | – | 350 | 700 | mV | $I_Q$ = 550 mA[1)] |
| Load regulation | $\Delta V_{Q,Lo}$ | – | 25 | 50 | mV | $I_Q$ = 5 to 550 mA; $V_I$ = 6 V |
| Line regulation | $\Delta V_{Q,Li}$ | – | 12 | 25 | mV | $V_I$ = 6 to 26 V $I_Q$ = 5 mA |
| Power supply Ripple rejection | $PSRR$ | – | 54 | – | dB | $f_r$ = 100 Hz; $V_r$ = 0.5 Vpp |
| **Reset Generator** | | | | | | |
| Switching threshold | $V_{RT}$ | 4.5 | 4.65 | 4.8 | V | – |
| Reset High voltage | $V_{ROH}$ | 4.5 | – | – | V | – |
| Reset low voltage | $V_{ROL}$ | – | 60 | – | mV | $R_{int}$ = 30 kΩ[2)]; 1.0 V ≤ $V_Q$ ≤ 4.5 V |
| Reset low voltage | $V_{ROL}$ | – | 200 | 400 | mV | $I_R$ = 3 mA, $V_Q$ = 4.4 V |
| Reset pull-up | $R_{int}$ | 18 | 30 | 46 | kΩ | internally connected to Q |
| Charge current | $I_{D,c}$ | 8 | 14 | 25 | µA | $V_D$ = 1.0 V |

**Table 4 Characteristics** (cont'd)

$V_I$ = 13.5 V; -40 °C ≤ $T_j$ ≤ 125 °C (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Upper reset timing threshold | $V_{DU}$ | 1.4 | 1.8 | 2.3 | V | – |
| Lower reset timing threshold | $V_{DL}$ | 0.2 | 0.45 | 0.8 | V | $V_Q < V_{RT}$ |
| Delay time | $t_{rd}$ | – | 13 | – | ms | $C_D$ = 100 nF |
| Reset reaction time | $t_{rr}$ | – | – | 3 | µs | $C_D$ = 100 nF |
| **Overvoltage Protection** | | | | | | |
| Turn-Off voltage | $V_{I,\,ov}$ | 42 | 44 | 46 | V | – |

1) Drop voltage = $V_I$ - $V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

2) Reset peak is always lower than 1.0 V.

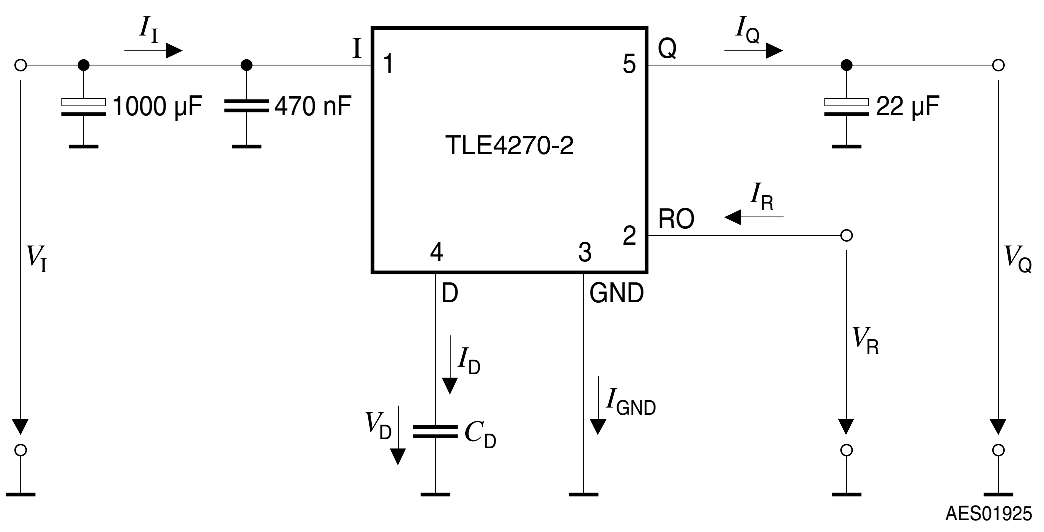



**Figure 3 Test Circuit**

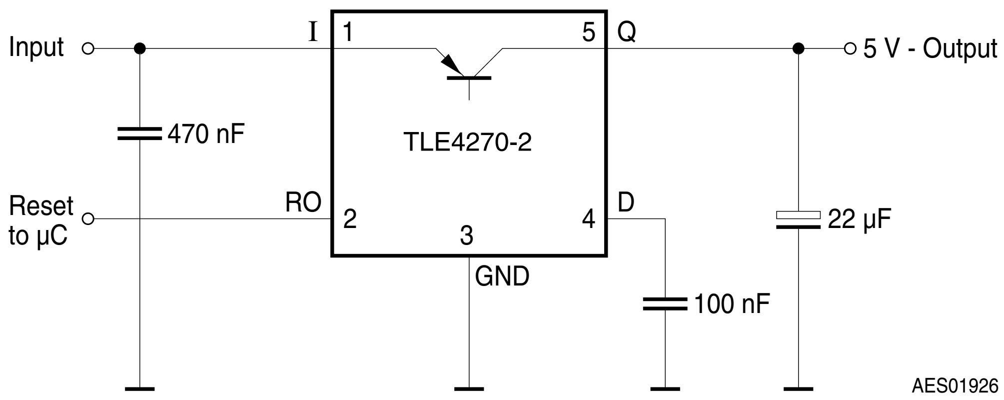



**Figure 4 Application Circuit**

## Design Notes for External Components

An input capacitor $C_I$ is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with $C_I$. An output capacitor $C_Q$ is necessary for the stability of the regulating circuit. Stability is guaranteed at values of $C_Q \geq 22$ µF and an ESR of < 3 Ω.

## Reset Circuitry

If the output voltage decreases below 4.5 V, an external capacitor $C_D$ on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below $V_{DL}$, a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above the reset threshold, $C_D$ will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches $V_{DU}$ and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of $C_D$.

## Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor $C_D$ which can be calculated as follows:

$$C_D = (\Delta t \times I_{D,c})/\Delta V \qquad (1)$$

Definitions:

- $C_D$ = delay capacitors
- $\Delta t$ = reset delay time $t_{rd}$
- $I_{D,c}$ = charge current, typical 14 µA
- $\Delta V = V_{DU}$, typical 1.8 V

$V_{DU}$ = upper reset timing threshold at $C_D$ for reset delay time

$$t_{rd} = \Delta V \times C_D / I_{D,c} \qquad (2)$$

The reset reaction time $t_{rr}$ is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 47 nF. For other values for $C_D$ the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20\ \text{s/F} \times C_D \qquad (3)$$

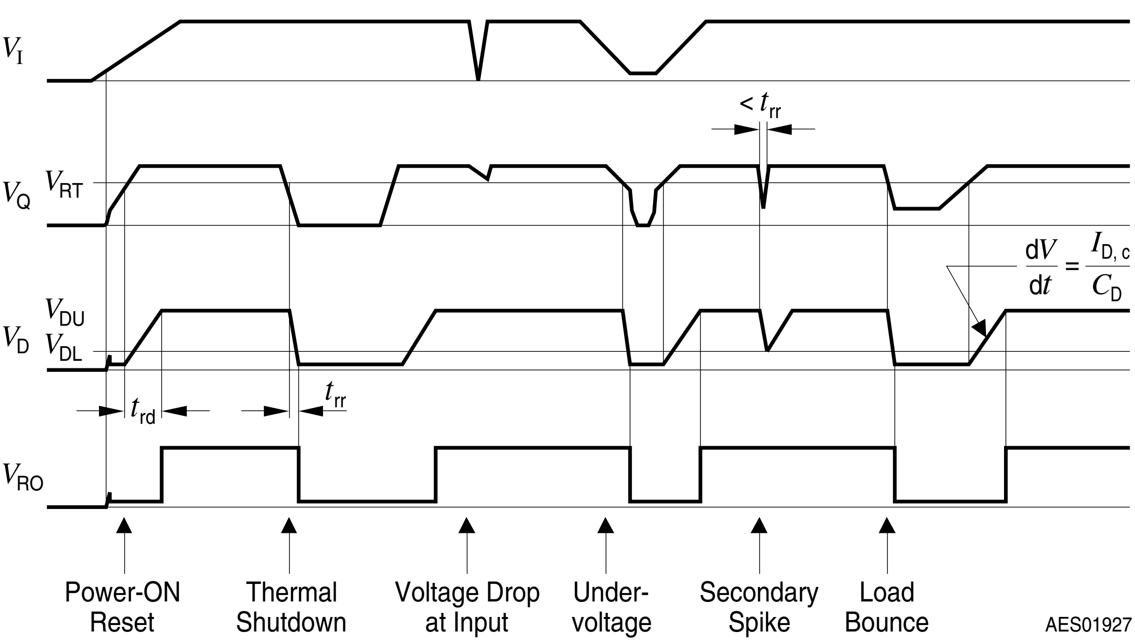
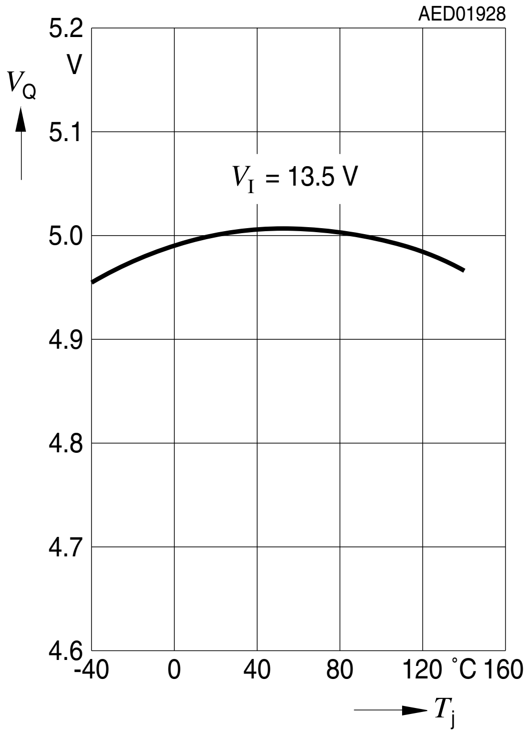
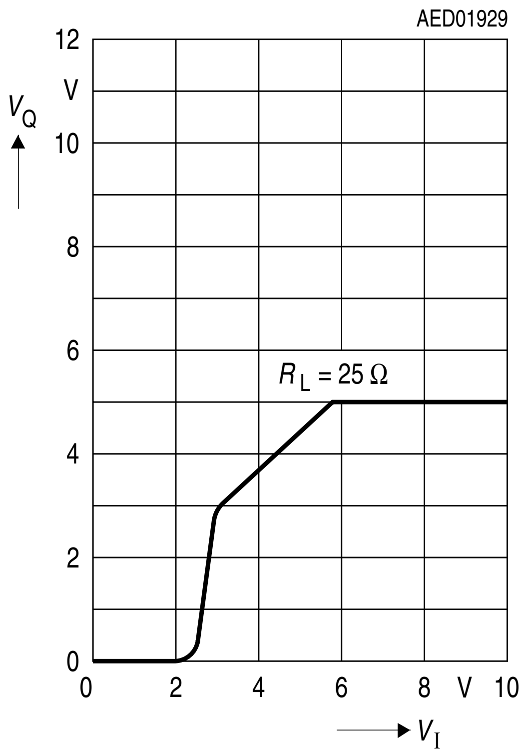



**Figure 5 Reset Time Response**

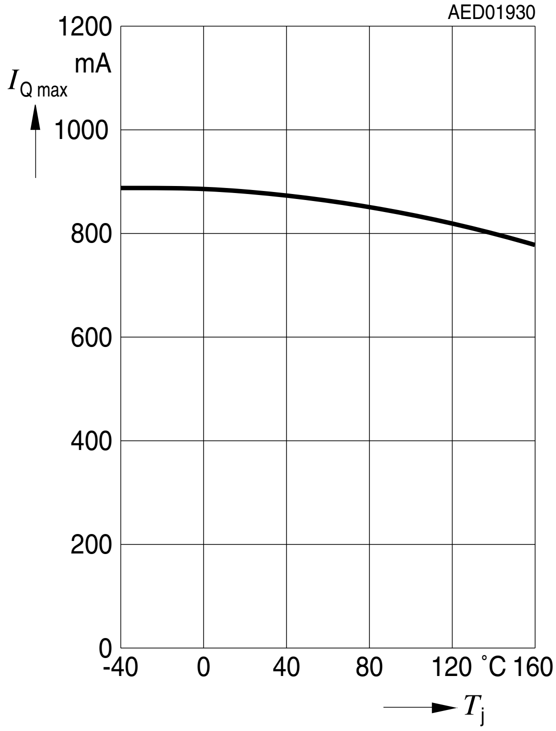
**Output Voltage $V_Q$ versus Temperature $T_j$**



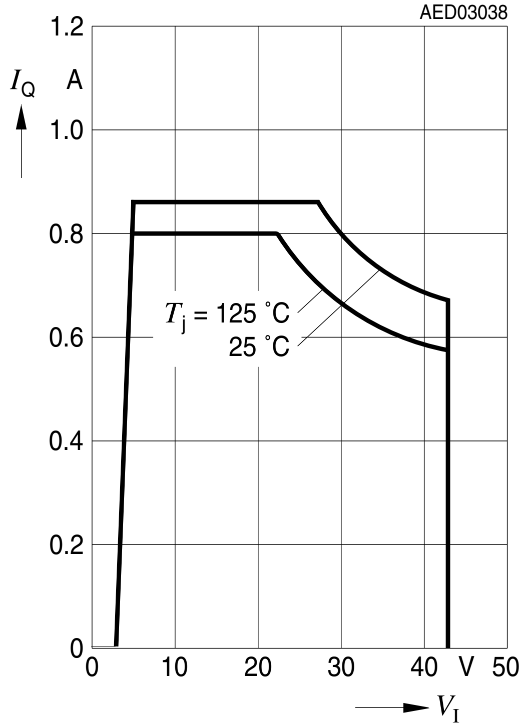

**Output Voltage $V_Q$ versus Input Voltage $V_I$**



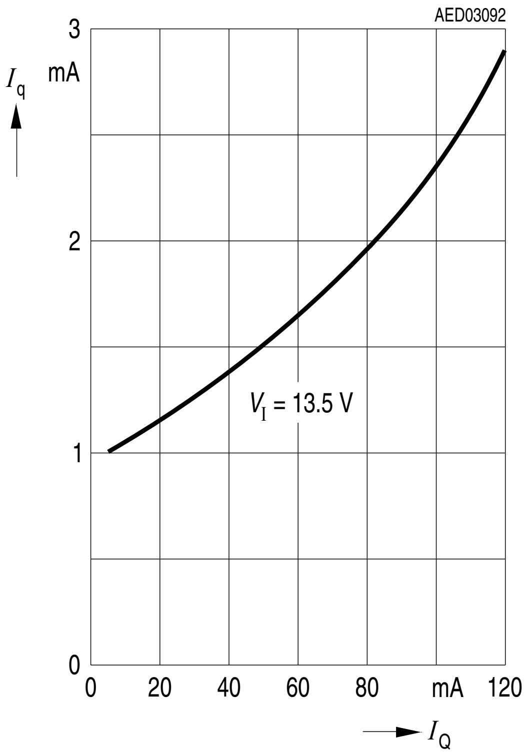

**Output Current $I_Q$ versus Temperature $T_j$**



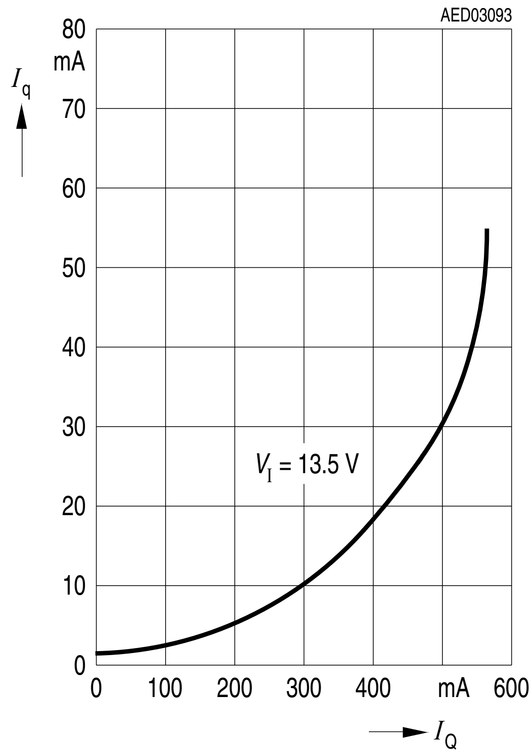

**Output Current $I_Q$ versus Input Voltage $V_I$**



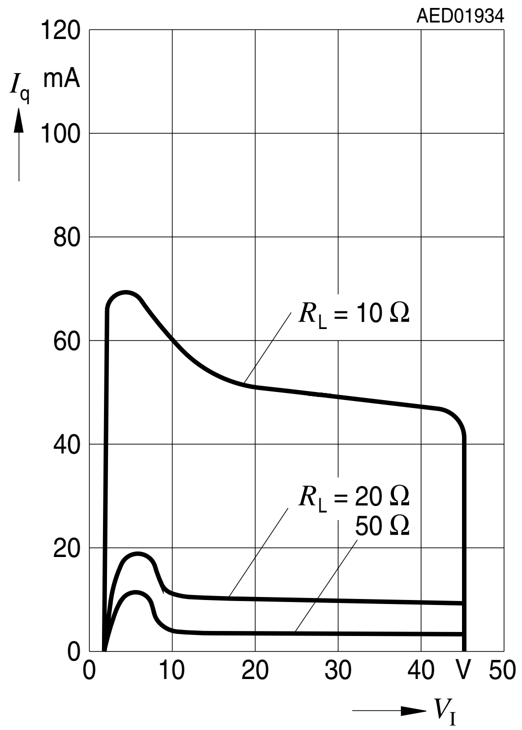
### Current Consumption $I_q$ versus Output Current $I_Q$



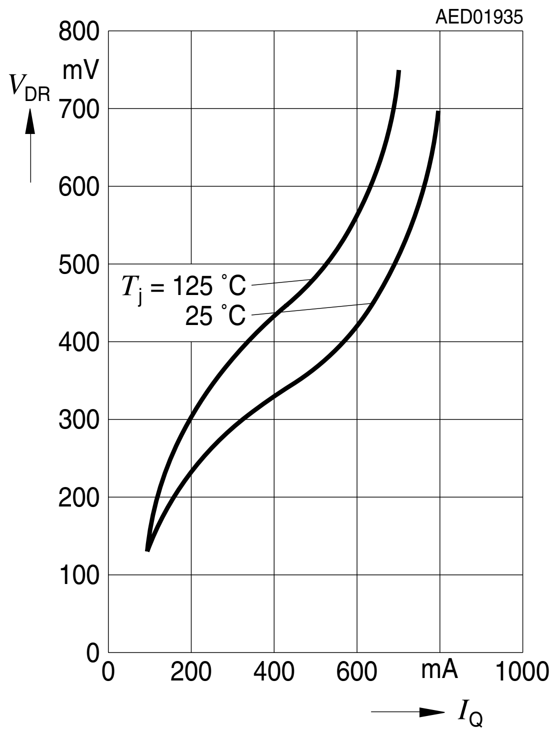

### Current Consumption $I_q$ versus Output Current $I_Q$



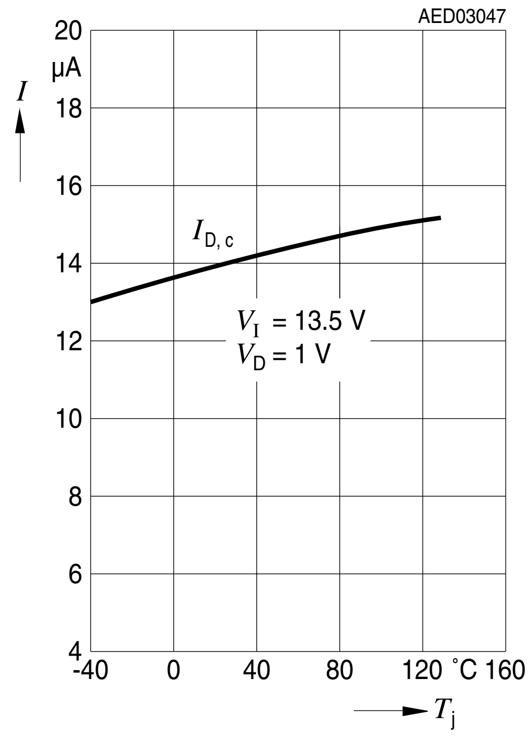

### Current Consumption $I_q$ versus Input Voltage $V_I$



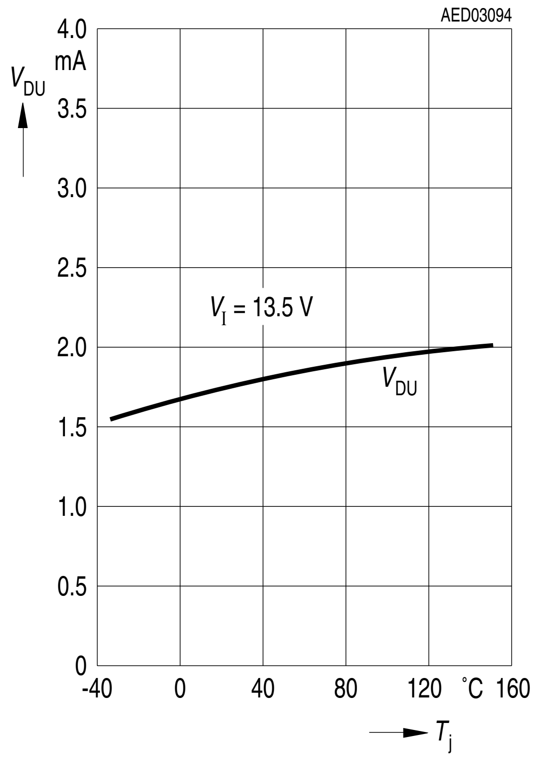

### Drop Voltage $V_{DR}$ versus Output Current $I_Q$



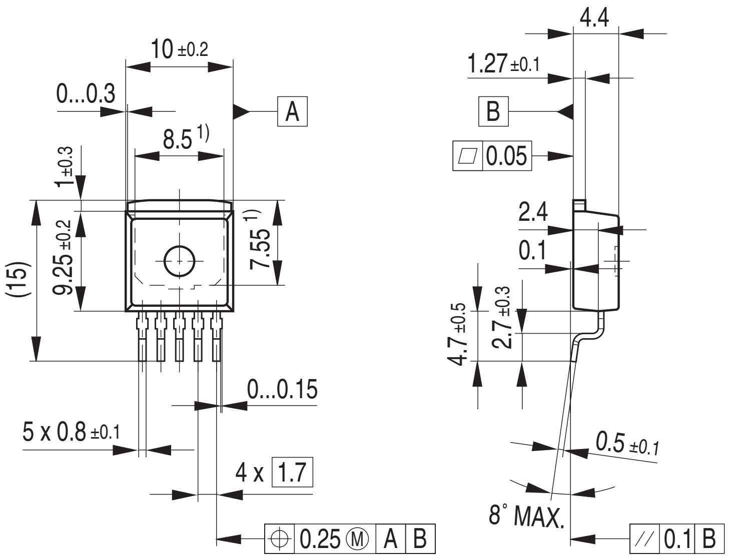
**Charge Current $I_{D,c}$ versus Temperature $T_j$**




**Upper Reset Timing Threshold $V_{DU}$ versus Temperature $T_j$**



## Package Outlines




1) Typical

Metal surface min. X = 7.25, Y = 6.9

All metal surfaces tin plated, except area of cut.

GPT09113

GPT09113

**Figure 6** **PG-TO263-5-1** (Plastic Transistor Single Outline)

### **Green Product** (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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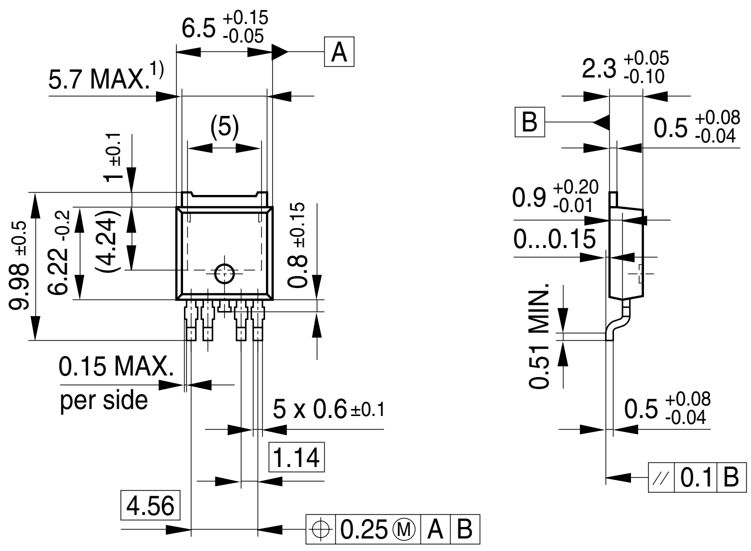
SMD = Surface Mounted Device

Dimensions in mm




1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

GPT09527

**Figure 7** **PG-TO252-5-11** (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

## Revision History

| Version | Date | Changes |
|---|---|---|
| Rev. 1.8 | 2007-11-09 | **Page 1**: Changed ESD specification from ">4000V" to "±2kV HBM" according to PCN No. 2007-089 |
| Rev. 1.7 | 2007-03-20 | Initial version of RoHS-compliant derivate of TLE 4270<br>Change of product name to TLE 4270-2 due to modified chip layout and size.<br>**Page 1**: AEC certified statement added<br>**Page 1** and **Page 14**: RoHS compliance statement and Green product feature added<br>**Page 1** and **Page 14**: Package changed to RoHS compliant version<br>Legal Disclaimer updated |

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**Телефон:** 8 (812) 309 58 32 (многоканальный)
**Факс:** 8 (812) 320-02-42
**Электронная почта:** org@eplast1.ru
**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.