Atmel AT42QT1050

Five-channel QTouch® Touch Sensor IC

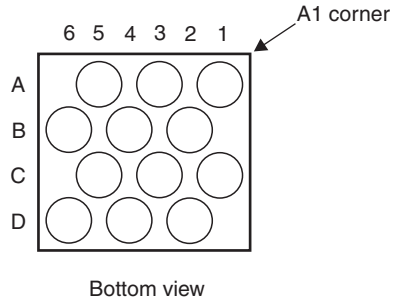
PRELIMINARY DATASHEET

Features

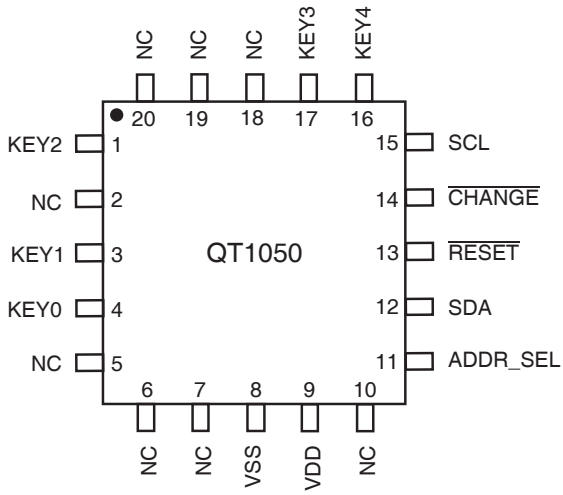
- Configurations:
  - Comms mode
- Number of Keys:
  - 1 to 5 keys (or 1 to 4 keys plus a Guard Channel)
- Technology:
  - Patented spread-spectrum QTouchADC charge-transfer
- Key Outline Sizes:
  - 6 mm × 6 mm or larger (panel thickness dependent); widely different sizes and shapes possible
- Layers Required:
  - One
- Electrode Materials:
  - Etched copper; Silver; Carbon; Indium Tin Oxide (ITO)
- Panel Materials:
  - Plastic; Glass; Composites; Painted surfaces (low particle density metallic paints possible)
- Panel Thickness:
  - Up to 10 mm glass (electrode size dependent)
  - Up to 5 mm plastic (electrode size dependent)
- Key Sensitivity:
  - Individually settable using simple commands over I^2C interface
- Interface:
  - I^2C slave mode (400 kHz). Discrete detection outputs
- Signal Processing:
  - Self-calibration
  - Auto-drift compensation
  - Noise filtering
  - Adjacent Key Suppression® (AKS®) – up to three groups possible
- Moisture Tolerance:
  - Increased moisture tolerance based on hardware design and firmware tuning
- Power Saving
  - Low Power (LP) mode supports both Low Power and Deep Sleep modes
- Power:
  - 1.8 V to 5.5 V
- Package:
  - 12-ball WLCSP RoHS-compliant IC
  - 20-pin VQFN RoHS-compliant IC

1. Pinouts and Schematics

1.1 Pinout Configuration (WLCSP)



1.2 Pinout Configuration (VQFN)



1.3 Pin Descriptions (WLCSP)

Table 1-1. Ball Listings (12-ball WLCSP)

Ball	Function	Type	Description	If Unused, Connect To...
A1	KEY2	O	Key 2	Open
A3	KEY0	O	Key 0	Open
A5	KEY1	O	Key 1	Open
B2	KEY4	O	Key 4	Open
B4	VSS	P	Ground	–
B6	VDD	P	Power	–
C1	KEY3	O	Key 3	Open
C3	SCL	OD	Connect to I^2C clock	Open
C5	SDA	OD	I^2C data line	Open
D2	$\overline{\text{CHANGE}}$	OD	$\overline{\text{CHANGE}}$ line for controlling the communications flow	Open
D4	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ – has internal pull-up 60 kΩ resistor	Open
D6	ADDR_SEL	I	I^2C Address select. See “I2C Addresses” on page 12.	–

I	Input only	0	Output only, push-pull
OD	Open-drain Output	P	Ground or Power

1.4 Pin Descriptions (VQFN)

Table 1-2. Pin Listings (20-pin VQFN)

Pin	Function	Type	Description	If Unused, Connect To...
1	KEY2	O	Key 2	Open
2	NC	–	Not Connected	–
3	KEY1	O	Key 1	Open
4	KEY0	O	Key 0	Open
5	NC	–	Not Connected	–
6	NC	–	Not Connected	–
7	NC	–	Not Connected	–
8	VSS	P	Ground	–
9	VDD	P	Power	–
10	NC	–	Not Connected	–
11	ADDR_SEL	I	I^2C Address select. See “I2C Addresses” on page 12.	–
12	SDA	OD	I^2C data line	Open
13	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ – has internal pull-up 60 kΩ resistor	Open
14	$\overline{\text{CHANGE}}$	OD	$\overline{\text{CHANGE}}$ line for controlling the communications flow	Open
15	SCL	OD	Connect to I^2C clock	Open
16	KEY4	O	Key 4	Open
17	KEY3	O	Key 3	Open
18	NC	–	Not Connected	–
19	NC	–	Not Connected	–
20	NC	–	Not Connected	–

I	Input only	0	Output only, push-pull
OD	Open-drain Output	P	Ground or Power

1.5 Schematic

Figure 1-1. Typical Circuit (12-ball WLCSP)

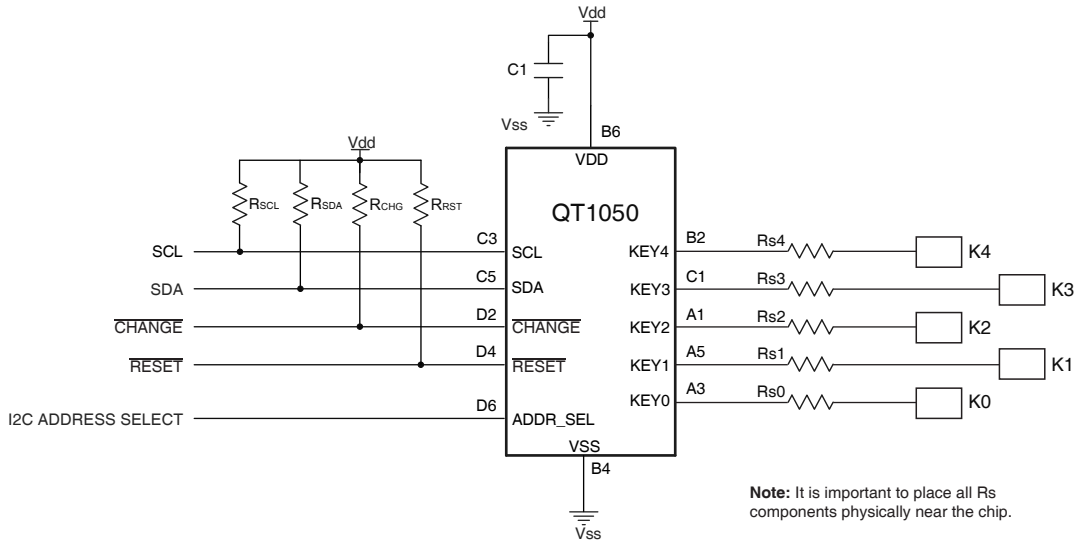
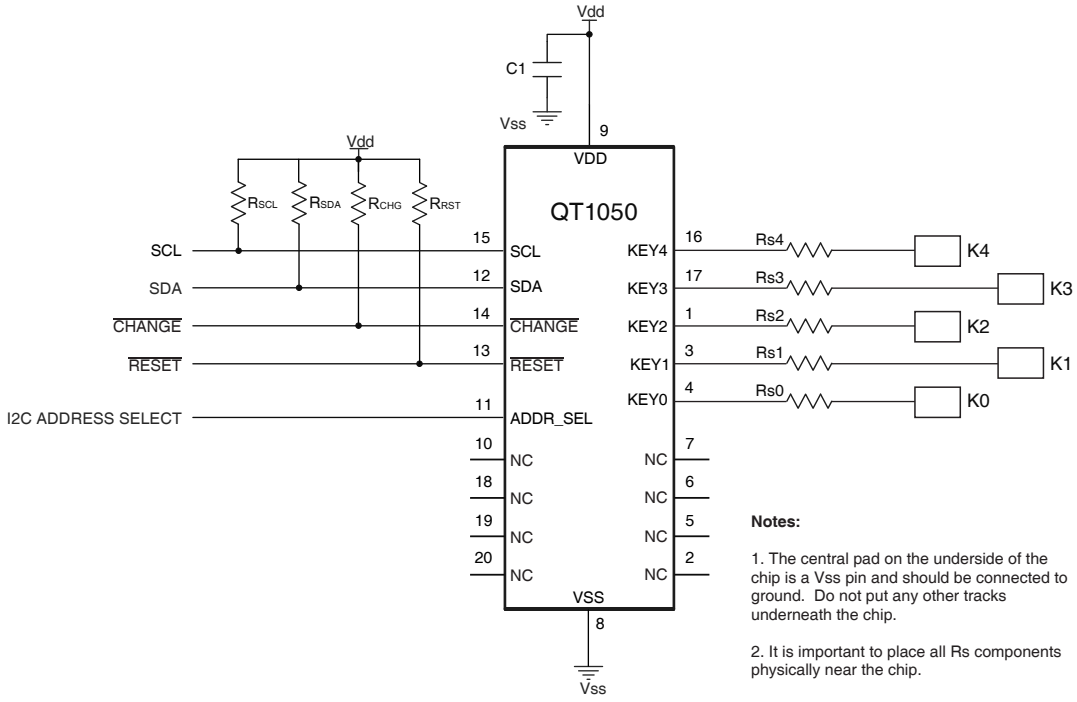


Figure 1-2. Typical Circuit (20-pin VQFN)



Check the following sections for component values and settings for Figure 1-1 and Figure 1-2:

- Section 3.1 on page 10: Series resistors (Rs0 – Rs4)
- Section 3.3 on page 10: LED traces
- Section 3.5 on page 11: Power Supply (voltage levels)
- Section 4.2 on page 12: I^2C Address selection
- Section 4.4 on page 14: SDA, SCL pull-up resistors (R_{SDA}, R_{SCL})
- Section 2.7 on page 7: $\overline{\text{CHANGE}}$ pull-up resistor (R_{CHG})
- Section 2.8.1 on page 7: $\overline{\text{RESET}}$ pull-up resistor (R_{RST})

2. Overview

2.1 Introduction

The AT42QT1050 (QT1050) is a QTouchADC sensor driver. The device can sense from one to five keys, dependent on mode.

The QT1050 includes all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions, and the outputs are fully debounced. Only a few external parts are required for operation and no external Cs capacitors are required.

The QT1050 modulates its bursts in a spread-spectrum fashion in order to heavily suppress the effects of external noise, and to suppress RF emissions. The QT1050 uses a QTouchADC method of acquisition. This provides greater noise immunity and eliminates the need for external sampling capacitors, allowing touch sensing using a single pin.

2.2 Comms Modes

The QT1050 operates in comms mode where a host can communicate with the device via an I^2C bus. This allows the user to configure settings for *Threshold*, *Adjacent Key Suppression* (AKS), *Detect Integrator*, *Low Power (LP) Mode*, *Guard Channel*, and *Max Time On* for keys.

2.3 Keys

The QT1050 can have a minimum of one key and a maximum of five keys. These can be constructed in different shapes and sizes. See "Features" on page 1 for the recommended dimensions.

- 1 to 5 keys (or 1 to 4 keys plus Guard Channel)

Unused keys should be disabled by setting the Detect Integrator (DI) to zero (see Section 5.10 on page 21).

The status register can be read to determine the touch status of the corresponding key. It is recommended using the open-drain $\overline{\text{CHANGE}}$ line to detect when a change of status has occurred.

2.4 Moisture Tolerance

The presence of water (condensation, sweat, spilt water, and so on) on a sensor can alter the signal values measured and thereby affect the performance of any capacitive device. The moisture tolerance of QTouch devices can be improved by designing the hardware and fine-tuning the firmware following the recommendations in the application note Atmel *AVR3002: Moisture Tolerant QTouch Design* (www.atmel.com/Images/doc42017.pdf).

2.5 Acquisition/Low Power Mode (LP)

There are 255 different acquisition times possible. These are controlled via the LP mode byte (see Section 5.11 on page 22) which can be written to via I^2C-compatible communication.

LP mode controls the intervals between acquisition measurements. Longer intervals consume lower power but have an increased response time. During calibration, touch and during the detect integrator (DI) period, the LP mode is temporarily set to LP mode 1 for a faster response.

The QT1050 operation is based on a fixed cycle time of approximately 8 ms. The LP mode setting indicates how many of these periods exist per measurement cycle. For example, If LP mode = 1, there is an acquisition every cycle (8 ms). If LP mode = 3, there is an acquisition every 3 cycles (24 ms). If a high Pulse/Scale (see Section 5.9 on page 19) setting is selected then the acquisition time may exceed 8 ms.

LP settings above mode 32 (512 ms) result in slower thermal drift compensation and should be avoided in applications where fast thermal transients occur.

2.6 Adjacent Key Suppression (AKS) Technology

The device includes the Atmel-patented Adjacent Key Suppression (AKS) technology, to allow the use of tightly spaced keys on a keypad with no loss of selectability by the user.

There can be up to three AKS groups, implemented so that only one key in the group may be reported as being touched at any one time. Once a key in a particular AKS group is in detect no other key in that group can go into detect. Only when the key in detect goes out of detection can another key go into detect state.

The keys which are members of the AKS groups can be set (see Section 5.9 on page 19). Keys outside the group may be in detect simultaneously.

Note: When multiple keys in an AKS group are touched then a key must be fully out of detect before the next key will report touch. So effectively a break-before-make operation.

2.7 $\overline{\text{CHANGE}}$ Line

The $\overline{\text{CHANGE}}$ line is active low and signals when there is a change of state in the Detection or Input key status bytes. It is cleared (allowed to float high) when the host reads the status bytes.

If the status bytes change back to their original state before the host has read the status bytes (for example, a touch followed by a release), the $\overline{\text{CHANGE}}$ line will be held low. In this case, a read to any memory location will clear the $\overline{\text{CHANGE}}$ line.

The $\overline{\text{CHANGE}}$ line is open-drain and should be connected via a 47 kΩ resistor to Vdd. It is necessary for minimum power operation as it ensures that the QT1050 can sleep for as long as possible. Communications wake up the QT1050 from sleep causing a higher power consumption if the part is randomly polled.

Note: The $\overline{\text{CHANGE}}$ line is pulled low 100 ms after power-up or reset.

2.8 Types of Reset

2.8.1 External Reset

An external reset logic line can be used, if desired, fed into the $\overline{\text{RESET}}$ pin. This pin should be pulled up by a 100 kΩ resistor to Vdd.

2.8.2 Soft Reset

The host can cause a device reset by writing `0x80` to the RESET / Calibrate byte. This soft reset triggers the internal watchdog timer on a 125 ms interval. After 125 ms the device resets and wakes again.

The device NACKs any attempts to communicate with it during the first 30 ms of its initialization period.

2.9 Calibration

Writing a non-zero value to low 7-bits of the RESET / Calibrate byte will force a recalibration at any time. This can be useful to clear out a stuck key condition after a prolonged period of uninterrupted detection.

Note: A calibrate command clears all key status bits and the overflow bit (until it is checked on the next cycle).

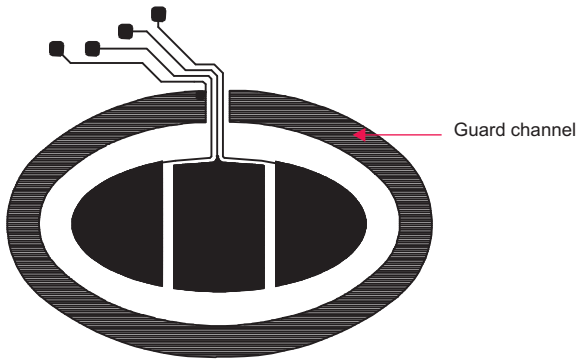
2.10 Guard Channel

A guard channel to help prevent false detection is available. This is programmable for comms mode.

Guard channel keys should be more sensitive than the other keys (physically bigger). Because the guard channel key is physically bigger it becomes more susceptible to noise so it has higher Oversampling (see Section 5.9 on page 19) and a lower Threshold (see Section 5.8 on page 19) than the other keys.

A channel set as the guard channel (there can only be one) is prioritised when the filtering of keys going into detect is taking place. So if a normal key is filtering into touch (touch present but DI has not been reached) and the key set as the guard key begins filtering in, then the normal key filter is reset and the guard key filters in first.

Figure 2-1. Guard Channel Example



2.11 Signal Processing

2.11.1 Detect Threshold

The device detects a touch when the signal has crossed a threshold level and remained there for a specified number of counts (see Section 5.10 on page 21). This can be altered on a key-by-key basis using the key threshold I^2C-compatible commands.

The reference level has the ability to adjust itself slowly in accordance with the drift compensation mechanism.

The drift mechanism will drift toward touch at a rate of 160 ms × 18 = 2.88 seconds and away from touch at a rate of 160 ms × 6 = 0.96 seconds. The 160 ms is based on 20 × 8 ms cycles. If the cycle time exceeds 8 ms then the overall times will be extended to match.

2.11.2 Detect Integrator

The device features a fast detection integrator counter (DI filter), which acts to filter out noise at the small expense of a slower response time. The DI filter requires a programmable number of consecutive samples confirmed in detection before the key is declared to be touched. The minimum number for the DI filter is 2. Settings of 1 for the DI also defaults to 2. Setting a DI of 0 disables the corresponding key.

The signal value which can be read in RAM is a filtered signal value. Using the Fast In option (Bit 6 of address 60) the chip can be made to enter fast mode (LPM = 1) when a raw signal reading is detected above threshold. This would allow the chip to react quicker to a touch in cases where a high LPM setting is being used.

Note: If the circuit is in a noisy environment this could have the effect of causing the chip to enter fast mode more often than is necessary.

The DI is also implemented when a touch is removed. There is also a Fast Out DI option. When bit 5 of Address 60 is set the key filters out with an integrator of 4.

2.11.3 Cx Limitations

The recommended range for key capacitance Cx is 1 pF – 30 pF. Larger values of Cx will give reduced sensitivity.

2.11.4 Max On Duration

If an object or material obstructs the sense pad the signal may rise enough to create a detection, preventing further operation. To prevent this, the sensor includes a timer which monitors detections. If a detection exceeds the timer setting the sensor performs a key recalibration. This is known as the Max On duration feature and is set to approximately 30s in standalone mode.

This feature can be changed by setting a value in the range 1 – 255 (160 ms – 40,800 ms) in steps of 160 ms. A setting of 0 disables the Max On Duration recalibration feature.

Note: If bit 4 of address 60 is clear then a recalibration of all keys occurs on *Max On Duration*, otherwise individual key recalibration occurs.

2.11.5 Positive Recalibration

If a key signal jumps in the negative direction (with respect to its reference) by more than the Positive Recalibration setting (25% of threshold or minimum 4 counts), then a recalibration of that key takes place.

2.11.6 Drift Hold Time

Drift Hold Time (DHT) is used to restrict drift on all keys while one or more keys are activated. DHT restricts the drifting on all keys until approximately four seconds after all touches have been removed.

This feature is particularly useful in cases of high-density keypads where touching a key or hovering a finger over the keypad would cause untouched keys to drift, and therefore create a sensitivity shift, and ultimately inhibit touch detection.

2.11.7 Hysteresis

Hysteresis is fixed at 12.5% of the Detect Threshold. When a key enters a detect state once the DI count has been reached, the NTHR value is changed by a small amount (12.5% of NTHR) in the direction away from touch. This is done to alter hysteresis and so makes it less likely a key will dither in and out of detect. NTHR is restored once the key drops out of detect.

Note: There is a minimum value for hysteresis of 2 so a threshold of 2 or less should never be selected.

3. Wiring and Parts

3.1 Rs Resistors

Series resistors Rs (Rs0 – Rs4) are in line with the electrode connections and should be used to limit electrostatic discharge (ESD) currents and to suppress radio frequency interference (RFI). Series resistors are recommended for noise reduction. They should be approximately 4.7 kΩ to 20 kΩ each. Care should be taken in this case that the sensor keys are fully charged. The Charge Share Delay time may need to be increased (see Section 5.15 on page 24). Each count increase will extend the charge pulse by approximately 2.5 µs.

For improved Conducted Immunity as increased Rs resistor is recommended. With an increased series resistor, the RC time constant formed in combination with sensor capacitance will slow down the charge transfer settling process. In order to obtain stable and repeatable results, it is important to ensure proper settling process. For an overview of charge transfer pulses and method to observe good and bad charge pulses using an oscilloscope, refer to the 'Charge transfer' section in the Atmel *Touch Sensor Design Guide*. In order to achieve good charge pulses, the firmware parameter to control the charge transfer time should be increased.

In the case of the QT1050 this is the Charge Share Delay byte. This setting increases the Charge Share time by approx 2.5 µs for every count increase.

3.2 Conducted Immunity

Although most applications do not require a high level of immunity to conducted noise, certain industry sectors have defined standards for EMC compliance. When using capacitive touch interfaces in such environments, it is important to understand the implications of conducted noise and how to mitigate the effects through careful design.

Capacitive touch applications are generally not affected by common-mode noise until human interaction takes place. This is because the power supply lines maintain a stable difference between Vdd and Vss and as no return path is provided to the noise source reference (usually earth), the circuit functions normally.

For further information, refer to: *Atmel AVR3000: QTouch Conducted Immunity Application Note.*

3.3 LED Traces and Other Switching Signals

Digital switching signals near the sense lines induce transients into the acquired signals, deteriorating the signal-to-noise (SNR) performance of the device. Such signals should be routed away from the sensing traces and electrodes, or the design should be such that these lines are not switched during the course of signal acquisition (bursts).

LED terminals which are multiplexed or switched into a floating state, and which are within, or physically very near, a key (even if on another nearby PCB) should be bypassed to either Vss or Vdd with at least a 10 nF capacitor. This is to suppress capacitive coupling effects which can induce false signal shifts. The bypass capacitor does not need to be next to the LED, in fact it can be quite distant. The bypass capacitor is noncritical and can be of any type.

LED terminals which are constantly connected to Vss or Vdd do not need further bypassing.

3.4 PCB Cleanliness

Modern no-clean flux is generally compatible with capacitive sensing circuits.

CAUTION: If a PCB is reworked in any way, it is highly likely that the behavior of the no-clean flux will change. This can mean that the flux changes from an inert material to one that can absorb moisture and dramatically affect capacitive measurements due to additional leakage currents. If so, the circuit can become erratic and exhibit poor environmental stability.

If a PCB is reworked in any way, clean it thoroughly to remove all traces of the flux residue around the capacitive sensor components. Dry it thoroughly before any further testing is conducted.

3.5 Power Supply

See Section 6.2 on page 25 for the power supply range. If the power supply fluctuates slowly with temperature, the device tracks and compensates for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The usual power supply considerations with QT™ parts apply to the device. The power should be clean and come from a separate regulator if possible. However, this device is designed to minimize the effects of unstable power, and except in extreme conditions should not require a separate Low Dropout (LDO) regulator.

CAUTION: A regulator IC shared with other logic can result in erratic operation and is **not** advised.

A single ceramic 0.1 µF bypass capacitor, with short traces, should be placed very close to the power pins of the IC. Failure to do so can result in device oscillation, high current consumption and erratic operation.

It is assumed that a larger bypass capacitor (such as 1 µF) is somewhere else in the power circuit; for example, near the regulator.

4. I²C Communications

4.1 I²C Protocol

4.1.1 Protocol

The I²C protocol is based around access to an address table (see Table 5-1 on page 15) and supports multi-byte reads and writes. The maximum clock rate is 400 kHz.

See Section A. on page 32 for an overview of I²C bus operation.

4.1.2 Signals

The I²C interface requires two signals to operate:

- **SDA** - Serial Data
- **SCL** - Serial Clock

A third line, $\overline{\text{CHANGE}}$, is used to signal when the device has seen a change in the status byte:

- $\overline{\text{CHANGE}}$**:** Open-drain, active low when any capacitive key has changed state since the last I²C-compatible read. After reading the two status bytes, this pin floats (high) again if it is pulled up with an external resistor. If the status bytes change back to their original state before the host has read the status bytes (for example, a touch followed by a release), the $\overline{\text{CHANGE}}$ line is held low. In this case, a read to any memory location clears the $\overline{\text{CHANGE}}$ line.

4.2 I²C Addresses

There are two selectable I²C addresses of `0x41` and `0x46`. Pulling the ADDR_SEL pin (D6) low on power up sets I²C address of `0x41` while pulling this pin high on power up sets I²C address of `0x46`.

4.3 Data Read/Write

4.3.1 Writing Data to the Device

The sequence of events required to write data to the device is:

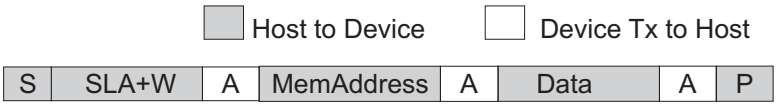


Table 4-1. Description of Write Data Bits

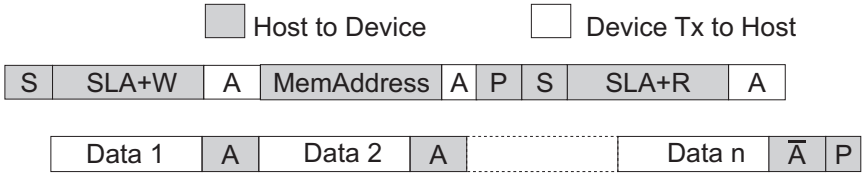
Key	Description
S	START condition
SLA+W	Slave address plus write bit
A	Acknowledge bit
MemAddress	Target memory address within device
Data	Data to be written
P	Stop condition

1. The host initiates the transfer by sending the START condition.
2. The host follows this by sending the slave address of the device together with the WRITE bit.
3. The device sends an ACK.
4. The host then sends the memory address within the device to which it wishes to write.
5. The device sends an ACK if the write address is in the range `0x00` – `0x7F`, otherwise it sends a NACK.
6. The host transmits one or more data bytes; each is acknowledged by the device (unless trying to write to an invalid address).
7. If the host sends more than one data byte, they are written to consecutive memory addresses.
8. The device automatically increments the target memory address after writing each data byte.
9. After writing the last data byte, the host should send the STOP condition.

Note: the host should not try to write to addresses outside the range `0x20` to `0x3F` because this is the limit of the device internal memory addresses.

4.3.2 Reading Data From the Device

The sequence of events required to read data from the device is:



1. The host initiates the transfer by sending the START condition.
2. The host follows this by sending the slave address of the device together with the WRITE bit.
3. The device sends an ACK.
4. The host then sends the memory address within the device it wishes to read from.
5. The device sends an ACK if the address to be read from is less than `0x80`, otherwise it sends a NACK.
6. The host must then send a STOP and a START condition followed by the slave address again but this time accompanied by the READ bit.

Note: Alternatively, instead of step 6, a repeated START can be sent so the host does not need to relinquish control of the bus.

7. The device returns an ACK, followed by a data byte.
8. The host must return either an ACK or NACK.
   1. If the host returns an ACK, the device subsequently transmits the data byte from the next address. Each time a data byte is transmitted, the device automatically increments the internal address. The device continues to return data bytes until the host responds with a NACK.
   2. If the host returns a NACK, it should then terminate the transfer by issuing the STOP condition. A repeated START can also be used instead of STOP condition.
9. The device resets the internal address to the location indicated by the memory address sent to it previously. Therefore, there is no need to send the memory address again when reading from the same location.

Note: Reading the 16-bit reference and signal values is not an atomic operation; reading the first byte of a 16-bit value does not lock the other byte. As a result glitches in the reported value may be seen as values increase from 255 to 256, or decrease from 256 to 255.
Use of a Repeated START to terminate a read-transfer is also supported.

4.4 SDA, SCL

The I^2C-compatible bus transmits data and clock with SDA and SCL respectively. They are open-drain; that is, I^2C-compatible master and slave devices can only drive these lines low or leave them open. The termination resistors pull the line up to Vdd if no I^2C-compatible device is pulling it down.

The pull-up resistors commonly range from 1 kΩ to 10 kΩ and should be chosen so that the rise times on SDA and SCL meet the I^2C-compatible specifications (≤300 ns maximum).

5. Setups

5.1 Introduction

The device calibrates and processes signals using a number of algorithms specifically designed to provide for high survivability in the face of adverse environmental challenges. User-defined Setups are employed to alter these algorithms to suit each application. These Setups are loaded into the device over the I^2C serial interfaces.

Note: Setups are volatile and will revert to defaults on power up or reset. I^2C address pointer is initialized to location 0.

Table 5-1. Internal Register Address Allocation

Address	Use	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
0x00	Chip ID	CHIP ID								R
0x01	Firmware Version	MAJOR VERSION				MINOR VERSION				R
0x02	Detection status	CALIBRATE	OVERFLOW	–	–	–	–	–	TOUCH	R
0x03	Key status	Reserved	Key 4	Key 3	Key 2	Reserved	Key 1	Key 0	Reserved	R
0x04 – 0x05	Reserved	Reserved								R
0x06 – 0x07	Key signal 0	Key signal 0 (MSByte) – Key signal 0 (LSByte)								R
0x08 – 0x09	Key signal 1	Key signal 1 (MSByte) – Key signal 1 (LSByte)								R
0x0A – 0x0B	Reserved	Reserved								R
0x0C – 0x0D	Key signal 2	Key signal 2 (MSByte) – Key signal 2 (LSByte)								R
0x0E – 0x0F	Key signal 3	Key signal 3 (MSByte) – Key signal 3 (LSByte)								R
0x10 – 0x11	Key signal 4	Key signal 4 (MSByte) – Key signal 4 (LSByte)								R
0x12 – 0x13	Reserved	Reserved								R
0x14 – 0x15	Reference data 0	Reference data 0 (MSByte) – Reference data 0 (LSByte)								R
0x16 – 0x17	Reference data 1	Reference data 1 (MSByte) – Reference data 1 (LSByte)								R
0x18 – 0x19	Reserved	Reserved								R
0x1A – 0x1B	Reference data 2	Reference data 2 (MSByte) – Reference data 2 (LSByte)								R
0x1C – 0x1D	Reference data 3	Reference data 3 (MSByte) – Reference data 3 (LSByte)								R
0x1E – 0x1F	Reference data 4	Reference data 4 (MSByte) – Reference data 4 (LSByte)								R
0x20	Reserved	Reserved								R
0x21	NTHR key 0	Negative Threshold level for key 0								R/W
0x22	NTHR key 1	Negative Threshold level for key 1								R/W
0x23	Reserved	Reserved								R/W
0x24	NTHR key 2	Negative Threshold level for key 2								R/W
0x25	NTHR key 3	Negative Threshold level for key 3								R/W
0x26	NTHR key 4	Negative Threshold level for key 4								R/W
0x27	Reserved	Reserved								R/W
0x28	Key 0 Pulse Scale	Pulse for Key 0				Scale for Key 0				R/W

Table 5-1. Internal Register Address Allocation

Address	Use	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
0x29	Key 1 Pulse Scale	Pulse for Key 1				Scale for Key 1				R/W
0x2A	Reserved	Reserved								R/W
0x2B	Key 2 Pulse Scale	Pulse for Key 2				Scale for Key 2				R/W
0x2C	Key 3 Pulse Scale	Pulse for Key 3				Scale for Key 3				R/W
0x2D	Key 4 Pulse Scale	Pulse for Key 4				Scale for Key 4				R/W
0x2E	Reserved	Reserved								R/W
0x2F	DI key 0	Detection integrator counter for key 0						AKS for key 0		R/W
0x30	DI key 1	Detection integrator counter for key 1						AKS for key 1		R/W
0x31	Reserved	Reserved								R/W
0x32	DI key 2	Detection integrator counter for key 2						AKS for key 2		R/W
0x33	DI key 3	Detection integrator counter for key 3						AKS for key 3		R/W
0x34	DI key 4	Detection integrator counter for key 4						AKS for key 4		R/W
0x35 – 0x3B	Charge Share Delay	Charge Share Delay								R/W
0x3C	FI / FO / MO / Guard No	FastIn / FastOutDI / Max Cal / Guard Channel								R/W
0x3D	LPM	Low Power (LP) Mode								R/W
0x3E	Max On Duration	Maximum On Duration								R/W
0x3F	RESET / Calibrate	RESET	Calibrate							R/W

5.2 Address 0x00: Chip ID

Table 5-2. Chip ID

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x00	CHIP ID							

CHIP ID: The chip ID. The value stored in this address is always 0x46.

5.3 Address 0x01: Firmware Version

Table 5-3. Firmware Version

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x01	MAJOR VERSION				MINOR VERSION			

MAJOR VERSION: This shows the major version of the firmware represented using 4-bits b0 to b3.

MINOR VERSION: This shows the minor version of the firmware represented using 4-bits b4 to b7.

5.4 Address 0x02: Detection Status

Table 5-4. Detection Status

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x02	CALIBRATE	OVERFLOW	–	–	–	–	–	TOUCH

CALIBRATE: This bit is set during a calibration sequence.

OVERFLOW: This bit is set if the time to acquire all key signals exceeds 8 ms.

TOUCH: This bit is set if any keys are in detect.

5.5 Address 0x03: Key Status

Table 5-5. Key Status

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x03	Reserved	Key 4	Key 3	Key 2	Reserved	Key 1	Key 0	Reserved

KEY0 – 4: bits 1, 2, and 4 to 6 indicate which keys are in detection, if any. Touched keys report as 1, untouched or disabled keys report as 0.

5.6 Address 0x04 – 0x11: Key Signals

Table 5-6. Key Signals

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x04 – 0x05	RESERVED							
0x06	MSByte of KEY SIGNAL for Key 0							
0x07	LSByte of KEY SIGNAL for Key 0							
0x08	MSByte of KEY SIGNAL for Key 1							
0x09	LSByte of KEY SIGNAL for Key 1							
0x0A – 0x0B	RESERVED							
0x0C – 0x11	MSByte/LSByte of KEY SIGNAL for Keys 2 – 4							

KEY SIGNAL: addresses 0x04 – 0x11 allow key signals to be read for each key, starting with key 0. There are two bytes of data for each key. These are the 16-bit key signals which are accessed as two 8-bit bytes, stored MSByte first. These addresses are read-only.

5.7 Address 0x12 – 0x1F: Reference Data

Table 5-7. Reference Data

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x12 – 0x13	RESERVED							
0x14	MSByte of REFERENCE DATA for Key 0							
0x15	LSByte of REFERENCE DATA for Key 0							
0x16	MSByte of REFERENCE DATA for Key 1							
0x17	LSByte of REFERENCE DATA for Key 1							
0x18 – 0x19	RESERVED							
0x1A – 0x1F	MSByte/LSByte of REFERENCE DATA for Keys 2 – 4							

REFERENCE DATA: addresses 0x12 – 0x1F allow reference data to be read for each key, starting with key 0. There are two bytes of data for each key. These are the 16-bit reference data for each key which is accessed as two 8-bit bytes, stored MSByte first. These addresses are read-only.

5.8 Address 0x20 – 0x26: Negative Threshold (NTHR)

Table 5-8. NTHR

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x20	RESERVED							
0x21	NEGATIVE THRESHOLD for Key 0							
0x22	NEGATIVE THRESHOLD for Key 1							
0x23	RESERVED							
0x24 – 0x26	NEGATIVE THRESHOLD for Keys 2 – 4							

NTHR Keys 0 – 4: these 8-bit values set the threshold value for each key to register a detection.

Default: 20 counts

Note: Do not use a setting of 0 as this causes a key to go into detection when its signal is equal to its reference.

5.9 Addresses 0x27 – 0x2D: Pulse/Scale for Keys

Table 5-9. Controls for Keys

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x27	RESERVED							
0x28	PULSE for Key 0				SCALE for Key 0			
0x29	PULSE for Key 1				SCALE for Key 1			
0x2A	RESERVED							
0x2B	PULSE for Key 2				SCALE for Key 2			
0x2C	PULSE for Key 3				SCALE for Key 3			
0x2D	PULSE for Key 4				SCALE for Key 4			

PULSE/SCALE: The PULSE/SCALE settings are used to set up a proximity key. The proximity key is set up by configuring a PULSE/SCALE setting for each key via an I^2C bus.

These bits represent two numbers; the low nibble is SCALE, high nibble is PULSE.

Each acquisition cycle consists signal accumulation and signal averaging. PULSE determines the number of measurements accumulated, SCALE the averaging factor.

The SCALE factor (averaging factor) for the accumulated signal is an exponent of 2.

PULSE is the number of measurements accumulated and is an exponent of 2.

For example:

Oversampling is used to enhance the resolution of the Analog-to-Digital-Converter (ADC). Oversampling theory says that for each additional bit of resolution, n, the signal must be oversampled four times (or $2^2 \times n$.) If two bits of addition resolution are required then the pulse setting would be 4 ($4^2 = 2^4$). If 3-bits of additional resolution are required the Pulse setting would be 6 ($4^3 = 2^6$). Here the result of each ADC pulse measurement is taken and added to the last.

The oversampling theory also states that this accumulated result must be scaled back by a factor of 2^n. This will be the Scale value. The signal value will be scaled to 16-bits in cases where a sufficiently high enough scale factor has not been set.

Table 5-10 shows some of the recommended oversampling settings.

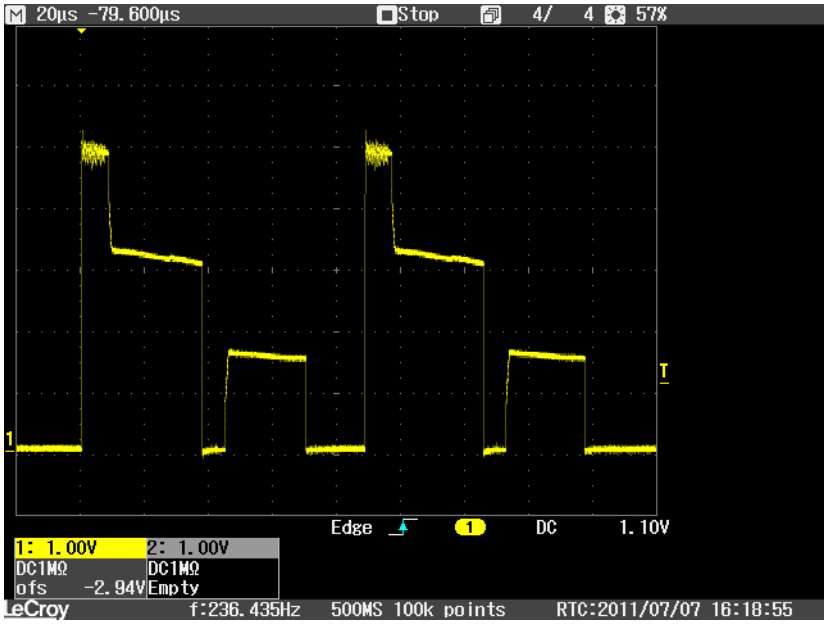
Table 5-10. Oversample for *n* Bits

Sample	Scaling	Bits Gained (*n*)
4^n	2^n	*n*
…	…	…
1	1	0 (Pulse = `0x00` / Scale = `0x00`)
4	2	1 (Pulse = `0x02` / Scale = `0x01`)
16	4	2 (Pulse = `0x04` / Scale = `0x02`)
64	8	3 (Pulse = `0x06` / Scale = `0x03`)
256	16	4 (Pulse = `0x08` / Scale = `0x04`)
1024	32	5 (Pulse = `0x0A` / Scale = `0x05`)
4096	64	6 (Pulse = `0x0C` / Scale = `0x06`)
16384	128	7 (Pulse = `0x0E` / Scale = `0x07`)

Note: Other settings are possible but the Pulse value should never be more than six higher than the Scale setting as the signal result is stored in a 16-bit variable.

Consideration should be taken on the overall effect on timing when setting Pulse values. A single pulse takes approximately 90 µs to complete. As all keys are acquired sequentially a high-bit gain setting will add considerably to the time taken to acquire all channels.

Figure 5-1. Pulse and Scale Settings



Defaults: PULSE0 – PULSE3 = 0

SCALE0 – SCALE3 = 0

5.10 Address `0x2E` – `0x34`: Detection Integrator (DI) / AKS

Table 5-11. Detection Integrator / AKS

Address	b7	b6	b5	b4	b3	b2	b1	b0
`0x2E`	RESERVED							
`0x2F`	DETECTION INTEGRATOR for Key 0						AKS for Key 0	
`0x30`	DETECTION INTEGRATOR for Key 1						AKS for Key 1	
`0x31`	RESERVED							
`0x32` – `0x34`	DETECTION INTEGRATOR for Keys 2 – 4						AKS for Keys 2 – 4	

DETECTION INTEGRATOR: bits 2 to 7 of addresses `0x2E` – `0x34` allow the DI level to be set for each key. This 6-bit value controls the number of consecutive measurements that must be confirmed as having passed the key threshold before that key is registered as being in detect. The minimum value for the DI filter is 2. Settings of 1 for the DI defaults to 2 because a minimum of two consecutive measurements must be confirmed. Setting a DI of 0 disables the corresponding key.

Default: 4

AKS 0 – 4: these bits control which keys are included in an AKS group. There can be up to three groups, each containing any number of keys (up to the maximum allowed for the mode).

Each key can have a value between 0 and 3, which assigns it to an AKS group of that number. A key may only go into detect when no other key in its AKS group is already in detect. A value of 0 means the key is not in any AKS group.

Default: `0x00`

5.11 Address 0x35 – 0x3B: Charge Share Delay

Table 5-12. Charge Share Delay

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x35	RESERVED							
0x36	CSD0							
0x37	CSD1							
0x38	RESERVED							
0x39	CSD2							
0x3A	CSD3							
0x3B	CSD4							

Prolongs the charge-transfer period of signal acquisition by 2.5 µs per count.

Allows full charge-transfer for keys with heavy Rs / Cx loading.

Range: 0 – 255

Default: 0

5.12 Address 0x3C: FastIn / FastOutDI / Max Cal / Guard Channel

Table 5-13. FastIn / FastOutDI / Max Cal / Guard Channel

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x3C	–	FI	FO	MAX CAL	GUARD CHANNEL			

FI: Fast In options – when bit 6 is set then chip will enter fast mode whenever an unfiltered signal value is detected.

FO: Fast Out DI – when bit 5 is set then a key filters out with an integrator of 4. Could have a DI in of 100 but filter out with DI of 4 (global setting for all keys).

MAX CAL: if this bit is clear then all keys recalibrate after a *Max On Duration* timeout, otherwise only the key with the incorrect timing gets recalibrated.

GUARD CHANNEL: bits 0 – 3 are used to set a key as the guard channel (which gets priority filtering). Valid values are 0 – 4, with any larger value disabling the guard key feature.

Default: 0x00

5.13 Address 0x3D: Low Power (LP) Mode

Table 5-14. Low Power Mode

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x3D	LP MODE							

LP MODE: this 8-bit value determines the number of 8 ms intervals between key measurements. Longer intervals between measurements yield a lower power consumption but at the expense of a slower response to touch.

0	Power Down
1	8 ms
2	16 ms
3	24 ms
4	32 ms
n	(n × 8) ms
254	2.032 s
255	2.040 s

Default: 2 (16 ms between key acquisitions)

A setting of 0 for LP mode puts the chip in Power-Down (Deep Sleep) mode.

To wake the device from Power-Down mode, a non-zero LP setting should be written to this address. The QT1050 can also be reset during power-down mode by writing 1 to bit 7 of address 0x3F.

5.14 Address 0x3E: Max On Duration

Table 5-15. Max On Duration

Address	b7	b6	b5	b4	b3	b2	b1	b0
0x3E	MAX ON DURATION							

MAX ON DURATION: this is a 8-bit value which determines how long any key can be in touch before it recalibrates itself.

A value of 0 turns *Max On Duration* off.

0	Off
1	160 ms
2	320 ms
3	480 ms
4	640 ms
n	(n × 160) ms
255	40.8s

Default: 180 (160 ms × 180 = 28.8 s)

5.15 Address `0x3F`: RESET / Calibrate

Table 5-16. RESET / Calibrate

Address	b7	b6	b5	b4	b3	b2	b1	b0
`0x3F`	RESET	CALIBRATE						

RESET: Writing a 1 to bit 7 of this address triggers the device to reset.

CALIBRATE: Writing any non-zero value into the CALIBRATE field triggers the device to start a calibration cycle. The CALIBRATE flag in the detection status register is set when the calibration begins and clears when the calibration has finished.

6. Specifications

6.1 Absolute Maximum Specifications

Parameter	Specification
Vdd	–0.5 to +6 V
Maximum continuous pin current, any control or drive pin	±10 mA
Short circuit duration to ground, any pin	infinite
Short circuit duration to Vdd, any pin	infinite
Voltage forced onto any pin	–0.5 V to (Vdd + 0.5) V
CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.	

6.2 Recommended Operating Conditions

Parameter	Specification
Operating temperature	–40°C to +85°C
Storage temperature	–65°C to +150°C
Vdd	+1.8 V to 5.5 V
Supply ripple+noise	±25 mV
Cx load capacitance per key	1 to 30 pF

6.3 DC Specifications

Vdd = 3.3 V, Cs = 10 nF, load = 5 pF, 32 ms default sleep, Ta(Ambient Temperature)= recommended range, unless otherwise noted

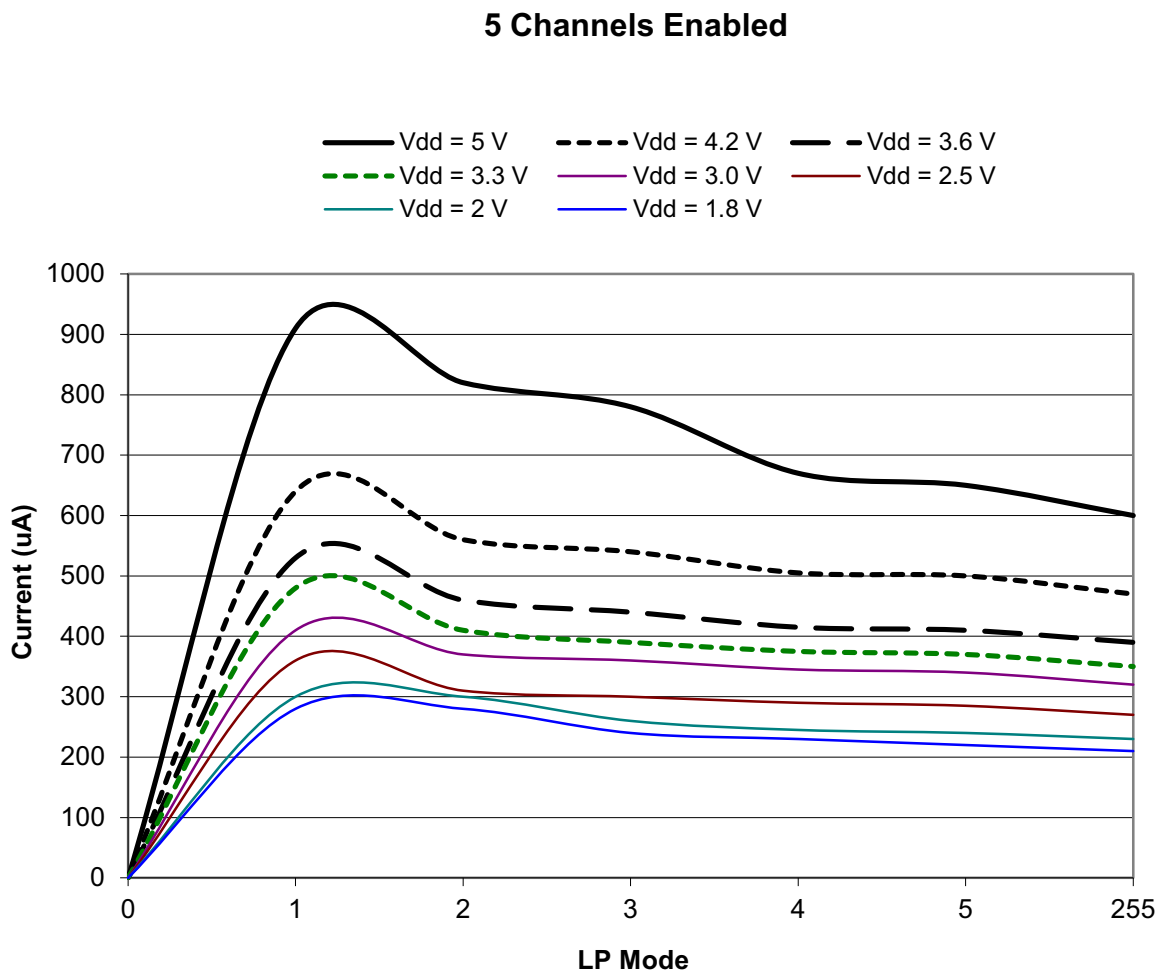
Parameter	Description	Minimum	Typical	Maximum	Units	Notes
Vil	Low input logic level	–0.5	–	0.2 × Vdd	V	
Vih	High input logic level	0.7 × Vdd	–	Vdd + 0.5	V	
Vol	Low output voltage	–	–	0.6	V	
Voh	High output voltage	Vdd – 0.7 V	–	–	V	
Iil	Input leakage current	–	–	±1	µA	

6.4 Power Consumption Measurements

Table 6-1. Supply current (µA) – 5 channels enabled; Pulse = 0 / Scale = 0

LPM	Supply Voltage							
	5	4.2	3.6	3.3	3	2.5	2	1.8
0	<1	<1	<1	<1	<1	<1	<1	<1
1	910	640	530	480	410	360	300	280
2	820	560	460	410	370	310	300	280
3	780	540	440	390	360	300	260	240
4	670	505	415	375	345	290	245	230
5	650	500	410	370	340	285	240	220
255	600	470	390	350	320	270	230	210

Figure 6-1. Power Consumption

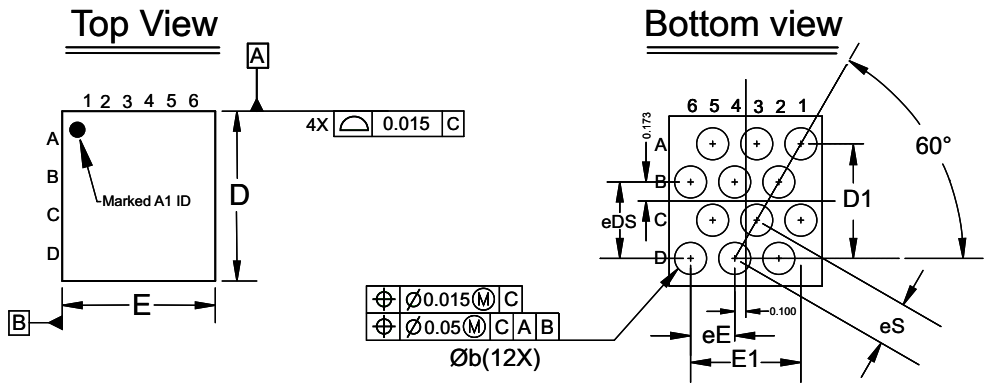


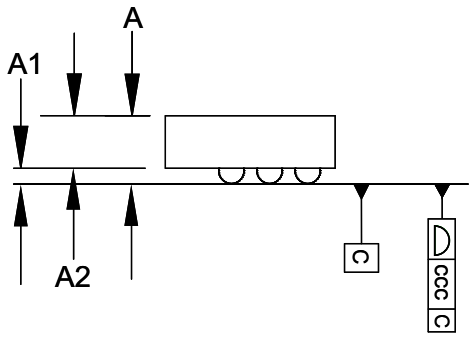
6.5 Timing Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
T_R	Response time	DI setting × 8	–	LP mode + (DI setting × 8)	ms	Under host control
F_{QT}	Sample frequency	162	180	198	kHz	Modulated spread-spectrum (chirp)
T_D	Power-up delay to operate/calibration time	–	<230	–	ms	Can be longer if burst very long
F_{I2C}	I^2C clock rate	–	–	400	kHz	
F_M	Burst modulation percentage	–	±8	–	%	
R_P	$\overline{\text{RESET}}$ pulse width	5	–	–	µs	

6.6 Mechanical Dimensions

6.6.1 AT42QT1050-UU





COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	0.538	
A1	0.164	-	-	
A2	0.280	0.305	0.330	
b	0.239	0.269	0.299	1
D(MAX)	1.555			
D1	1.039 BSC			
E(MAX)	1.403			
E1	1.000 BSC			
eDS	0.693 BSC			
eE	0.400 BSC			
eS	0.400 BSC			
ccc	0.075			2

Note 1: Dimension "b" is measured at the maximum ball dia. in a plane parallel to seating plane.

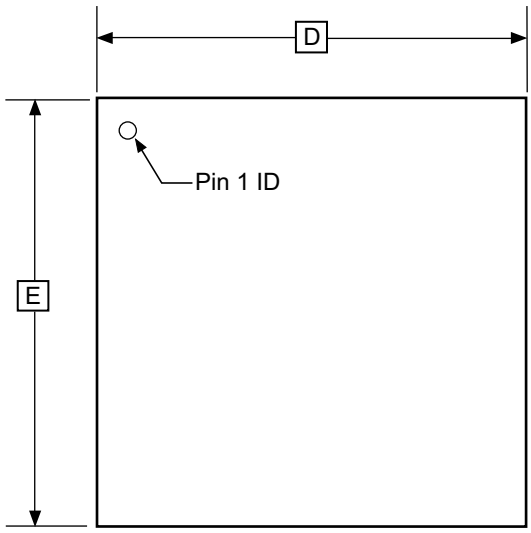
Note 2: "CCC" applied to whole wafer.

Pin Assignment Matrix

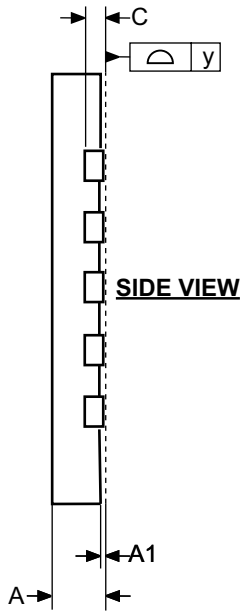
	1	2	3	4	5	6
A	PA4		PA1		PA2	
B		PA6		GND		VDD
C	PA5		PA7		PB1	
D		PB2		PB3		PB0

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **12U-3**, 12-ball 1.555 x 1.403mm Body, 0.538 mm thick, 0.40 mm Pitch (4x6 Staggered Array), WLCSP (354A0)	GPC GGF	DRAWING NO. 12U-3	REV. A

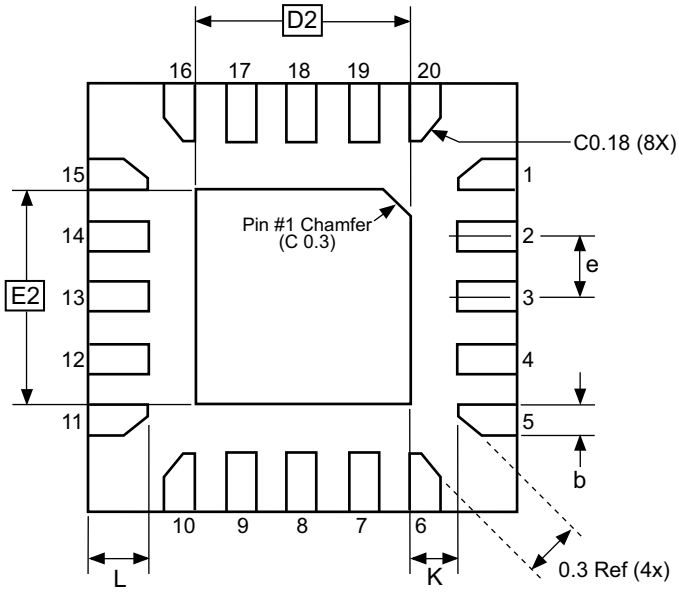
6.6.2 AT42QT1050-MMH



TOP VIEW



SIDE VIEW



BOTTOM VIEW

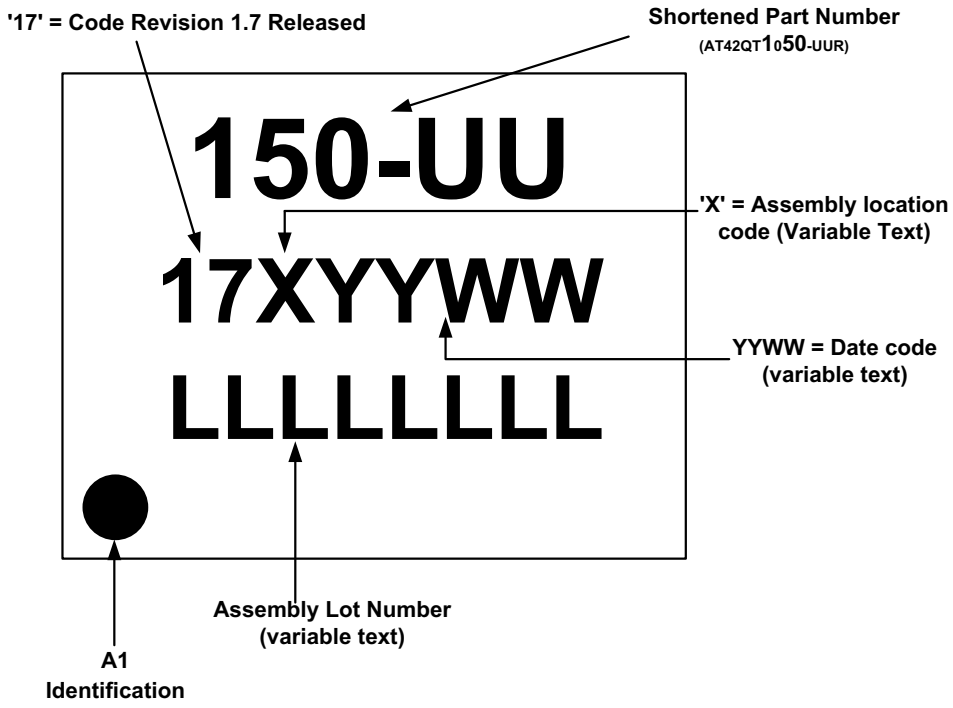
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.75	0.80	0.85	
A1	0.00	0.02	0.05	
b	0.17	0.22	0.27	
C		0.152		
D	2.90	3.00	3.10	
D2	1.40	1.55	1.70	
E	2.90	3.00	3.10	
E2	1.40	1.55	1.70	
e	-	0.45	-	
L	0.35	0.40	0.45	
K	0.20	-	-	
y	0.00	-	0.08	

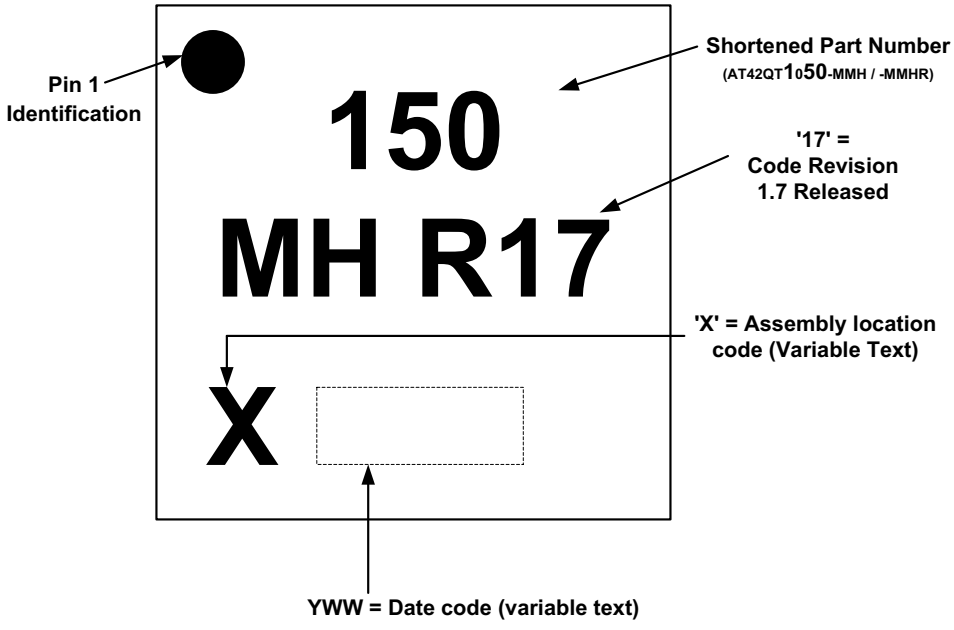
Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **20M2**, 20-pad, 3 x 3 x 0.85 mm Body, Lead Pitch 0.45 mm, 1.55 x 1.55 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	GPC ZFC	DRAWING NO. 20M2	REV. C

6.7 Marking

6.7.1 AT42QT1050 – 12-ball WLCSP



6.7.2 AT42QT1050 – 20-pin VQFN



6.8 Part Number

Part Number	Description
AT42QT1050-UUR	12-ball 1.555x1.403 mm WLCSP RoHS compliant IC - Tape and reel
AT42QT1050-MMH	20-pad 3x3 mm VQFN RoHS compliant IC
AT42QT1050-MMHR	20-pad 3x3 mm VQFN RoHS compliant IC - Tape and reel

The part number comprises:

AT = Atmel

42 = Touch Business Unit

QT = Charge-transfer technology

1050 = (1) Keys only (05) number of channels (0) variant number

UU = WLCSP package

MMH = VQFN package

R = Tape and reel

6.9 Moisture Sensitivity Level (MSL)

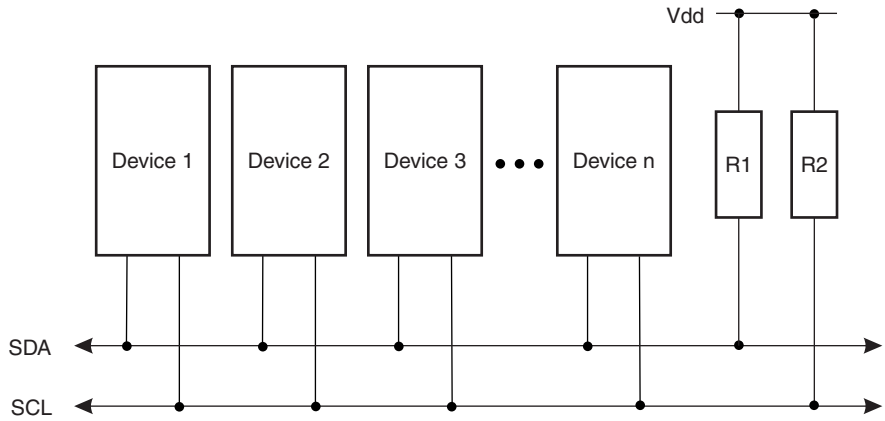
MSL Rating	Peak Body Temperature	Specifications
MSL3	260°C	IPC/JEDEC J-STD-020

Appendix A. I²C Operation

A.1 Interface Bus

The device communicates with the host over an I²C bus. The following sections give an overview of the bus; more detailed information is available from www.i2C-bus.org. Devices are connected to the I²C bus as shown in Figure A-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C devices must be open-drain type. This implements a wired AND function that allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

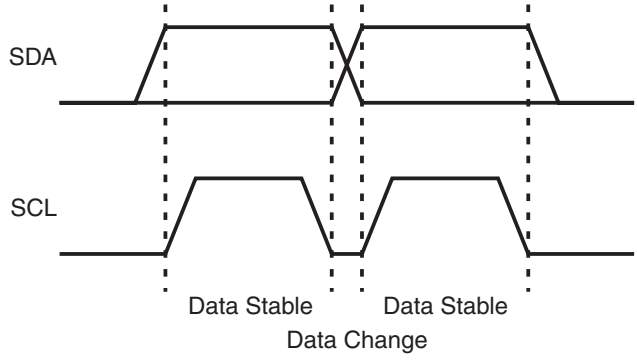
Figure A-1. I²C Interface Bus



A.2 Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; the only exception to this rule is for generating START and STOP conditions.

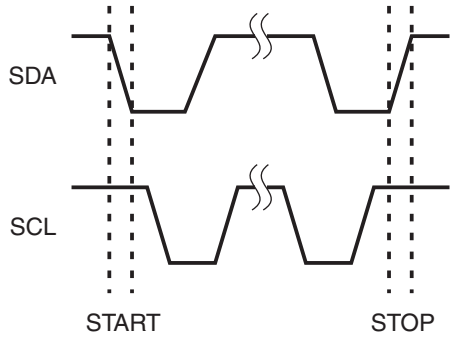
Figure A-2. Data Transfer



A.3 START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between the START and STOP conditions, the bus is considered busy. As shown in Figure A-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure A-3. START and STOP Conditions

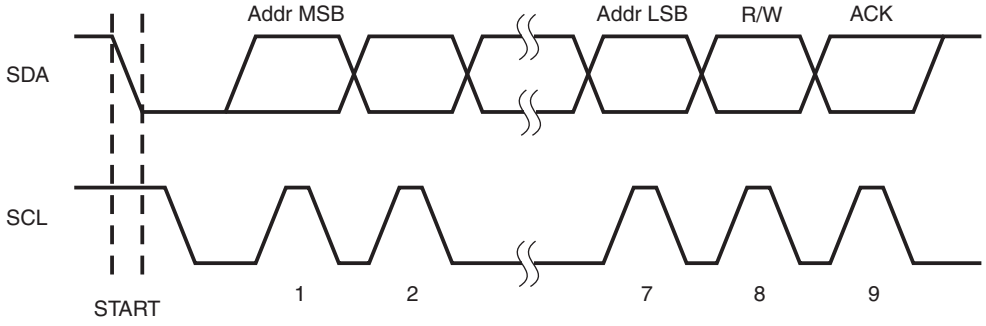


A.4 Address Byte Format

All address bytes are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address byte consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

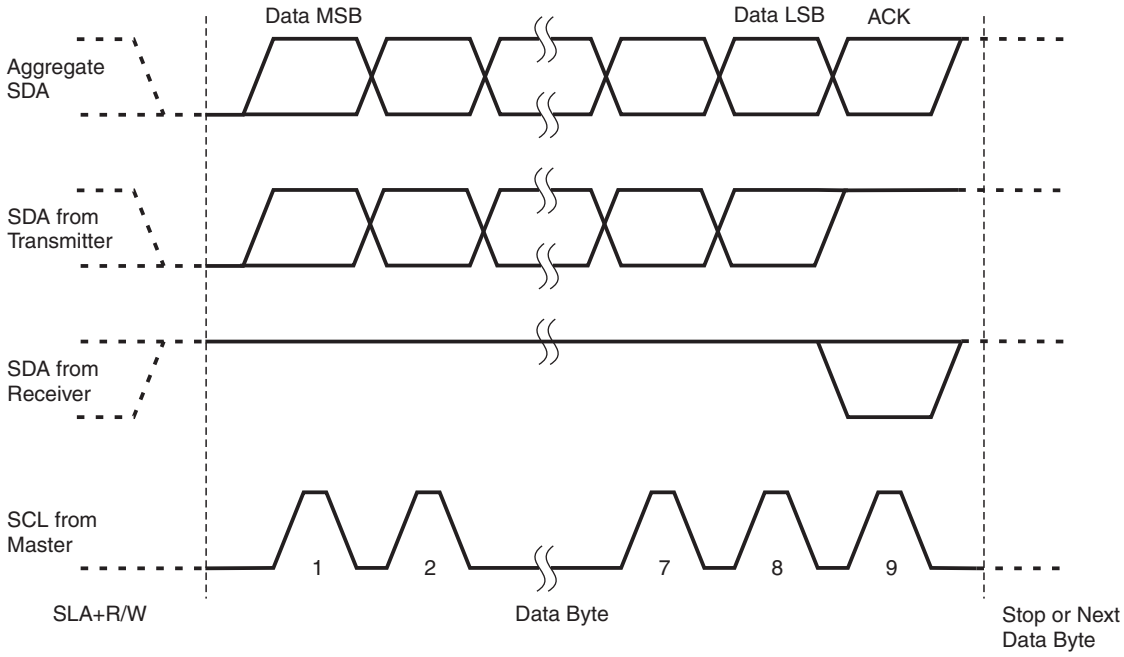
Figure A-4. Address Byte Format



A.5 Data Byte Format

All data bytes are 9 bits long, consisting of 8 data bits and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

Figure A-5. Data Byte Format



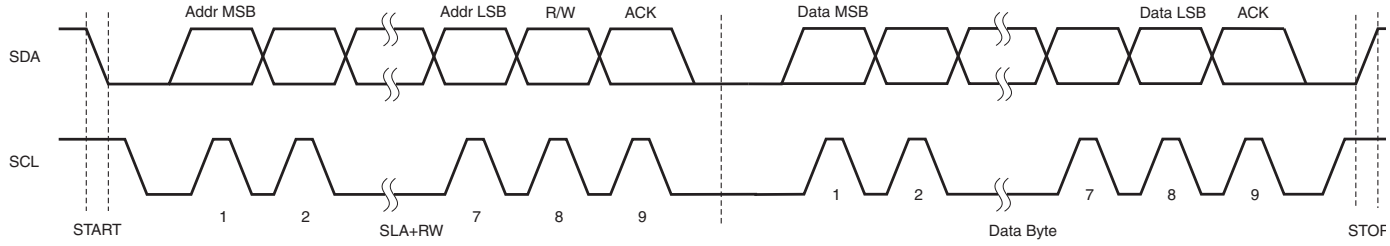
A.6 Combining Address and Data Bytes into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data bytes and a STOP condition. The wired *ANDing* of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Note: Each write or read cycle must end with a stop condition. The device may not respond correctly if a cycle is terminated by a new start condition.

Figure A-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure A-6. Byte Transmission



A.7

Associated Documents

- *QTAN0079 – Buttons, Sliders, and Wheels Sensors Design Guide*
- *QTAN0087 – Proximity Design Guide*
- *Atmel AVR3000: QTouch Conducted Immunity Application Note*

Revision History

Revision Number	History
Revision AX – February 2012	• Preliminary release of document for code revision X.X
Revision BX – February 2012	• Addition of Charge Share Delay field • Changes to RESET field
Revision CX – August 2012	• Addition of selectable I^2C Address • Other minor changes
Revision DX – January 2013	• Added VQFN package
Revision EX – March 2013	• Amended power consumption figures and chart • Added Timing Specification • Added Part Marking drawings
Revision FX- January 2014	• Amended Specifications in Section 6.7.1 and 6.7.2 • Amended information on Chip ID and Firmware versions in Section 5.1, 5.2, and 5.3 • Amended Section 2.11.2 • Removed QS Number from Section 6.8 • Other minor changes

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