

## Computer On Module

- Processor Quad ARM® Cortex®-A9 based NXP i.MX6 Quad, 1GHz
- RAM 1GB DDR3 SDRAM 64-bit
- ROM 128MB SLC NAND Flash
- Power supply Single 3.1V to 5.5V
- Size 31mm SO-DIMM
- Temperature Grade Extended Consumer (-20°C to 105°C Tj)

## Key Features

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- Full HD LCD controller, 24bpp
- OpenGL ES 2.0 and OpenVG 1.1 hardware accelerators
- Multi-format HD 1080p60 video decoder and 1080p30 encoder hardware engine
- Two Camera Interfaces
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - dual, single-precision floating point execute pipeline
- Unified 1MB L2 cache
- Several interfaces:
  - 3x UART, 2x SDIO, 2x SSI/AC97/I2S, I2C, CSPI, Keypad, Ext. Memory I/F
- 3.3V I/O
- IEEE1588 support
- 2x Controller Area Network (FlexCAN)
- PCIe 2.0 (1-lane)

## LVDS Option only:

- Dual LVDS display port
- SATA

## OS Support

- Windows Embedded Compact 7
- Linux
- Android by kernel concepts [www.kernelconcepts.de](http://www.kernelconcepts.de)
- QNX by SITRE [www.sitre.fr](http://www.sitre.fr)



**Quad  
Cortex®-A9**



**Board highlights:**

- Highly integrated
- Standard TX-DIMM pinout
- as small as possible - only 31mm
- 3.3V I/O

The TX6 is a member of the TXCOM module series, specially designed for i.MX multimedia processors. TXCOM modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TXCOM modules includes an i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX6 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

**Computer on module**

- NXP i.MX6 Quad, 1 GHz
- 1GByte SDRAM (64bit) DDR3-1066
- 128 MByte SLC NAND Flash memory
- DIMM200-module (67,6mm x 31 mm x 4mm)
- Operating temperature ranges (Processor junction temperature)  
Extended Consumer Grade: -20°C ..105°C  
Industrial Grade: -40°C ..105°C  
Automotive Grade: -40°C ..125°C, AEC-Q100 Grade 3

**Processor**

The i.MX 6Dual and i.MX 6Quad processors represent NXP Semiconductors' latest achievement in integrated multimedia applications processors. These processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption. The i.MX 6Dual and i.MX 6Quad processors feature NXP's advanced implementation of the quad ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3/LPDDR2-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

**High Performance CPU : Quad ARM® Cortex®-A9**

- Quad ARM® Cortex®-A9, with ARMv7™, Neon, VFPv3 and Trustzone support
- 32K instruction and data L1 caches and 256 KB to 1 MB of L2 cache
- Multi-stream-capable HD video engine delivering 1080p60 decode, 1080p30 encode and 3D video playback in HD in high performance families
- Superior 3D graphics performance with up to quad shaders performing 200 MT/s  
Separate 2D and/or Vertex acceleration engines for an optimal user interface experience
- Stereoscopic image sensor support for 3D imaging

**Standard TXCOM pinout:**

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

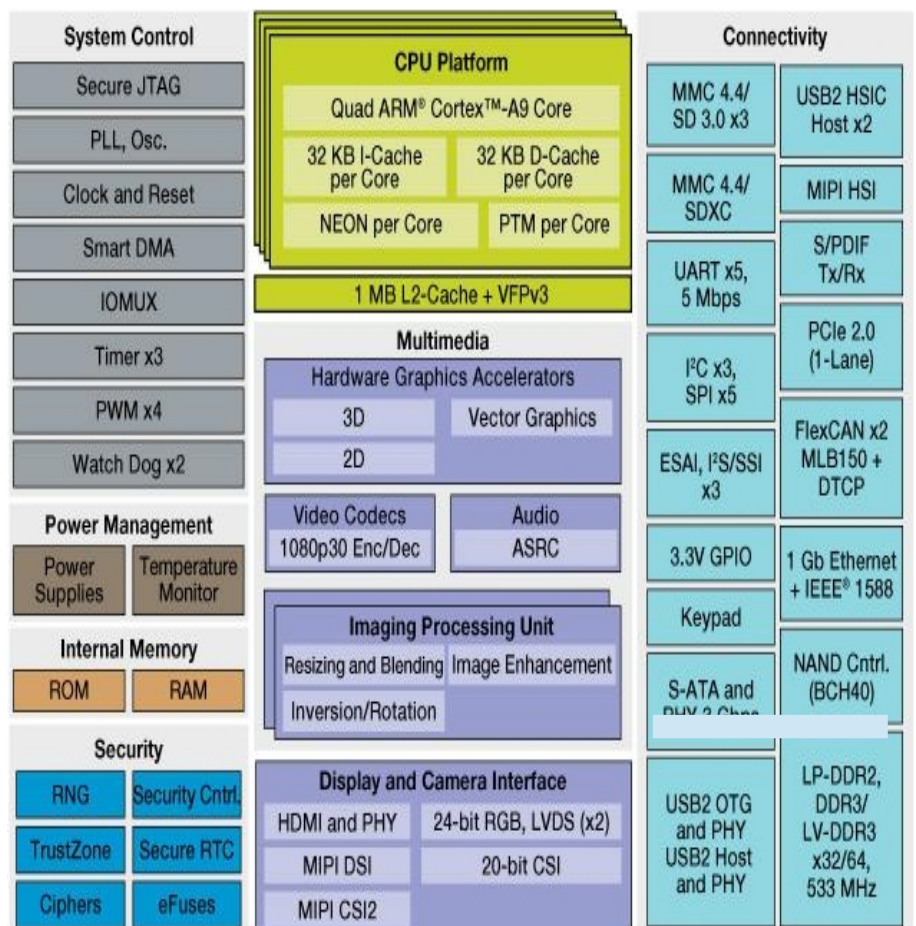
**Power Supply**

The TX6 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (up to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

**Read more in our TX-Guide:**

[www.karo-electronics.com/TX-Guide](http://www.karo-electronics.com/TX-Guide)



| Order Number              | CPU                              | SDRAM | Flash | Temp. Grade       |
|---------------------------|----------------------------------|-------|-------|-------------------|
| TX6Q/1000/1024S/128F      | 1GHz MCIMX6Q5 Quad Core Consumer | 1GB   | 128MB | Extended Consumer |
| TX6Q/1000/1024S/8GF       | 1GHz MCIMX6Q5 Quad Core Consumer | 1GB   | 8GB   | Extended Consumer |
| TX6Q/1000/1024S/128F/MIPI | 1GHz MCIMX6Q5 Quad Core Consumer | 1GB   | 128MB | Extended Consumer |

## PINOUT

| PIN | Type | Function | i.MX6 Quad Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|----------|---------------------|---------------------|------|-------------------------------------------------------|
|-----|------|----------|---------------------|---------------------|------|-------------------------------------------------------|

## POWER SUPPLY &amp; RESET

|           |       |              |                                                      |                                                                                                     |           |                                                                                                                                                                                                                                                                                                                                              |
|-----------|-------|--------------|------------------------------------------------------|-----------------------------------------------------------------------------------------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-4       | power | VIN          |                                                      |                                                                                                     |           | Module power supply input (3.3V-5V, observe DIMM socket contact current rating)                                                                                                                                                                                                                                                              |
| 5-7, 9-12 | power | VOUT         |                                                      |                                                                                                     |           | 3.3V power supply output. Supplied by RN5T567 LDO2 (max. 300mA)                                                                                                                                                                                                                                                                              |
| 8         | 3V3   | BOOTMODE     |                                                      |                                                                                                     | 10K-PU    | Boot mode select H: Boot from NAND / L: Boot from UART/USB                                                                                                                                                                                                                                                                                   |
| 13        | power | VBACKUP      | Version with DS1339 RTC                              |                                                                                                     |           |                                                                                                                                                                                                                                                                                                                                              |
|           |       |              |                                                      |                                                                                                     |           | DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.                              |
|           |       |              | Version without DS1339 RTC                           |                                                                                                     |           |                                                                                                                                                                                                                                                                                                                                              |
|           |       |              | Connected through a 240 Ohms resistor to VDD_SNVS_IN |                                                                                                     |           | i.MX6 SNVS backup power supply. Supply voltage must be held between 2.9V and 3.3V if the system requires keeping real time and other data on OFF state. This pin is connected to RN5T567 LDORTC1 (3V/30mA) through an onboard 240R resistor. Leave unconnected if the system does not require keeping real time and other data on OFF state. |
| 14        | VIN   | PMIC_PWR_BTN |                                                      |                                                                                                     |           | Connected to RN5T567 PWRON, 10K-PU connected to VIN. Leave unconnected, if not used.                                                                                                                                                                                                                                                         |
| 15        | 3V3   | #RESET_OUT   | GPIO_17                                              | ESAI1_TX0<br>ENET_1588_EVENT3_IN<br>CCM_PMIC_RDY<br>SDMA_EXT_EVENT[0]<br>SPDIF_OUT1<br>SJC_JTAG_ACT | GPIO7[12] | #RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.                                                                                                                                                                                                           |
| 16        |       | #POR         | POR_B                                                |                                                                                                     | 10K-PU    | Power On Reset — Active low input signal. Leave unconnected, if not used.                                                                                                                                                                                                                                                                    |
| 17        |       | #RESET_IN    | POR_B                                                |                                                                                                     |           | Wire or'ed to pin 16                                                                                                                                                                                                                                                                                                                         |
| 18        | GND   | GND          |                                                      |                                                                                                     |           |                                                                                                                                                                                                                                                                                                                                              |

## Ethernet

|    |        |           |  |  |  |                                                                                                                                                                  |
|----|--------|-----------|--|--|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19 | analog | ETN_TXN   |  |  |  | Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.                                                                        |
| 20 | 3V3    | #ETN_LED2 |  |  |  | Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation. |
| 21 | analog | ETN_TXP   |  |  |  | Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.                                                                        |
| 22 | power  | ETN_3V3   |  |  |  | +3.3V analog power supply output to magnetics                                                                                                                    |
| 23 | analog | ETN_RXN   |  |  |  | Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.                                                                         |
| 24 | 3V3    | #ETN_LED1 |  |  |  | Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.                                                   |
| 25 | analog | ETN_RXP   |  |  |  | Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.                                                                         |
| 26 | GND    | GND       |  |  |  |                                                                                                                                                                  |

## USB-HOST

|    |        |             |             |                                                                                                                            |                     |                                                                                                   |
|----|--------|-------------|-------------|----------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------------------------------------------------------------------------------------|
| 27 | 3V3    | USBH_VBUSEN | EIM_D31     | WEIM_D[31]<br>IPU1_DISP1_DAT[20]<br>IPU1_DIO_PIN12<br>IPU1_CSI0_D[2]<br>UART3_RTS<br>USBOH3_USBH1_PWR<br>MX6Q_PER_HPROT[1] | GPIO3[31]           | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply. |
| 28 | 3V3    | #USBH_OC    | EIM_D30     | WEIM_D[30]<br>IPU1_DISP1_DAT[21]<br>IPU1_DIO_PIN11<br>IPU1_CSI0_D[3]<br>UART3_CTS<br>USBOH3_USBH1_OC<br>MX6Q_PER1_HPROT[0] | GPIO3[30]<br>10K-PU | Active low over-current indicator input connected to a GPIO.                                      |
| 29 | analog | USBH_DM     | USB_H1_DN   |                                                                                                                            |                     | D- pin of the USB cable                                                                           |
| 30 | analog | USBH_VBUS   | USB_H1_VBUS |                                                                                                                            |                     | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.                       |
| 31 | analog | USBH_DP     | USB_H1_DP   |                                                                                                                            |                     | D+ pin of the USB cable                                                                           |
| 32 | GND    | GND         |             |                                                                                                                            |                     |                                                                                                   |



| PIN                                                    | Type   | Function                | i.MX6 Quad Pad Name | Alternate functions                                                                                                      | GPIO               | Description (refer to i.MX6 Dual manuals for details)                                                                                         |
|--------------------------------------------------------|--------|-------------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| <b>USB-OTG / 2<sup>nd</sup> CAN</b>                    |        |                         |                     |                                                                                                                          |                    |                                                                                                                                               |
| 33                                                     | 3V3    | USBOTG_ID               | EIM_D23             | WEIM_D[23]<br>DI0_D0_CS<br>UART3_CTS<br>UART1_DCD<br>IPU2_CSI1_DATA_EN<br>IPU1_DI1_PIN2<br>IPU1_DI1_PIN14                | GPIO3[23]          |                                                                                                                                               |
| 34                                                     | 3V3    | USBOTG_VBUSEN<br>CAN_TX | GPIO_7              | ESAI1_TX4_RX1<br>ECSP15_RDY<br>EPIT1_EPITO<br>CAN1_TXCAN<br>UART2_TXD_MUX<br>SPDIF_PLOCK<br>OTGUSB_HOST_MODE             | GPIO1[7]           | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.                                             |
| 35                                                     | analog | USBOTG_DM               | USB_OTG_DN          |                                                                                                                          |                    | D- pin of the USB cable                                                                                                                       |
| 36                                                     | 3V3    | #USBOTG_OC<br>CAN_RX    | GPIO_8              | ESAI1_TX5_RX0<br>EPIT2_EPITO<br>CAN1_RXCAN<br>UART2_RXD_MUX<br>SPDIF_SRCLK<br>USB_PWRCTL_WAKEUP                          | GPIO1[8]<br>10K-PU | Active low over-current indicator input connected to a GPIO.                                                                                  |
| 37                                                     | analog | USBOTG_DP               | USB_OTG_DP          |                                                                                                                          |                    | D+ pin of the USB cable                                                                                                                       |
| 38                                                     | analog | USBOTG_VBUS             | USB_OTG_VBUS        |                                                                                                                          |                    | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.                                                                   |
| 39                                                     | GND    | GND                     |                     |                                                                                                                          |                    |                                                                                                                                               |
| <b>I2C</b>                                             |        |                         |                     |                                                                                                                          |                    |                                                                                                                                               |
| 40                                                     | 3V3    | I2C_DATA                | GPIO_6              | ESAI1_SCKT<br>OBSRV_INT_OUT1<br><b>I2C3_SDA</b><br>CCM_CCM_OUT_0<br>CSU_CSU_INT_DEB<br>USDHC2_LCTL<br>MLB_MLB SIG        | GPIO1[6]           | I2C Data                                                                                                                                      |
| 41                                                     | 3V3    | I2C_CLK                 | GPIO_3              | ESAI1_HCKR<br>OBSRV_INT_OUT0<br><b>I2C3_SCL</b><br>CCM_CLK02<br>USBOH3_USBH1_OC<br>MLB_MLBCLK                            | GPIO1[3]           | I2C Clock                                                                                                                                     |
| <b>PWM</b>                                             |        |                         |                     |                                                                                                                          |                    |                                                                                                                                               |
| 42                                                     | 3V3    | PWM                     | GPIO_1              | ESAI1_SCKR<br>WDOG2_WDOG_B<br>KPP_ROW[5]<br><b>PWM2_PWM0</b><br>USDHC1_CD<br>SRC_TESTER_ACK                              | GPIO1[1]           | PWM Output                                                                                                                                    |
| <b>1-WIRE</b>                                          |        |                         |                     |                                                                                                                          |                    |                                                                                                                                               |
| 43                                                     | 3V3    | OWDAT                   | GPIO_18             | ESAI1_TX1<br>ENET_RX_CLK<br>USDHC3_VSELECT<br>SDMA_EXT_EVENT[1]<br>ASRC_ASRC_EXT_CLK<br>SNVS_VIO_5_CTL<br>SRC_SYSTEM_RST | GPIO7[13]          | 1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system. |
| <b>CSPI – Configurable Serial Peripheral Interface</b> |        |                         |                     |                                                                                                                          |                    |                                                                                                                                               |
| 44                                                     | 3V3    | CSPI_SS                 | EIM_EB2             | WEIM_EB[2]<br><b>ECSP11_SS0</b><br>CCM_DI1_EXT_CLK<br>IPU2_CSI1_D[19]<br>HDMI_TX_DDC_SCL<br>I2C2_SCL<br>SRC_BT_CFG[30]   | GPIO2[30]          | Slave Select (Selectable polarity) signal                                                                                                     |
| 45                                                     | 3V3    | CSPI_SS                 | EIM_D19             | WEIM_D[19]<br><b>ECSP11_SS1</b><br>IPU1_DI0_PIN8<br>IPU2_CSI1_D[16]<br>UART1_CTS<br>EPIT1_EPITO<br>MX6Q_PER_HRESP        | GPIO3[19]          | Slave Select (Selectable polarity) signal                                                                                                     |

| PIN | Type | Function  | i.MX6 Quad Pad Name | Alternate functions                                                                                                       | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|-----------|---------------------|---------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 46  | 3V3  | CSPI_MOSI | EIM_D18             | WEIM_D[18]<br><b>ECSPI1_MOSI</b><br>IPU1_DIO_PIN7<br>IPU2_CSI1_D[17]<br>IPU1_DI1_D0_CS<br>I2C3_SDA<br>MX6Q_PER_HBURST[2]  | GPIO3[18] | Master Out/Slave In signal                            |
| 47  | 3V3  | CSPI_MISO | EIM_D17             | WEIM_D[17]<br><b>ECSPI1_MISO</b><br>IPU1_DIO_PIN6<br>IPU2_CSI1_PIXCLK<br>DCIC1_DCIC_OUT<br>I2C3_SCL<br>MX6Q_PER_HBURST[1] | GPIO3[17] | Master In/Slave Out signal                            |
| 48  | 3V3  | CSPI_SCLK | EIM_D16             | WEIM_D[16]<br><b>ECSPI1_SCLK</b><br>IPU1_DIO_PIN5<br>IPU2_CSI1_D[18]<br>HDMI_TX_DDC_SDA<br>I2C2_SDA                       | GPIO3[16] | Serial Clock signal                                   |
| 49  | 3V3  | CSPI_RDY  | GPIO_19             | KPP_COL[5]<br>ENET_1588_EVENT0<br>SPDIF_OUT1<br>CCM_CLKO<br><b>ECSPI1_RDY</b><br>ENET_TX_ER<br>SRC_INT_BOOT               | GPIO4[5]  | Serial Data Ready signal                              |
| 50  | GND  | GND       |                     |                                                                                                                           |           |                                                       |

## SD – Secure Digital Interface 1

|    |     |          |          |                                                                                                                                               |                 |                                                                                                                                                                                               |
|----|-----|----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 51 | 3V3 | SD1_CD   | SD3_CMD  | USDHC3_CMD<br>UART2_CTS<br>CAN1_TXCAN<br>USBOH3_UH3_<br>DFD_OUT[4]<br>USBOH3_UH2_<br>DFD_OUT[4]<br>MIPI_CORE_DPHY_<br>TEST_IN[16]             | <b>GPIO7[2]</b> | SD Card Detect – connected to a GPIO                                                                                                                                                          |
| 52 | 3V3 | SD1_D[0] | SD1_DAT0 | <b>USDHC1_DAT0</b><br>ECSPI5_MISO<br>CAAM_WRAPPER_<br>RNG_OSC_OBS<br>GPT_CAPIN1<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[8]<br>HDMI_TX_OPHYDTB[1] | GPIO1[16]       | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added. |
| 53 | 3V3 | SD1_D[1] | SD1_DAT1 | <b>USDHC1_DAT1</b><br>ECSPI5_SS0<br>PWM3_PWM0<br>GPT_CAPIN2<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[7]<br>HDMI_TX_OPHYDTB[0]                     | GPIO1[17]       |                                                                                                                                                                                               |
| 54 | 3V3 | SD1_D[2] | SD1_DAT2 | <b>USDHC1_DAT2</b><br>ECSPI5_SS1<br>GPT_CMPOUT2<br>PWM2_PWM0<br>WDOG1_WDOG_B<br>WDOG1_WDOG_<br>RST_B_DEB                                      | GPIO1[19]       |                                                                                                                                                                                               |
| 55 | 3V3 | SD1_D[3] | SD1_DAT3 | <b>USDHC1_DAT3</b><br>ECSPI5_SS2<br>GPT_CMPOUT3<br>PWM1_PWM0<br>WDOG2_WDOG_B<br>WDOG2_WDOG_<br>RST_B_DEB                                      | GPIO1[21]       |                                                                                                                                                                                               |
| 56 | 3V3 | SD1_CMD  | SD1_CMD  | <b>USDHC1_CMD</b><br>ECSPI5_MOSI<br>PWM4_PWM0<br>GPT_CMPOUT1                                                                                  | GPIO1[18]       | SD Command bidirectional signal                                                                                                                                                               |
| 57 | 3V3 | SD1_CLK  | SD1_CLK  | <b>USDHC1_CLK</b><br>ECSPI5_SCLK<br>OSC32K_32K_OUT<br>GPT_CLKIN<br>PHY_DTB[0]<br>SATA_PHY_DTB[0]                                              | GPIO1[20]       | SD Output Clock.                                                                                                                                                                              |
| 58 | GND | GND      |          |                                                                                                                                               |                 |                                                                                                                                                                                               |

| PIN                        | Type | Function | i.MX6 Quad Pad Name | Alternate functions                                                                                                                                                      | GPIO      | Description (refer to i.MX6 Dual manuals for details)  |
|----------------------------|------|----------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------------------------------------------|
| <b>1<sup>st</sup> UART</b> |      |          |                     |                                                                                                                                                                          |           |                                                        |
| 59                         | 3V3  | TXD      | SD3_DAT7            | USDHC3_DAT7<br><b>UART1_TXD_MUX</b><br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[24]<br>USBOH3_UH3_<br>DFD_OUT[0]<br>USBOH3_UH2_<br>DFD_OUT[0]<br>MIPI_CORE_<br>DPHY_TEST_IN[12] | GPIO6[17] | Application UART 1 Transmit Data output signal         |
| 60                         | 3V3  | RXD      | SD3_DAT6            | USDHC3_DAT6<br><b>UART1_RXD_MUX</b><br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[25]<br>USBOH3_UH3_<br>DFD_OUT[1]<br>USBOH3_UH2_<br>DFD_OUT[1]<br>MIPI_CORE_<br>DPHY_TEST_IN[13] | GPIO6[18] | Application UART 1 Receive Data input signal           |
| 61                         | 3V3  | RTS      | SD3_DAT1            | USDHC3_DAT1<br><b>UART1_RTS</b><br>CAN2_RXCAN<br>USBOH3_UH3_<br>DFD_OUT[7]<br>USBOH3_UH2_<br>DFD_OUT[7]<br>MIPI_CORE_<br>DPHY_TEST_IN[19]                                | GPIO7[5]  | Application UART 1 Request to Send <b>input</b> signal |
| 62                         | 3V3  | CTS      | SD3_DAT0            | USDHC3_DAT0<br><b>UART1_CTS</b><br>CAN2_TXCAN<br>USBOH3_UH3_<br>DFD_OUT[6]<br>USBOH3_UH2_<br>DFD_OUT[6]<br>MIPI_CORE_<br>DPHY_TEST_IN[18]                                | GPIO7[4]  | Application UART 1 Clear to Send <b>output</b> signal  |
| <b>2<sup>nd</sup> UART</b> |      |          |                     |                                                                                                                                                                          |           |                                                        |
| 63                         | 3V3  | TXD      | SD4_DAT7            | RAWNAND_D15<br>USDHC4_DAT7<br><b>UART2_TXD_MUX</b><br>USBOH3_UH2_<br>DFD_OUT[31]<br>USBOH3_UH3_<br>DFD_OUT[31]<br>IPU1_IPU_DIAG_BUS[15]<br>IPU2_IPU_DIAG_BUS[15]         | GPIO2[15] | Application UART 2 Transmit Data output signal         |
| 64                         | 3V3  | RXD      | SD4_DAT4            | RAWNAND_D12<br>USDHC4_DAT4<br><b>UART2_RXD_MUX</b><br>USBOH3_UH2_<br>DFD_OUT[28]<br>USBOH3_UH3_<br>DFD_OUT[28]<br>IPU1_IPU_DIAG_BUS[12]<br>IPU2_IPU_DIAG_BUS[12]         | GPIO2[12] | Application UART 2 Receive Data input signal           |
| 65                         | 3V3  | RTS      | SD4_DAT5            | RAWNAND_D13<br>USDHC4_DAT5<br><b>UART2_RTS</b><br>USBOH3_UH2_<br>DFD_OUT[29]<br>USBOH3_UH3_<br>DFD_OUT[29]<br>IPU1_IPU_DIAG_BUS[13]<br>IPU2_IPU_DIAG_BUS[13]             | GPIO2[13] | Application UART 2 Request to Send <b>input</b> signal |
| 66                         | 3V3  | CTS      | SD4_DAT6            | RAWNAND_D14<br>USDHC4_DAT6<br><b>UART2_CTS</b><br>USBOH3_UH2_<br>DFD_OUT[30]<br>USBOH3_UH3_<br>DFD_OUT[30]<br>IPU1_IPU_DIAG_BUS[14]<br>IPU2_IPU_DIAG_BUS[14]             | GPIO2[14] | Application UART 2 Clear to Send <b>output</b> signal  |

| PIN                                | Type | Function  | i.MX6 Quad Pad Name | Alternate functions                                                                                                                                                   | GPIO      | Description (refer to i.MX6 Dual manuals for details)  |
|------------------------------------|------|-----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------------------------------------------|
| <b>3<sup>rd</sup> UART</b>         |      |           |                     |                                                                                                                                                                       |           |                                                        |
| 67                                 | 3V3  | TXD       | EIM_D24             | WEIM_D[24]<br>ECSP14_SS2<br><b>UART3_TXD_MUX</b><br>ECSP11_SS2<br>ECSP12_SS2<br>AUDMUX_AUD5_RXFS<br>UART1_DTR                                                         | GPIO3[24] | Application UART 3 Transmit Data output signal         |
| 68                                 | 3V3  | RXD       | EIM_D25             | WEIM_D[25]<br>ECSP14_SS3<br><b>UART3_RXD_MUX</b><br>ECSP11_SS3<br>ECSP12_SS3<br>AUDMUX_AUD5_RXC<br>UART1_DSR                                                          | GPIO3[25] | Application UART 3 Receive Data input signal           |
| 69                                 | 3V3  | RTS       | SD3_RST             | USDHC3_RST<br><b>UART3_RTS</b><br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[30]<br>USBOH3_UH3_<br>DFD_OUT[10]<br>USBOH3_UH2_<br>DFD_OUT[10]<br>MIPI_CORE_<br>DPHY_TEST_IN[22] | GPIO7[8]  | Application UART 3 Request to Send <b>input</b> signal |
| 70                                 | 3V3  | CTS       | SD3_DAT3            | USDHC3_DAT3<br><b>UART3_CTS</b><br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[29]<br>USBOH3_UH3_<br>DFD_OUT[9]<br>USBOH3_UH2_<br>DFD_OUT[9]<br>MIPI_CORE_<br>DPHY_TEST_IN[21]  | GPIO7[7]  | Application UART 3 Clear to Send <b>output</b> signal  |
| 71                                 | GND  | GND       |                     |                                                                                                                                                                       |           |                                                        |
| <b>KEYPAD / 1<sup>st</sup> CAN</b> |      |           |                     |                                                                                                                                                                       |           |                                                        |
| 72                                 | 3V3  | KP_COL[0] | GPIO_9              | ESAI1_FSR<br>WDOG1_WDOG_B<br><b>KPP_COL[6]</b><br>CCM_REF_EN_B<br>PWM1_PWMO<br>USDHC1_WP<br>SRC_EARLY_RST                                                             | GPIO1[9]  |                                                        |
| 73                                 | 3V3  | KP_COL[1] | GPIO_4              | ESAI1_HCKT<br>OBSRV_INT_OUT3<br><b>KPP_COL[7]</b><br>CCM_CCM_OUT_2<br>CSU_ALARM_AUT[1]<br>USDHC2_CD<br>OCOTP_CTRL_WRAPPER<br>_FUSE_LATCHED                            | GPIO1[4]  |                                                        |
| 74                                 | 3V3  | KP_COL[2] | KEY_COL2            | ECSP11_SS1<br>ENET_RDATA[2]<br>CAN1_TXCAN<br><b>KPP_COL[2]</b><br>ENET_MDC<br>USBOH3_H1USB_<br>PWRCTL_WAKEUP<br>MX6Q_PER1_HADDR[3]                                    | GPIO4[10] |                                                        |
| 75                                 | 3V3  | KP_COL[3] | KEY_COL3            | ECSP11_SS3<br>ENET_CRS<br>HDMI_TX_DDC_SCL<br><b>KPP_COL[3]</b><br>I2C2_SCL<br>SPDIF_IN1<br>MX6Q_PER1_HADDR[5]                                                         | GPIO4[12] |                                                        |
| 76                                 | 3V3  | TXCAN     | KEY_COL4            | <b>CAN2_TXCAN</b><br>IPU1_SIGS[4]<br>USBOH3_USBOTG_OC<br>KPP_COL[4]<br>UART5_RTS<br>MMD5_DEBUG[49]<br>MX6Q_PER1_HADDR[7]                                              | GPIO4[14] |                                                        |

| PIN | Type | Function  | i.MX6 Quad Pad Name | Alternate functions                                                                                                             | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|-----------|---------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 77  | 3V3  | KP_ROW[0] | GPIO_2              | ESAI1_FST<br>OBSRV_INT_OUT2<br>KPP_ROW[6]<br>CCM_CCM_OUT_1<br>CSU_ALARM_AUT[0]<br>USDHC2_WP<br>MLB_MLBDAT                       | GPIO1[2]  |                                                       |
| 78  | 3V3  | KP_ROW[1] | GPIO_5              | ESAI1_TX2_RX3<br>OBSRV_INT_OUT4<br><b>KPP_ROW[7]</b><br>CCM_CLKO<br>CSU_ALARM_AUT[2]<br>I2C3_SCL<br>MPCORE_EVENTI               | GPIO1[5]  |                                                       |
| 79  | 3V3  | KP_ROW[2] | KEY_ROW2            | ECSP11_SS2<br>ENET_TDATA[2]<br>CAN1_RXCAN<br><b>KPP_ROW[2]</b><br>USDHC2_VSELECT<br>HDMI_TX_CEC_LINE<br>MX6Q_PER1_HADDR[4]      | GPIO4[11] |                                                       |
| 80  | 3V3  | KP_ROW[3] | KEY_ROW3            | OSC32K_32K_OUT<br>ASRC_ASRC_EXT_CLK<br>HDMI_TX_DDC_SDA<br><b>KPP_ROW[3]</b><br>I2C2_SDA<br>USDHC1_VSELECT<br>MX6Q_PER1_HADDR[6] | GPIO4[13] |                                                       |
| 81  | 3V3  | RXCAN     | KEY_ROW4            | <b>CAN2_RXCAN</b><br>IPU1_SISG[5]<br>USBOH3_USBOTG_PWR<br>KPP_ROW[4]<br>UART5_CTS<br>MMDC_DEBUG[50]<br>MX6Q_PER1_HADDR[8]       | GPIO4[15] |                                                       |
| 82  | GND  | GND       |                     |                                                                                                                                 |           |                                                       |

### SSI 1 - Serial Audio Port 1

|    |     |          |          |                                                                                                                               |                  |                                           |
|----|-----|----------|----------|-------------------------------------------------------------------------------------------------------------------------------|------------------|-------------------------------------------|
| 83 | 3V3 | SSI1_INT | EIM_D26  | WEIM_D[26]<br>IPU1_DI1_PIN11<br>IPU1_CSI0_D[1]<br>IPU2_CSI1_D[14]<br>UART2_TXD_MUX<br>IPU1_SISG[2]<br>IPU1_DISP1_DAT[22]      | <b>GPIO3[26]</b> | GPIO                                      |
| 84 | 3V3 | SSI1_RXD | KEY_ROW1 | ECSP11_SS0<br>ENET_COL<br><b>AUDMUX_AUD5_RXD</b><br>KPP_ROW[1]<br>UART5_RXD_MUX<br>USDHC2_VSELECT<br>MX6Q_PER1_HADDR[2]       | GPIO4[9]         | Serial Audio Interface serial data line 1 |
| 85 | 3V3 | SSI1_TXD | KEY_ROW0 | ECSP11_MOSI<br>ENET_TDATA[3]<br><b>AUDMUX_AUD5_TXD</b><br>KPP_ROW[0]<br>UART4_RXD_MUX<br>DCIC2_DCIC_OUT<br>MX6Q_PER1_HADDR[0] | GPIO4[7]         | Serial Audio Interface serial data line 0 |
| 86 | 3V3 | SSI1_CLK | KEY_COL0 | ECSP11_SCLK<br>ENET_RDATA[3]<br><b>AUDMUX_AUD5_TXC</b><br>KPP_COL[0]<br>UART4_TXD_MUX<br>DCIC1_DCIC_OUT<br>SRC_ANY_PU_RST     | GPIO4[6]         | Serial Audio Interface serial bit clock   |
| 87 | 3V3 | SSI1_FS  | KEY_COL1 | ECSP11_MISO<br>ENET_MDIO<br><b>AUDMUX_AUD5_TXFS</b><br>KPP_COL[1]<br>UART5_TXD_MUX<br>USDHC1_VSELECT<br>MX6Q_PER1_HADDR[1]    | GPIO4[8]         | Serial Audio Interface left/right clock   |
| 88 | GND | GND      |          |                                                                                                                               |                  |                                           |



| PIN                                | Type | Function | i.MX6 Quad Pad Name | Alternate functions                                                                                                               | GPIO      | Description (refer to i.MX6 Dual manuals for details)                                                                                                                                         |
|------------------------------------|------|----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>SSI 2 - Serial Audio Port 2</b> |      |          |                     |                                                                                                                                   |           |                                                                                                                                                                                               |
| 89                                 | 3V3  | SSI2_INT | EIM_D27             | WEIM_D[27]<br>IPU1_DI1_PIN13<br>IPU1_CSI0_D[0]<br>IPU2_CSI1_D[13]<br>UART2_RXD_MUX<br>IPU1_SISG[3]<br>IPU1_DISP1_DAT[23]          | GPIO3[27] | GPIO                                                                                                                                                                                          |
| 90                                 | 3V3  | SSI2_RXD | CSI0_DAT7           | IPU1_CSI0_D[7]<br>WEIM_D[5]<br>ECSPI1_SS0<br>KPP_ROW[6]<br><b>AUDMUX_AUD3_RXD</b><br>MMDC_DEBUG[46]<br>MPCORE_TRACE[4]            | GPIO5[25] | Serial Audio Interface serial data line 1                                                                                                                                                     |
| 91                                 | 3V3  | SSI2_TXD | CSI0_DAT5           | IPU1_CSI0_D[5]<br>WEIM_D[3]<br>ECSPI1_MOSI<br>KPP_ROW[5]<br><b>AUDMUX_AUD3_TXD</b><br>MMDC_DEBUG[44]<br>MPCORE_TRACE[2]           | GPIO5[23] | Serial Audio Interface serial data line 0                                                                                                                                                     |
| 92                                 | 3V3  | SSI2_CLK | CSI0_DAT4           | IPU1_CSI0_D[4]<br>WEIM_D[2]<br>ECSPI1_SCLK<br>KPP_COL[5]<br><b>AUDMUX_AUD3_TXC</b><br>MMDC_DEBUG[43]<br>MPCORE_TRACE[1]           | GPIO5[22] | Serial Audio Interface serial bit clock                                                                                                                                                       |
| 93                                 | 3V3  | SSI2_FS  | CSI0_DAT6           | IPU1_CSI0_D[6]<br>WEIM_D[4]<br>ECSPI1_MISO<br>KPP_COL[6]<br><b>AUDMUX_AUD3_TXFS</b><br>MMDC_DEBUG[45]<br>MPCORE_TRACE[3]          | GPIO5[24] | Serial Audio Interface left/right clock                                                                                                                                                       |
| 94                                 | GND  | GND      |                     |                                                                                                                                   |           |                                                                                                                                                                                               |
| <b>Secure Digital Interface 2</b>  |      |          |                     |                                                                                                                                   |           |                                                                                                                                                                                               |
| 95                                 | 3V3  | SD2_CD   | SD3_CLK             | USDHC3_CLK<br>UART2_RTS<br>CAN1_RXCAN<br>USBOH3_UH3_<br>DFD_OUT[5]<br>USBOH3_UH2_<br>DFD_OUT[5]<br>MIPI_CORE_DPHY_<br>TEST_IN[17] | GPIO7[3]  | SD Card Detect – connected to a GPIO                                                                                                                                                          |
| 96                                 | 3V3  | SD2_D[0] | SD2_DAT0            | <b>USDHC2_DAT0</b><br>ECSPI5_MISO<br>AUDMUX_AUD4_RXD<br>KPP_ROW[7]<br>DCIC2_DCIC_OUT                                              | GPIO1[15] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added. |
| 97                                 | 3V3  | SD2_D[1] | SD2_DAT1            | <b>USDHC2_DAT1</b><br>ECSPI5_SS0<br>WEIM_CS[2]<br>AUDMUX_AUD4_TXFS<br>KPP_COL[7]<br>CCM_WAIT                                      | GPIO1[14] |                                                                                                                                                                                               |
| 98                                 | 3V3  | SD2_D[2] | SD2_DAT2            | <b>USDHC2_DAT2</b><br>ECSPI5_SS1<br>WEIM_CS[3]<br>AUDMUX_AUD4_TXD<br>KPP_ROW[6]<br>CCM_STOP                                       | GPIO1[13] |                                                                                                                                                                                               |
| 99                                 | 3V3  | SD2_D[3] | SD2_DAT3            | <b>USDHC2_DAT3</b><br>ECSPI5_SS3<br>KPP_COL[6]<br>AUDMUX_AUD4_TXC<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[11]<br>SJC_DONE            | GPIO1[12] |                                                                                                                                                                                               |

| PIN                          | Type | Function   | i.MX6 Quad Pad Name | Alternate functions                                                                                                                               | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|------------------------------|------|------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 100                          | 3V3  | SD2_CMD    | SD2_CMD             | <b>USDHC2_CMD</b><br>ECSPI5_MOSI<br>KPP_ROW[5]<br>AUDMUX_AUD4_RXC<br>PCIE_CTRL_DIAG_STATU<br>S_BUS_MUX[10]                                        | GPIO1[11] | SD Command bidirectional signal                       |
| 101                          | 3V3  | SD2_CLK    | SD2_CLK             | <b>USDHC2_CLK</b><br>ECSPI5_SCLK<br>KPP_COL[5]<br>AUDMUX_AUD4_RXFS<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[9]<br>PHY_DTB[1]<br>SATA_PHY_DTB[1]       | GPIO1[10] | SD Output Clock.                                      |
| 102                          | GND  | GND        |                     |                                                                                                                                                   |           |                                                       |
| <b>CMOS Sensor Interface</b> |      |            |                     |                                                                                                                                                   |           |                                                       |
| 103                          | 3V3  | CSI0_DAT12 | CSI0_DAT12          | IPU1_CSI0_D[12]<br>WEIM_D[8]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[16]<br>UART4_TXD_MUX<br>SDMA_DEBUG_PC[6]<br>MMDC_DEBUG[35]<br>MPCORE_TRACE[9]   | GPIO5[30] |                                                       |
| 104                          | 3V3  | CSI0_DAT13 | CSI0_DAT13          | IPU1_CSI0_D[13]<br>WEIM_D[9]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[17]<br>UART4_RXD_MUX<br>SDMA_DEBUG_PC[7]<br>MMDC_DEBUG[36]<br>MPCORE_TRACE[10]  | GPIO5[31] |                                                       |
| 105                          | 3V3  | CSI0_DAT14 | CSI0_DAT14          | IPU1_CSI0_D[14]<br>WEIM_D[10]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[18]<br>UART5_TXD_MUX<br>SDMA_DEBUG_PC[8]<br>MMDC_DEBUG[37]<br>MPCORE_TRACE[11] | GPIO6[0]  |                                                       |
| 106                          | 3V3  | CSI0_DAT15 | CSI0_DAT15          | IPU1_CSI0_D[15]<br>WEIM_D[11]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[19]<br>UART5_RXD_MUX<br>SDMA_DEBUG_PC[9]<br>MMDC_DEBUG[38]<br>MPCORE_TRACE[12] | GPIO6[1]  |                                                       |
| 107                          | 3V3  | CSI0_DAT16 | CSI0_DAT16          | IPU1_CSI0_D[16]<br>WEIM_D[12]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[20]<br>UART4_RTS<br>SDMA_DEBUG_PC[10]<br>MMDC_DEBUG[39]<br>MPCORE_TRACE[13]    | GPIO6[2]  |                                                       |
| 108                          | 3V3  | CSI0_DAT17 | CSI0_DAT17          | IPU1_CSI0_D[17]<br>WEIM_D[13]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[21]<br>UART4_CTS<br>SDMA_DEBUG_PC[11]<br>MMDC_DEBUG[40]<br>MPCORE_TRACE[14]    | GPIO6[3]  |                                                       |
| 109                          | 3V3  | CSI0_DAT18 | CSI0_DAT18          | IPU1_CSI0_D[18]<br>WEIM_D[14]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[22]<br>UART5_RTS<br>SDMA_DEBUG_PC[12]<br>MMDC_DEBUG[41]<br>MPCORE_TRACE[15]    | GPIO6[4]  |                                                       |

| PIN | Type | Function    | i.MX6 Quad Pad Name | Alternate functions                                                                                                            | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|-------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 110 | 3V3  | CSI0_DAT19  | CSI0_DAT19          | IPU1_CSI0_D[19]<br>WEIM_D[15]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[23]<br>UART5_CTS<br>SDMA_DEBUG_PC[13]<br>MMDC_DEBUG[42]     | GPIO6[5]  |                                                       |
| 111 | GND  | GND         |                     |                                                                                                                                |           |                                                       |
| 112 | 3V3  | CSI0_HSYNC  | CSI0_MCLK           | IPU1_CSI0_HSYNC<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[13]<br>CCM_CLKO<br>SDMA_DEBUG_PC[1]<br>MMDC_DEBUG[30]<br>MPCORE_TRCTL     | GPIO5[19] |                                                       |
| 113 | 3V3  | CSI0_VSYNC  | CSI0_VSYNC          | IPU1_CSI0_VSYNC<br>WEIM_D[1]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[15]<br>SDMA_DEBUG_PC[3]<br>MMDC_DEBUG[32]<br>MPCORE_TRACE[0] | GPIO5[21] |                                                       |
| 114 | 3V3  | CSI0_PIXCLK | CSI0_PIXCLK         | IPU1_CSI0_PIXCLK<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[12]<br>SDMA_DEBUG_PC[0]<br>MMDC_DEBUG[29]<br>MPCORE_EVENTO               | GPIO5[18] |                                                       |
| 115 | 3V3  | CSI0_MCLK   | GPIO_0              | CCM_CLKO<br>KPP_COL[5]<br>EPIT1_EPITO<br>USBOH3_USBH1_PWR<br>SNVS_HP_WRAPPER_<br>SNVS_VIO_5                                    | GPIO1[0]  |                                                       |
| 116 | GND  | GND         |                     |                                                                                                                                |           |                                                       |

### LCD Controller and Smart LCD Controller

|     |      |     |                   |                                                                                                                                                                |           |                                               |
|-----|------|-----|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------------------------------------------|
| 117 | 3V3  | LD0 | <b>DISP0_DAT0</b> | IPU1_DISP0_DAT[0]<br>IPU2_DISP0_DAT[0]<br>ECSPI3_SCLK<br>USDHC1_USDHC_<br>DEBUG[0]<br>SDMA_DEBUG_<br>CORE_RUN<br>MMDC_DEBUG[5]                                 | GPIO4[21] | TX6Q standard version: LCD Data Bus           |
|     | LVDS |     | LVDS1_TX2_N       | not available                                                                                                                                                  |           | TX6Q LVDS version: LVDS display output port 1 |
| 118 | 3V3  | LD1 | <b>DISP0_DAT1</b> | IPU1_DISP0_DAT[1]<br>IPU2_DISP0_DAT[1]<br>ECSPI3_MOSI<br>USDHC1_USDHC_<br>DEBUG[1]<br>SDMA_DEBUG_<br>EVENT_CHANNEL_SEL<br>MMDC_DEBUG[6]<br>MX6Q_PER1_HADDR[12] | GPIO4[22] | TX6Q standard version: LCD Data Bus           |
|     | LVDS |     | LVDS1_TX1_N       | not available                                                                                                                                                  |           | TX6Q LVDS version: LVDS display output port 1 |
| 119 | 3V3  | LD2 | <b>DISP0_DAT2</b> | IPU1_DISP0_DAT[2]<br>IPU2_DISP0_DAT[2]<br>ECSPI3_MISO<br>USDHC1_USDHC_<br>DEBUG[2]<br>SDMA_DEBUG_MODE<br>MMDC_DEBUG[7]<br>MX6Q_PER1_HADDR[13]                  | GPIO4[23] | TX6Q standard version: LCD Data Bus           |
|     | LVDS |     | LVDS1_TX2_P       | not available                                                                                                                                                  |           | TX6Q LVDS version: LVDS display output port 1 |
| 120 | 3V3  | LD3 | <b>DISP0_DAT3</b> | IPU1_DISP0_DAT[3]<br>IPU2_DISP0_DAT[3]<br>ECSPI3_SS0<br>USDHC1_USDHC_<br>DEBUG[3]<br>SDMA_DEBUG_BUS_ERR<br>MMDC_DEBUG[8]<br>MX6Q_PER1_HADDR[14]                | GPIO4[24] | TX6Q standard version: LCD Data Bus           |
|     | LVDS |     | LVDS1_TX1_P       | not available                                                                                                                                                  |           | TX6Q LVDS version: LVDS display output port 1 |

| PIN | Type | Function | i.MX6 Quad Pad Name | Alternate functions                                                                                                                                   | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|----------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 121 | 3V3  | LD4      | <b>DISP0_DAT4</b>   | IPU1_DISP0_DAT[4]<br>IPU2_DISP0_DAT[4]<br>ECSP13_SS1<br>USDHC1_USDHC_DEBUG[4]<br>SDMA_DEBUG_BUS_RWB<br>MMDC_DEBUG[9]<br>MX6Q_PER1_HADDR[15]           | GPIO4[25] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_TX3_N         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 122 | 3V3  | LD5      | <b>DISP0_DAT5</b>   | IPU1_DISP0_DAT[5]<br>IPU2_DISP0_DAT[5]<br>ECSP13_SS2<br>AUDMUX_AUD6_RXFS<br>SDMA_DEBUG_MATCHED_DMBUS<br>MMDC_DEBUG[10]<br>MX6Q_PER1_HADDR[16]         | GPIO4[26] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_TX0_N         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 123 | 3V3  | LD6      | <b>DISP0_DAT6</b>   | IPU1_DISP0_DAT[6]<br>IPU2_DISP0_DAT[6]<br>ECSP13_SS3<br>AUDMUX_AUD6_RXC<br>SDMA_DEBUG_RTBUFFER_WRITE<br>MMDC_DEBUG[11]<br>MX6Q_PER1_HADDR[17]         | GPIO4[27] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_TX3_P         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 124 | 3V3  | LD7      | <b>DISP0_DAT7</b>   | IPU1_DISP0_DAT[7]<br>IPU2_DISP0_DAT[7]<br>ECSP13_RDY<br>USDHC1_USDHC_DEBUG[5]<br>SDMA_DEBUG_EVENT_CHANNEL[0]<br>MMDC_DEBUG[12]<br>MX6Q_PER1_HADDR[18] | GPIO4[28] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_TX0_P         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 125 | 3V3  | LD8      | <b>DISP0_DAT8</b>   | IPU1_DISP0_DAT[8]<br>IPU2_DISP0_DAT[8]<br>PWM1_PWM0<br>WDOG1_WDOG_B<br>SDMA_DEBUG_EVENT_CHANNEL[1]<br>MMDC_DEBUG[13]<br>MX6Q_PER1_HADDR[19]           | GPIO4[29] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_CLK_N         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 126 | 3V3  | LD9      | <b>DISP0_DAT9</b>   | IPU1_DISP0_DAT[9]<br>IPU2_DISP0_DAT[9]<br>PWM2_PWM0<br>WDOG2_WDOG_B<br>SDMA_DEBUG_EVENT_CHANNEL[2]<br>MMDC_DEBUG[14]<br>MX6Q_PER1_HADDR[20]           | GPIO4[30] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX3_P         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 0         |
| 127 | 3V3  | LD10     | <b>DISP0_DAT10</b>  | IPU1_DISP0_DAT[10]<br>IPU2_DISP0_DAT[10]<br>USDHC1_USDHC_DEBUG[6]<br>SDMA_DEBUG_EVENT_CHANNEL[3]<br>MMDC_DEBUG[15]<br>MX6Q_PER1_HADDR[21]             | GPIO4[31] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS1_CLK_P         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 1         |
| 128 | 3V3  | LD11     | <b>DISP0_DAT11</b>  | IPU1_DISP0_DAT[11]<br>IPU2_DISP0_DAT[11]<br>USDHC1_USDHC_DEBUG[7]<br>SDMA_DEBUG_EVENT_CHANNEL[4]<br>MMDC_DEBUG[16]<br>MX6Q_PER1_HADDR[22]             | GPIO5[5]  | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX3_N         | not available                                                                                                                                         |           | TX6Q LVDS version: LVDS display output port 0         |

| PIN | Type | Function | i.MX6 Quad Pad Name | Alternate functions                                                                                                                           | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 129 | GND  | GND      |                     |                                                                                                                                               |           |                                                       |
| 130 | 3V3  | LD12     | <b>DISP0_DAT12</b>  | IPU1_DISP0_DAT[12]<br>IPU2_DISP0_DAT[12]<br>SDMA_DEBUG_<br>EVENT_CHANNEL[5]<br>MMDC_DEBUG[17]<br>MX6Q_PER1_HADDR[23]                          | GPIO5[6]  | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_CLK_P         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 131 | 3V3  | LD13     | <b>DISP0_DAT13</b>  | IPU1_DISP0_DAT[13]<br>IPU2_DISP0_DAT[13]<br>AUDMUX_AUD5_RXFS<br>SDMA_DEBUG_<br>EVT_CHN_LINES[0]<br>MMDC_DEBUG[18]<br>MX6Q_PER1_HADDR[24]      | GPIO5[7]  | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX2_P         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 132 | 3V3  | LD14     | <b>DISP0_DAT14</b>  | IPU1_DISP0_DAT[14]<br>IPU2_DISP0_DAT[14]<br>AUDMUX_AUD5_RXC<br>SDMA_DEBUG_<br>EVT_CHN_LINES[1]<br>MMDC_DEBUG[19]                              | GPIO5[8]  | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_CLK_N         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 133 | 3V3  | LD15     | <b>DISP0_DAT15</b>  | IPU1_DISP0_DAT[15]<br>IPU2_DISP0_DAT[15]<br>ECSP11_SS1 ECSP12_SS1<br>SDMA_DEBUG_<br>EVT_CHN_LINES[2]<br>MMDC_DEBUG[20]<br>MX6Q_PER1_HADDR[25] | GPIO5[9]  | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX2_N         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 134 | 3V3  | LD16     | <b>DISP0_DAT16</b>  | IPU1_DISP0_DAT[16]<br>IPU2_DISP0_DAT[16]<br>ECSP12_MOSI<br>AUDMUX_AUD5_TXC<br>SDMA_EXT_EVENT[0]<br>MMDC_DEBUG[21]<br>MX6Q_PER1_HADDR[26]      | GPIO5[10] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX1_P         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 135 | 3V3  | LD17     | <b>DISP0_DAT17</b>  | IPU1_DISP0_DAT[17]<br>IPU2_DISP0_DAT[17]<br>ECSP12_MISO<br>AUDMUX_AUD5_TXD<br>SDMA_EXT_EVENT[1]<br>MMDC_DEBUG[22]<br>MX6Q_PER1_HADDR[27]      | GPIO5[11] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX0_P         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 136 | 3V3  | LD18     | <b>DISP0_DAT18</b>  | IPU1_DISP0_DAT[18]<br>IPU2_DISP0_DAT[18]<br>ECSP12_SS0<br>AUDMUX_AUD5_TXFS<br>AUDMUX_AUD4_RXFS<br>MMDC_DEBUG[23]<br>WEIM_CS[2]                | GPIO5[12] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX1_N         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |
| 137 | 3V3  | LD19     | <b>DISP0_DAT19</b>  | IPU1_DISP0_DAT[19]<br>IPU2_DISP0_DAT[19]<br>ECSP12_SCLK<br>AUDMUX_AUD5_RXD<br>AUDMUX_AUD4_RXC<br>MMDC_DEBUG[24]<br>WEIM_CS[3]                 | GPIO5[13] | TX6Q standard version: LCD Data Bus                   |
|     | LVDS |          | LVDS0_TX0_N         | not available                                                                                                                                 |           | TX6Q LVDS version: LVDS display output port 0         |



| PIN | Type | Function | i.MX6 Quad Pad Name | Alternate functions                                                                                                                                           | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|----------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 138 | 3V3  | LD20     | <b>DISP0_DAT20</b>  | IPU1_DISP0_DAT[20]<br>IPU2_DISP0_DAT[20]<br>ECSP11_SCLK<br>AUDMUX_AUD4_TXC<br>SDMA_DEBUG_<br>EVT_CHN_LINES[7]<br>MMDC_DEBUG[25]<br>MX6Q_PER1_HADDR[28]        | GPIO5[14] | TX6Q standard version: LCD Data Bus                   |
|     | SATA |          | SATA_RXM            | not available                                                                                                                                                 |           | TX6Q LVDS version: SATA port                          |
| 139 | 3V3  | LD21     | <b>DISP0_DAT21</b>  | IPU1_DISP0_DAT[21]<br>IPU2_DISP0_DAT[21]<br>ECSP11_MOSI<br>AUDMUX_AUD4_TXD<br>SDMA_DEBUG_<br>BUS_DEVICE[0]<br>MMDC_DEBUG[26]<br>MX6Q_PER1_HADDR[29]           | GPIO5[15] | TX6Q standard version: LCD Data Bus                   |
|     | SATA |          | SATA_TXM            | not available                                                                                                                                                 |           | TX6Q LVDS version: SATA port                          |
| 140 | 3V3  | LD22     | <b>DISP0_DAT22</b>  | IPU1_DISP0_DAT[22]<br>IPU2_DISP0_DAT[22]<br>ECSP11_MISO<br>AUDMUX_AUD4_TXFS<br>SDMA_DEBUG_<br>BUS_DEVICE[1]<br>MMDC_DEBUG[27]<br>MX6Q_PER1_HADDR[30]          | GPIO5[16] | TX6Q standard version: LCD Data Bus                   |
|     | SATA |          | SATA_RXP            | not available                                                                                                                                                 |           | TX6Q LVDS version: SATA port                          |
| 141 | 3V3  | LD23     | <b>DISP0_DAT23</b>  | IPU1_DISP0_DAT[23]<br>IPU2_DISP0_DAT[23]<br>ECSP11_SS0<br>AUDMUX_AUD4_RXD<br>SDMA_DEBUG_<br>BUS_DEVICE[2]<br>MMDC_DEBUG[28]<br>MX6Q_PER1_HADDR[31]            | GPIO5[17] | TX6Q standard version: LCD Data Bus                   |
|     | SATA |          | SATA_TXP            | not available                                                                                                                                                 |           | TX6Q LVDS version: SATA port                          |
| 142 | GND  | GND      |                     |                                                                                                                                                               |           |                                                       |
| 143 | 3V3  | HSYNC    | DIO_PIN2            | IPU1_DIO_PIN2<br>IPU2_DIO_PIN2<br>AUDMUX_AUD6_TXD<br>MIPI_CORE_<br>DPHY_TEST_OUT[30]<br>SDMA_DEBUG_<br>CORE_STATE[2]<br>MMDC_DEBUG[2]<br>MX6Q_PER1_HADDR[9]   | GPIO4[18] |                                                       |
| 144 | 3V3  | VSYNC    | DIO_PIN3            | IPU1_DIO_PIN3<br>IPU2_DIO_PIN3<br>AUDMUX_AUD6_TXFS<br>MIPI_CORE_<br>DPHY_TEST_OUT[31]<br>SDMA_DEBUG_<br>CORE_STATE[3]<br>MMDC_DEBUG[3]<br>MX6Q_PER1_HADDR[10] | GPIO4[19] |                                                       |
| 145 | 3V3  | OE_ACD   | DIO_PIN15           | IPU1_DIO_PIN15<br>IPU2_DIO_PIN15<br>AUDMUX_AUD6_TXC<br>MIPI_CORE_<br>DPHY_TEST_OUT[29]<br>SDMA_DEBUG_<br>CORE_STATE[1]<br>MMDC_DEBUG[1]                       | GPIO4[17] |                                                       |
| 146 | 3V3  | LSCLK    | DIO_DISP_CLK        | IPU1_DIO_DISP_CLK<br>IPU2_DIO_DISP_CLK<br>MIPI_CORE_<br>DPHY_TEST_OUT[28]<br>SDMA_DEBUG_<br>CORE_STATE[0]<br>MMDC_DEBUG[0]                                    | GPIO4[16] |                                                       |
| 147 | GND  | GND      |                     |                                                                                                                                                               |           |                                                       |

| PIN                            | Type | Function    | i.MX6 Quad Pad Name | Alternate functions                                                                                                         | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|--------------------------------|------|-------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| <b>Module Specific Signals</b> |      |             |                     |                                                                                                                             |           |                                                       |
| 148                            | 3V3  | CSI1_MCLK   | NANDE_CS2           | RAWNAND_CE2N<br>IPU1_SISG[0]<br>ESAI1_TX0<br>WEIM_CRE<br>CCM_CLKO2<br>IPU2_SISG[0]<br>WEIM_A[16]                            | GPIO6[15] |                                                       |
| 149                            | 3V3  | CSI1_PIXCLK | EIM_A16             | IPU1_DI1_DISP_CLK<br>IPU2_CSI1_PIXCLK<br>MIPI_CORE_<br>DPHY_TEST_OUT[23]<br>TPSMP_HDATA[6]<br>SRC_BT_CFG[16]                | GPIO2[22] |                                                       |
| 150                            | 3V3  | CSI1_VSYNC  | EIM_D29             | WEIM_D[29]<br>IPU1_DI1_PIN15<br>ECSPI4_SS0<br>UART2_RTS<br>IPU2_CSI1_VSYNC<br>IPU1_DIO_PIN14                                | GPIO3[29] |                                                       |
| 151                            | 3V3  | CSI1_HSYNC  | EIM_EB3             | WEIM_EB[3]<br>ECSPI4_RDY<br>UART3_RTS<br>UART1_RI<br>IPU2_CSI1_HSYNC<br>IPU1_DI1_PIN3<br>SRC_BT_CFG[31]                     | GPIO2[31] |                                                       |
| 152                            | 3V3  | CSI1_D[12]  | EIM_A17             | WEIM_A[17]<br>IPU1_DISP1_DAT[12]<br>IPU2_CSI1_D[12]<br>MIPI_CORE_<br>DPHY_TEST_OUT[22]<br>TPSMP_HDATA[5]<br>SRC_BT_CFG[17]  | GPIO2[21] |                                                       |
| 153                            | 3V3  | CSI1_D[13]  | EIM_A18             | WEIM_A[18]<br>IPU1_DISP1_DAT[13]<br>IPU2_CSI1_D[13]<br>MIPI_CORE_<br>DPHY_TEST_OUT[21]<br>TPSMP_HDATA[4]<br>SRC_BT_CFG[18]  | GPIO2[20] |                                                       |
| 154                            | 3V3  | CSI1_D[14]  | EIM_A19             | WEIM_A[19]<br>IPU1_DISP1_DAT[14]<br>IPU2_CSI1_D[14]<br>MIPI_CORE_<br>DPHY_TEST_OUT[20]<br>TPSMP_HDATA[3]<br>SRC_BT_CFG[19]  | GPIO2[19] |                                                       |
| 155                            | 3V3  | CSI1_D[15]  | EIM_A20             | WEIM_A[20]<br>IPU1_DISP1_DAT[15]<br>IPU2_CSI1_D[15]<br>MIPI_CORE_<br>DPHY_TEST_OUT[19]<br>TPSMP_HDATA[2]<br>SRC_BT_CFG[20]  | GPIO2[18] |                                                       |
| 156                            | 3V3  | CSI1_D[16]  | EIM_A21             | WEIM_A[21]<br>IPU1_DISP1_DAT[16]<br>IPU2_CSI1_D[16]<br>MIPI_CORE_<br>DPHY_TEST_OUT[18]<br>TPSMP_HDATA[1]<br>SRC_BT_CFG[21]  | GPIO2[17] |                                                       |
| 157                            | 3V3  | CSI1_D[17]  | EIM_A22             | WEIM_A[22]<br>IPU1_DISP1_DAT[17]<br>IPU2_CSI1_D[17]<br>TPSMP_HDATA[0]<br>SRC_BT_CFG[22]                                     | GPIO2[16] |                                                       |
| 158                            | 3V3  | CSI1_D[18]  | EIM_A23             | WEIM_A[23]<br>IPU1_DISP1_DAT[18]<br>IPU2_CSI1_D[18]<br>IPU2_SISG[3]<br>IPU1_SISG[3]<br>MX6Q_PER1_HPROT[3]<br>SRC_BT_CFG[23] | GPIO6[6]  |                                                       |

| PIN | Type | Function   | i.MX6 Quad Pad Name | Alternate functions                                                                                                          | GPIO      | Description (refer to i.MX6 Dual manuals for details)            |
|-----|------|------------|---------------------|------------------------------------------------------------------------------------------------------------------------------|-----------|------------------------------------------------------------------|
| 159 | 3V3  | CSI1_D[19] | EIM_A24             | WEIM_A[24]<br>IPU1_DISP1_DAT[19]<br>IPU2_CSI1_D[19]<br>IPU2_SISG[2]<br>IPU1_SISG[2]<br>MX6Q_PER1_HPROT[2]<br>SRC_BT_CFG[24]  | GPIO5[4]  |                                                                  |
| 160 | GND  | GND        |                     |                                                                                                                              |           |                                                                  |
| 161 | 3V3  |            | CSI0_DAT8           | IPU1_CSI0_D[8]<br>WEIM_D[6]<br>ECSP12_SCLK<br>KPP_COL[7]<br>I2C1_SDA<br>MMD_C_DEBUG[47]<br>MPCORE_TRACE[5]                   | GPIO5[26] |                                                                  |
| 162 | 3V3  |            | CSI0_DAT9           | IPU1_CSI0_D[9]<br>WEIM_D[7]<br>ECSP12_MOSI<br>KPP_ROW[7]<br>I2C1_SCL<br>MMD_C_DEBUG[48]<br>MPCORE_TRACE[6]                   | GPIO5[27] |                                                                  |
| 163 | 3V3  |            | CSI0_DAT10          | IPU1_CSI0_D[10]<br>AUDMUX_AUD3_RXC<br>ECSP12_MISO<br>UART1_TXD_MUX<br>SDMA_DEBUG_PC[4]<br>MMD_C_DEBUG[33]<br>MPCORE_TRACE[7] | GPIO5[28] |                                                                  |
| 164 | 3V3  |            | CSI0_DAT11          | IPU1_CSI0_D[11]<br>AUDMUX_AUD3_RXFS<br>ECSP12_SS0<br>UART1_RXD_MUX<br>SDMA_DEBUG_PC[5]<br>MMD_C_DEBUG[34]<br>MPCORE_TRACE[8] | GPIO5[29] |                                                                  |
| 165 | 3V3  |            | EIM_D22             | WEIM_D[22]<br>ECSP14_MISO<br>IPU1_DI0_PIN1<br>IPU2_CSI1_D[10]<br>USBOTG3_USBOTG_PWR<br>SPDIF_OUT1<br>MX6Q_PER_HWRITE         | GPIO3[22] |                                                                  |
| 166 | LVDS |            | CLK1_N              |                                                                                                                              |           | Alternate reference clock for PCIe                               |
|     |      |            | CSI_CLK0M           |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface CLK0  |
| 167 | LVDS |            | PCIE_RXM            |                                                                                                                              |           |                                                                  |
|     |      |            | CSI_D1M             |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface DATA1 |
| 168 | LVDS |            | CLK1_P              |                                                                                                                              |           | Alternate reference clock for PCIe                               |
|     |      |            | CSI_CLK0P           |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface CLK0  |
| 169 | LVDS |            | PCIE_RXP            |                                                                                                                              |           |                                                                  |
|     |      |            | CSI_D1P             |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface DATA1 |
| 170 | LVDS |            | PCIE_TXM            |                                                                                                                              |           |                                                                  |
|     |      |            | CSI_D0M             |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface DATA0 |
| 171 | GND  | GND        |                     |                                                                                                                              |           |                                                                  |
| 172 | LVDS |            | PCIE_TXP            |                                                                                                                              |           |                                                                  |
|     |      |            | CSI_D0P             |                                                                                                                              |           | MIPI version only! MIPI_CSI - MIPI Camera Serial Interface DATA0 |
| 173 | 3V3  | EIM_CS0    | EIM_CS0             | WEIM_CS[0]<br>IPU1_DI1_PIN5<br>ECSP12_SCLK<br>MIPI_CORE_<br>DPHY_TEST_OUT[24]<br>TPSMP_HDATA[7]                              | GPIO2[23] |                                                                  |
| 174 | 3V3  | EIM_CS1    | EIM_CS1             | WEIM_CS[1]<br>IPU1_DI1_PIN6<br>ECSP12_MOSI<br>MIPI_CORE_<br>DPHY_TEST_OUT[25]<br>TPSMP_HDATA[8]                              | GPIO2[24] |                                                                  |

| PIN | Type  | Function     | i.MX6 Quad Pad Name     | Alternate functions                                                                                                                        | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|-------|--------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 175 | 3V3   | GPIO         | CSIO_DATA_EN            | IPU1_CSIO_DATA_EN<br>WEIM_D[0]<br>PCIE_CTRL_DIAG_<br>STATUS_BUS_MUX[14]<br>SDMA_DEBUG_PC[2]<br>MMDC_DEBUG[31]<br>MPCORE_TRCLK              | GPIO5[20] |                                                       |
| 176 | 3V3   | EIM_WAIT     | EIM_WAIT                | WEIM_WAIT<br>WEIM_DTACK_B<br>TPSMP_HDATA[30]<br>SRC_BT_CFG[25]                                                                             | GPIO5[0]  |                                                       |
| 177 | 3V3   | EIM_EB0      | EIM_EB0                 | WEIM_EB[0]<br>IPU1_DISP1_DAT[11]<br>IPU2_CSI1_D[11]<br>MIPI_CORE_<br>DPHY_TEST_OUT[0]<br>CCM_PMIC_RDY<br>TPSMP_HDATA[12]<br>SRC_BT_CFG[27] | GPIO2[28] |                                                       |
| 178 | 3V3   | EIM_EB1      | EIM_EB1                 | WEIM_EB[1]<br>IPU1_DISP1_DAT[10]<br>IPU2_CSI1_D[10]<br>MIPI_CORE_<br>DPHY_TEST_OUT[1]<br>TPSMP_HDATA[13]<br>SRC_BT_CFG[28]                 | GPIO2[29] |                                                       |
| 179 | 3V3   | EIM_OE       | EIM_OE                  | WEIM_OE<br>IPU1_DI1_PIN7<br>ECSP12_MISO<br>MIPI_CORE_<br>DPHY_TEST_OUT[26]<br>TPSMP_HDATA[9]                                               | GPIO2[25] |                                                       |
| 180 | 3V3   | EIM_LBA      | EIM_LBA                 | WEIM_LBA<br>IPU1_DI1_PIN17<br>ECSP12_SS1<br>TPSMP_HDATA[11]<br>SRC_BT_CFG[26]                                                              | GPIO2[27] |                                                       |
| 181 | 3V3   | EIM_RW       | EIM_RW                  | WEIM_RW<br>IPU1_DI1_PIN8<br>ECSP12_SS0<br>MIPI_CORE_<br>DPHY_TEST_OUT[27]<br>TPSMP_HDATA[10]<br>SRC_BT_CFG[29]                             | GPIO2[26] |                                                       |
| 182 | 3V3   | EIM_BCLK     | EIM_BCLK                | WEIM_BCLK<br>IPU1_DI1_PIN16<br>GPIO6_GPIO[31]<br>TPSMP_HDATA[31]                                                                           | GPIO6[31] |                                                       |
|     | POWER |              | NVCC_RGMII<br>NVCC_ENET | 1V8 power supply output<br>RN5T618 LOD4<br>max.:180mA                                                                                      |           | <b>TX6Q-1020</b>                                      |
| 183 | GND   | GND          |                         |                                                                                                                                            |           |                                                       |
| 184 | 3V3   | EIM_DA0      | EIM_DA0                 | WEIM_DA_A[0]<br>IPU1_DISP1_DAT[9]<br>IPU2_CSI1_D[9]<br>MIPI_CORE_<br>DPHY_TEST_OUT[2]<br>TPSMP_HDATA[14]<br>SRC_BT_CFG[0]                  | GPIO3[0]  |                                                       |
|     | 1V8   | ENET_REF_CLK | ENET_REF_CLK            | ENET_TX_CLK<br>ESAI_RX_FS<br>SPDIF_SR_CLK                                                                                                  | GPIO1[23] | <b>TX6Q-1020</b>                                      |
| 185 | 3V3   | EIM_DA1      | EIM_DA1                 | WEIM_DA_A[1]<br>IPU1_DISP1_DAT[8]<br>IPU2_CSI1_D[8]<br>MIPI_CORE_<br>DPHY_TEST_OUT[3]<br>TPSMP_HDATA[15]<br>SRC_BT_CFG[1]                  | GPIO3[1]  |                                                       |
|     | 1V8   | ENET0_MDC    | ENET0_MDC               | Fixed function                                                                                                                             |           | <b>TX6Q-1020</b>                                      |

| PIN | Type  | Function   | i.MX6 Quad Pad Name | Alternate functions                                                                                                        | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|-------|------------|---------------------|----------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 186 | 3V3   | EIM_DA2    | EIM_DA2             | WEIM_DA_A[2]<br>IPU1_DISP1_DAT[7]<br>IPU2_CSI1_D[7]<br>MIPI_CORE_<br>DPHY_TEST_OUT[4]<br>TPSMP_HDATA[16]<br>SRC_BT_CFG[2]  | GPIO3[2]  |                                                       |
|     | 1V8   | ENET0_MDIO | ENET0_MDIO          | Fixed function                                                                                                             |           | <b>TX6Q-1020</b>                                      |
| 187 | 3V3   | EIM_DA3    | EIM_DA3             | WEIM_DA_A[3]<br>IPU1_DISP1_DAT[6]<br>IPU2_CSI1_D[6]<br>MIPI_CORE_<br>DPHY_TEST_OUT[5]<br>TPSMP_HDATA[17]<br>SRC_BT_CFG[3]  | GPIO3[3]  |                                                       |
|     | POWER |            |                     | 1V2 power supply output<br>RN5T618 LOD5<br>max.:200mA                                                                      |           | <b>TX6Q-1020</b>                                      |
| 188 | 3V3   | EIM_DA4    | EIM_DA4             | WEIM_DA_A[4]<br>IPU1_DISP1_DAT[5]<br>IPU2_CSI1_D[5]<br>MIPI_CORE_<br>DPHY_TEST_OUT[6]<br>TPSMP_HDATA[18]<br>SRC_BT_CFG[4]  | GPIO3[4]  |                                                       |
|     | 1V8   | RGMII_RXC  | RGMII_RXC           | USB_H3_STROBE                                                                                                              | GPIO6[30] | <b>TX6Q-1020</b>                                      |
| 189 | 3V3   | EIM_DA5    | EIM_DA5             | WEIM_DA_A[5]<br>IPU1_DISP1_DAT[4]<br>IPU2_CSI1_D[4]<br>MIPI_CORE_<br>DPHY_TEST_OUT[7]<br>TPSMP_HDATA[19]<br>SRC_BT_CFG[5]  | GPIO3[5]  |                                                       |
|     | 1V8   | RGMII_RD3  | RGMII_RD3           | HSI_TX_WAKE                                                                                                                | GPIO6[29] | <b>TX6Q-1020</b>                                      |
| 190 | 3V3   | EIM_DA6    | EIM_DA6             | WEIM_DA_A[6]<br>IPU1_DISP1_DAT[3]<br>IPU2_CSI1_D[3]<br>MIPI_CORE_<br>DPHY_TEST_OUT[8]<br>TPSMP_HDATA[20]<br>SRC_BT_CFG[6]  | GPIO3[6]  |                                                       |
|     | 1V8   | RGMII_RD2  | RGMII_RD2           | HSI_TX_DATA                                                                                                                | GPIO6[28] | <b>TX6Q-1020</b>                                      |
| 191 | 3V3   | EIM_DA7    | EIM_DA7             | WEIM_DA_A[7]<br>IPU1_DISP1_DAT[2]<br>IPU2_CSI1_D[2]<br>MIPI_CORE_<br>DPHY_TEST_OUT[9]<br>TPSMP_HDATA[21]<br>SRC_BT_CFG[7]  | GPIO3[7]  |                                                       |
|     | 1V8   | RGMII_RD1  | RGMII_RD1           | HSI_TX_FLAG                                                                                                                | GPIO6[27] | <b>TX6Q-1020</b>                                      |
| 192 | 3V3   | EIM_DA8    | EIM_DA8             | WEIM_DA_A[8]<br>IPU1_DISP1_DAT[1]<br>IPU2_CSI1_D[1]<br>MIPI_CORE_<br>DPHY_TEST_OUT[10]<br>TPSMP_HDATA[22]<br>SRC_BT_CFG[8] | GPIO3[8]  |                                                       |
|     | 1V8   | RGMII_RD0  | RGMII_RD0           | HSI_RX_READY                                                                                                               | GPIO6[25] | <b>TX6Q-1020</b>                                      |

| PIN | Type | Function     | i.MX6 Quad Pad Name | Alternate functions                                                                                                                                           | GPIO      | Description (refer to i.MX6 Dual manuals for details) |
|-----|------|--------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------|
| 193 | 3V3  | EIM_DA9      | EIM_DA9             | WEIM_DA_A[9]<br>IPU1_DISP1_DAT[0]<br>IPU2_CSI1_D[0]<br>MIPI_CORE_<br>DPHY_TEST_OUT[11]<br>TPSMP_HDATA[23]<br>SRC_BT_CFG[9]                                    | GPIO3[9]  |                                                       |
|     | 1V8  | RGMII_RX_CTL | RGMII_RX_CTL        | USB_H3_DATA                                                                                                                                                   | GPIO6[24] | <b>TX6Q-1020</b>                                      |
| 194 | 3V3  | EIM_DA10     | EIM_DA10            | WEIM_DA_A[10]<br>IPU1_DI1_PIN15<br>IPU2_CSI1_DATA_EN<br>MIPI_CORE_<br>DPHY_TEST_OUT[12]<br>TPSMP_HDATA[24]<br>SRC_BT_CFG[10]                                  | GPIO3[10] |                                                       |
|     | 1V8  | RGMII_TD3    | RGMII_TD3           | HSI_RX_WAKE                                                                                                                                                   | GPIO6[23] | <b>TX6Q-1020</b>                                      |
| 195 | 3V3  | EIM_DA11     | EIM_DA11            | WEIM_DA_A[11]<br>IPU1_DI1_PIN2<br>IPU2_CSI1_HSYNC<br>MIPI_CORE_<br>DPHY_TEST_OUT[13]<br>SDMA_DEBUG_<br>EVT_CHN_LINES[6]<br>TPSMP_HDATA[25]<br>SRC_BT_CFG[11]  | GPIO3[11] |                                                       |
|     | 1V8  | RGMII_TD2    | RGMII_TD2           | HSI_RX_DATA                                                                                                                                                   | GPIO6[22] | <b>TX6Q-1020</b>                                      |
| 196 | 3V3  | EIM_DA12     | EIM_DA12            | WEIM_DA_A[12]<br>IPU1_DI1_PIN3<br>IPU2_CSI1_VSYNC<br>MIPI_CORE_<br>DPHY_TEST_OUT[14]<br>SDMA_DEBUG_<br>EVT_CHN_LINES[3]<br>TPSMP_HDATA[26]<br>SRC_BT_CFG[12]  | GPIO3[12] |                                                       |
|     | 1V8  | RGMII_TD1    | RGMII_TD1           | HSI_RX_FLAG                                                                                                                                                   | GPIO6[21] | <b>TX6Q-1020</b>                                      |
| 197 | 3V3  | EIM_DA13     | EIM_DA13            | WEIM_DA_A[13]<br>IPU1_DI1_D0_CS<br>CCM_DI1_EXT_CLK<br>MIPI_CORE_<br>DPHY_TEST_OUT[15]<br>SDMA_DEBUG_<br>EVT_CHN_LINES[4]<br>TPSMP_HDATA[27]<br>SRC_BT_CFG[13] | GPIO3[13] |                                                       |
|     | 1V8  | RGMII_TD0    | RGMII_TD0           | HSI_TX_READY                                                                                                                                                  | GPIO6[20] | <b>TX6Q-1020</b>                                      |
| 198 | 3V3  | EIM_DA14     | EIM_DA14            | WEIM_DA_A[14]<br>IPU1_DI1_D1_CS<br>CCM_DI0_EXT_CLK<br>MIPI_CORE_<br>DPHY_TEST_OUT[16]<br>SDMA_DEBUG_<br>EVT_CHN_LINES[5]<br>TPSMP_HDATA[28]<br>SRC_BT_CFG[14] | GPIO3[14] |                                                       |
|     | 1V8  | RGMII_TX_CTL | RGMII_TX_CTL        | USB_H2_STROBE<br>ENET_REF_CLK                                                                                                                                 | GPIO6[26] | <b>TX6Q-1020</b>                                      |
| 199 | 3V3  | EIM_DA15     | EIM_DA15            | WEIM_DA_A[15]<br>IPU1_DI1_PIN1<br>IPU1_DI1_PIN4<br>MIPI_CORE_<br>DPHY_TEST_OUT[17]<br>TPSMP_HDATA[29]<br>SRC_BT_CFG[15]                                       | GPIO3[15] |                                                       |
|     | 1V8  | RGMII_TXC    | RGMII_TXC           | USB_H2_DATA<br>SPDIF_EXT_CLK<br>XTALOSC_REF_CLK_24M                                                                                                           | GPIO6[19] | <b>TX6Q-1020</b>                                      |
| 200 | GND  | GND          |                     |                                                                                                                                                               |           |                                                       |





Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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