

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 3.5  $\mu$ A
  - Maximum standby current: 8.7  $\mu$ A
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP II) and 32-pin small-outline integrated circuit (SOIC) packages

## Functional Description

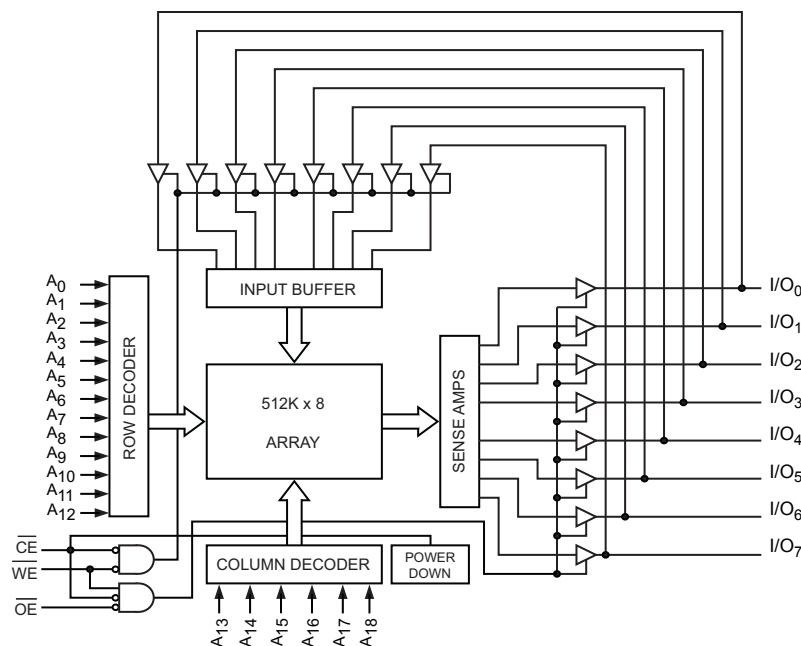
The CY62148GN is a high-performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH). The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), Outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during an active Write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

To write to the device, take Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

To read from the device, take Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

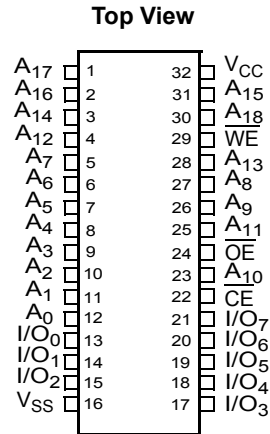


## Contents

<b>Pin Configurations</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>11</b>
<b>Product Portfolio</b> .....	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>13</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>13</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	13
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>14</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>15</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	15
<b>Data Retention Waveform</b> .....	<b>6</b>	Products .....	15
<b>Switching Characteristics</b> .....	<b>7</b>	PSoC <sup>®</sup> Solutions .....	15
<b>Switching Waveforms</b> .....	<b>8</b>	Cypress Developer Community .....	15
<b>Truth Table</b> .....	<b>10</b>	Technical Support .....	15

## Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
				f = 1 MHz		f = f <sub>max</sub>			
				Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62148GN30	Industrial	2.2 V–3.6 V	45	–	6	–	20	3.5	8.7
CY62148GN		4.5 V–5.5 V							

**Note**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to + 150 °C
Ambient temperature with power applied .....	-55 °C to + 125 °C
Supply voltage to ground potential .....	-0.5 V to V <sub>CC</sub> + 0.5 V
DC voltage applied to outputs in high Z state <sup>[2, 3]</sup> .....	-0.5 V to V <sub>CC</sub> + 0.5 V
DC input voltage <sup>[2, 3]</sup> .....	-0.5 V to V <sub>CC</sub> + 0.5 V

Output current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch-up current .....	> 140 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[4]</sup>
CY62148GN	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V, 4.5 V to 5.5 V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	2.2 V to 2.7 V V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	2	-	-	V
		2.7 V to 3.6 V V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5 <sup>[6]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	2.2 V to 2.7 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 V to 3.6 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4	
		4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	2.2 V to 2.7 V -	1.8	-	V <sub>CC</sub> + 0.3 <sup>[3]</sup>	V
		2.7 V to 3.6 V -	2	-	V <sub>CC</sub> + 0.3 <sup>[3]</sup>	
		4.5 V to 5.5 V -	2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Input LOW voltage	2.2 V to 2.7 V -	-0.3 <sup>[2]</sup>	-	0.6	V
		2.7 V to 3.6 V -	-0.3 <sup>[2]</sup>	-	0.8	
		4.5 V to 5.5 V -	-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CC(max)</sub> , I <sub>OUT</sub> = 0 mA CMOS levels	-	-	20	mA
		f = 1 MHz	-	-	6	
I <sub>SB1</sub> <sup>[7]</sup>	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$ , $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$ ,  f = f <sub>max</sub> (address and data only),  f = 0 ( $\overline{OE}$ and $\overline{WE}$ ) V <sub>CC</sub> = V <sub>CC(max)</sub>	-	3.5	8.7	μA
I <sub>SB2</sub> <sup>[7]</sup>	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$ , $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$ , f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	-	3.5	8.7	μA

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- This parameter is guaranteed by design and not tested.
- Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

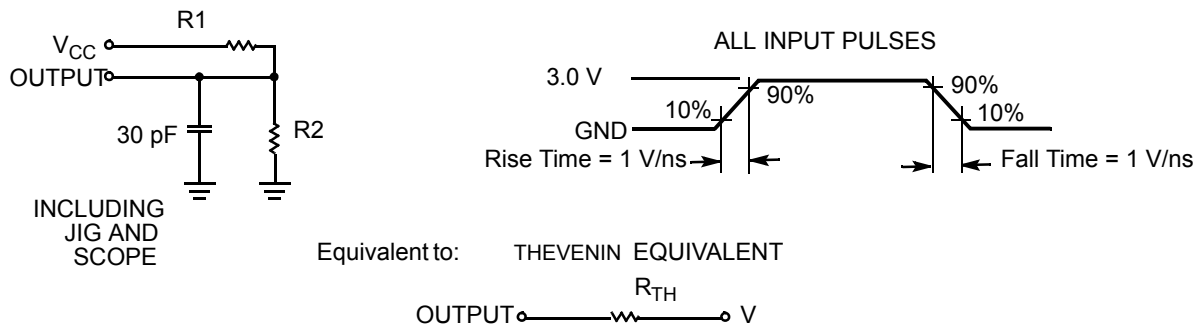
Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(Typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		25.12	17.44	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms<sup>[9]</sup>



Parameter <sup>[8]</sup>	2.5 V	3.0 V	5.0 V	Unit
R <sub>1</sub>	16667	1103	1800	Ω
R <sub>2</sub>	15385	1554	990	Ω
R <sub>TH</sub>	8000	645	639	Ω
V <sub>TH</sub>	1.20	1.75	1.77	V

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V<sub>CC</sub> ramp from VDR to V<sub>CC(min)</sub> > 100 μs or stable at V<sub>CC(min)</sub> > 100 μs.

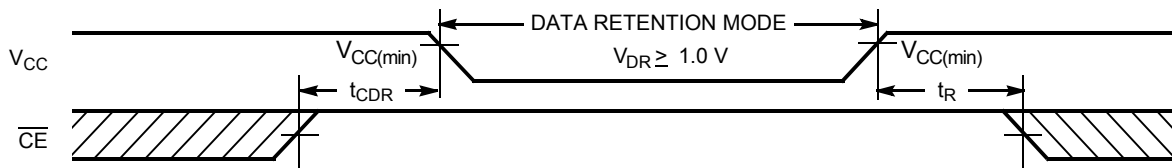
## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1	–	–	V
$I_{CCDR}$ <sup>[11, 12]</sup>	Data retention current	$V_{CC} = 1.2V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	–	13	$\mu A$
$t_{CDR}$ <sup>[13]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[13, 14]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

10. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^\circ C$ .
11. Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
12.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
13. These parameters are guaranteed by design.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} > 100 \mu s$  or stable at  $V_{CC(min)} > 100 \mu s$ .

## Switching Characteristics

Over the operating range

Parameter <sup>[15]</sup>	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	45	–	ns
$t_{AA}$	Address to data valid	–	45	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[16]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[16, 17]</sup>	–	18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[16]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[16, 17]</sup>	–	18	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	45	ns
<b>Write Cycle<sup>[18, 19]</sup></b>				
$t_{WC}$	Write cycle time	45	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	ns
$t_{AW}$	Address setup to write end	35	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[16, 17]</sup>	–	18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[16]</sup>	10	–	ns

### Notes

- Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

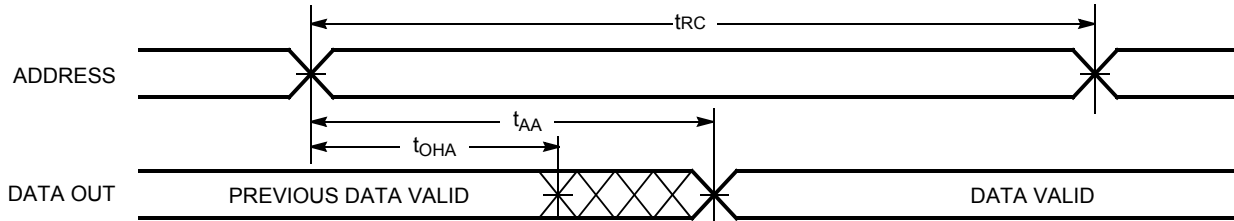


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [21, 22]

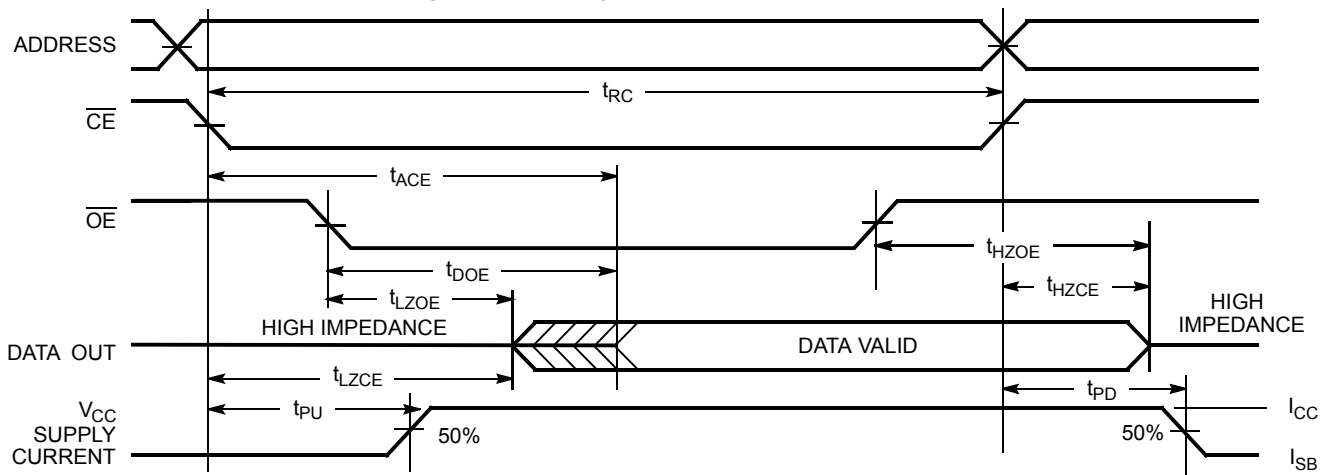
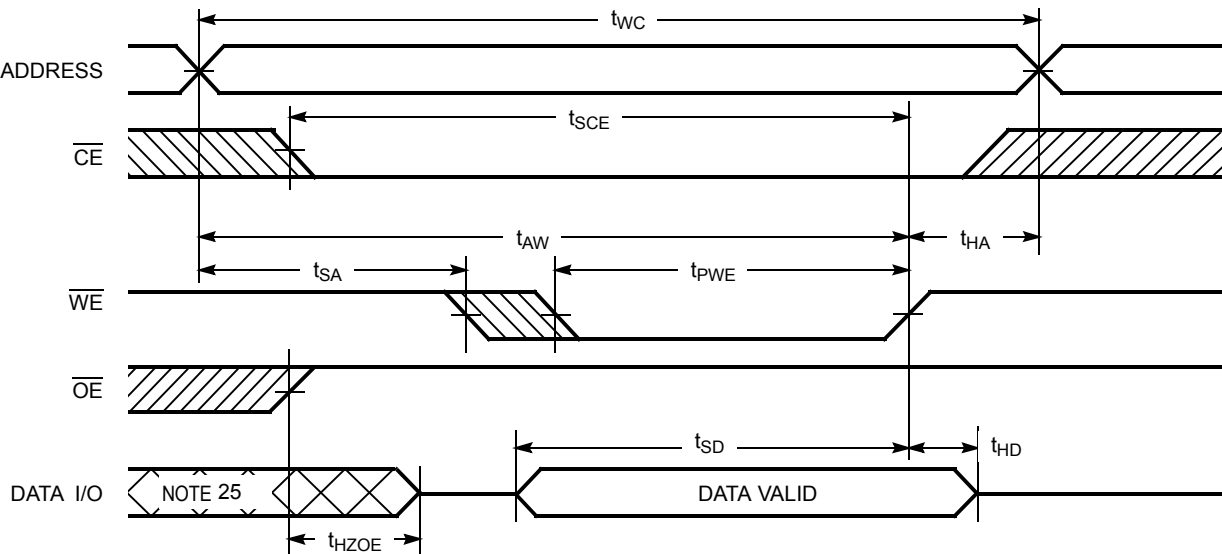


Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [23, 24]

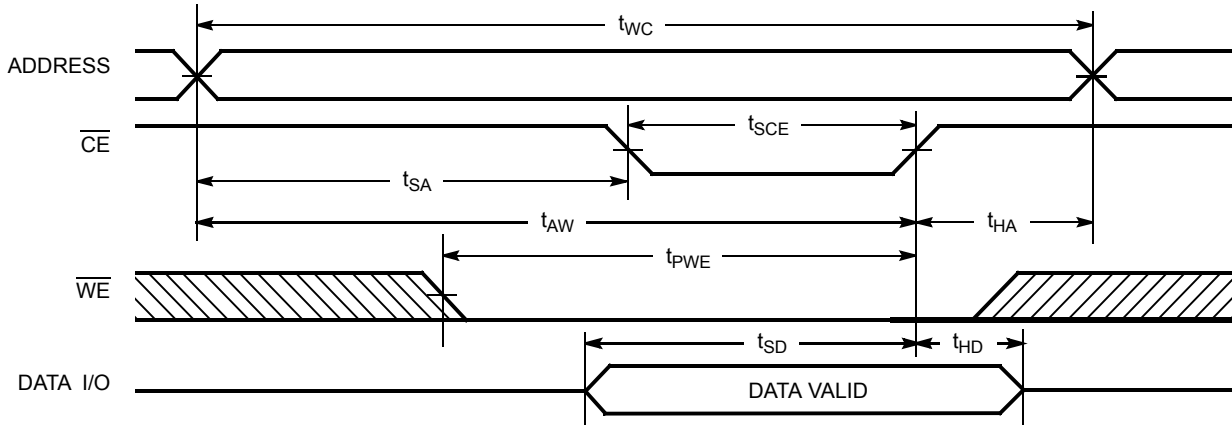
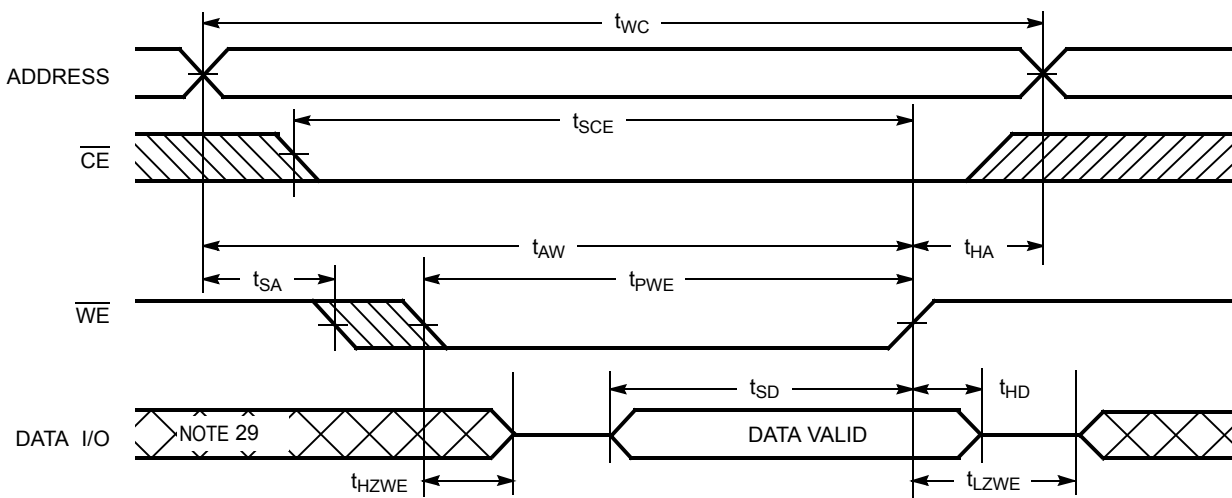


### Notes

20. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
21.  $\overline{WE}$  is HIGH for read cycles.
22. Address valid before or similar to  $\overline{CE}$  transition LOW.
23. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
24. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals must not be applied.



**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [26, 27]

**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [27, 28]

**Notes**

26. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .

27. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.

28. The minimum write cycle pulse width should be equal to the sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

29. During this period, the I/Os are in output state and input signals must not be applied.

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Mode	Power
H <sup>[30]</sup>	X	X	High Z	Deselect/power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data in	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )

**Note**

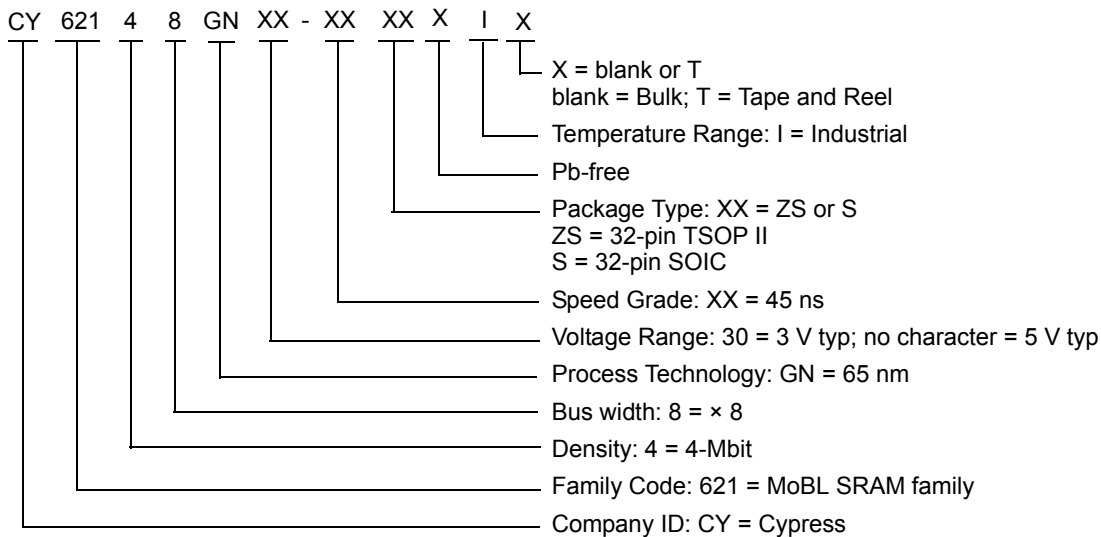
30. Chip enable ( $\overline{\text{CE}}$ ) must be HIGH at CMOS level to meet the  $I_{\text{SB2}} / I_{\text{CCDR}}$  spec. Other inputs can be left floating.

## Ordering Information

Table 1. Key features and Ordering Information

Speed (ns)	Voltage Range (V)	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148GN30-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
		CY62148GN30-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN30-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN30-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	
	4.5 V–5.5 V	CY62148GN-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
		CY62148GN-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	

## Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095

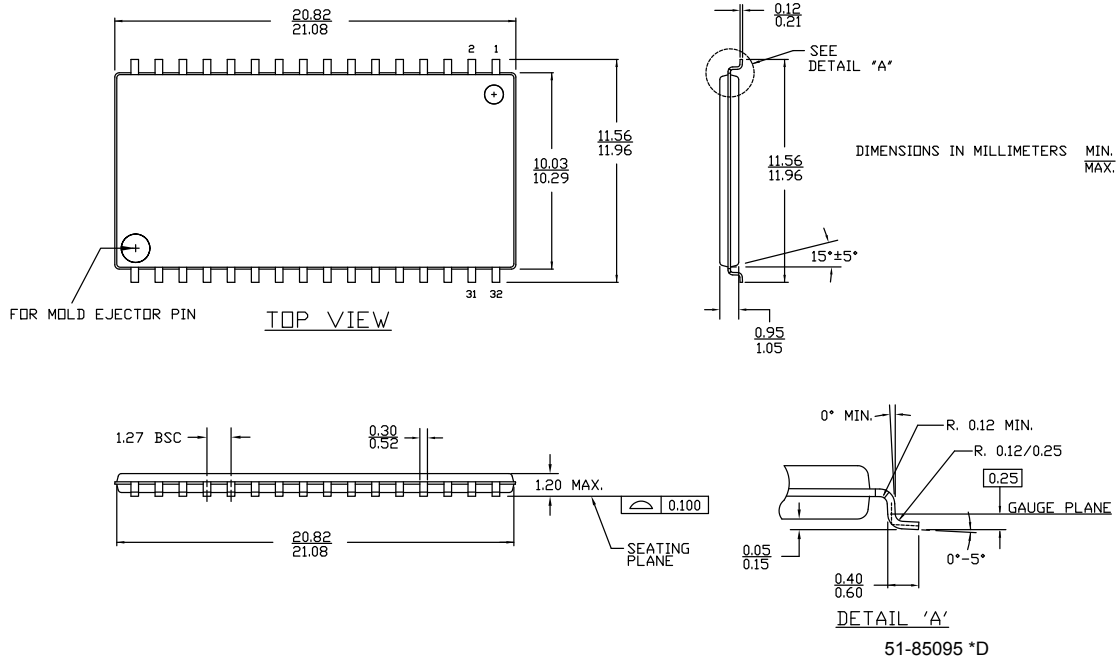
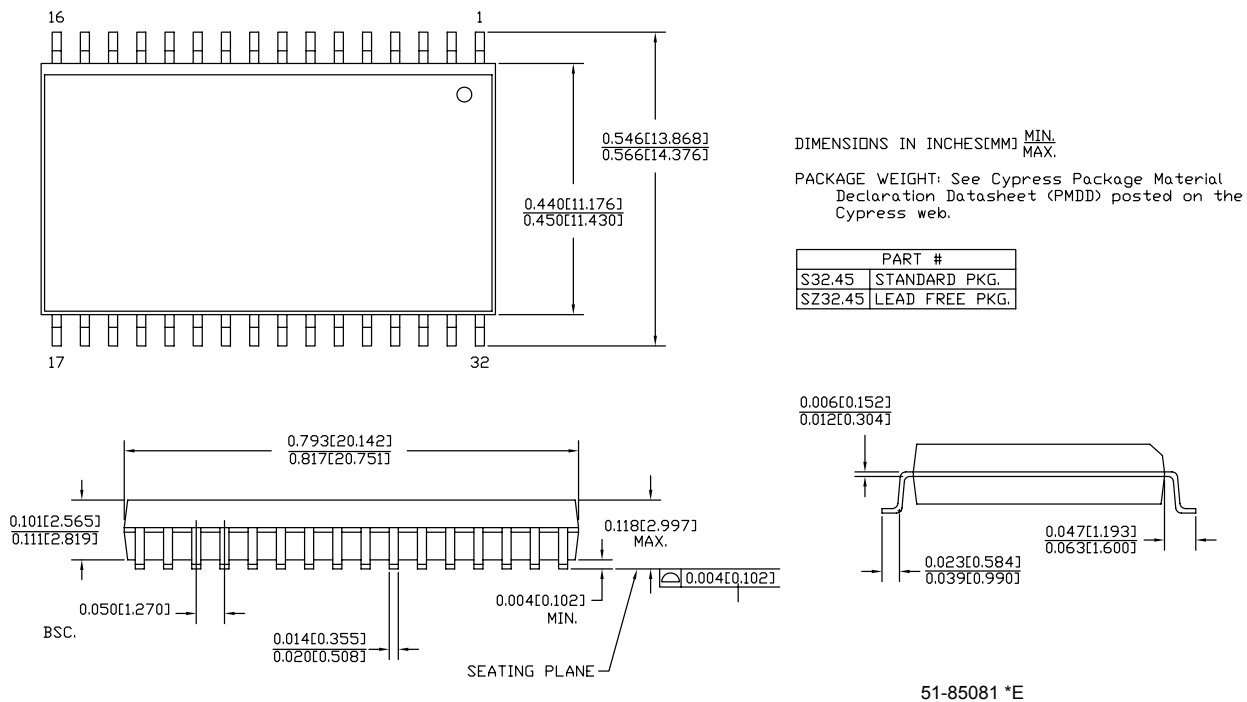


Figure 10. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



## Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
MoBL	More Battery Life
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
WE	write enable

## Document Conventions

### Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

## Document History Page

Document Title: CY62148GN MoBL®, 4-Mbit (512K × 8) Static RAM				
Document Number: 001-95418				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5056496	NILE	12/29/2015	New data sheet.
*A	5092456	NILE	01/19/2016	Added "2.2 V to 3.6 V" range related information in all instances across the document. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*B	5422041	NILE	09/09/2016	Updated <a href="#">Electrical Characteristics</a> : Changed minimum value of V <sub>OH</sub> parameter corresponding to "2.7 V to 3.6 V" from 2.2 V to 2.4 V. Changed minimum value of V <sub>IH</sub> parameter corresponding to "2.2 V to 2.7 V" from 2.0 V to 1.8 V. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated Disclaimer. Updated to new template.
*C	5546908	NILE	12/08/2016	Updated <a href="#">Ordering Information</a> : No change in part numbers. Removed Disclaimer (text referencing to contact sales). Completing Sunset Review.
*D	6002325	AESATMP9	12/21/2017	Updated logo and copyright.

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